

ML605 MIG Design Creation

October 2010

Revision History

Date	Version	Description
10/05/10	12.3	Recompiled under 12.3. Added slides on measuring the Read Data Window with VIO
07/23/10	12.2	Recompiled under 12.2.

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Overview

- **Virtex-6 DDR3 Memory Interface**
- **ML605 Board**
- **ML605 Setup**
- **Generate MIG Example Design**
- **Modifications to Example Design**
- **Compile Example Design**
- **Run MIG Example Design**
- **Adjust Data Pattern using VIO Console**
- **Example Design VIO Consoles**
- **Measure Read Data Window with VIO**
- **References**

Note: This presentation applies to the ML605

Virtex-6 DDR3 Memory Interface

- **Pre-Engineered Controller and Physical Layer (PHY) memory interface**
- **300-533 MHz (600-1066 Mb/s) Performance**
 - Center Column Interfaces
 - 400 MHz in a -1 speed device
 - 533 MHz in -2, -3 devices
- **1 Gb density memory device support**
- **X4, x8, x16 device support**
- **Configurable data bus widths**
 - Multiples of 8 bits, up to 72 bits

Virtex-6 Memory Controller and Interfaces

■ Improved performance

- Higher data rates
 - Faster circuitry (40 nm)
 - Enhanced I/O (50 ps IODELAY)
 - Dedicated clocking paths
 - Real-time calibration
- Higher effective bandwidth
 - Reordering controller (DDR3/DDR2)

■ Improved functionality

- DDR3 DIMM write leveling

■ Easy to use

- MIG for ISE design flow
- MPMC for EDK design flow

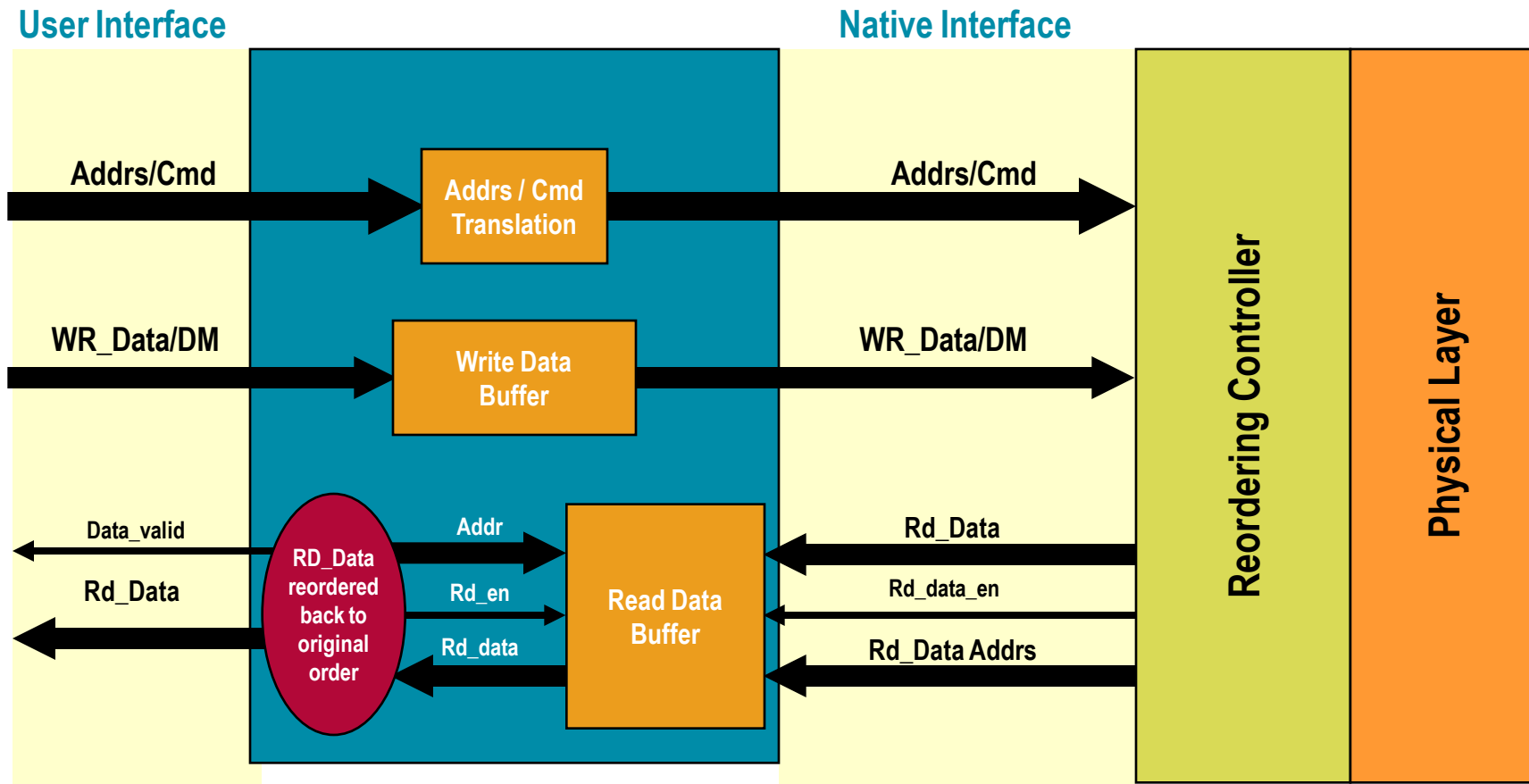
ML605 provides DDR3 SO-DIMM



Xilinx makes it easier and faster to design with Virtex-6

DDR3 User Interfaces

- **Virtex-6 FPGA user interface similar to Virtex-5 architecture**
 - Native interface option available for the advanced users to achieve lower latency

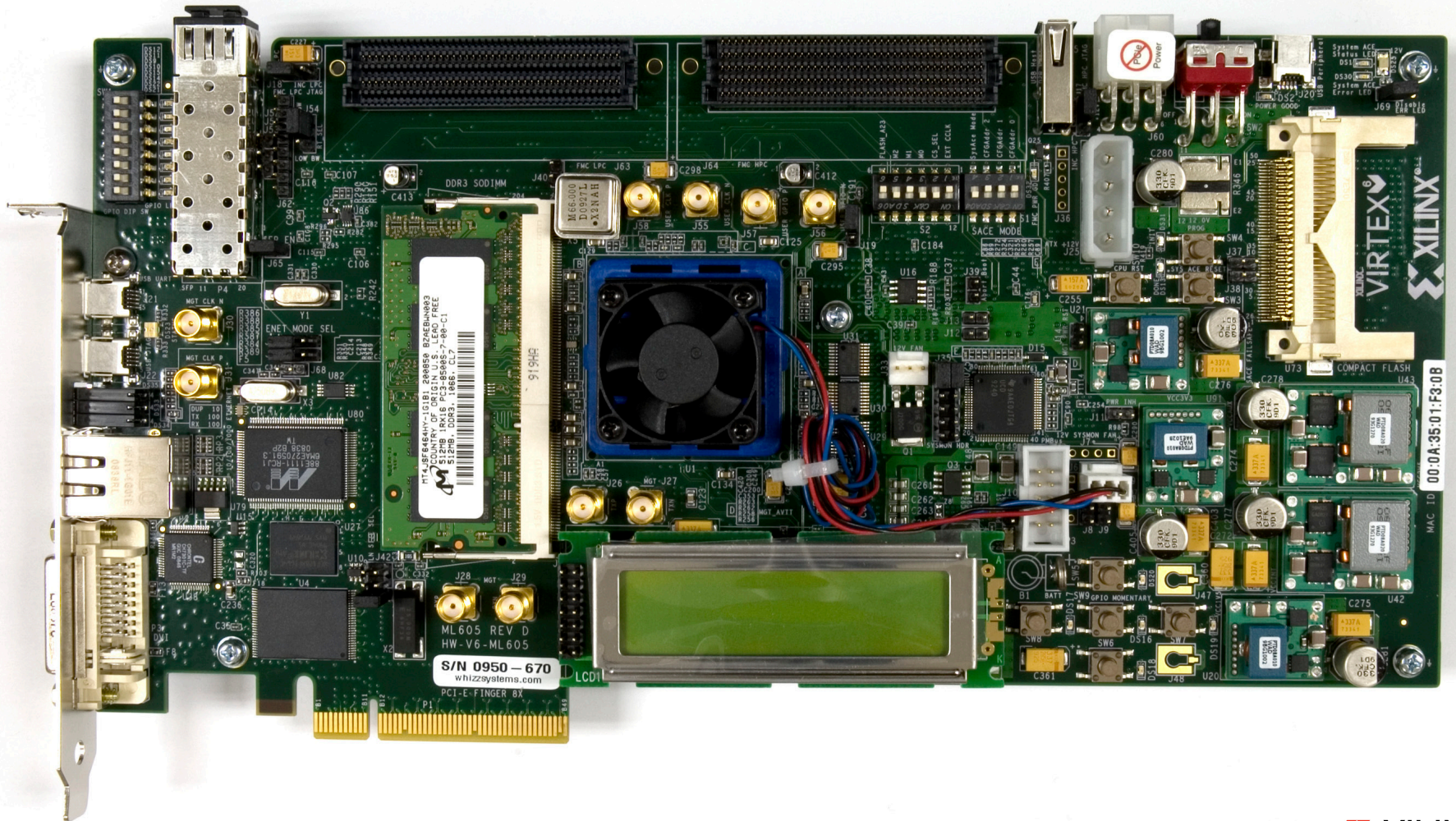


Reordering for Higher Effective Bandwidth

- **Half-frequency DDR2/DDR3 controller**
 - Control state machine runs at half the memory clock rate
- **Reorder READs to avoid precharge time penalty**
 - Example : Execute out-of-order READs to a different bank while performing precharge for the current bank
- **Regroup READs and WRITEs to minimize bus turnaround**
 - Example : Read A - Write B - Read C - Write D
 - Reordered to: Read A - Read C - Write B - Write D
- **Reordering controller looks ahead several commands**
 - Efficiency is dependent on applications (address / command patterns)

Reordering can more than double the throughput

Xilinx ML605 Board



ISE Software Requirements

- Xilinx ISE 12.3 software



ChipScope Pro Software Requirement

- Xilinx ChipScope Pro 12.3 software

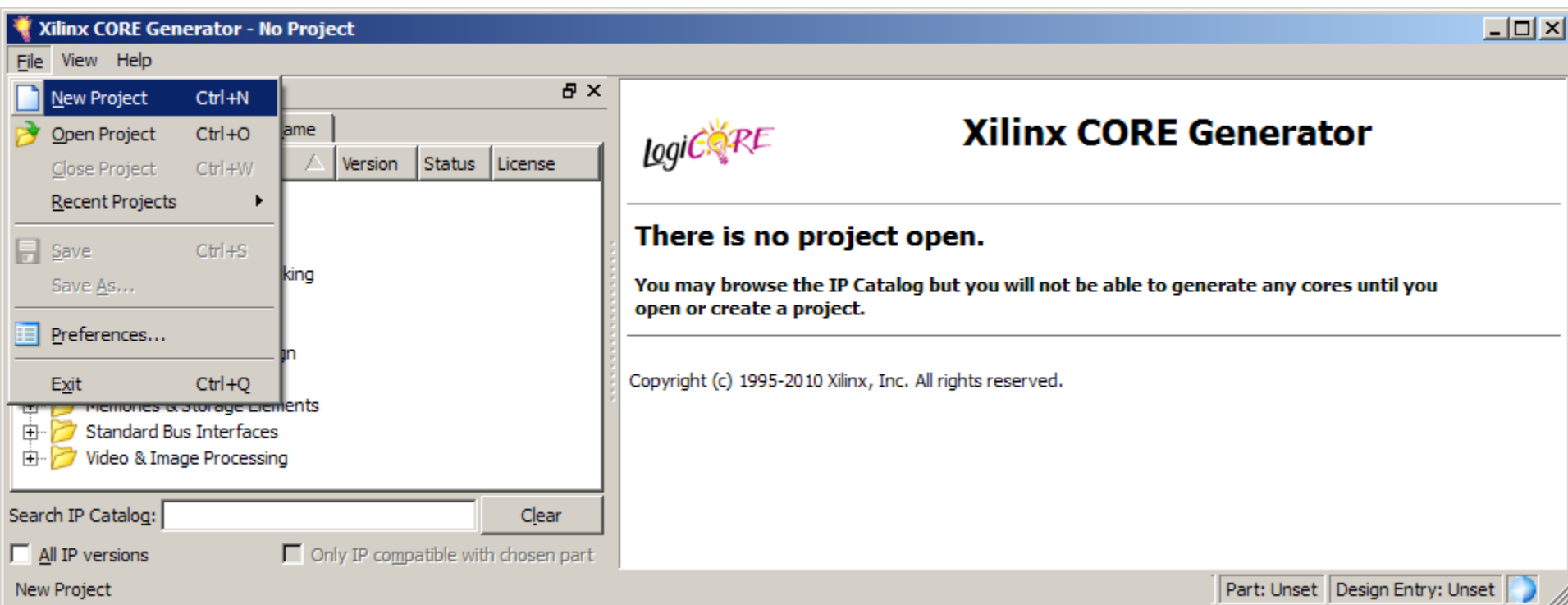


Generate MIG Example Design

- **Open the CORE Generator**

**Start → All Programs → Xilinx ISE Design Suite 12.3 →
ISE → Accessories → CORE Generator**

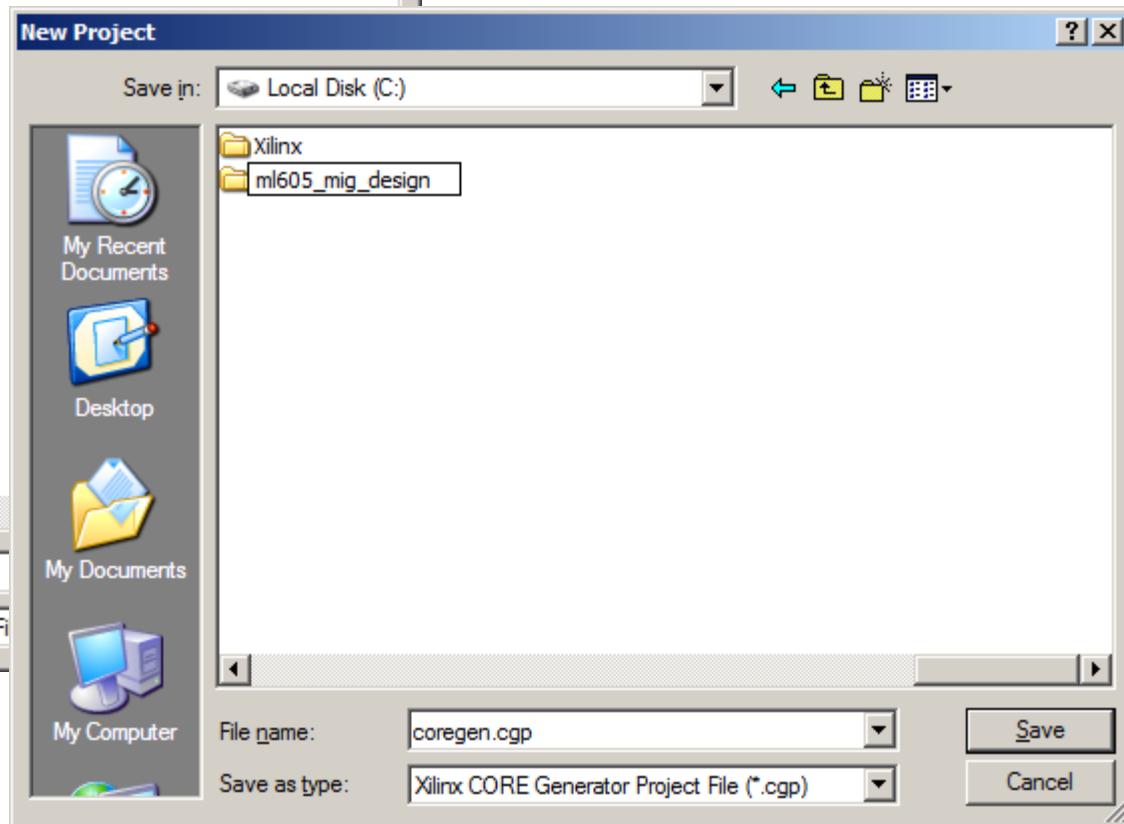
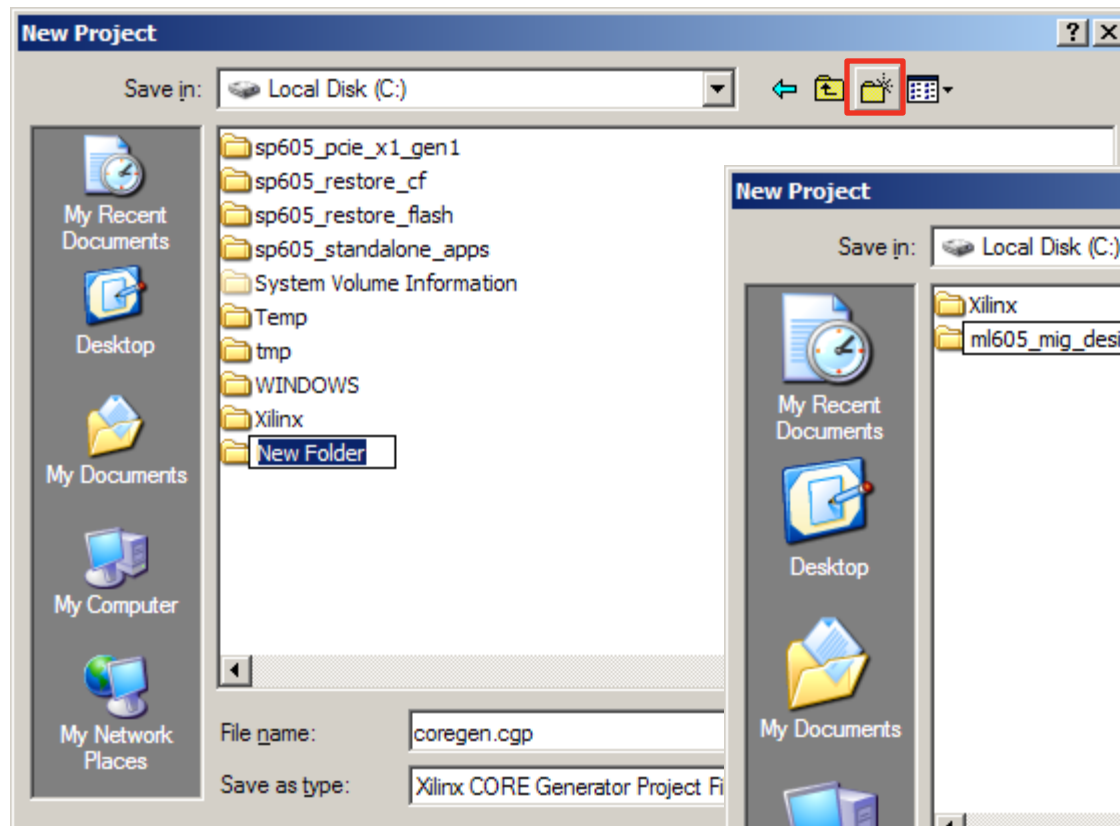
- **Create a new project; select File → New Project**



Note: Presentation applies to the ML605

Generate MIG Example Design

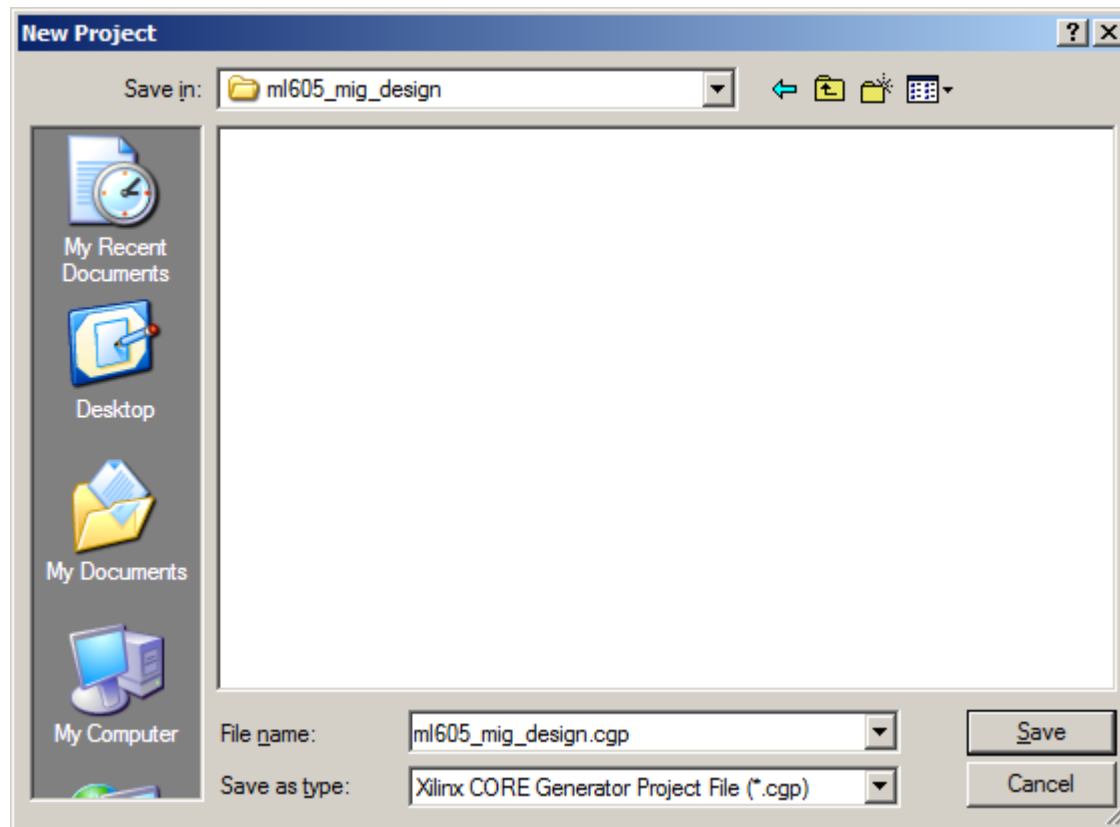
- Create a project directory: ml605_mig_design



Note: Presentation applies to the ML605

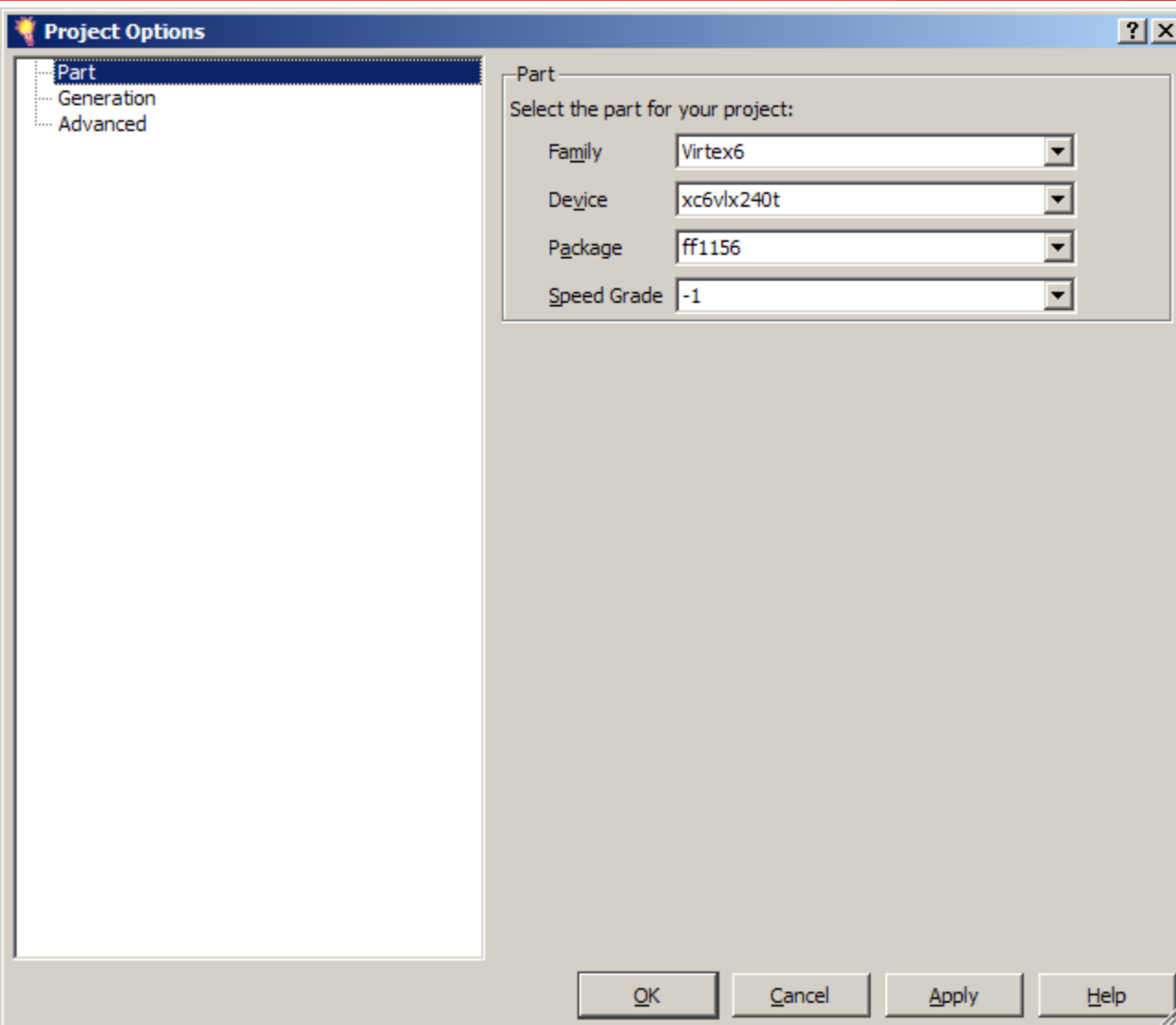
Generate MIG Example Design

- Name the project: ml605_mig_design.cgp



Note: Presentation applies to the ML605

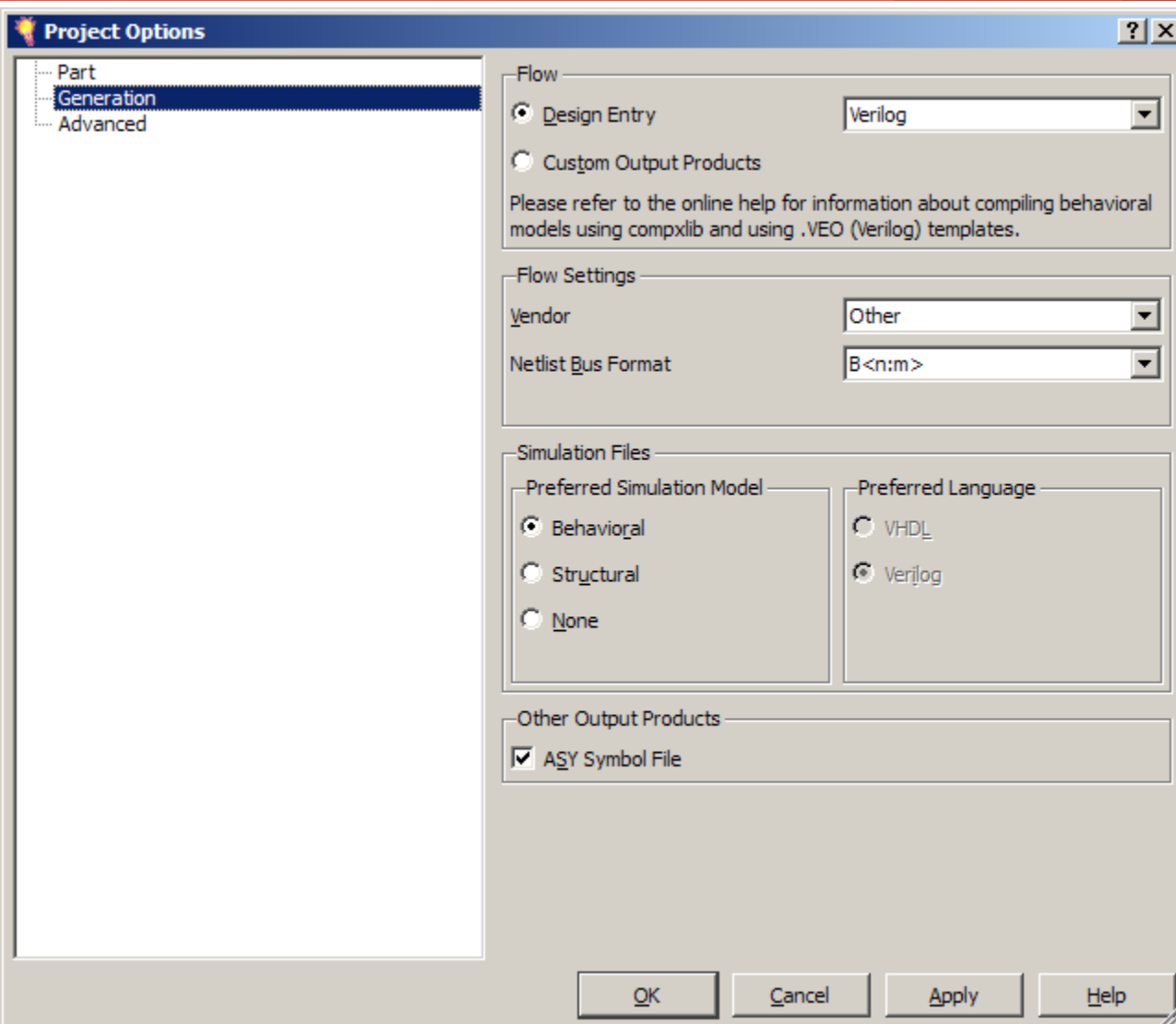
Generate MIG Example Design



- **Select Part**
- **Set the Part (as shipped on the ML605):**
 - Family: Virtex6
 - Device: xc6vlx240t
 - Package: ff1156
 - Speed Grade: -1
- **Select Generation**

Note: Presentation applies to the ML605

Generate MIG Example Design

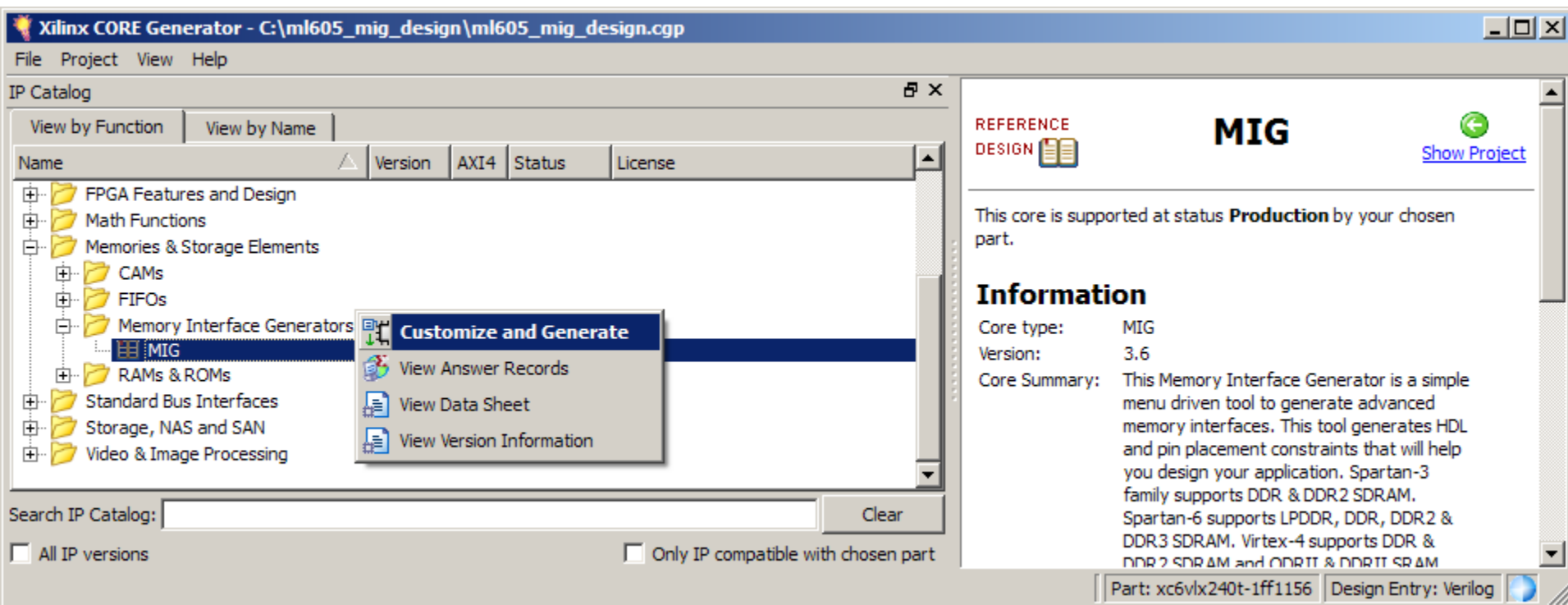


- **Under Generation**
 - Set the Design Entry to Verilog
- **Click OK**

Note: Presentation applies to the ML605

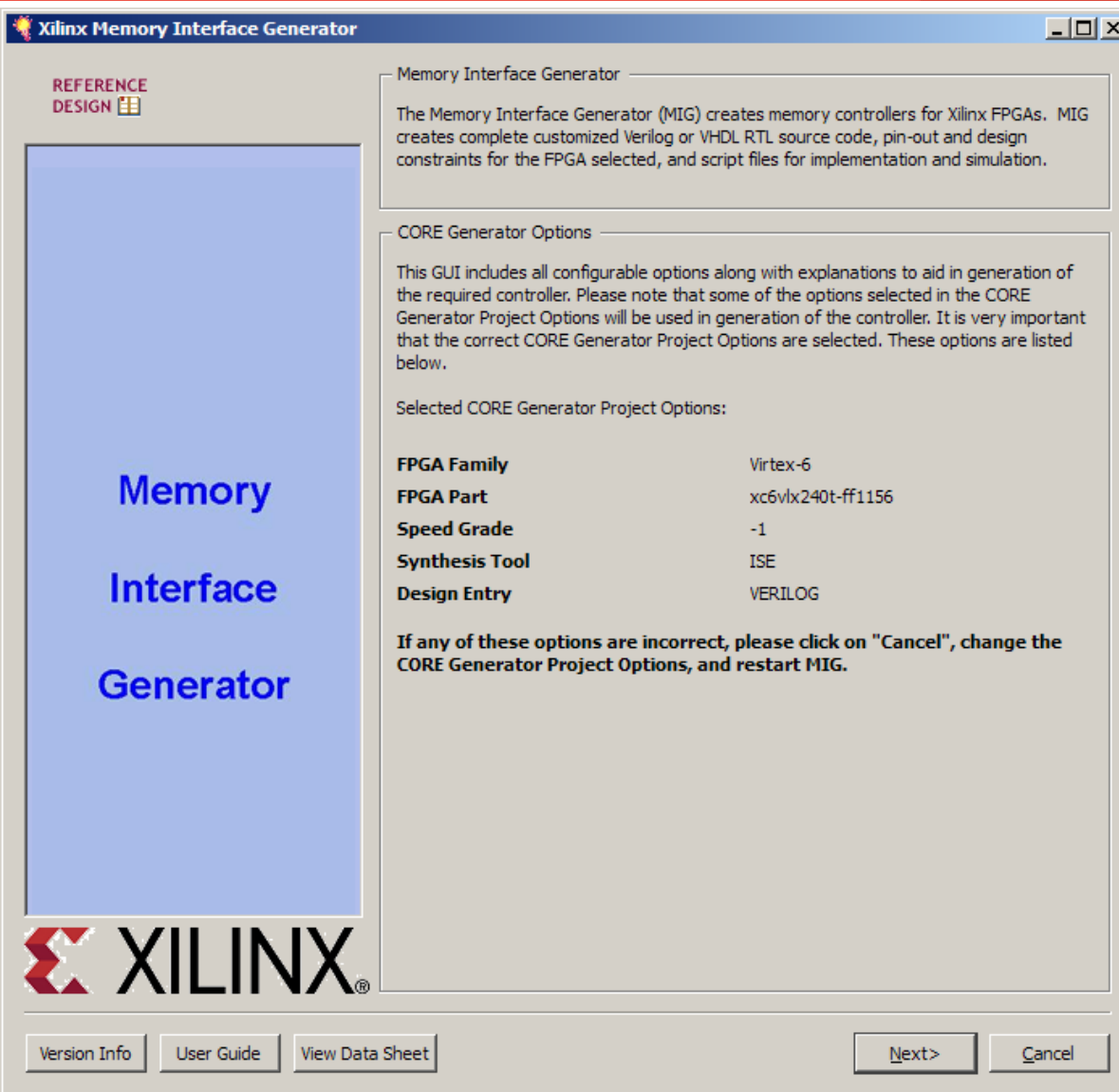
Generate MIG Example Design

- Right click on MIG Version 3.6
 - Select **Customize and Generate**



Note: Presentation applies to the ML605

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Memory Interface Generator

XILINX

MIG Output Options

☒ **Create Design**

Select this option to generate a new memory controller. Generating a memory controller will create RTL, design constraints (UCF), implementation and simulation files.

☐ **Xilinx Reference Boards**

Select this option for information on specific designs for Xilinx reference boards.

☐ **Verify UCF and Update Design and UCF**

Selecting this feature verifies the modified UCF for a design already generated through MIG. It updates the input UCF file to be compatible with the current version of MIG. While updating the UCF it preserves the pin outs of the input UCF. This option will also generate the new design with the Component Name you selected in this page.

Component Name

Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design", "user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.

Component Name mig_v3_6

Multi-Controller

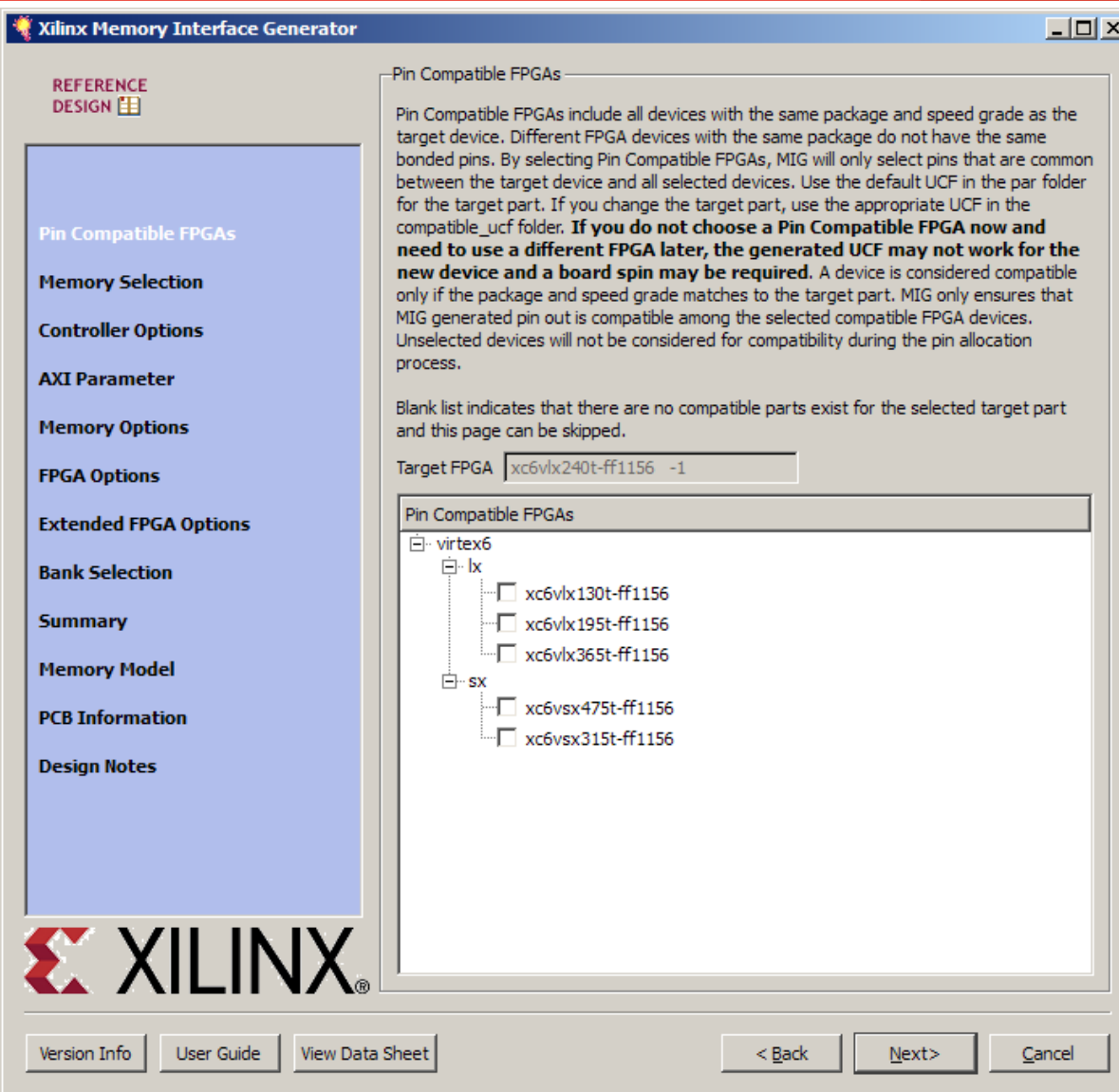
Up to 8 DDR3 SDRAM controllers or 8 QDRII+ SRAM controllers or a combination of both can be generated. DDR2 and RDRAM II are not supported for more than 1 controller. The number of controllers that can be accommodated may be limited by the data width and the number of banks utilized.

Number of Controllers 1

Version Info User Guide View Data Sheet < Back Next > Cancel

- Leave this page as is
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design



■ Select Memory Type

- DDR3 SDRAM
- Click Next

Generate MIG Example Design

Options for Controller 0 - DDR3 SDRAM

Frequency: The allowed frequency range is a function of the selected FPGA part, FPGA speed grade, and memory controller type. Choose the clock period for the desired frequency. Refer to User Guide for supported frequency range.

2500 ps 400.00 MHz

The frequency range shown here is preliminary value. Final range will be determined after characterization.

Memory Type: Select the memory type. Parts marked with a warning symbol are not compatible with the frequency selection above. Based on the FPGA package, DIMMs selection is not allowed due to the unavailability of required number of pins. For RDRAM II only CIO parts are supported.

SODIMMs

Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part you want is not listed here. The "Create Custom Part" feature is not supported for RDRAM II.

MT4JSF6464HY-1G1

Create Custom Part

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.

64

ECC: MIG supports ECC for 72 bit and 144 bit data width configurations. To be able to select ECC, you will need to select a data width that has ECC supported.

Disabled

Data Mask: You will be able to enable/disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part you have selected has DM pins. Uncheck this box if you would like to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs will not use Data Mask.

☒

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.

Strict

Memory Details: 512MB, x16, row:13, col:10, bank:3, unbuffered, data bits per strobe:8, with data mask, single rank

a Sheet

< Back Next > Cancel

■ Select

- Type: SODIMMs
- Part: MT4JSF6464HY-1G1
- Ordering: Strict

Generate MIG Example Design

Memory Options for Controller 0 - DDR3 SDRAM

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Burst Length
Determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

8 - Fixed

Read Burst Type
The ordering of accesses within a burst is determined by the burst type.

Sequential

Output Driver Impedance Control
Programmable impedance for the output buffer.

RZQ/7

RTT (nominal) - On Die Termination (ODT)
Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the DIMM. This value will be used for the unwritten slot during a write in 2 slot configurations. The value will also be used for the unselected slot during a read in 2 slot configurations. Use board level simulation to choose the optimum value. The default is the value listed at the JEDEC 2007 DDR3 Workshop (http://www.jedecddr3.org/Todd_Farreell_ODT_And_Dynamic_ODT.pdf).

RZQ/4

[Data Sheet](#) [< Back](#) [Next >](#) [Cancel](#)

- Leave this page as is
 - Click Next

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Pin Compatible FPGAs ✓

Memory Selection ✓

Controller Options ✓

AXI Parameter

Memory Options ✓

FPGA Options

Extended FPGA Options

Bank Selection

Summary

Memory Model

PCB Information

Design Notes

XILINX

Version Info User Guide View Data Sheet

< Back Next > Cancel

System Clock

Choose the desired input clock configuration. Both Design clock and Idelay Control clock will be affected. Either both the clocks can be Differential or both can be Single-Ended.

System Clock Differential

Debug Signals Control

This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. The debug signals width is calibrated based on the selected design data width. If the design data width is greater than 72 bit and/or the number of DQS/DQS# pins of the design is greater than 18, then the debug signals width is calibrated only for first 72 bits of data.

Debug Signals for Memory Controller ON

IODELAY Power Versus Performance

Choose **High** Performance Mode for lowest IODELAY jitter and maximum interface performance. Choose **Normal** Performance Mode to reduce power by approximately "(TBD)" per pin when interface performance requirements are less stringent.

Performance Mode HIGH

Internal Vref

Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This can free 2 pins per bank where inputs are used. In some topologies these 2 additional free pins will improve bank utilization. This setting has no effect on banks with only outputs.

Internal Vref ☐

- **Select**
 - Debug: ON

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- AXI Parameter
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options
- Bank Selection
- Summary
- Memory Model
- PCB Information
- Design Notes

DDR3 SDRAM

Digitally Controlled Impedance (DCI)

The DCI (Digitally Controlled Impedance) I/O Standard is applied only for certain signals in Data group banks. In Address/Control group bank, DCI Standard is not applied on any signals. In Data group bank, only DQ and DQS/DQS# signals have DCI Standards (SSTL15_T_DCI for DQ's and DIFF_SSTL15_T_DCI for DQS and DQS#). If VRN/VRP pins in Data group banks are utilized, then DCI Cascading have to be applied. In such scenario, you have to select a Master Bank from the drop down box in the bank selection page. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy.

Pin/Bank Selection Mode

- ☒ New Design: Pick the optimum banks for a new design
- ☐ Fixed Pin Out: Pre-existing pin out is known and fixed

Version Info User Guide View Data Sheet < Back Next > Cancel

- **Select New Design**
 - Click Next

Generate MIG Example Design

Bank Selections | Description

Bank Selection For Controller 0 - DDR3 SDRAM

Address/Control: 25/25 ✓ Data: 96/96 ✓ System Clock: 9/9 ✓

Master Bank [Dropdown] Master Bank [Dropdown] Master Bank [Dropdown]

Left Column **Inner Left Column** **Inner Right Column**

Bank	Available IOs	Address/Control	Data	System Clock
Bank: 16	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 15	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 14	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 26	2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 25	14	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 24*	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 36	2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 35	13	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 34*	31	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

*Bank 24 and 34 contain configuration pins. MIG tries to avoid usage of these banks for default configurations. If bank 24 or 34 is selected for your memory controller, UCF should be verified to ensure no conflicts with the configuration pin.

Notes:
Press "Next" to proceed.

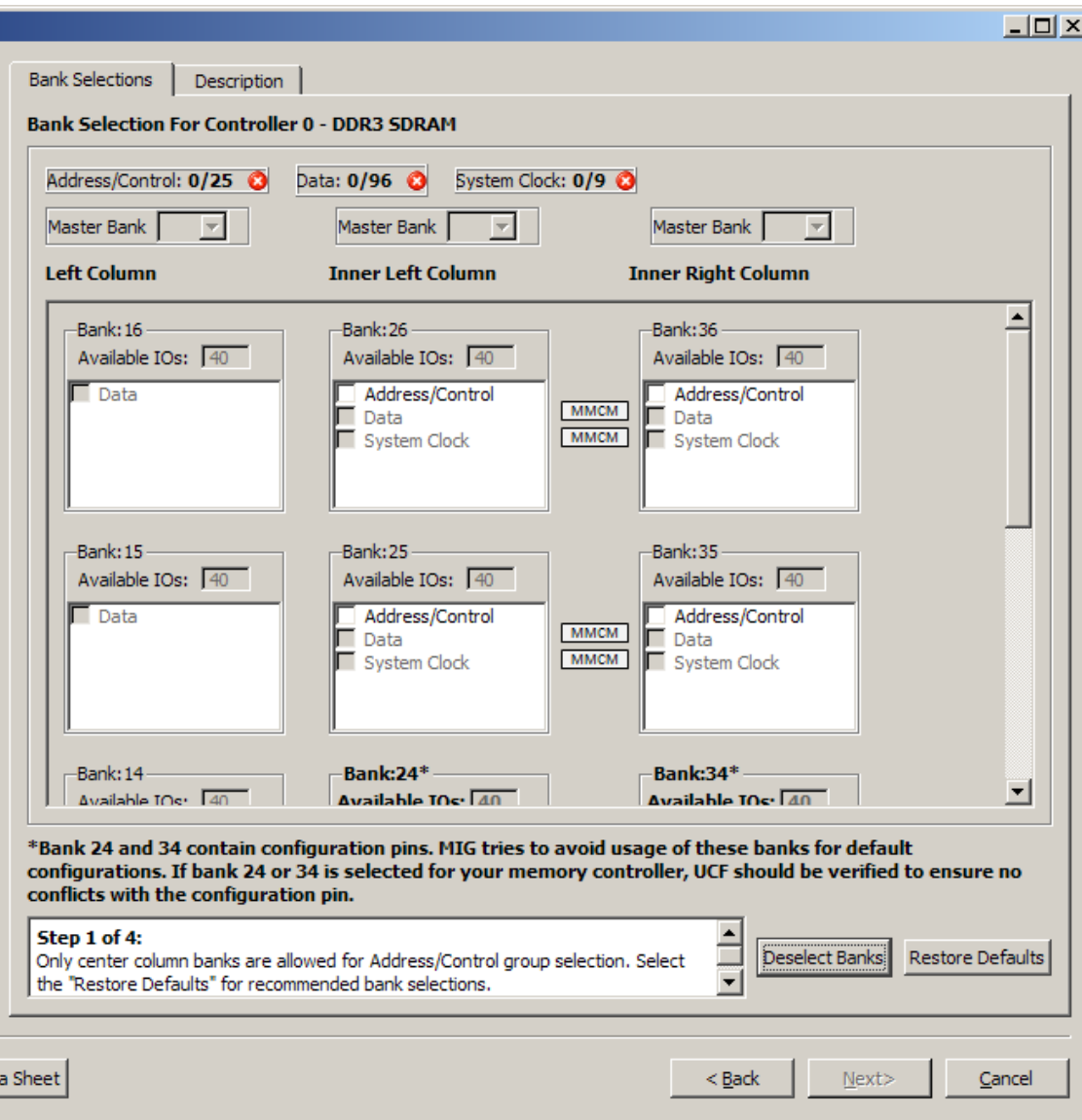
Deselect Banks Restore Defaults

< Back Next > Cancel

- On this screen select the banks as used on the ML605 SODIMM interface
- Click Deselect Banks

Generate MIG Example Design

- All Banks Deselected



The image shows a software window titled "Bank Selection For Controller 0 - DDR3 SDRAM". It has two tabs: "Bank Selections" (active) and "Description".

At the top, there are three status indicators: "Address/Control: 0/25" with a red 'x', "Data: 0/96" with a red 'x', and "System Clock: 0/9" with a red 'x'. Below these are three "Master Bank" dropdown menus, all of which are empty.

The main area is divided into three columns: "Left Column", "Inner Left Column", and "Inner Right Column". Each column contains three bank selection boxes:

- Left Column:** Bank: 16, Bank: 15, and Bank: 14. Each has an "Available IOs: 40" label and a "Data" checkbox.
- Inner Left Column:** Bank: 26, Bank: 25, and Bank: 24*. Each has an "Available IOs: 40" label and checkboxes for "Address/Control", "Data", and "System Clock".
- Inner Right Column:** Bank: 36, Bank: 35, and Bank: 34*. Each has an "Available IOs: 40" label and checkboxes for "Address/Control", "Data", and "System Clock".

Between the Inner Left and Inner Right columns, there are two "MMCM" labels.

At the bottom, there is a text box with the following text: "Step 1 of 4: Only center column banks are allowed for Address/Control group selection. Select the 'Restore Defaults' for recommended bank selections." To the right of this text box are two buttons: "Deselect Banks" and "Restore Defaults".

At the very bottom of the window are three buttons: "< Back", "Next >", and "Cancel".

Generate MIG Example Design

Bank Selections | Description

Bank Selection For Controller 0 - DDR3 SDRAM

Address/Control: 25/25 ✓ Data: 0/96 ✗ System Clock: 0/9 ✗

Master Bank [▼] Master Bank [▼] Master Bank [▼]

Left Column	Inner Left Column	Inner Right Column
<p>Bank: 16</p> <p>Available IOs: 40</p> <p><input type="checkbox"/> Data</p>	<p>Bank: 26</p> <p>Available IOs: 40</p> <p><input type="checkbox"/> Address/Control</p> <p><input type="checkbox"/> Data</p> <p><input type="checkbox"/> System Clock</p> <p>MMCM</p> <p>MMCM</p>	<p>Bank: 36</p> <p>Available IOs: 14</p> <p><input checked="" type="checkbox"/> Address/Control</p> <p><input type="checkbox"/> Data</p> <p><input type="checkbox"/> System Clock</p>
<p>Bank: 15</p> <p>Available IOs: 40</p> <p><input type="checkbox"/> Data</p>	<p>Bank: 25</p> <p>Available IOs: 40</p> <p><input type="checkbox"/> Address/Control</p> <p><input type="checkbox"/> Data</p> <p><input type="checkbox"/> System Clock</p> <p>MMCM</p> <p>MMCM</p>	<p>Bank: 35</p> <p>Available IOs: 40</p> <p><input type="checkbox"/> Address/Control</p> <p><input type="checkbox"/> Data</p> <p><input type="checkbox"/> System Clock</p>
<p>Bank: 14</p> <p>Available IOs: 40</p>	<p>Bank: 24*</p> <p>Available IOs: 40</p>	<p>Bank: 34*</p> <p>Available IOs: 40</p>

*Bank 24 and 34 contain configuration pins. MIG tries to avoid usage of these banks for default configurations. If bank 24 or 34 is selected for your memory controller, UCF should be verified to ensure no conflicts with the configuration pin.

Step 2 of 4:

Banks inside the box are allowed for Data group selection. Center column banks are recommended for Data group selection for best performance.

[Deselect Banks] [Restore Defaults]

< Back Next > Cancel

- **Select**
 - Bank 36: Address/Control

Generate MIG Example Design

Bank Selections | Description

Bank Selection For Controller 0 - DDR3 SDRAM

Address/Control: 25/25 ✓ Data: 96/96 ✓ System Clock: 0/9 ✗

Master Bank [] Master Bank [] Master Bank []

Left Column **Inner Left Column** **Inner Right Column**

Bank	Available IOs	Address/Control	Data	System Clock
Bank: 16	40			
Bank: 26	1		✓	
Bank: 36	14	✓		
Bank: 15	40			
Bank: 25	2		✓	
Bank: 35	14		✓	
Bank: 14	40			
Bank: 24*	40			
Bank: 34*	40			

*Bank 24 and 34 contain configuration pins. MIG tries to avoid usage of these banks for default configurations. If bank 24 or 34 is selected for your memory controller, UCF should be verified to ensure no conflicts with the configuration pin.

Step 3 of 4:
Select System Clock groups from the enabled banks. Banks outside the vicinity box can also be selected, if enabled.

Deselect Banks Restore Defaults

< Back Next > Cancel

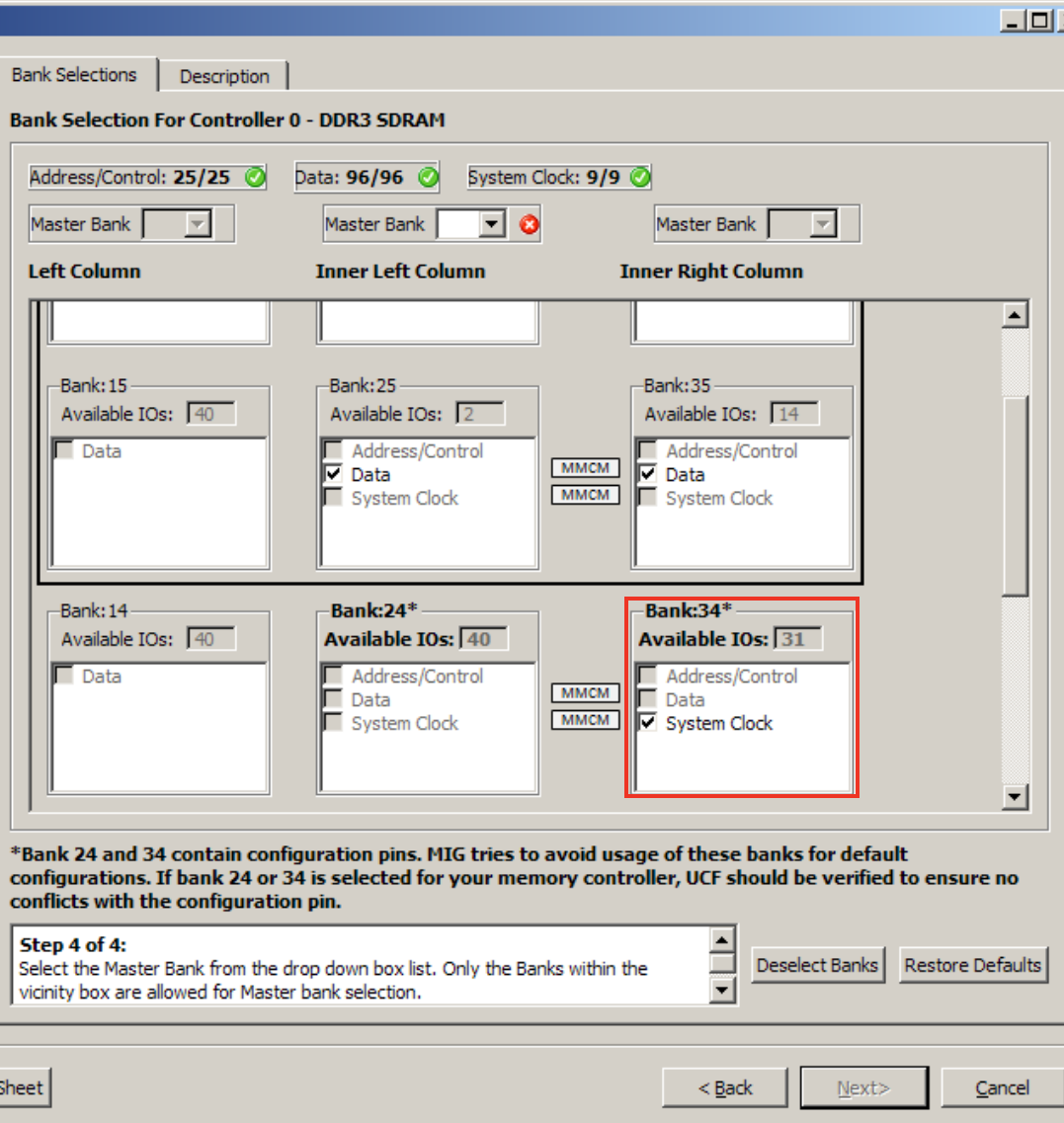
■ Select

- Bank 26: Data
- Bank 25: Data
- Bank 35: Data

Generate MIG Example Design

■ Select

- Bank 34: System Clock



The image shows a software window titled "Bank Selection For Controller 0 - DDR3 SDRAM". It has two tabs: "Bank Selections" (active) and "Description".

At the top, there are three status indicators: "Address/Control: 25/25" with a green checkmark, "Data: 96/96" with a green checkmark, and "System Clock: 9/9" with a green checkmark. Below these are three "Master Bank" dropdown menus. The first and third are empty, while the middle one has a red 'x' icon.

The main area is divided into three columns: "Left Column", "Inner Left Column", and "Inner Right Column". Each column contains a list of banks with their "Available IOs" and a list of functions to be selected.

Column	Bank	Available IOs	Selected Functions
Left Column	Bank: 15	40	Data
	Bank: 14	40	Data
Inner Left Column	Bank: 25	2	Address/Control, Data, System Clock
	Bank: 24*	40	Address/Control, Data, System Clock
Inner Right Column	Bank: 35	14	Address/Control, Data, System Clock
	Bank: 34*	31	Address/Control, Data, System Clock

*Bank 24 and 34 contain configuration pins. MIG tries to avoid usage of these banks for default configurations. If bank 24 or 34 is selected for your memory controller, UCF should be verified to ensure no conflicts with the configuration pin.

At the bottom, there is a "Step 4 of 4:" section with instructions: "Select the Master Bank from the drop down box list. Only the Banks within the vicinity box are allowed for Master bank selection." Below this are "Deselect Banks" and "Restore Defaults" buttons.

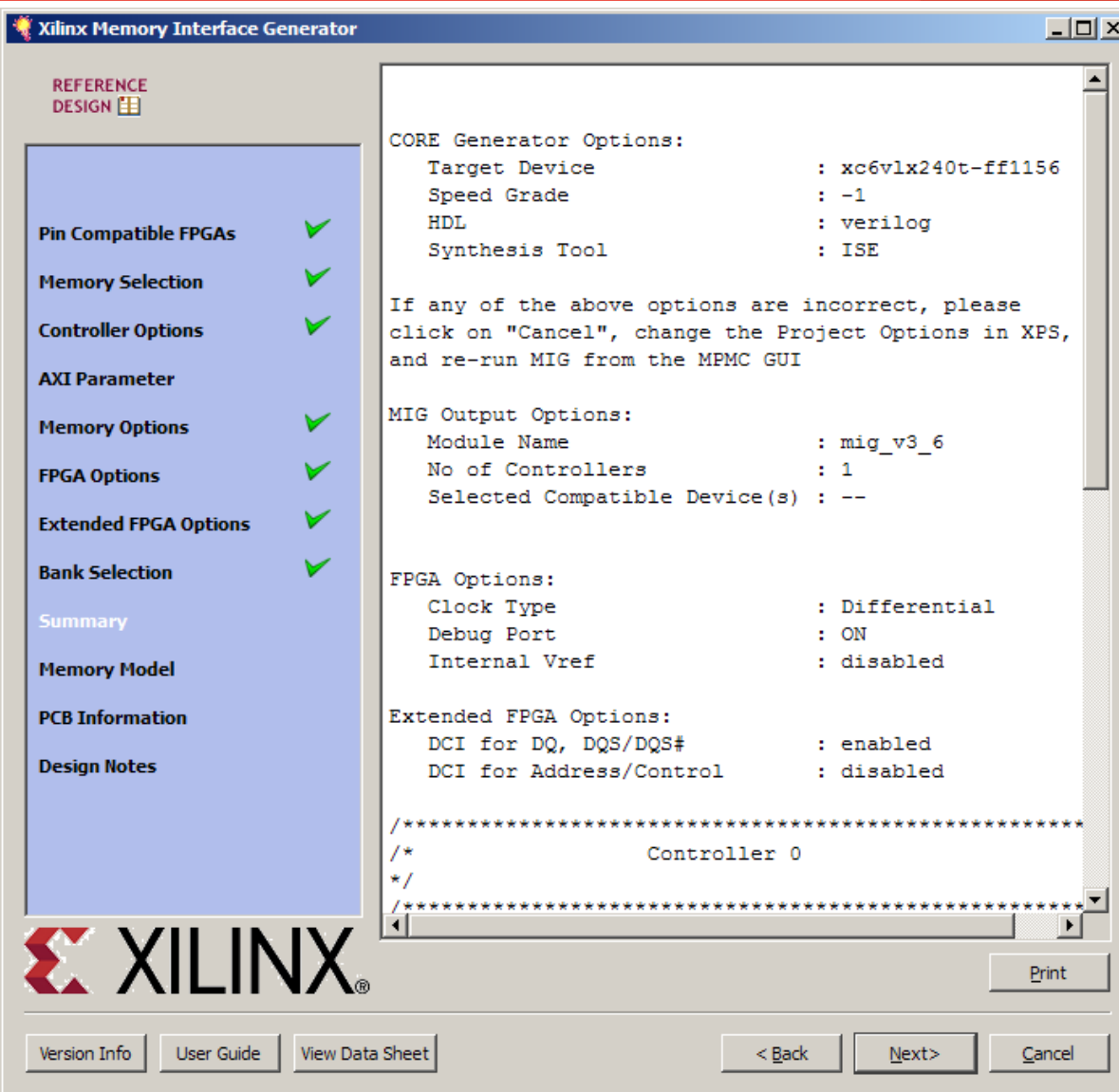
The bottom of the window has navigation buttons: "< Back", "Next >", and "Cancel".

Generate MIG Example Design

a Sheet

- **Select**
 - Master Bank: 25
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design

The screenshot shows the Xilinx Memory Interface Generator (MIG) software window. The title bar reads "Xilinx Memory Interface Generator". On the left is a sidebar with a "REFERENCE DESIGN" icon and a list of configuration steps, each with a green checkmark: "Pin Compatible FPGAs", "Memory Selection", "Controller Options", "AXI Parameter", "Memory Options", "FPGA Options", "Extended FPGA Options", "Bank Selection", "Summary", "Memory Model", "PCB Information", and "Design Notes". The main area displays the "Micron Technology, Inc. Simulation Model License Agreement". The text includes a paragraph about the simulation model license agreement, followed by a "SOFTWARE LICENSE" section and a "MODEL LICENSE" section. At the bottom of the main area, there is a "Print" button. Below the main area, there is a checkbox for "Accept" and a radio button for "Decline". At the very bottom, there are buttons for "Version Info", "User Guide", "View Data Sheet", "< Back", "Next >", and "Cancel".

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- AXI Parameter
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options ✓
- Bank Selection ✓
- Summary ✓
- Memory Model
- PCB Information
- Design Notes

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Print

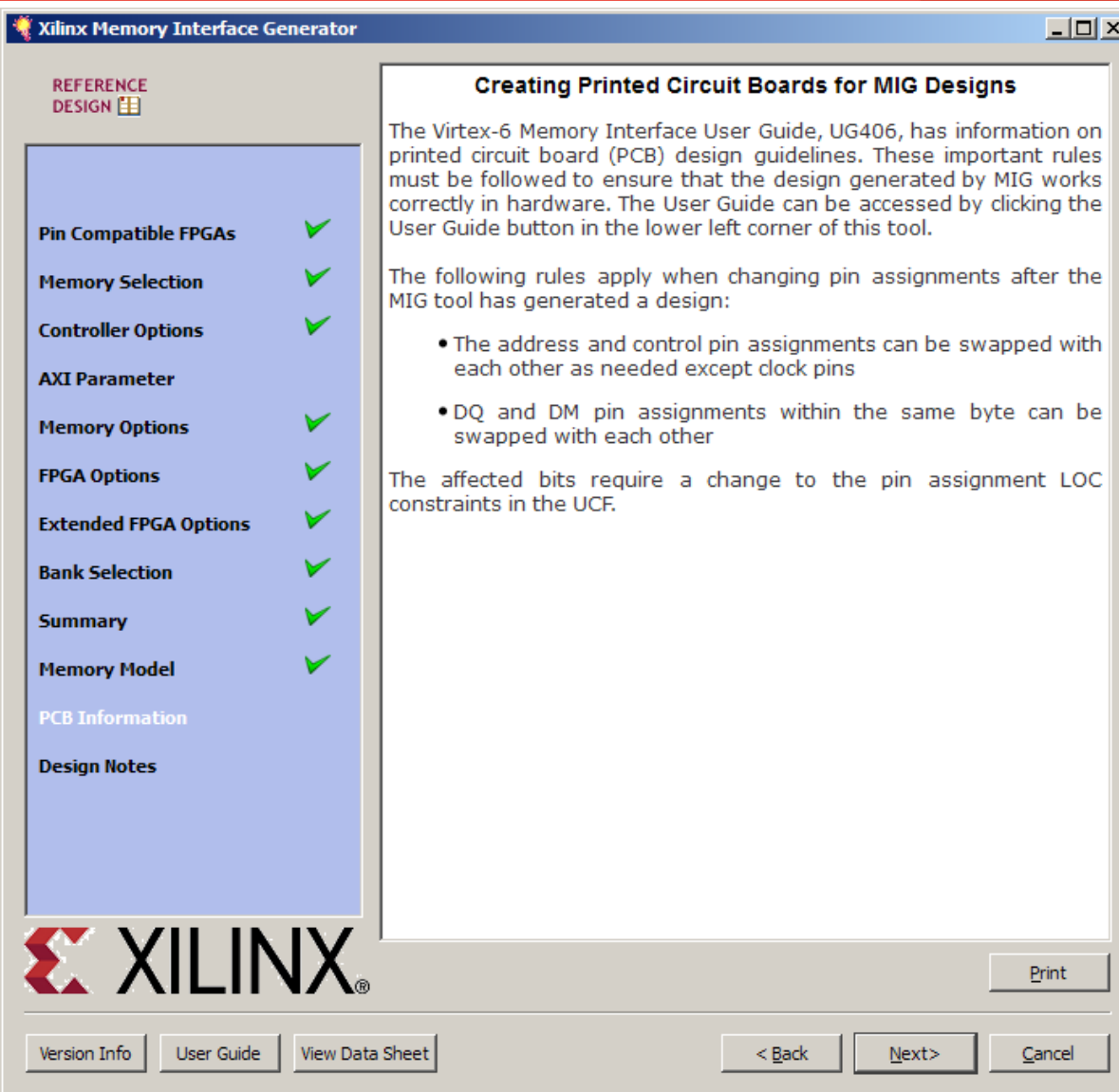
☒ Accept ☐ Decline

Check Accept or Decline to proceed. By clicking Accept, memory model will be outputted in output simulation directory. By clicking Decline, you will need to acquire and configure a memory model appropriately.

Version Info User Guide View Data Sheet < Back Next > Cancel

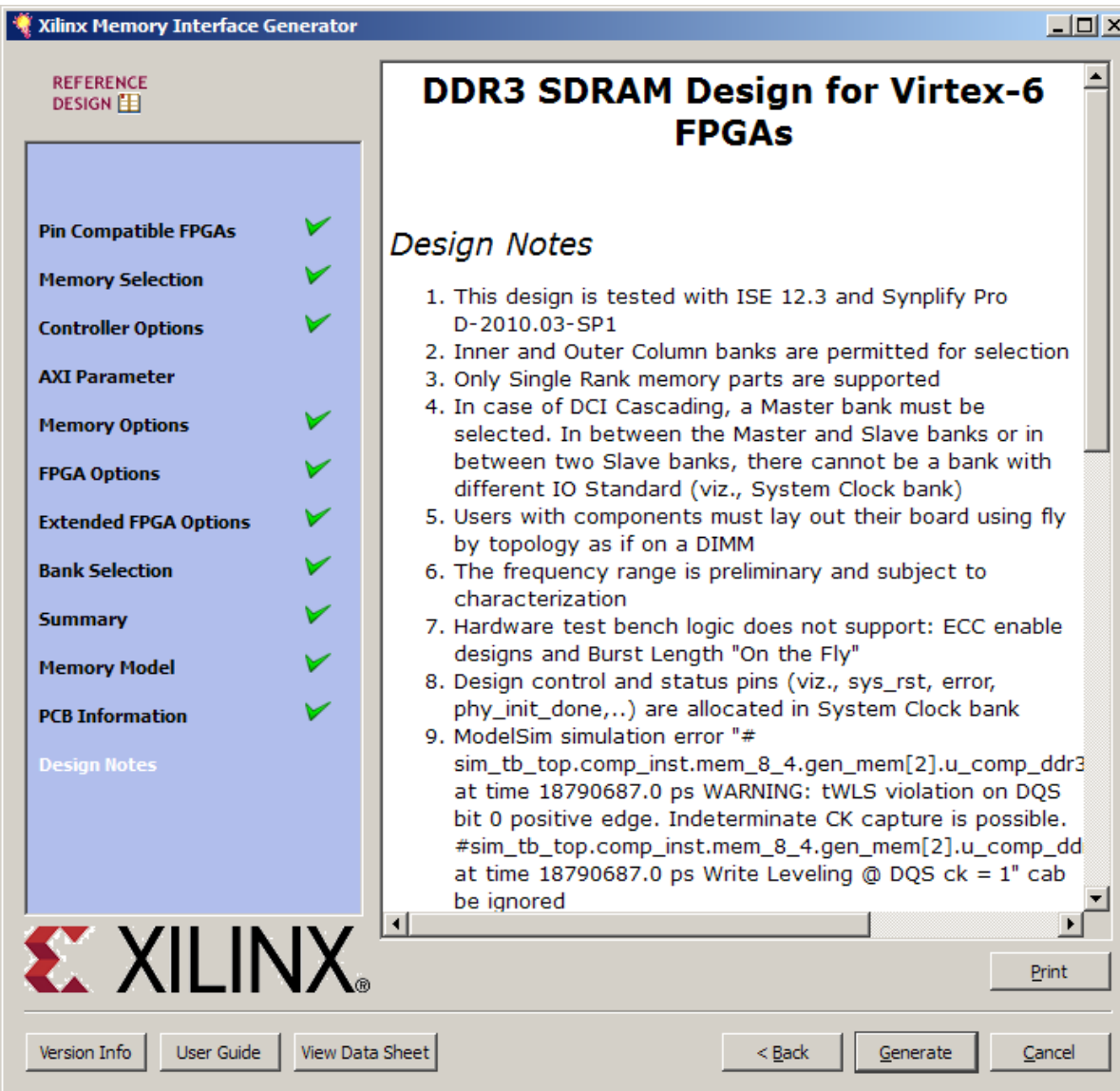
- **Accept Simulation license, if desired**
 - Otherwise, Decline license
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

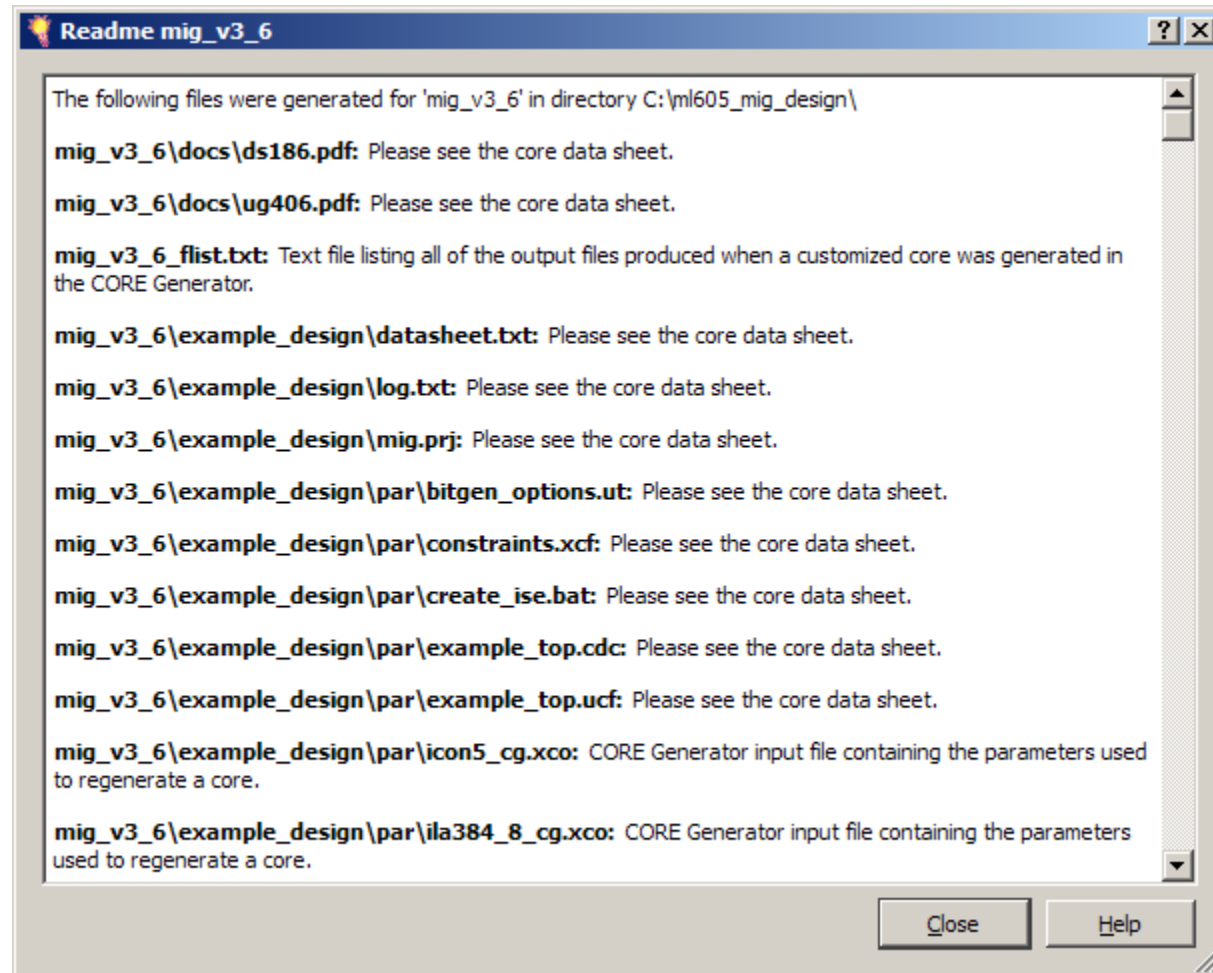
Generate MIG Example Design



■ Click Generate

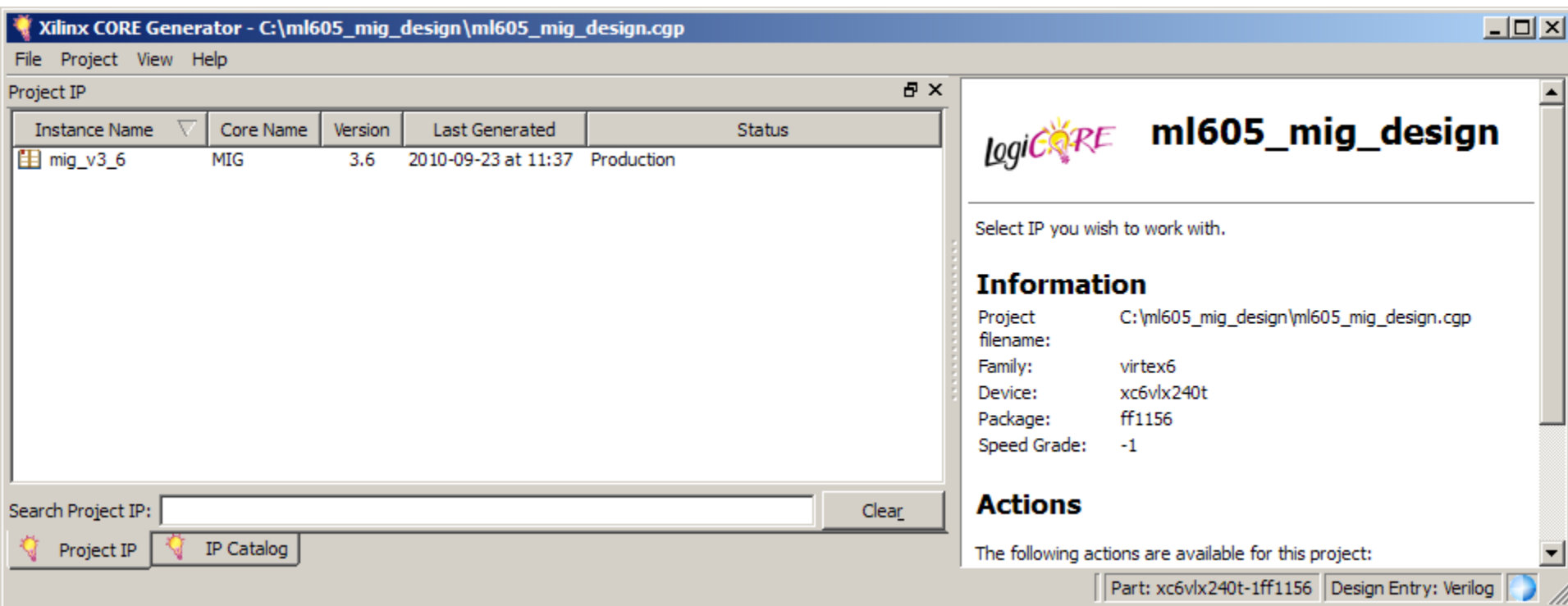
Generate MIG Example Design

- After the MIG core finishes generating, click Close on the Datasheet window



Generate MIG Example Design

- MIG design appears in Project IP



Note: Presentation applies to the ML605

Modifications to Example Design

- **RDF0011.zip includes**

- ChipScope Project File, UCF, and Verilog Files

- **Modifications to RTL Files for ML605 Example Design**

- Changed design to support a single 200 MHz LVDS clock input
- Added Debug display code to drive LEDs
- Added ChipScope ILA and VIO port assignments for ML605 board debug
- Removed IIC Signals – sda, scl
- Changed various parameter to match the ML605 board
 - DIVCLK_DIVIDE = 1 (was 2)
 - nDQS_COLx
 - DQS_LOC_COLx
 - RST_ACT_LOW = 0 (was 1)

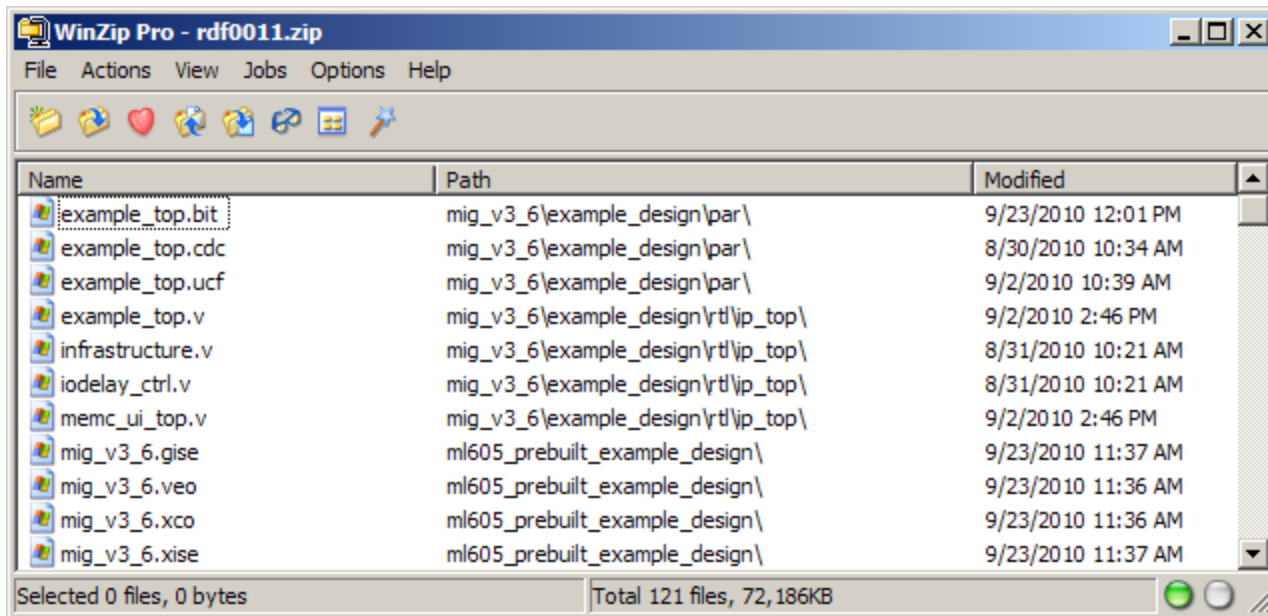
Modifications to Example Design

▪ Updates to UCF file specifically required for ML605 board:

- Updated IO Locations to match ML605
- Remove IIC Signals – sda, scl
- Merged Default two clocks into one clock for ML605
- Moved sys_reset to CPU_RESET
- Edited DCI_CASCADE to match ML605
- Removed CONFIG_PROHIBIT lines
- Added LOC for GPIO LED signals (2.5V bank voltage)
- Added LOCs for RSYNC OSERDES and IODELAY

Modifications to Example Design

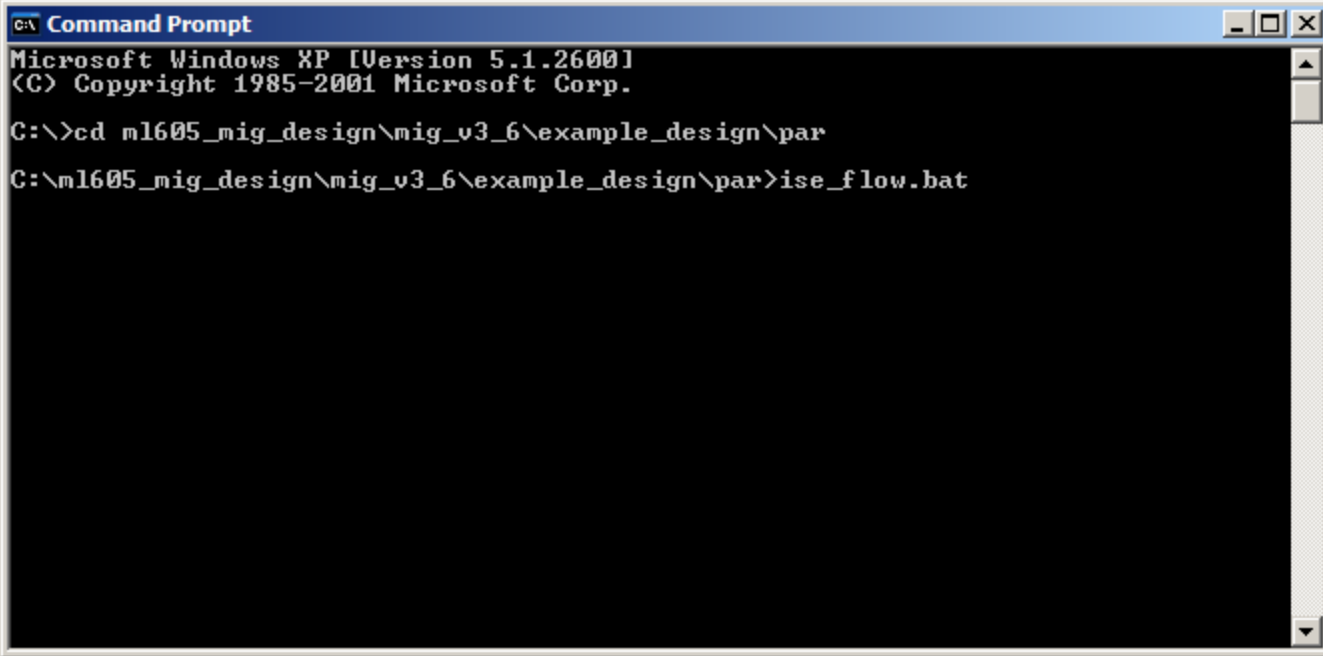
- **Unzip the rdf0011.zip file to your C:\ml605_mig_design directory**
 - Available through <http://www.xilinx.com/ml605>
 - This adds modifications to the example design (1)
 - A fully pre-built ML605 example design is included in the zip file (2)
 - Use the included bitstream to [run MIG with ChipScope](#)
 - Run **ise_flow.bat** in <design directory>\ml605_prebuilt_example_design\mig_v3_6\example_design\par to recompile the pre-built example design



Compile Example Design

- Start a windows command shell and enter these commands:

```
cd ml605_mig_design\mig_v3_6\example_design\par  
ise_flow.bat
```



```
C:\> Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd ml605_mig_design\mig_v3_6\example_design\par
C:\ml605_mig_design\mig_v3_6\example_design\par>ise_flow.bat
```

Run MIG Example Design

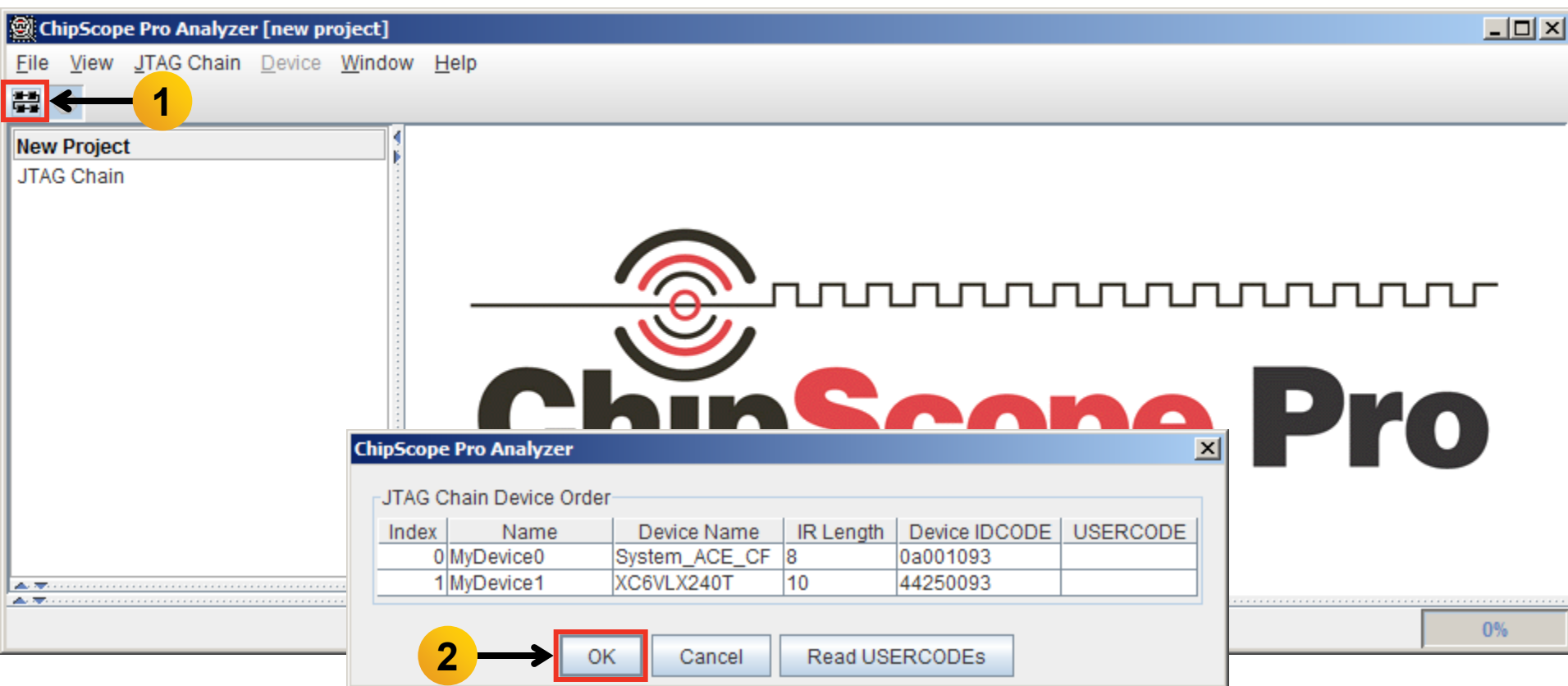
- Power on the ML605 board
- Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board
 - Connect this cable to your PC



Note: Presentation applies to the ML605

Run MIG Example Design

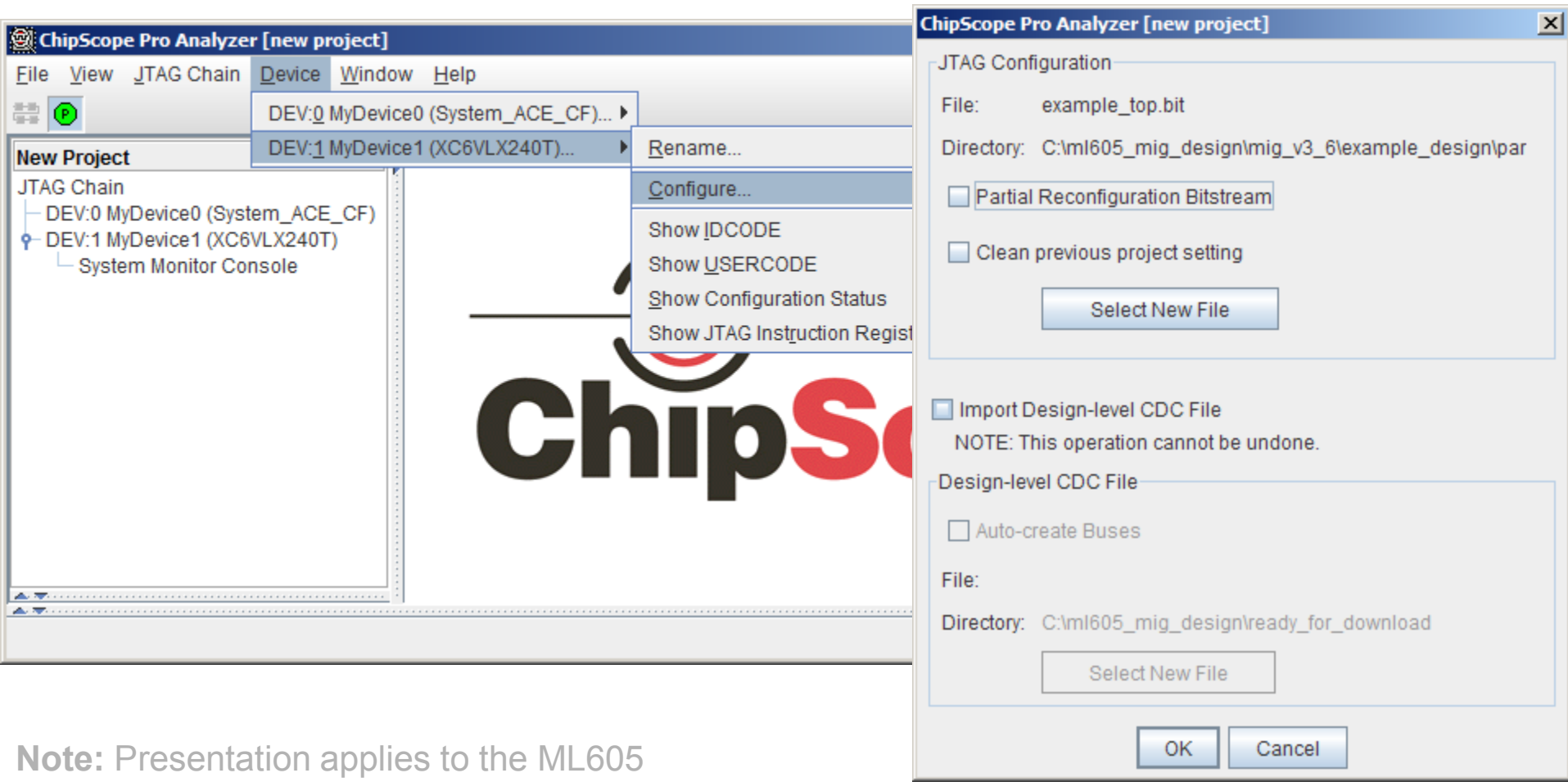
- **After the design compiles, open ChipScope Pro Analyzer**
 - Click on the Open Cable Button (1)
 - Click OK (2)



Note: Presentation applies to the ML605

Run MIG Example Design

- Select Device → DEV:0 MyDevice0 (XC6VLX240T) → Configure...
- Select <Design Path>\mig_v3_6\example_design\par\example_top.bit



Note: Presentation applies to the ML605

Run MIG Example Design

- **Select File → Open Project...**
- **Select <Design Path>\ready_for_download\ML605_SODIMM_example_design.cpj**



Note: Presentation applies to the ML605

Run MIG Example Design

- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1

The screenshot displays the ChipScope Pro Analyzer interface for the project **ML605_SODIMM_example_design**. The **Trigger Setup** window is active, showing the configuration for **DEV:1 MyDevice1 (XC6VLX240T) UNIT:0 MyILA0 (ILA)**.

Match Unit Table:

Match Unit	Function	Value	Radix	Counter
M0:TRIG0	==	XX1X_XXXX	Bin	disabled
/TRIG0[7]			X	
/TRIG0[6]			X	
error			1	
/dfi_init_complete			X	
/dbg_rdlvl_err[1]			X	
/dbg_rdlvl_err[0]			X	
/dbg_rdlvl_done[1]			X	
/dbg_rdlvl_done[0]			X	

Capture Settings:

- Type: Window
- Windows: 1
- Depth: 1024
- Position: 512
- Storage Qualification: All Data

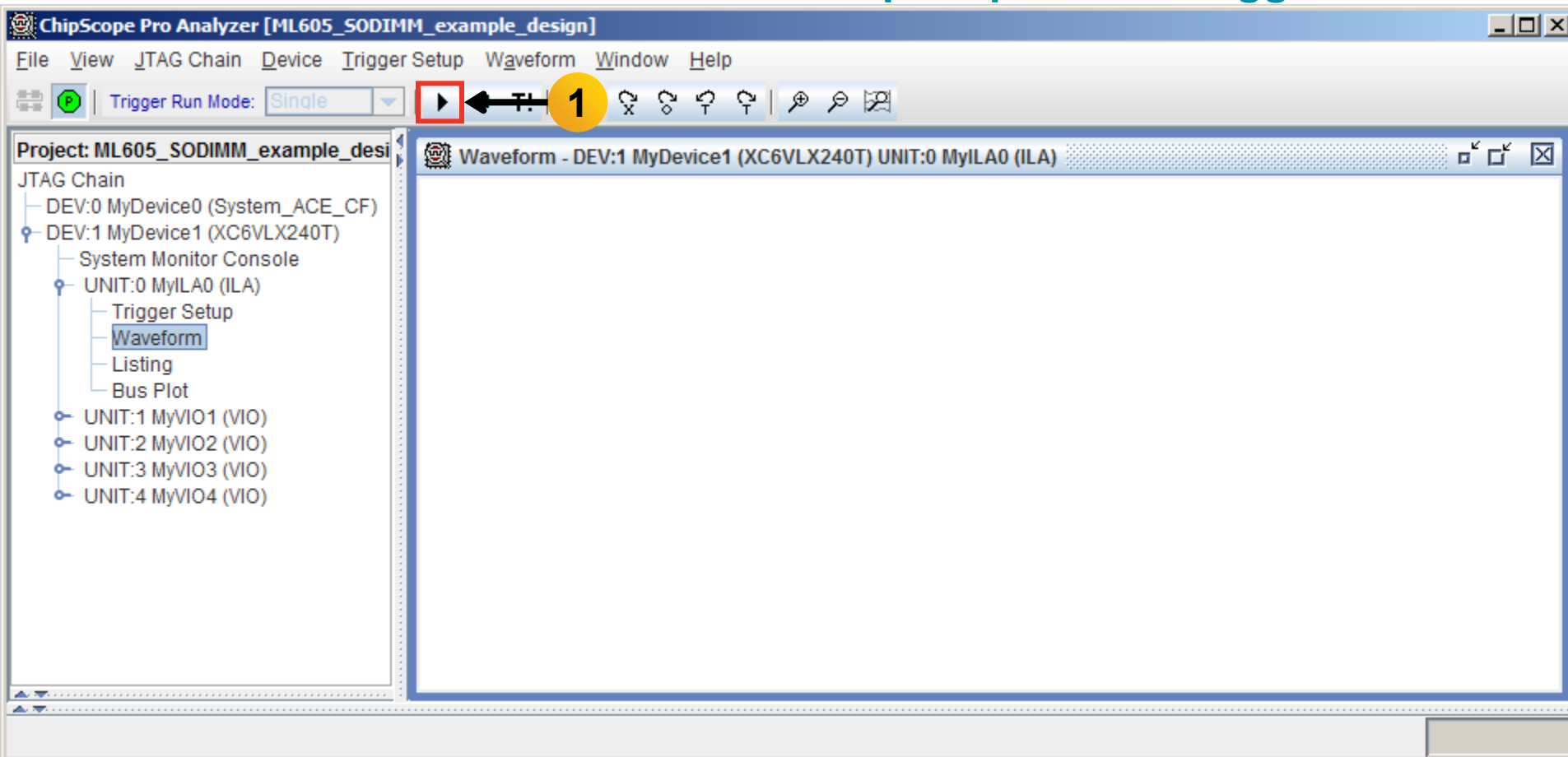
Trigger Conditions:

The status bar at the bottom indicates the device is in **IDLE** state.

Reading project file: C:\ml605_mig_design\ready_for_download\ML605_SODIMM_example_design.cpj

Run MIG Example Design

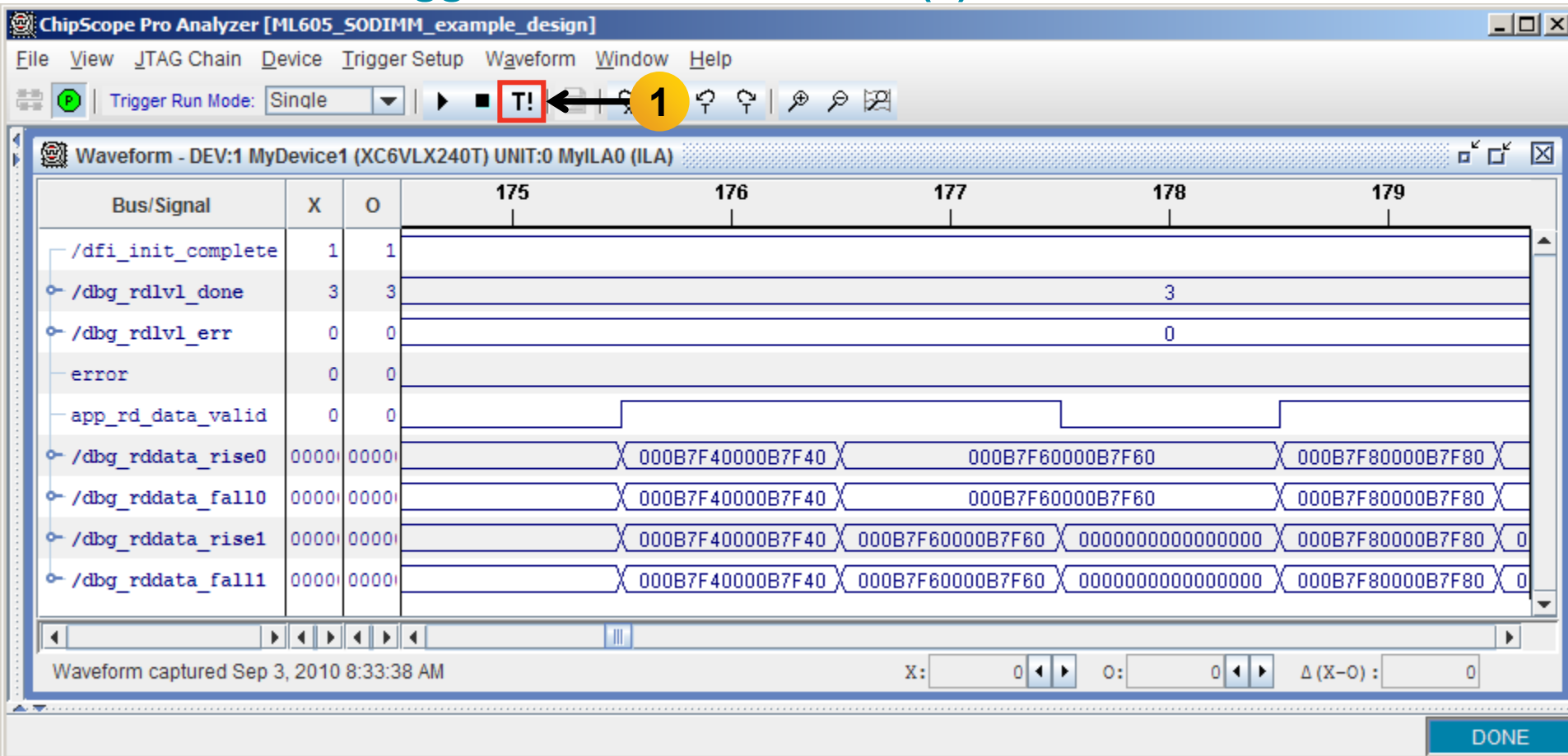
- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger



Note: Presentation applies to the ML605

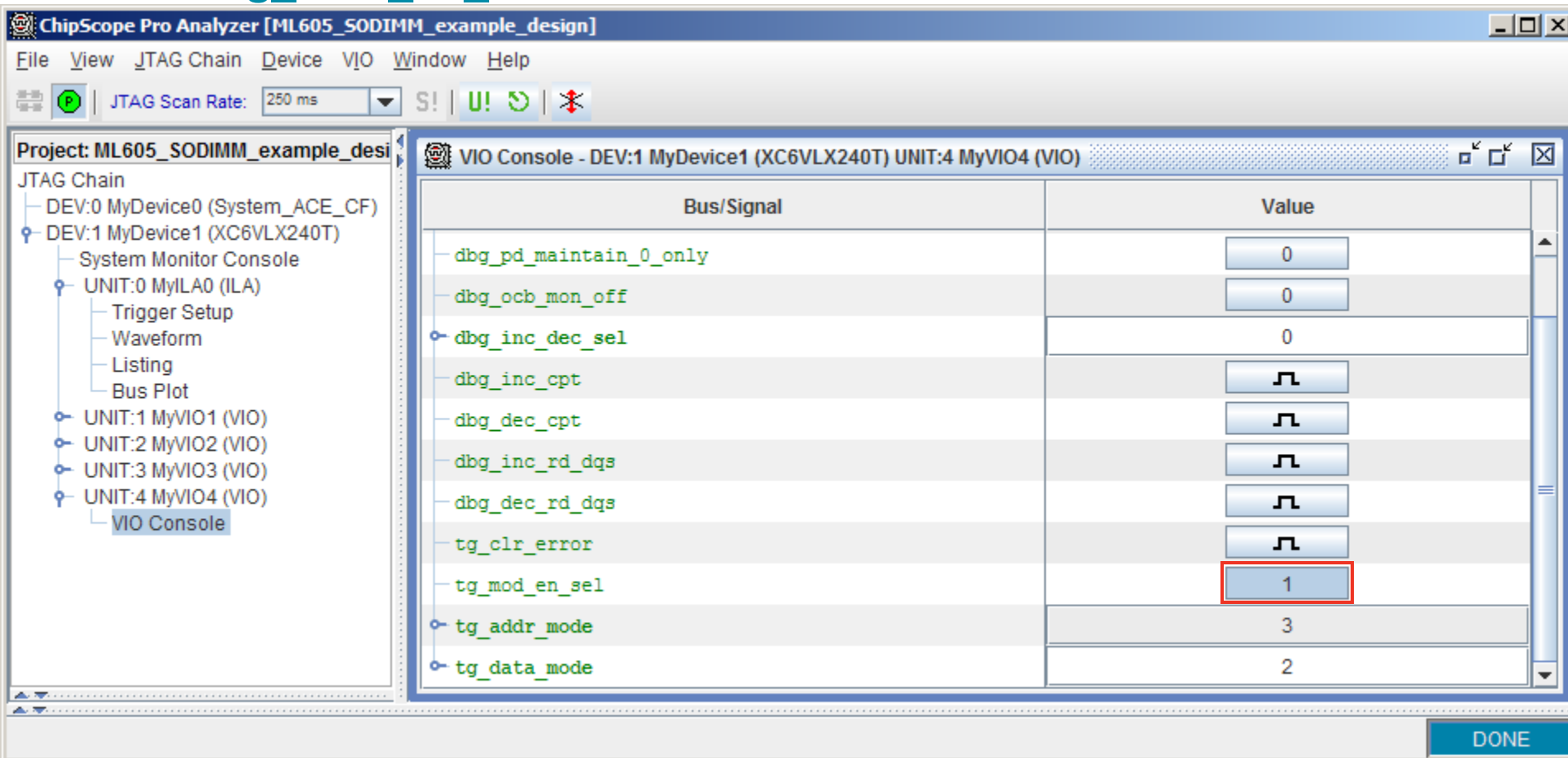
Run MIG Example Design

- The Example Design should run error free (no trigger on error)
- To force a trigger, click the T! button (1)



Adjust Data Pattern using VIO Console

- Select VIO Console 4
- Set `tg_mod_en_sel` to 1



The screenshot shows the ChipScope Pro Analyzer interface for the project `ML605_SODIMM_example_design`. The JTAG Chain on the left lists the following components:

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6VLX240T)
 - System Monitor Console
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - UNIT:2 MyVIO2 (VIO)
 - UNIT:3 MyVIO3 (VIO)
 - UNIT:4 MyVIO4 (VIO)
 - VIO Console

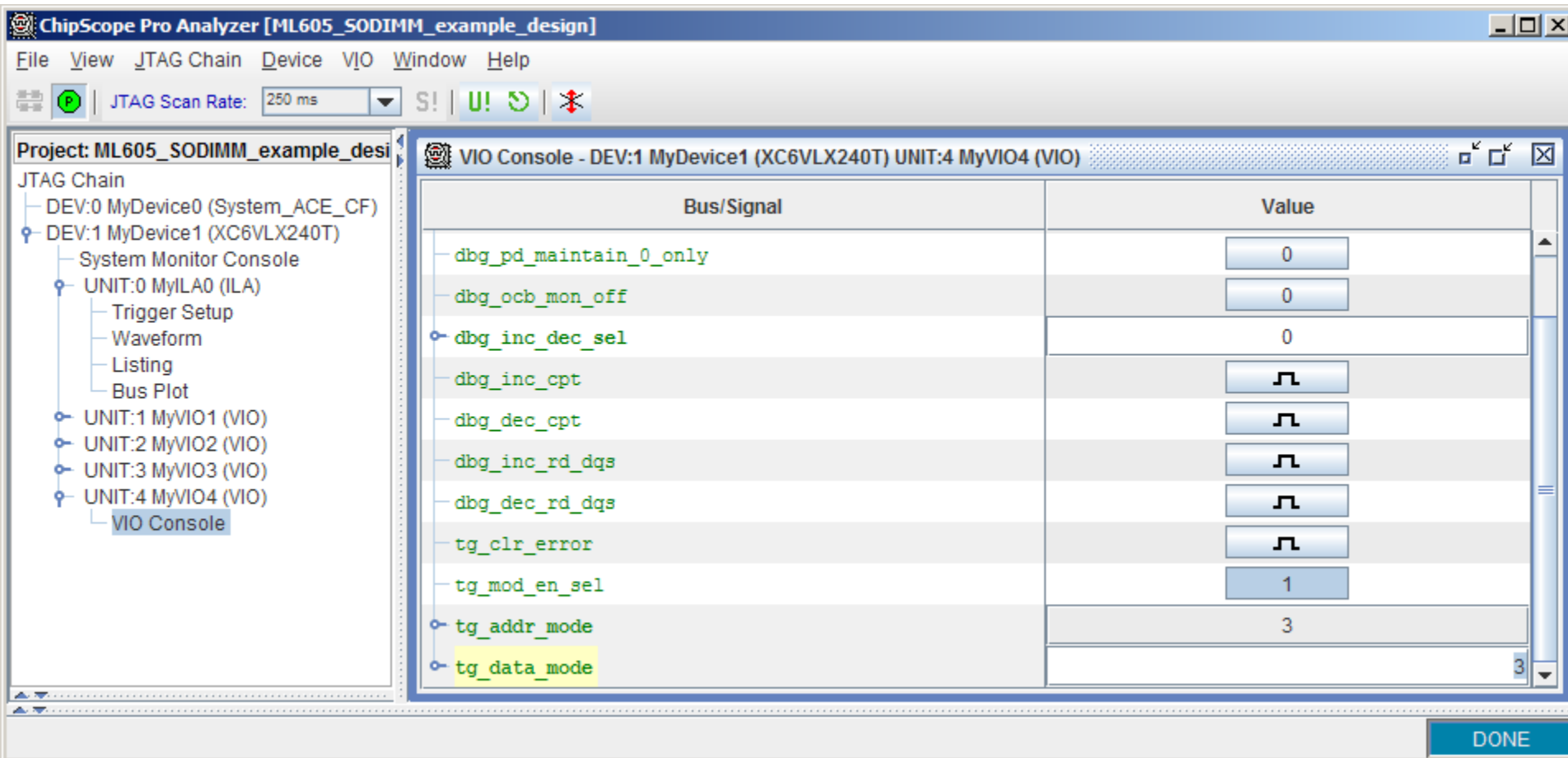
The VIO Console for UNIT:4 MyVIO4 (VIO) displays the following signals and values:

Bus/Signal	Value
<code>dbg_pd_maintain_0_only</code>	0
<code>dbg_ocb_mon_off</code>	0
<code>dbg_inc_dec_sel</code>	0
<code>dbg_inc_cpt</code>	1
<code>dbg_dec_cpt</code>	1
<code>dbg_inc_rd_dqs</code>	1
<code>dbg_dec_rd_dqs</code>	1
<code>tg_clr_error</code>	1
<code>tg_mod_en_sel</code>	1
<code>tg_addr_mode</code>	3
<code>tg_data_mode</code>	2

The `tg_mod_en_sel` signal is highlighted with a red box, indicating its value is 1.

Adjust Data Pattern using VIO Console

- Set `tg_data_mode` to “3” for `HAMMER_DATA_MODE`



The screenshot shows the ChipScope Pro Analyzer interface for the project `ML605_SODIMM_example_design`. The VIO Console window is open, displaying the configuration for `DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO)`. The console shows a list of signals and their current values:

Bus/Signal	Value
<code>dbg_pd_maintain_0_only</code>	0
<code>dbg_ocb_mon_off</code>	0
<code>dbg_inc_dec_sel</code>	0
<code>dbg_inc_cpt</code>	1
<code>dbg_dec_cpt</code>	1
<code>dbg_inc_rd_dqs</code>	1
<code>dbg_dec_rd_dqs</code>	1
<code>tg_clr_error</code>	1
<code>tg_mod_en_sel</code>	1
<code>tg_addr_mode</code>	3
<code>tg_data_mode</code>	3

The `tg_data_mode` signal is highlighted in yellow, and its value is set to 3. The `tg_addr_mode` signal is also set to 3. The `dbg_inc_cpt`, `dbg_dec_cpt`, `dbg_inc_rd_dqs`, `dbg_dec_rd_dqs`, and `tg_clr_error` signals are set to 1. The `dbg_pd_maintain_0_only` and `dbg_ocb_mon_off` signals are set to 0.

DONE

Adjust Data Pattern using VIO Console

- Select VIO Console 1
- Note error is active

The screenshot shows the ChipScope Pro Analyzer interface. The main window is titled "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO)". The left sidebar shows the project hierarchy: "Project: ML605_SODIMM_example_desi" > "JTAG Chain" > "DEV:1 MyDevice1 (XC6VLX240T)" > "UNIT:1 MyVIO1 (VIO)" > "VIO Console". The main panel displays a table of bus signals and their values.

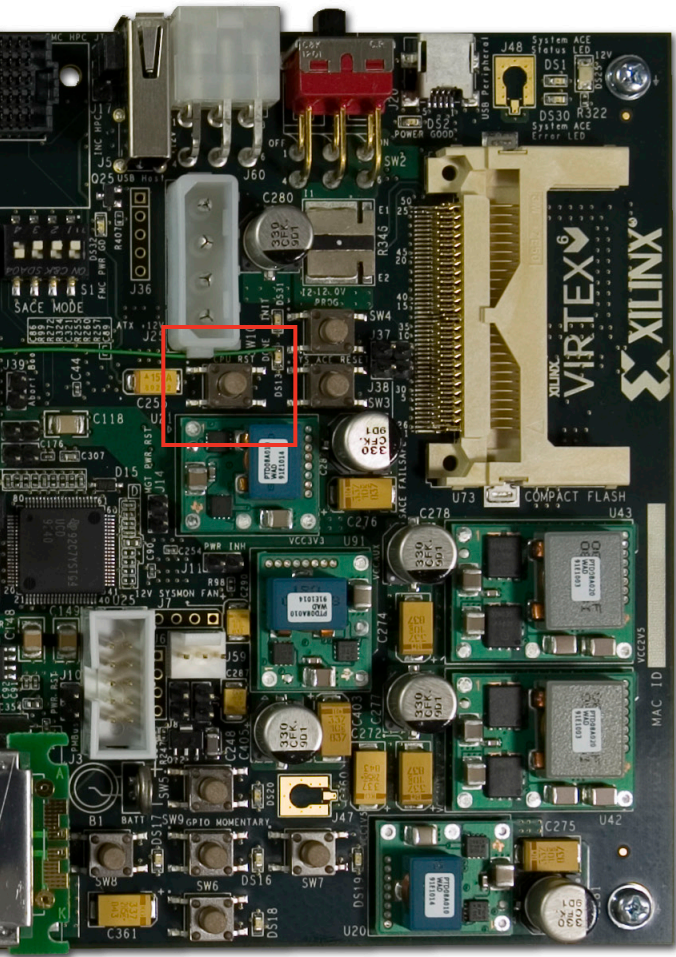
Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06
dbg_wl_odelay_dqs_tap_cnt_1	10
dbg_wl_odelay_dq_tap_cnt_1	08

A "DONE" button is located at the bottom right of the window.

Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

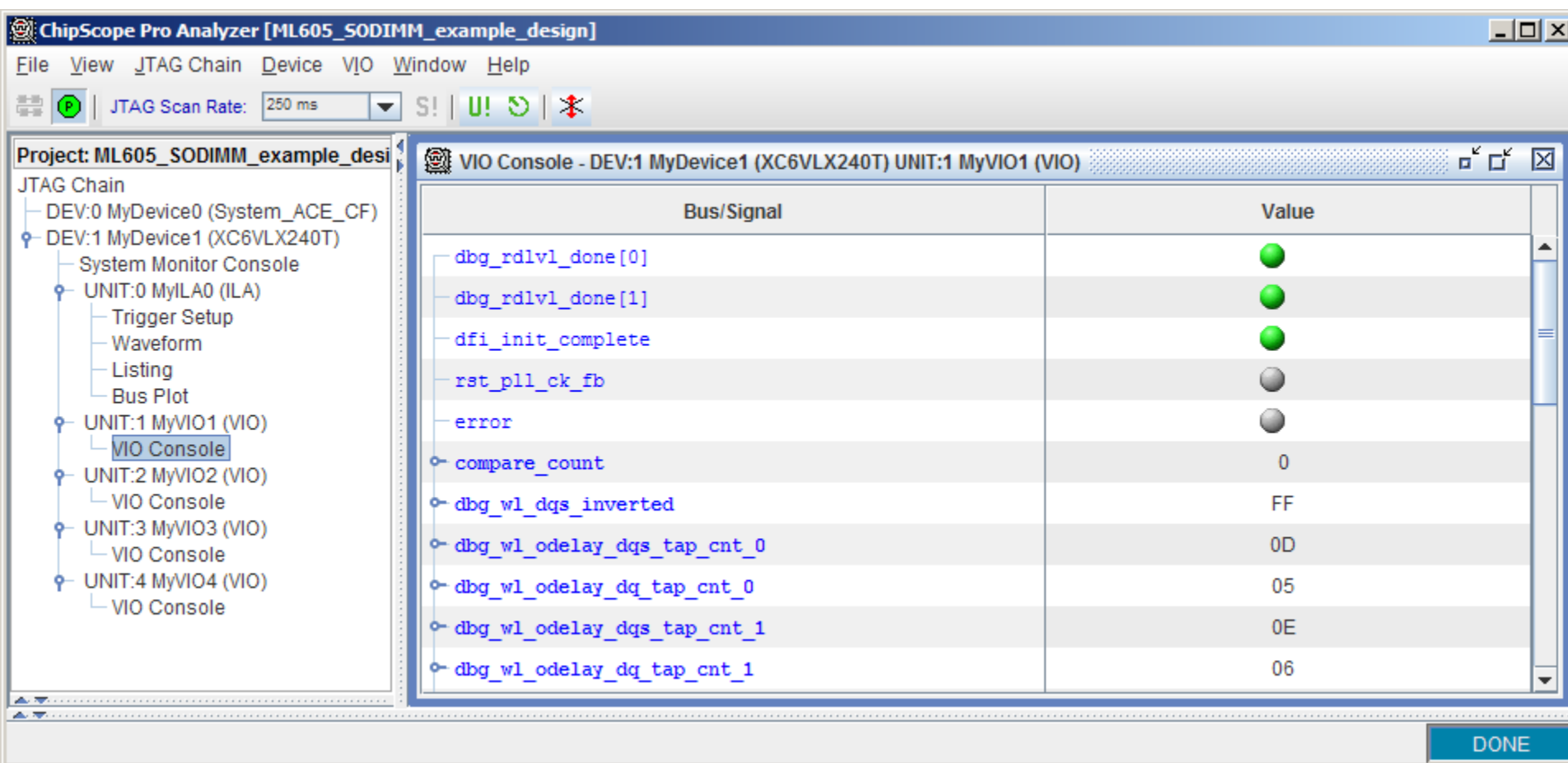
- Press and release the CPU RESET switch, SW10, after each change to `tg_mod_en_sel` or `tg_data_mode`








Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

- Error is now cleared



The screenshot shows the ChipScope Pro Analyzer interface for the project 'ML605_SODIMM_example_design'. The VIO Console window is open, displaying a list of signals and their current values. The JTAG Chain on the left shows the hierarchy: DEV:0 MyDevice0 (System_ACE_CF), DEV:1 MyDevice1 (XC6VLX240T), and its sub-units. The VIO Console window title is 'VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO)'. The table below lists the signals and their values.

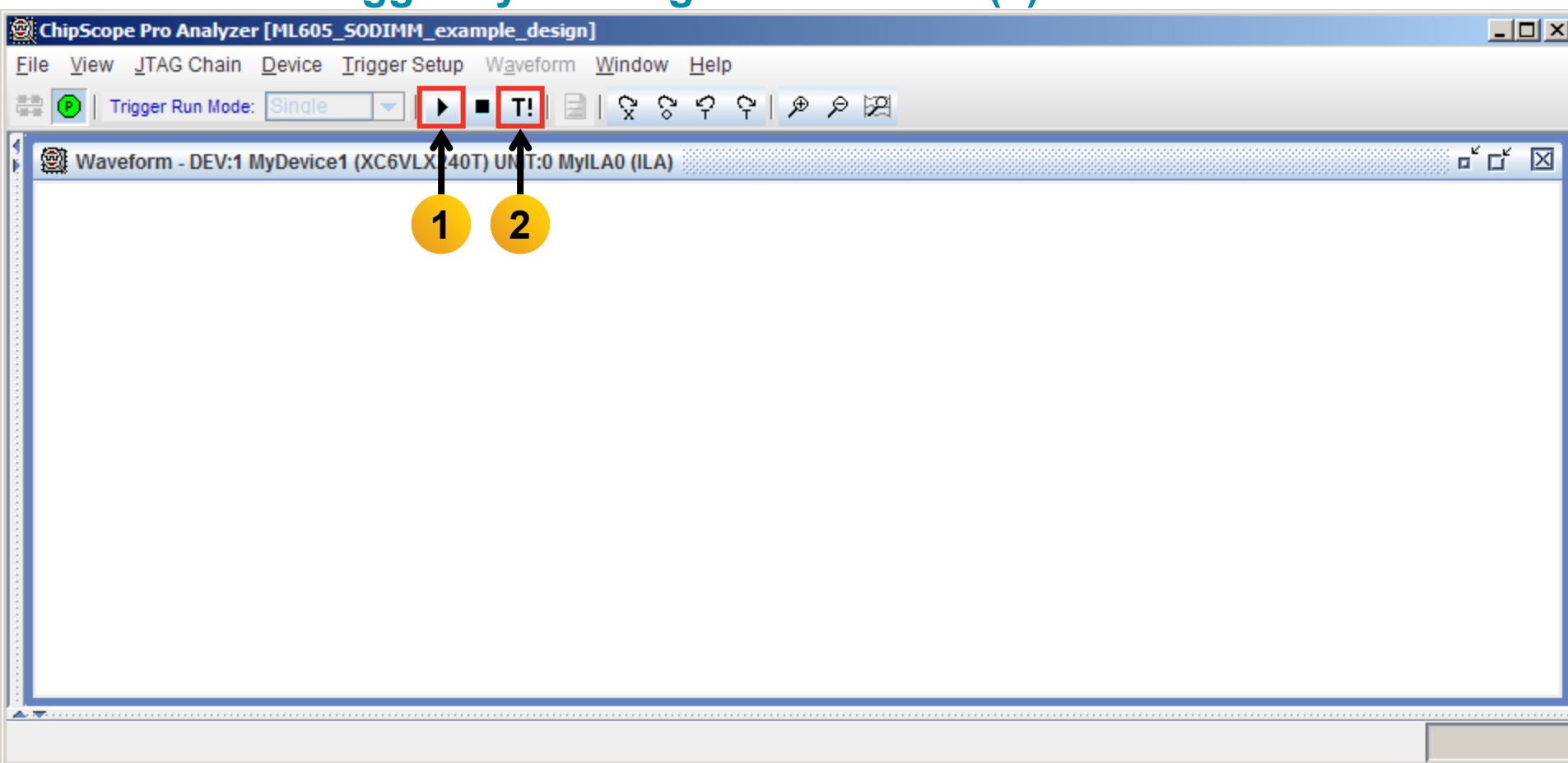
Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0D
dbg_wl_odelay_dq_tap_cnt_0	05
dbg_wl_odelay_dqs_tap_cnt_1	0E
dbg_wl_odelay_dq_tap_cnt_1	06

A 'DONE' button is visible at the bottom right of the interface.

Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

- Click on Waveform; click the Arm Trigger button (1)
- Force a trigger by clicking the T! button (2)

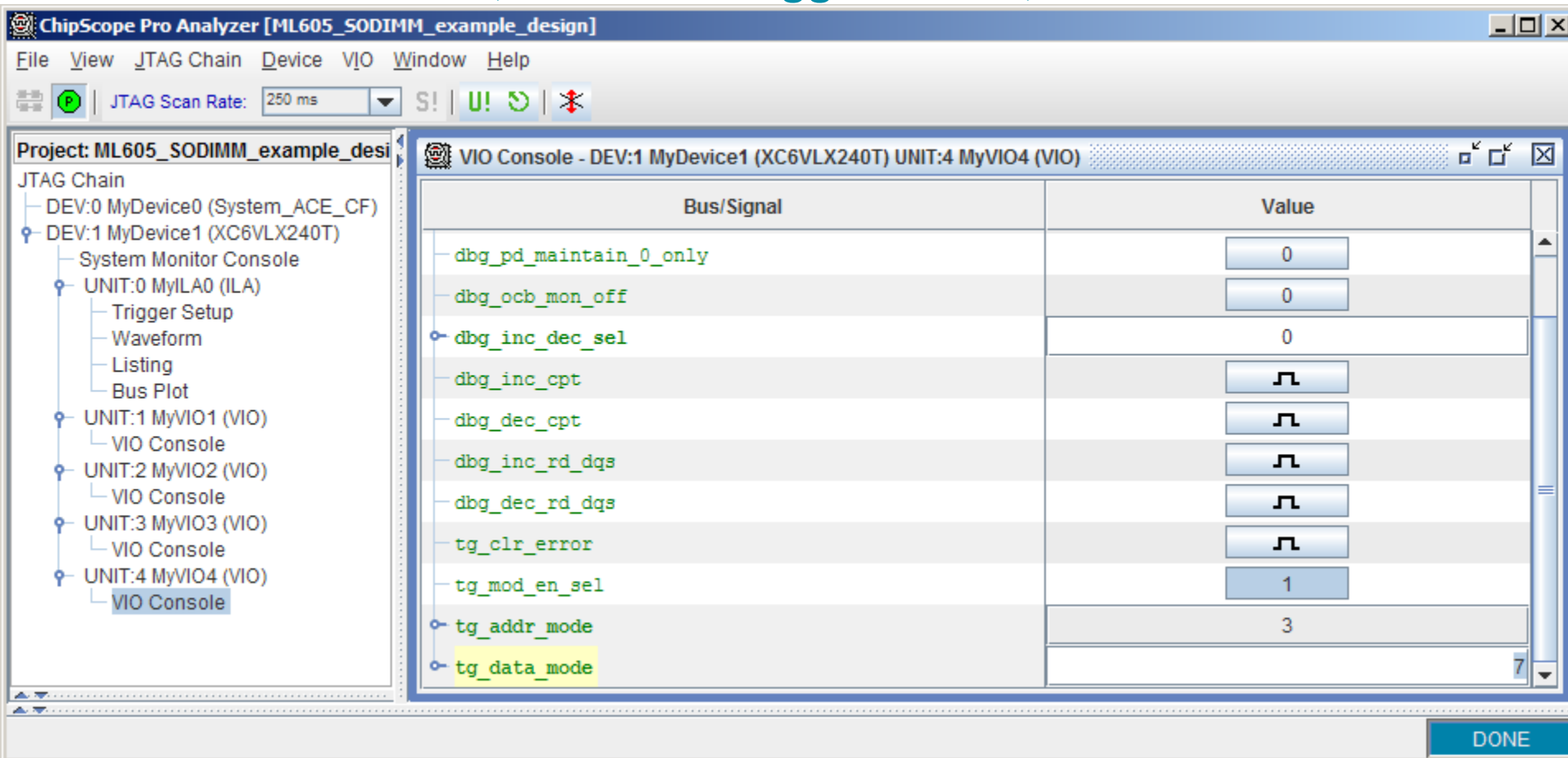


- 64 bit DQ data bus hammer pattern



Adjust Data Pattern using VIO Console

- Set `tg_data_mode` to “7” for PRBS data pattern
- Push CPU Reset, click Arm Trigger button, click T! button



ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

Project: ML605_SODIMM_example_desi

JTAG Chain

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6VLX240T)
 - System Monitor Console
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - VIO Console
 - UNIT:2 MyVIO2 (VIO)
 - VIO Console
 - UNIT:3 MyVIO3 (VIO)
 - VIO Console
 - UNIT:4 MyVIO4 (VIO)
 - VIO Console

VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO)

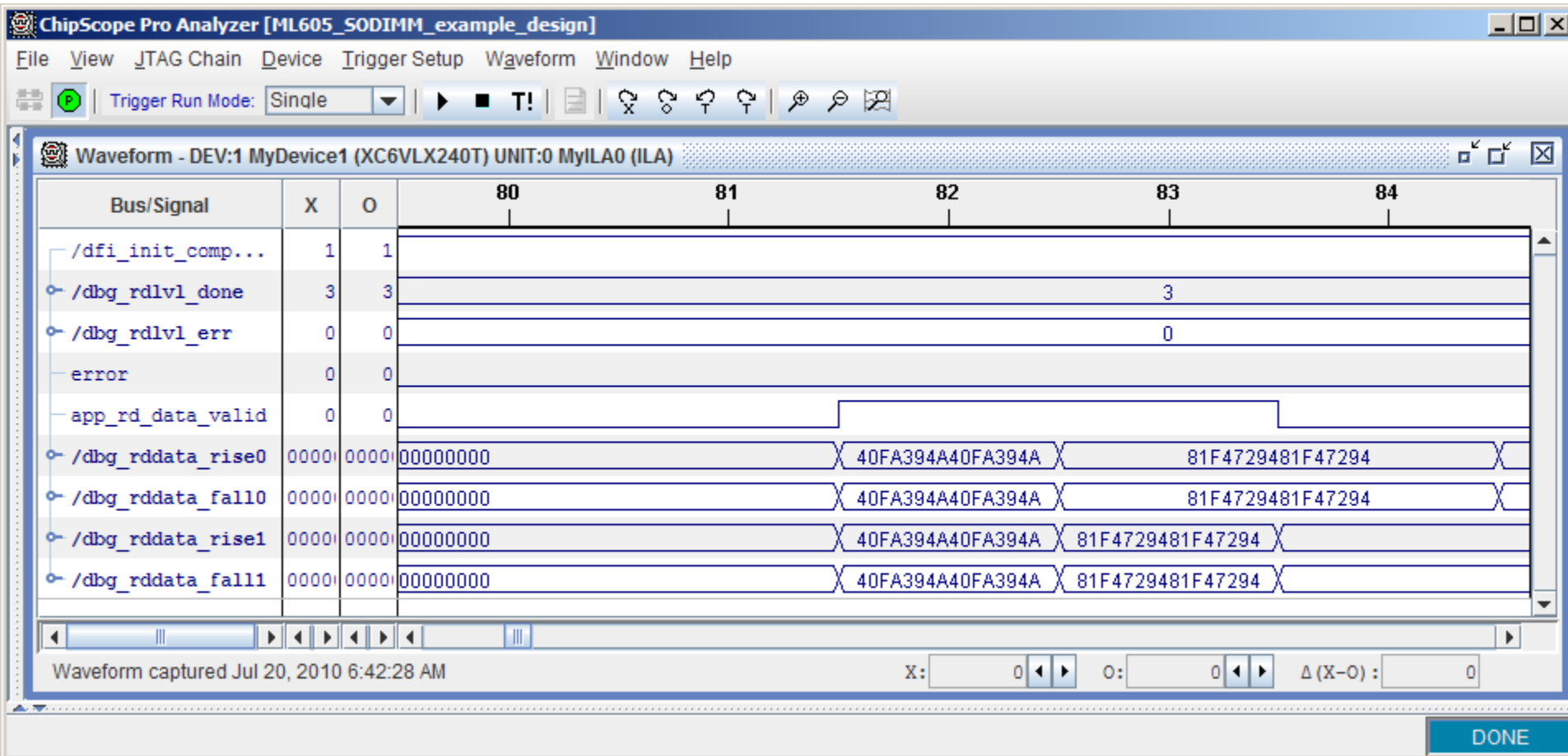
Bus/Signal	Value
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	1
dbg_dec_cpt	1
dbg_inc_rd_dqs	1
dbg_dec_rd_dqs	1
tg_clr_error	1
tg_mod_en_sel	1
tg_addr_mode	3
tg_data_mode	7

DONE

Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

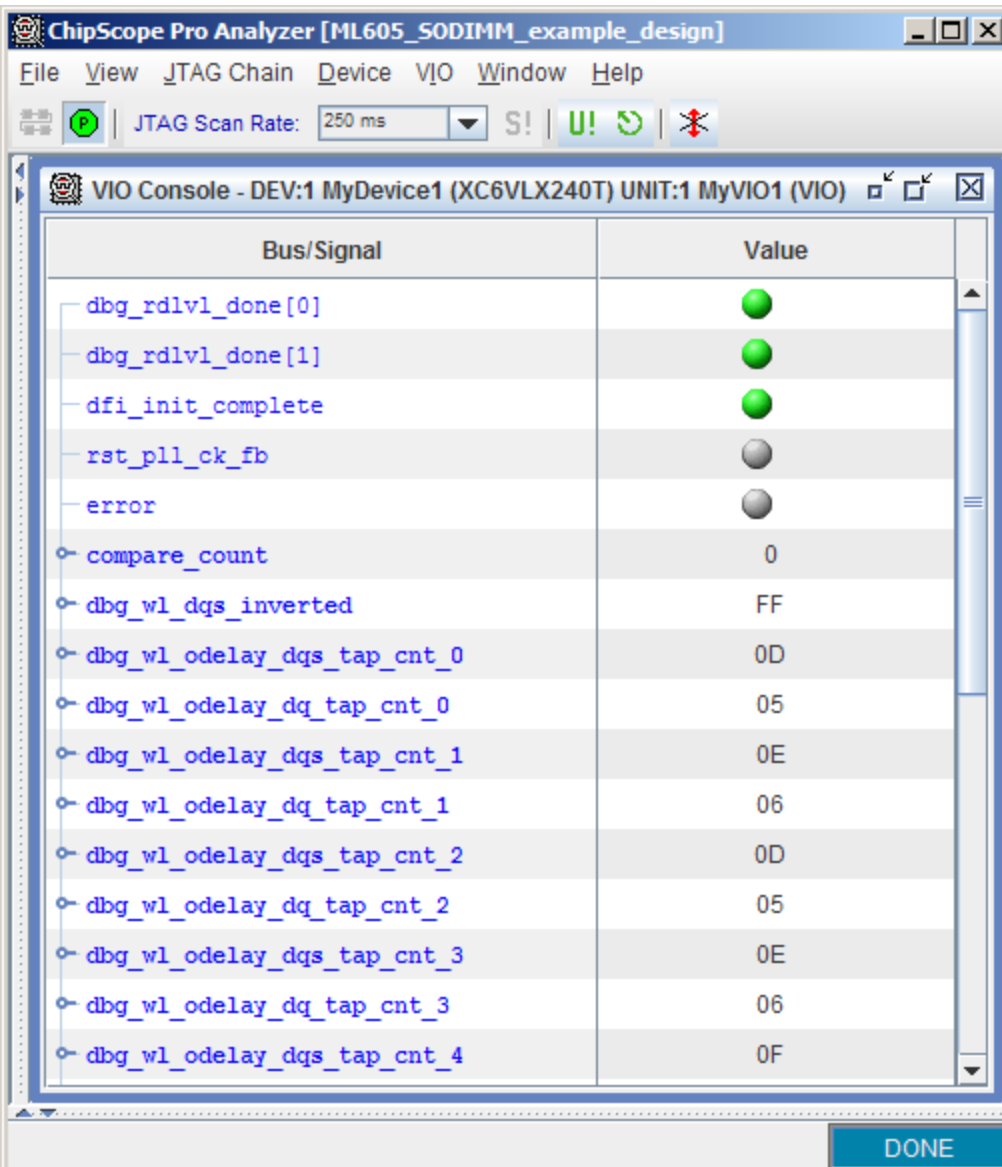
▪ PRBS Data Mode



Example Design VIO Consoles

- **Useful for PHY layer logic debug and status**
- **Available if “debug” option is checked in MIG GUI**
 - Monitor PHY outputs
 - Status of write calibration
 - Status of read calibration
 - Phase detector control
 - Read data capture clock adjustment
 - Disable selected PHY features
- **Reference documentation in UG406**
 - “PHY Layer Debug Port” section
 - Table 1-25 for signal definitions and descriptions
- **VIO port assignments (4 cores) defined in “example_top.v”**

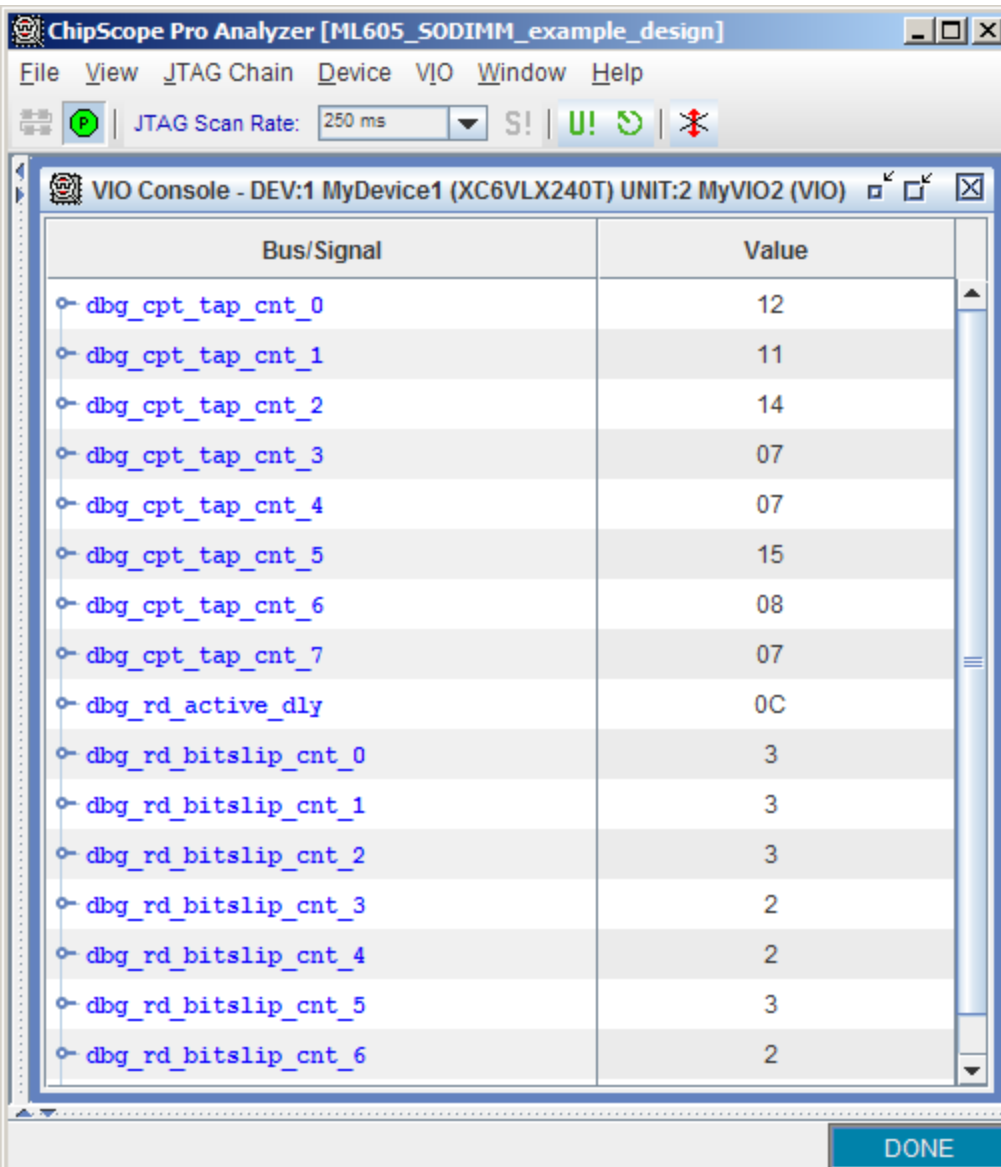
Example Design VIO Consoles



■ VIO Console 1

- Write Path Calibration Status
- Read Leveling Done, Read Leveling Error
- Initialization complete, PLL reset
- Note: Press CPU RESET to clear error status in this VIO console

Example Design VIO Consoles



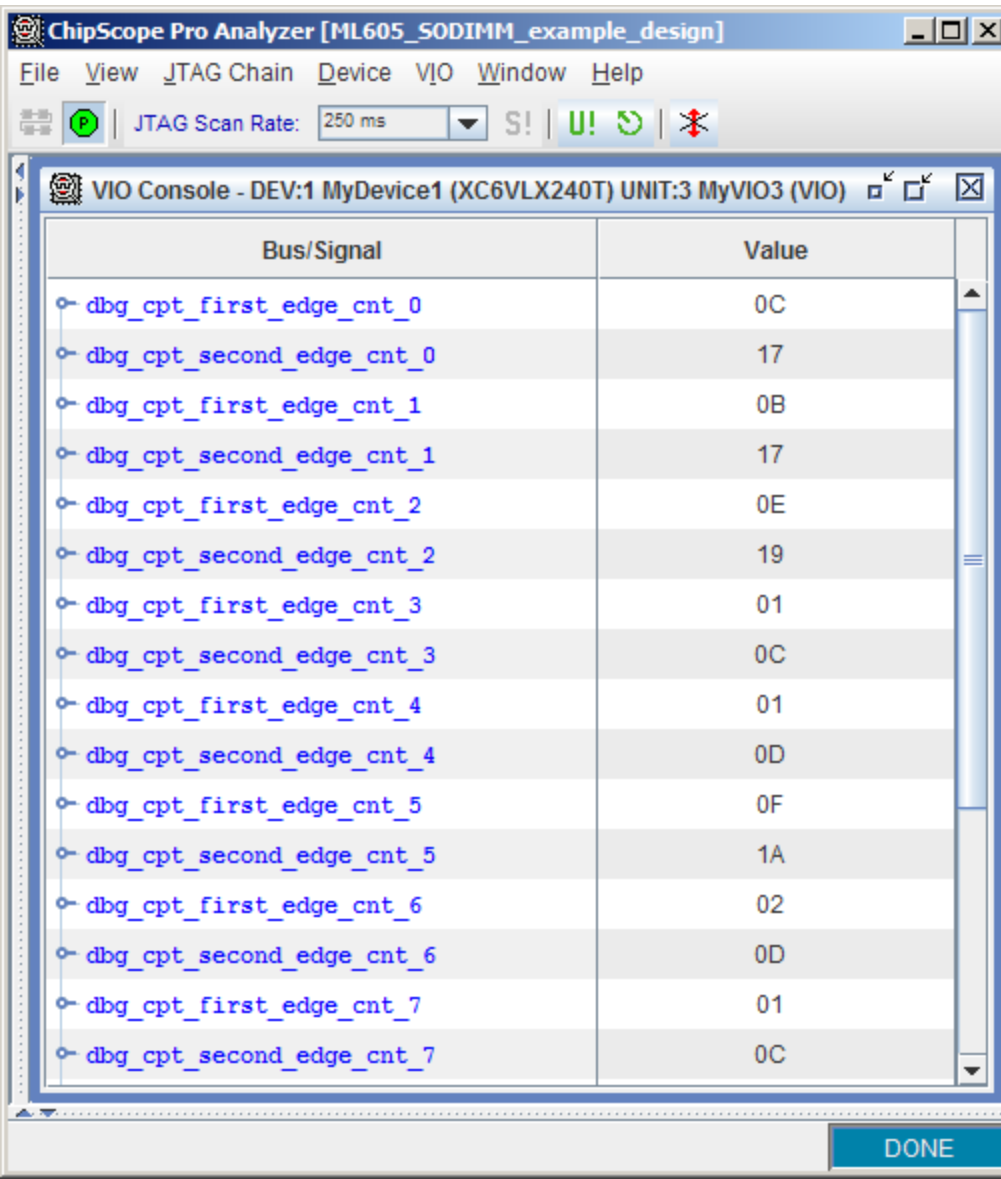
The screenshot shows the ChipScope Pro Analyzer interface for the design 'ML605_SODIMM_example_design'. The VIO Console window is open, displaying a table of bus/signal values for 'DEV:1 MyDevice1 (XC6VLX240T) UNIT:2 MyVIO2 (VIO)'. The table has two columns: 'Bus/Signal' and 'Value'. The signals listed are debug counters for tap and bitslip, with values ranging from 07 to 15. A 'DONE' button is visible at the bottom right of the console window.

Bus/Signal	Value
dbg_cpt_tap_cnt_0	12
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	14
dbg_cpt_tap_cnt_3	07
dbg_cpt_tap_cnt_4	07
dbg_cpt_tap_cnt_5	15
dbg_cpt_tap_cnt_6	08
dbg_cpt_tap_cnt_7	07
dbg_rd_active_dly	0C
dbg_rd_bitslip_cnt_0	3
dbg_rd_bitslip_cnt_1	3
dbg_rd_bitslip_cnt_2	3
dbg_rd_bitslip_cnt_3	2
dbg_rd_bitslip_cnt_4	2
dbg_rd_bitslip_cnt_5	3
dbg_rd_bitslip_cnt_6	2

- VIO Console 2 & VIO Console 3

- Read Path Calibration Status

Example Design VIO Consoles



The screenshot shows the ChipScope Pro Analyzer interface for the design 'ML605_SODIMM_example_design'. The VIO Console window is open, displaying a table of data for 'DEV:1 MyDevice1 (XC6VLX240T) UNIT:3 MyVIO3 (VIO)'. The table has two columns: 'Bus/Signal' and 'Value'. The data is organized into pairs of rows for each of the eight channels (0 through 7), with the first row of each pair showing the first edge count and the second row showing the second edge count. The values are in hexadecimal format.

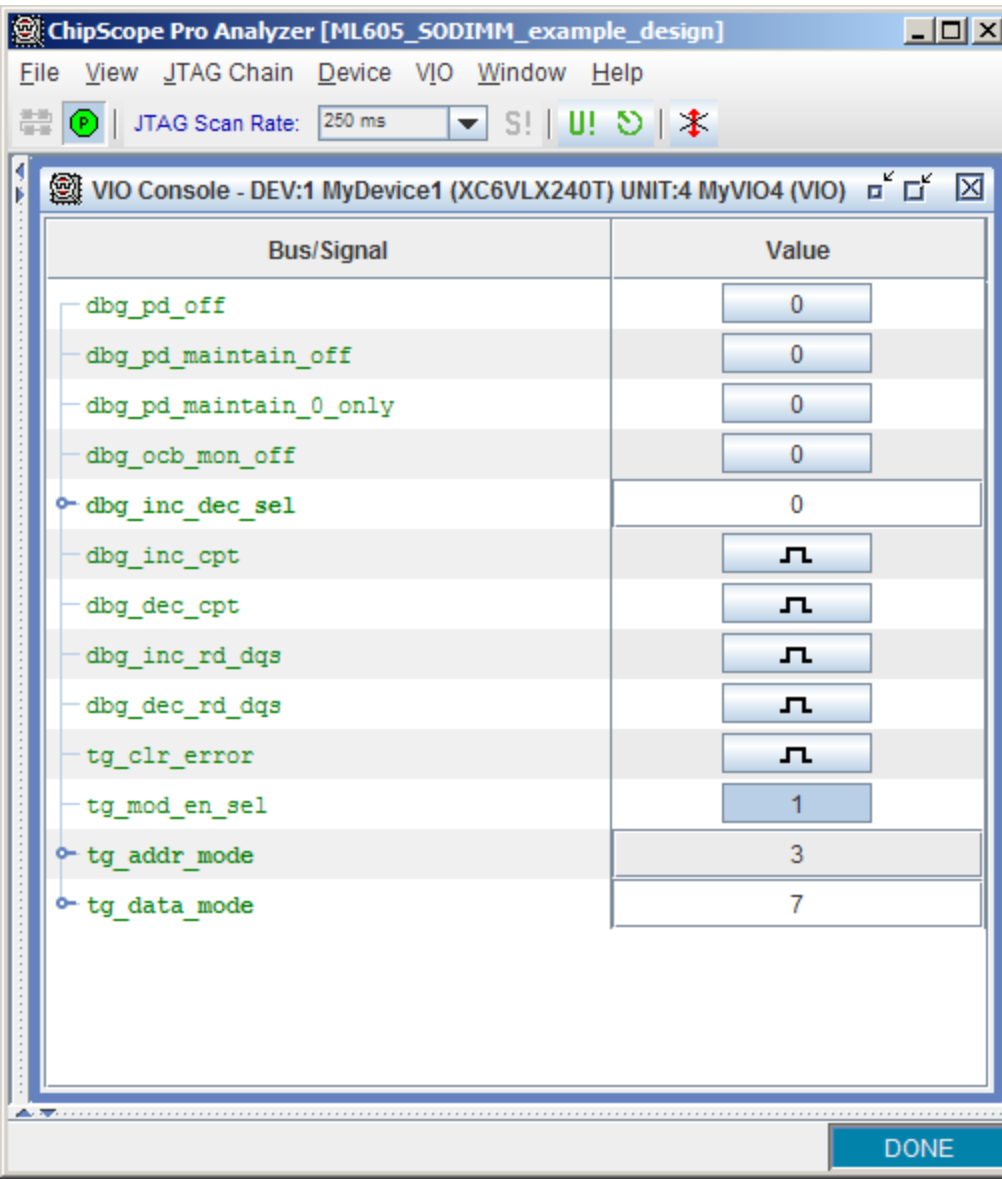
Bus/Signal	Value
dbg_cpt_first_edge_cnt_0	0C
dbg_cpt_second_edge_cnt_0	17
dbg_cpt_first_edge_cnt_1	0B
dbg_cpt_second_edge_cnt_1	17
dbg_cpt_first_edge_cnt_2	0E
dbg_cpt_second_edge_cnt_2	19
dbg_cpt_first_edge_cnt_3	01
dbg_cpt_second_edge_cnt_3	0C
dbg_cpt_first_edge_cnt_4	01
dbg_cpt_second_edge_cnt_4	0D
dbg_cpt_first_edge_cnt_5	0F
dbg_cpt_second_edge_cnt_5	1A
dbg_cpt_first_edge_cnt_6	02
dbg_cpt_second_edge_cnt_6	0D
dbg_cpt_first_edge_cnt_7	01
dbg_cpt_second_edge_cnt_7	0C

A 'DONE' button is visible at the bottom right of the console window.

■ VIO Console 2 & VIO Console 3

- Read Path Calibration Status

Example Design VIO Consoles



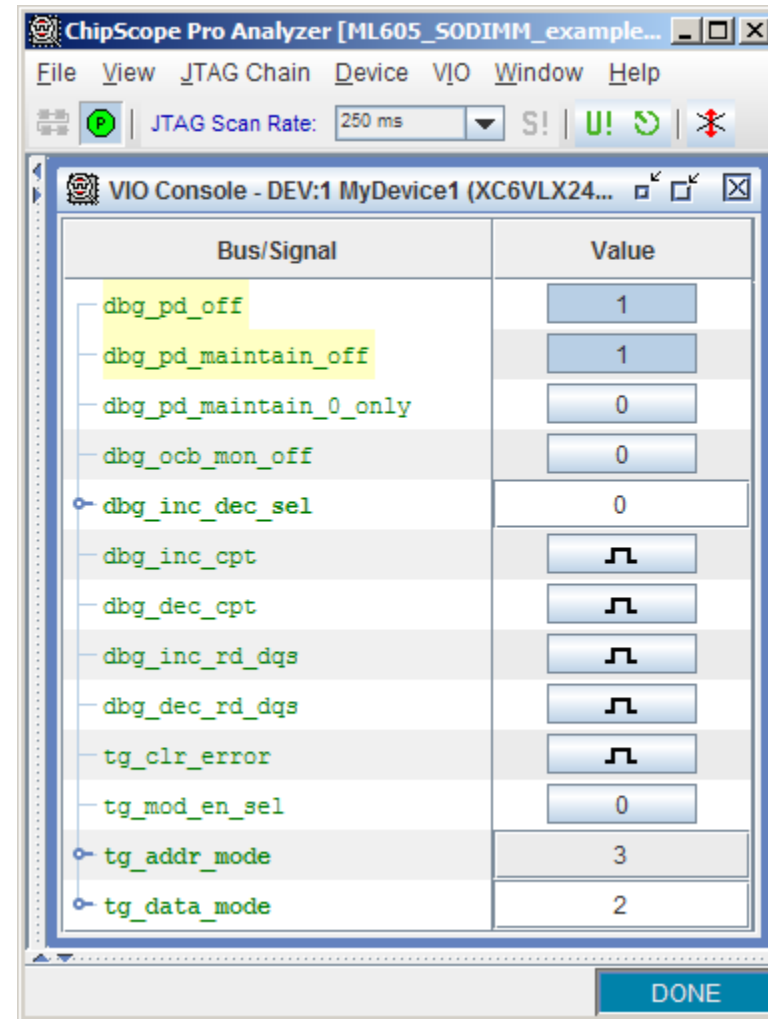
■ VIO Console 4

- Phase Detector Controls
- Read Data Capture Clock Adjustment

Measure Read Data Window with VIO

■ VIO Console 4

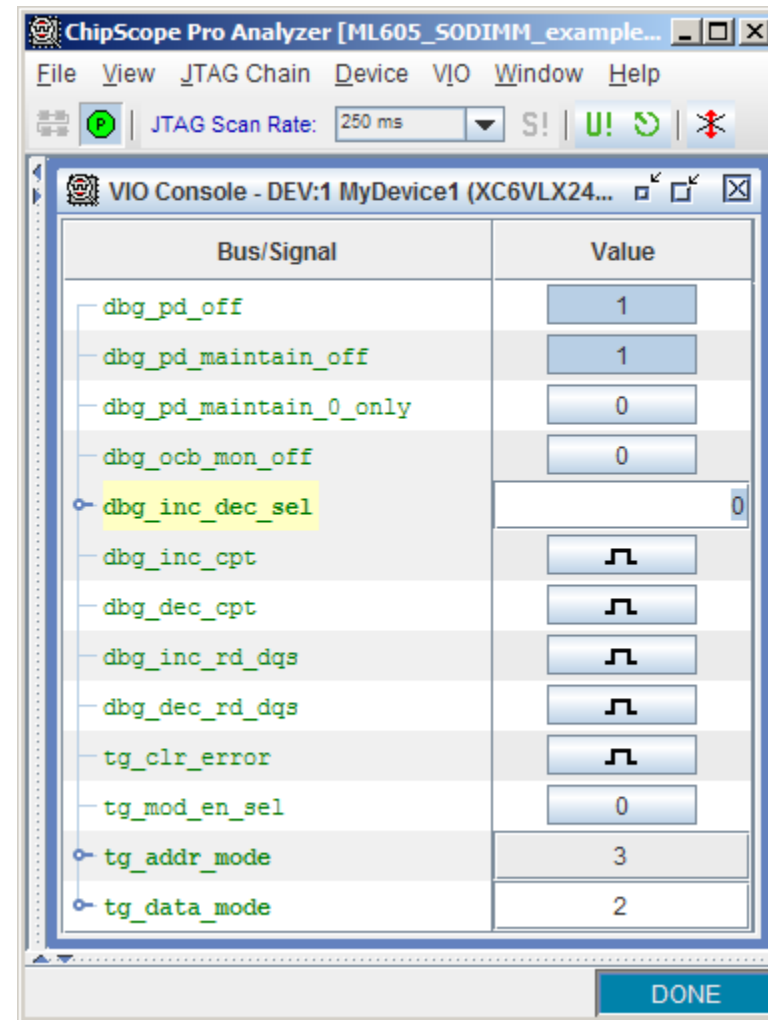
- Set **dbg_pd_off** to 1
- This turns off the Phase Detector
- Set **dbg_pd_maintain_off** to 1
- This turns off the Phase Detector Maintenance
- Select data group (0, 1, 2, etc,)



Measure Read Data Window with VIO

■ VIO Console 4

- Set **dbg_inc_dec_sel** to 0
- This selects the data group (0, 1, 2, etc,)



Change tap delays to measure window

▪ Increment Taps

- Note the initial value of **dbg_cpt_tap_cnt_0**, in this case 11
- The error LED should be off

ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

VIO Console - DEV:1 MyDevice1 (XC6...)

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	
dbg_dec_cpt	
dbg_inc_rd_dqs	
dbg_dec_rd_dqs	

VIO Console - DEV:1 MyDevice1 (XC6...)

Bus/Signal	Value
dbg_cpt_tap_cnt_0	11
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D

VIO Console - DEV:1 MyDevice1 (XC6VL...)

Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

DONE

Change tap delays to measure window

■ Increment Taps

- Increment tap delay by clicking on **dbg_inc_cpt** until an error occurs
- Note tap value that causes the error and subtract one: $17 - 1 = 16$
- Take the difference of the final value and the initial value: $16 - 11 = 5$

ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

VIO Console - DEV:1 MyDevice1 (XC6...

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	
dbg_dec_cpt	
dbg_inc_rd_dqs	
dbg_dec_rd_dqs	

VIO Console - DEV:1 MyDevice1 (XC6...

Bus/Signal	Value
dbg_cpt_tap_cnt_0	17
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D

VIO Console - DEV:1 MyDevice1 (XC6VL...

Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

DONE

Change tap delays to measure window

▪ Reset using Switch SW10

- Note that **dbg_cpt_tap_cnt_0** returns to its original value, 11
- The error LED should be off

ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

VIO Console - DEV:1 MyDevice1 (XC6...

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	
dbg_dec_cpt	
dbg_inc_rd_dqs	
dbg_dec_rd_dqs	

VIO Console - DEV:1 MyDevice1 (XC6...

Bus/Signal	Value
dbg_cpt_tap_cnt_0	11
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D

VIO Console - DEV:1 MyDevice1 (XC6VL...

Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

DONE

Change tap delays to measure window

▪ Decrement Taps

- Decrement tap delays by clicking on **dbg_dec_cpt** until an error occurs
- Note tap value that causes the error and add one: $0B + 1 = 0C$
- Take the difference of the initial value and the final value: $11 - 0C = 5$

ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

VIO Console - DEV:1 MyDevice1 (XC6...)

Bus/Signal	Value
dbg_pd_off	1
dbg_pd_maintain_off	1
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	
dbg_dec_cpt	
dbg_inc_rd_dqs	
dbg_dec_rd_dqs	

VIO Console - DEV:1 MyDevice1 (XC6...)

Bus/Signal	Value
dbg_cpt_tap_cnt_0	0B
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	13
dbg_cpt_tap_cnt_3	13
dbg_cpt_tap_cnt_4	06
dbg_cpt_tap_cnt_5	13
dbg_cpt_tap_cnt_6	06
dbg_cpt_tap_cnt_7	06
dbg_rd_active_dly	0D

VIO Console - DEV:1 MyDevice1 (XC6VL...)

Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0E
dbg_wl_odelay_dq_tap_cnt_0	06

DONE

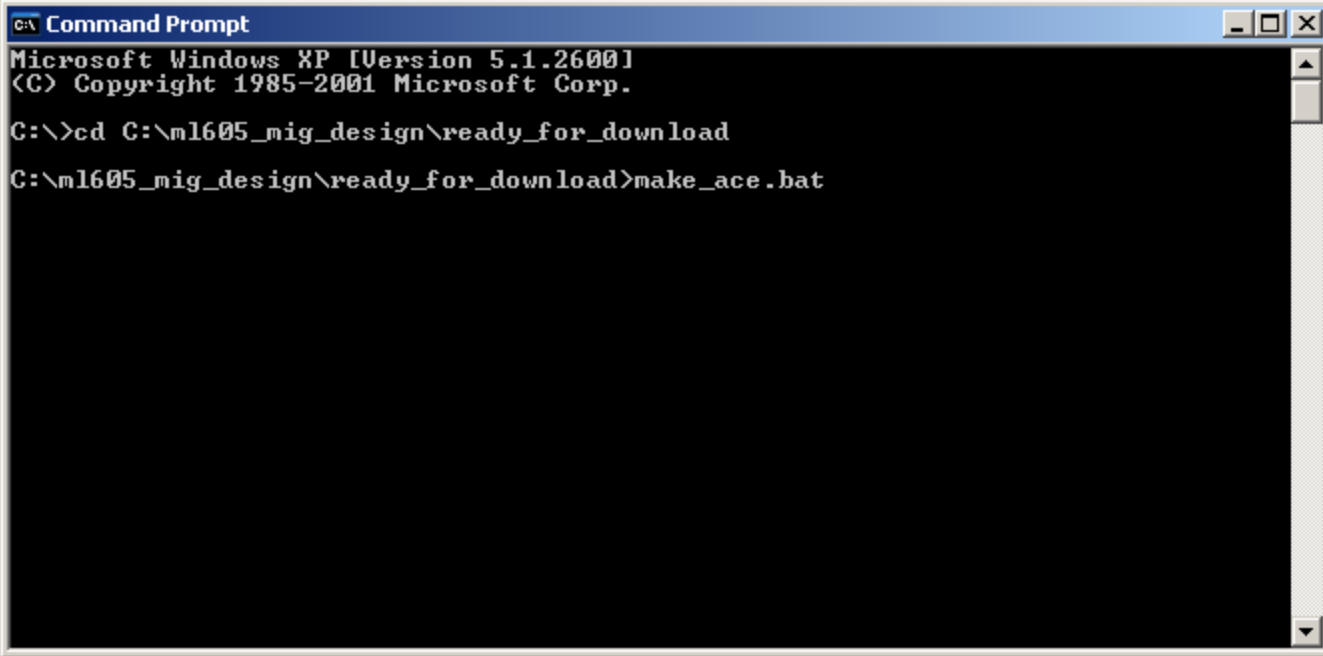
Change tap delays to measure window

- **Add the two values and multiply by the average tap delay:**
 - $10 \times 78 \text{ ps} = 780 \text{ ps}$
- **Total data period = 1250 ps (800 Mbps)**
 - From [DS152](#), page 35: “Average Tap Delay at 200 MHz = 78 ps”

Generate MIG ACE File (Optional)

- Type these commands in a windows command shell:

```
cd C:\ml605_mig_design\ready_for_download  
make_ace.bat
```



A screenshot of a Windows Command Prompt window. The title bar reads "C:\ Command Prompt". The window content shows the following text: "Microsoft Windows XP [Version 5.1.2600] Copyright 1985-2001 Microsoft Corp." followed by a new line. The next line shows the command "C:\>cd C:\ml605_mig_design\ready_for_download" and the following line shows the command "C:\ml605_mig_design\ready_for_download>make_ace.bat". The cursor is at the end of the second command line.

References

References

▪ Virtex-6 Memory

- Virtex-6 FPGA Memory Interface Solutions User Guide – UG406
http://www.xilinx.com/support/documentation/ip_documentation/ug406.pdf
- Virtex-6 FPGA Memory Interface Solutions – DS186
http://www.xilinx.com/support/documentation/ip_documentation/ds186.pdf
- Virtex-6 FPGA Data Sheet: DC and Switching Characteristics – DS152
http://www.xilinx.com/support/documentation/data_sheets/ds152.pdf

Documentation

Documentation

■ Virtex-6

- Virtex-6 FPGA Family

<http://www.xilinx.com/products/virtex6/index.htm>

■ ML605 Documentation

- Virtex-6 FPGA ML605 Evaluation Kit

<http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Getting Started Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug533.pdf

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf