Spartan-3A/3AN Starter Kit Board Schematic
(Annotated)
21-AUG-2007

For additional information …
www.xilinx.com/s3astarter

See UG334: Spartan-3A/3AN Starter Kit User Guide for further information on each board feature
The PS/2 connector has primary and secondary connections to the FPGA. The secondary connections are available by attaching an external Y-splitter cable.

NOTE: See schematic Page 13 for details.
Spartan-3A/3AN Starter Kit Board

Voltage regulators

www.national.com/pf/LP/LP3906.html

FPGA core supply (1.2V)

FPGA I/O Banks 0, 1, 2 (3.3V)

FPGA auxiliary supply (3.3V)

Embedded USB/JTAG Programmer (1.8V)

Bank 0

Bank 2

Bank 3

Bank 1

FPGA DDR2 SDRAM Termination (0.9V)

FPGA DDR2 SDRAM Device, FPGA I/O Bank 3 (1.8V)

DAC Reference Voltage (3.3V)

DDR2 SDRAM Voltage Ref. (0.9V)

Power switch

Wall power adapter input

Power switch

Voltage regulators

National Semiconductor

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Spartan-3A/3AN Starter Kit Board

Voltage regulators

www.national.com/pf/LP/LP3906.html

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DDCR 500-112

Revision C 01-30-2008 30 50
**Spartan-3A/3AN Starter Kit Board**

**FPGA I/O Bank 0 and Bank 1, Clock Oscillators**

- **FPGA**: XC3S700A/AN-4FGG484C(E)

**Clock Oscillators**
- 50 MHz Oscillator
- Auxiliary Oscillator Socket

**Diagram Details**
- Bank 0
- Bank 1
- Connection points labeled with IO numbers
- Placement of FPGA and other components

**Xilinx**

**Digilent**

**Description**
- FPGA I/O Bank 0 and Bank 1, Clock Oscillators

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**Sheet**
- 1

**Revision**
- C

**Date**
- 12-31-2000
Spartan-3A/AN Starter Kit Board

FPGA I/O Bank 3 is dedicated to the DDR2 SDRAM interface.

FPGA: XC3S700A/AN-4FGG484C(ES)

AWAKE LED

FPGA I/O Bank 2 and Bank 3

FPGA: XC3S700A/AN-4FGG484C(ES)
Analog-to-Digital Converter (ADC)
LTC1407-1, two-channel, 12-bit resolution, serial
www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1001,C1158,P2484

Digital-to-Analog Converter (DAC)
LTC2624, four-channel, 12-bit resolution, serial
www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1005,C1156,P2048

Programmable Gain Amplifier (AMP)
LTC6912-1, two-channel, serial
www.linear.com/pc/productDetail.do?navId=H0,C1,C1154,C1009,C1121,P7596

The DAC_REF_CD voltage is programmable via the I2C control interface on the LP3906 voltage regulator designated as IC18 on sheet 5. At power-up, this reference voltage is 3.3V.

Thevenin termination to improve the signal integrity on these high-fanout signals.

ADC, DAC, pre-amplifier
Analog headers (see sheet 2)
The DDR2 SDRAM interface has specific pin assignment and layout requirements to support the Xilinx Memory Interface Generator (MIG) software. See the "DDR SDRAM" chapter in UG334: Spartan-3A/3AN Starter Kit User Guide.

**DESIGN NOTE:**

The Revision C board has an inductor in this location. Shorting across this location improves high-frequency DDR2 SDRAM interface performance. The Revision D board uses a 0Ω resistor.

The DDR2 SDRAM interface has specific pin assignment and layout requirements to support the Xilinx Memory Interface Generator (MIG) software. See the "DDR SDRAM" chapter in UG334: Spartan-3A/3AN Starter Kit User Guide.

**DESIGN NOTE:**

The Revision C board has an inductor in this location. Shorting across this location improves high-frequency DDR2 SDRAM interface performance. The Revision D board uses a 0Ω resistor.
To configure from parallel NOR Flash, remove Jumper J46 to disable the Platform Flash PROM.

To configure from parallel NOR Flash, set the FPGA mode select pins using Jumper J46 as shown.
The Spartan-3A Starter Kit board supports multiple pad landings for each SPI Flash architecture. However, only one STMicro and one Atmel PROM are mounted on the board.

### STMicroelectronics M25P16 16 Mbit SPI serial Flash PROM

- **Configuration:**
  - **Atmel Select Signal:** SPI_SS_B
  - **STMicro Select Signal:** ALT_SS_B

### Atmel AT45DB161D 16 Mbit serial DataFlash PROM®

- **Platform Flash Jumper:** (Jumper J46)
- **Configure From:**
  - **Atmel:** SPI_SS_B
  - **STMicro:** ALT_SS_B

### Mode Select Jumpers (Jumper J26)

- **Master SPI Mode:** M[2:0]=<0:0:1>

**NOTE:** Jumper J1 appears on schematic Page 3.
Spartan-3A/3AN Starter Kit Board

Slide switches, Rotary knob, Character LCD, Pushbutton switches, discrete LEDs
The DDR2 SDRAM interface has specific pin assignment and layout requirements to support the Xilinx Memory Interface Generator (MIG) software. See the "DDR SDRAM" chapter in UG33: Spartan-3A/3AN Starter Kit User Guide.
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Pairs of pins on the header form potential differential I/O pairs. Optionally, each pin can be a single-ended I/O pin.

Each individual differential I/O pair is routed with matched 100-ohm impedance.

If using differential inputs, set the DIFF_TERM=TRUE constraint. There are no external termination resistors provided on the board.

```
INST <I/O_BUFFER_INSTANTIATION_NAME> DIFF_TERM = "TRUE" ;
```