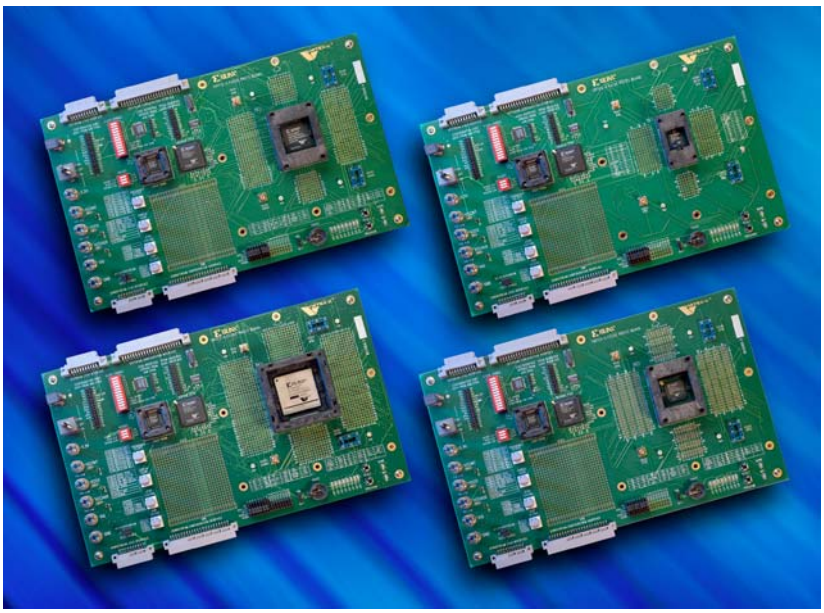
Virtex-II Prototype Platform

User Guide

UG015 / PN0401974 (v1.1) January 14, 2003



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UG015 / PN0401974 (v1.1) January 14, 2003

The following table shows the revision history for this document.

	Version	Revision
06/29/01	1.0	Initial Xilinx release.
01/14/03	1.1	Trademark updates and correction to V_{CCO} Supply Jumpers section.

Table of Contents

About This Manual

This document describes the features and operation of Virtex-II Prototype Platform prototype and demonstration boards.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Book	Pages from *The Programmable Logic Data Book*, which contains device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *`design_name`*
Helvetica bold	Commands that you select from a menu	**File** → **Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *`design_name`*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr ={on|off}`**
Vertical bar |	Separates items in a list of choices	**`lowpwr ={on|off}`**

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *`block_name loc1 loc2 ... locn;`*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current file or in another file in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Virtex-II Prototype Platform

Package Contents

- Xilinx Virtex™-II Prototype Platform board
- User guide
- Device vacuum tool
- BNC to SMB cable
- Headers for test points
- CD-ROM

CD-ROM Contents

- User guide in PDF format
- Example design demonstration that flashes the on-board LED. This design includes the Verilog source code, **demo.v**, **demo.ucf**, and a **readme.txt** file
- Bitstream files (***.bit**) for each part type supported by the board (Bitstream synthesized using FPGA Compiler Version 1999.10)
- Full schematics of the board in both PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in ***.pho** and ***.pdf** for the PC board (There are many free or shareware Gerber file viewers available on the Web for viewing and printing these files)

Introduction

Virtex-II Prototype Platforms are prototype and demonstration boards that allow designers to investigate and experiment with the features of Virtex-II series FPGAs. This document describes the features and operation of the boards, including how to configure chains of FPGAs and serial PROMs. Prototype Platforms are intended strictly for evaluating the functionality of Virtex-II features and are not intended for A/C characterization or high-speed I/O evaluation.

Features

- Independent power supply jacks for V_{CCINT}, V_{AUX}, and V_{CCO}
- Selectable V_{CCO} for each SelectIO™ bank
- Configuration port for use with MultiLINX™ or Parallel Cable III cables
- Configuration mode switch

- Four global clock (GCLK) inputs
  - two 50Ω SMB connectors
  - two LVTTL-type oscillator sockets
- On-board programmable oscillator
- Selectable on-board clock frequency (from 25 MHz to 90 MHz)
- Power indicator LED
- 44-pin, VQFP PROM socket for any configuration mode
- JTAG port for reprogramming the XC17Vxx and XC18Vxx series reconfigurable PROMs and the User FPGA (DUT)
- Upstream and downstream System ACE and Configuration Interface connectors
- On-board battery holder

The kit contains headers that can be soldered to the breakout area, if desired. These headers are useful with certain types of oscilloscope probes for either connecting function generators or wiring pins to the prototype area.

The Virtex-II Prototype Platform board (referred to as "the board") contains two FPGAs, a Device Under Test (DUT) FPGA and a Service FPGA.

The DUT can be configured either by a PROM in the User PROM socket or by the PROM Daughter Card Interface header. The header allows the PROM to be substituted with a daughter board, permitting daisy-chaining of PROMs and experimentation with other configuration methods. (Consult the Xilinx data book, http://www.xilinx.com/partinfo/databook.htm, for selecting the appropriate PROM device for each particular Virtex-II device.)

In addition to the User PROM socket and the PROM Daughter Card Interface header, there are two upstream connectors and two downstream connectors. The upstream connectors can be connected to configure the DUT using any configuration source, such as a MultiLINX cable, Parallel Cable III, Parallel Cable IV, or System ACE. The downstream connectors can be used to connect to another board in a chain.

The Service FPGA is a switch matrix used to control the routing of all of the configuration signals on the board. This enables simple rotary switches (rather than jumpers) to control the board, minimizing training and errors. An XC18V01 serial PROM configures the Service FPGA. Neither this PROM nor the Service FPGA are part of the user configuration chain. Only the DUT and its related configuration PROM are part of the configuration chain.

Warning! Do not use the JTAG Interface Service PROM and FPGA header. This can cause the board to malfunction. This header is for internal use only.

Figure 1 shows a block diagram of the board.

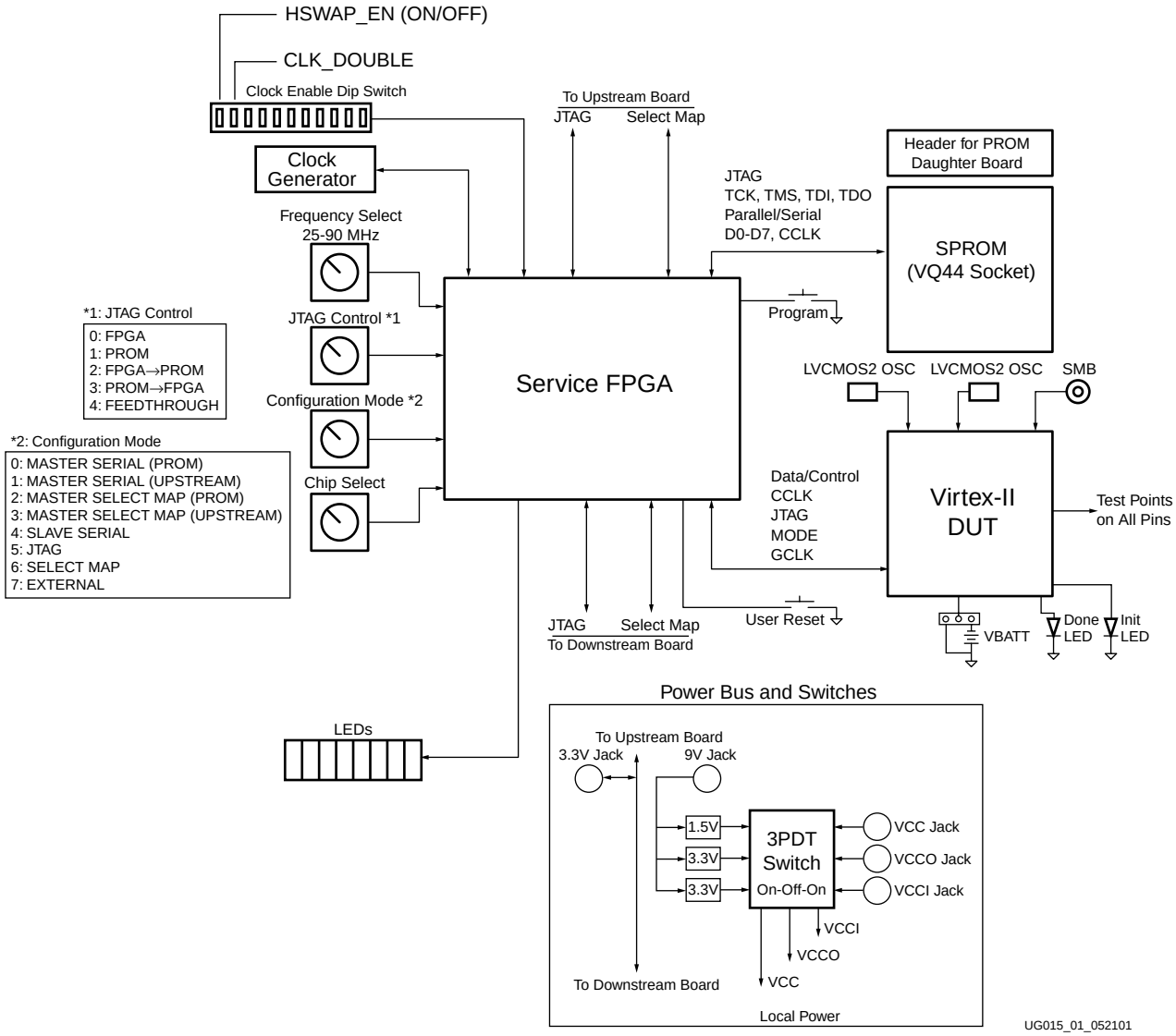

Figure 1: **Virtex-II Prototype Platform Block Diagram**

Detailed Description

The Virtex-II Prototype Platform board is shown in Figure 2. Each feature is detailed in the numbered sections that follow.

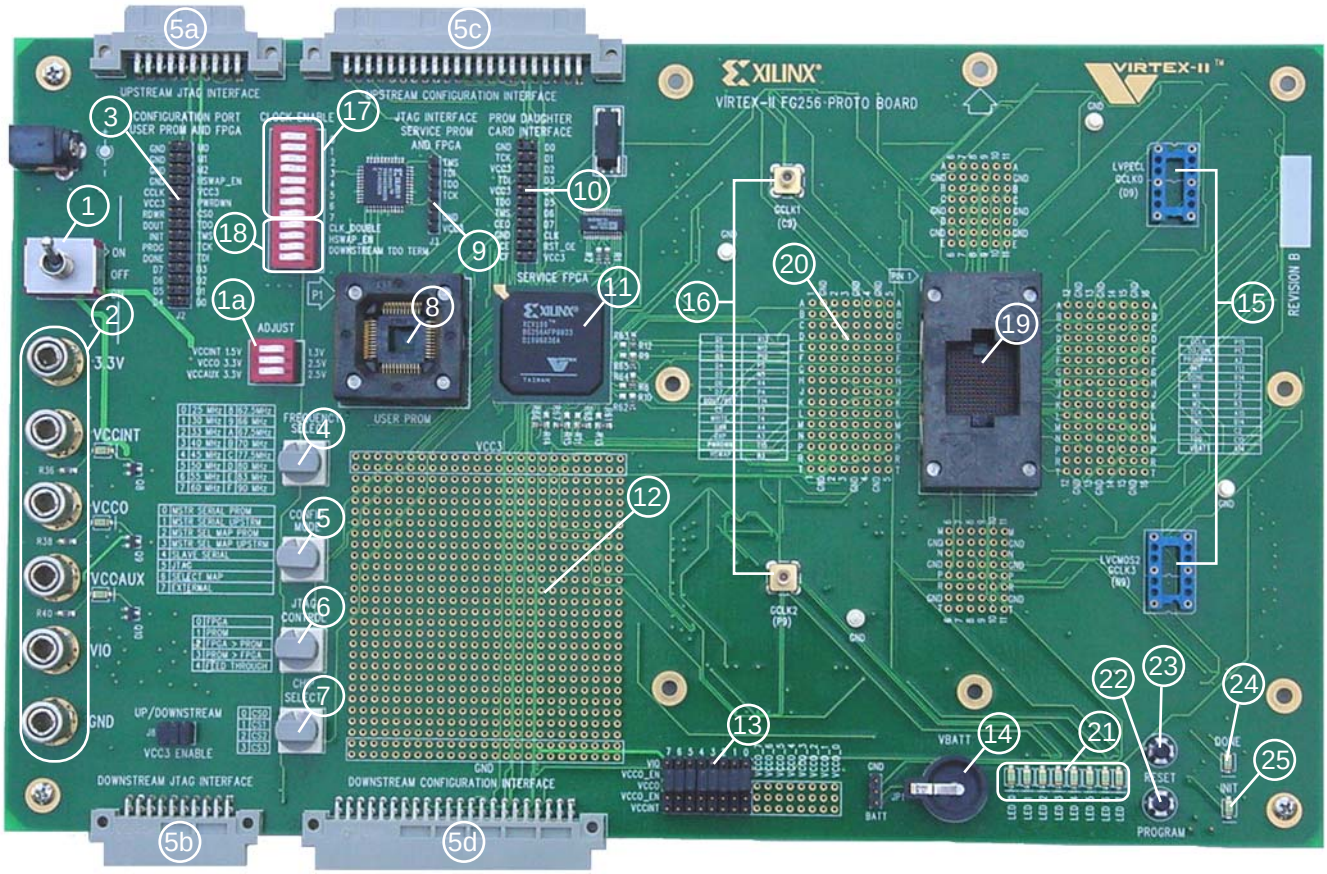

Figure 2: **Detailed Description of Virtex-II Prototype Platform Components**

1. Power Switch

The board has an on-board power supply and a three-position power switch: upward on, off, and downward on. When lit, a green LED indicates power to the device core when V_{CCINT} is 1.5V or higher.

Upward On Position

In the upward on position, the power switch enables delivery of all power to the board by way of voltage regulators situated on the backside of the board. These regulators feed off an external power brick with a voltage range from 5-14V. Special circuitry delivers the required power to the Service FPGA and Service PROM.

The voltage regulators deliver fixed voltages; however, you can adjust these voltages by changing the settings on the dip switch site marked ADJUST (1a) as shown in Figure 2. Maximum current range for each supply is 500 mA.

Table 1: **Voltage Ranges**

Label	Max Voltage	Min Voltage
VCCINT	1.5V	1.3V
VCCO	3.3V	2.5V
VCCAUX	3.3V	2.5V

Off Position

In the off position, the power switch disables all modes of powering the DUT in stand-alone operation.

Downward On Position

In the downward on position, the power switch enables delivery of all power from the six power supply jacks.

2. Power Supply Jacks

In the downward on position, the power switch enables delivery of power to the board by way of the power supply jacks. These six jacks are:

- 3.3V
  - Supplies power to the on-board serial PROM, to the Service FPGA and its supporting PROM, to the two oscillators, and to all pins marked V_{CC3} on the board. This includes pins in the configuration port (user PROM and FPGA), the prototyping area, and the V_{CC3} enable jumpers
- VCCINT
  - Supplies voltage to the core of the DUT (Consult the Xilinx data book, http://www.xilinx.com/partinfo/databook.htm, for the maximum V_{CCINT} voltage for the device you are using)
- VCCO
  - Supplies I/O voltages to the DUT
  - Each can be powered from one of three sources (V_{CCO}, V_{CCINT}, or V_{IO}) by appropriate placement of jumpers on the header
- VCCAUX
  - Supplies voltage to the V_{AUX} header and the V_{AUX} DUT pins
- VIO
  - Supplies voltage to the V_{IO} header (not to the DUT)
  - Provides the option of an additional voltage source for the V_{CCO} banks
  - Can be driven externally or from the board
- GND

3. Configuration Port User PROM and FPGA Header

This header is used to connect a MultiLINX cable or Parallel Cable III cable to the board and supports all Virtex-II device configuration modes. (See Table 4 for connecting cables to the Configuration Port User PROM and FPGA header.)

4. Frequency Select Switch

The frequency select switch sets the frequency of the on-board clock generator. One of sixteen frequencies can be selected as shown in Table 2.

Table 2: **Clock Generator Frequencies**

Switch Position	Clock Frequency	Switch Position	Clock Frequency
0	25 MHz	8	62.5 MHz
1	30 MHz	9	66 MHz
2	33 MHz	A	67.5 MHz
3	40 MHz	B	70 MHz
4	45 MHz	C	77.5 MHz
5	50 MHz	D	80 MHz
6	55 MHz	E	83 MHz
7	60 MHz	F	90 MHz

5. Configuration Mode Switch

The configuration mode switch determines the configuration mode of the DUT using the options shown in Table 3.

Table 3: **Configuration Mode Options**

Switch Position	Mode Label
0	MSTR SERIAL PROM
1	MSTR SERIAL UPSTRM
2	MSTR SEL MAP PROM
3	MSTR SEL MAP UPSTRM
4	SLAVE SERIAL
5	JTAG
6	SELECT MAP
7	EXTERNAL

In master serial configuration modes, the DUT is configured from either the on-board serial PROM, the Upstream Configuration Interface connector, or the Configuration Port User PROM and FPGA header.

In either of the master serial configuration modes, the **CCLK** and **DIN** (**D0**) signals are routed to the Downstream Configuration Interface connector to allow daisy-chaining to downstream slave serial devices.

Note: Only one master serial device is allowed in a chain and it must be the first FPGA device in the stream.

In master select map modes, the **CCLK** and **D0-D7** signals are routed to the Downstream Configuration Interface connector to allow daisy-chaining to downstream devices.

Note: For more details on configuration modes, consult the Xilinx Data Book located at: http://www.xilinx.com/partinfo/databook.htm.

Master Serial PROM Mode

In switch position 0 (Master Serial PROM) the on-board PROM is used as the configuration data source.

Master Serial UPSTREAM Mode

In switch position 1 (Master Serial UPSTREAM) the Upstream Configuration Interface connector or the Configuration User PROM and FPGA header can be used as the configuration data source. All configuration signals from/to the DUT are then routed accordingly.

Table 4 shows the Configuration Port User PROM and FPGA header pins on the board and the corresponding pins for connecting MultiLINX or Parallel Cable III cables for serial mode.

Table 4: **Serial Mode**

Configuration Port User PROM and FPGA Header	MultiLINX Pins	Parallel Cable III Pins
VCC3	PWR	VCC
GND	GND	GND
CCLK	CCLK	CCLK
DONE	DONE	D/P
D0	DIN	DIN
PROG	PROG	PROG
INIT	INIT	

Master Select Map PROM Mode

In switch position 2 (Master Select Map PROM) the on-board PROM or PROM daughter card interface is used as the configuration data source for the DUT. The PROM, the **M0-M2**, **CS**, and the **RW** signals are set by the Service FPGA.

Master Select Map UPSTREAM Mode

In switch position 3 (Master Select Map UPSTREAM) the Upstream Configuration Interface connector or the Configuration Port User PROM and FPGA header can be used as a configuration data source for the DUT. All configuration signals from/to the DUT are then routed accordingly. In this mode, the **CCLK** and **D0-D7** are routed to the Downstream Configuration Interface connector to allow daisy-chaining to downstream

devices. When configuring from the Upstream Configuration Interface connector, the **M0-M2**, **CS**, and **RW** signals are set by the Upstream Configuration Interface connector or the Configuration User PROM and FPGA header pins.

Table 5 shows the Configuration Port User PROM and FPGA header pins on the board and the corresponding pins for connecting the MultiLINX cable for select map mode.

Table 5: **Select Map Mode**

Configuration Port User PROM and FPGA Header	MultiLINX Pins
VCC3	PWR
GND	GND
CCLK	CCLK
DONE	DONE
PROG	PROG
INIT	INIT
CS0	CS0 (CS)
RDWR	RS (RDWR)
DOUT	RDY/BUSY
D0	D0
D1	D1
D2	D2
D3	D3
D4	D4
D5	D5
D6	D6
D7	D7

Slave Serial Mode

In switch position 4 (Slave Serial) either the Upstream Configuration Interface connector or the Configuration Port User PROM and FPGA header are used as a configuration data source for configuring the DUT in slave serial format. In this mode, the upstream device supplies the **CCLK** and **DIN** signals, as well as all other configuration signals to the DUT. (See Table 4 for connecting to the Configuration Port User PROM and FPGA header.)

JTAG Mode

In switch position 5 (JTAG) the System ACE connectors to upstream and downstream boards are selected. Each System ACE connector contains pins for each of the four JTAG signals: **TCK**, **TMS**, **TDI**, and **TDO**.

TCK and TMS are parallel feedthrough connections from the upstream System ACE connector to the downstream System ACE connector and drive the **TCK** and **TMS** pins of

the on-board PROM and the DUT. **TDI** is a serial JTAG chain input and **TDO** is a serial JTAG chain output.

Note: The DOWNSTREAM_TDO TERM switch must be set to the "on" position on the last board in the chain to connect the **TDO** pin of the final device to the TDO feedback chain.

Table 6: **JTAG Mode**

Configuration Port User PROM and FPGA Header	MultiLINX Pins	Parallel Cable III Pins
VCC3	PWR	VCC
GND	GND	GND
TMS	TMS	TMS
TDI	TDI	TDI
TDO	RD (TDO)	TDO
TCK	TCK	TCK

Select Map Mode

In switch position 6 (Select Map) the configuration data is supplied byte wide from the Upstream Configuration Interface connector or from the Configuration Port User PROM and FPGA Header and requires an external clock source. The mode pins **M0**-**M2** are set by the Service FPGA. The **CS** and **RDWR** signals are generated from the Upstream Configuration Interface connector. (See Table 5 for connecting to the Configuration Port User PROM and FPGA header.)

Configuration/Readback from the Upstream Connector

To use configuration/readback mode, you must set the configuration mode switch to position 6 (Select Map). You must also set the chip select switch to provide each device in the chain a unique ID. (See "7. Chip Select Switch".)

In this mode of configuration, byte-wide data is obtained from the Upstream Configuration Interface connector. The **CS** and **RDWR** pins are also supplied by the Upstream Configuration Interface connector.

The **RDWR** pin on the Upstream Configuration Interface connector determines the data direction. When **RDWR** is low, the data flows from the DUT to the Upstream Configuration Interface connector.

The value of the **INIT** pin on the Upstream Configuration Interface connector will be the value of the **INIT** pin on the DUT, AND'ed with the **INIT** pin from the Downstream Configuration Interface connector. Therefore, **INIT** will only be high when all **INIT** pins in the chain are high.

The value of the **DONE** pin on the Upstream Configuration Interface connector will be the value of the **DONE** pin on the DUT, AND'ed with the **DONE** pin from the downstream configuration connector. Therefore, **DONE** will only be high when all **DONE** pins in the chain are high. There is a 330Ω pullup resistor on the **DONE** pin of the DUT.

External Mode

In switch position 7 (External) the external configuration mode places all connections from the Service FPGA to the DUT in a high-impedance condition. In this mode, the prototype board acts as a simple breakout board and all connections to the DUT (except for power)

must be provided by the user. The only services provided by the board in this mode are the on-board oscillators, the DONE and INIT LEDs, and VBATT. All connections to the configuration pins must be made using the breakout test points.

5a. Upstream System ACE Connector

The Upstream System ACE connector, as shown in Figure 3, can be used to configure the DUT. This connector can be sourced by any JTAG configuration stream. For example, a System ACE Controller with CompactFlash can be used to generate very large JTAG streams for configuring multiple Virtex-II Prototype Platforms using the Downstream System ACE connector.

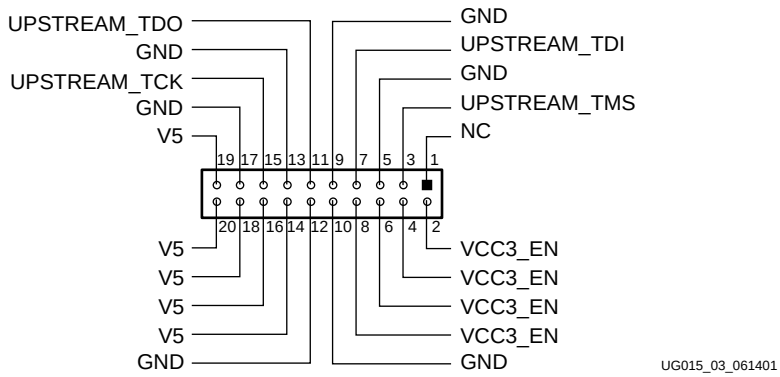

Figure 3: **Upstream System ACE Connector, 20-Pin Female**

5b. Downstream System ACE Connector

The Downstream System ACE connector, as shown in Figure 4, is used to pass configuration information to a DUT in a downstream prototype platform from sources such as a MultiLINX cable, Parallel Cable III, or an Upstream System ACE connector.

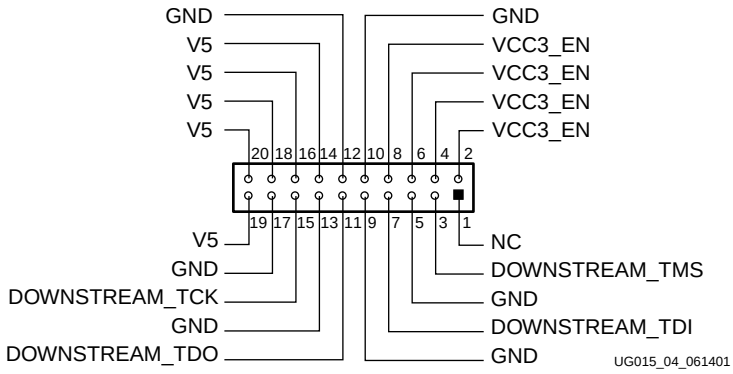

Figure 4: **Downstream System ACE Connector, 20-Pin Male**

5c. Upstream Configuration Interface Connector

The Upstream Configuration Interface connector, as shown in Figure 5, is used to configure the DUT in select-map or slave-serial mode. This connector can only be sourced by a the Downstream Configuration Interface connector of another prototype platform.

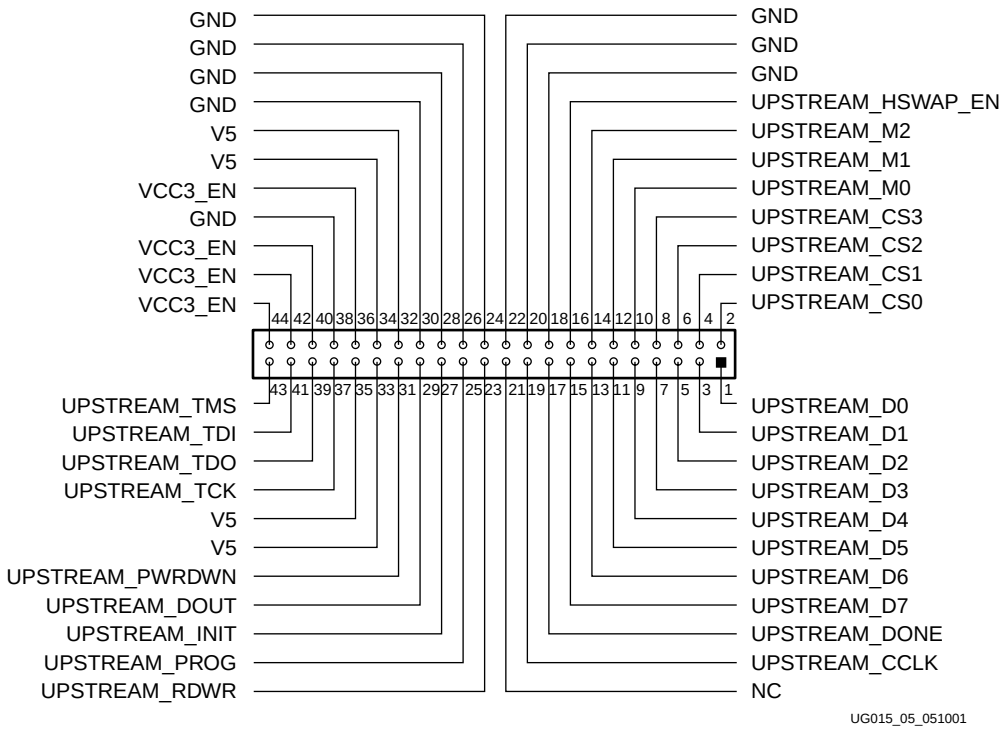

Figure 5: **Upstream Configuration Interface Connector, 44-Pin Female**

5d. Downstream Configuration Interface Connector

The Downstream Configuration Interface connector, as shown in Figure 6, passes select-map or slave-serial configuration information to a DUT in a downstream prototype platform from sources such as a MultiLINX cable or a Parallel Cable III.

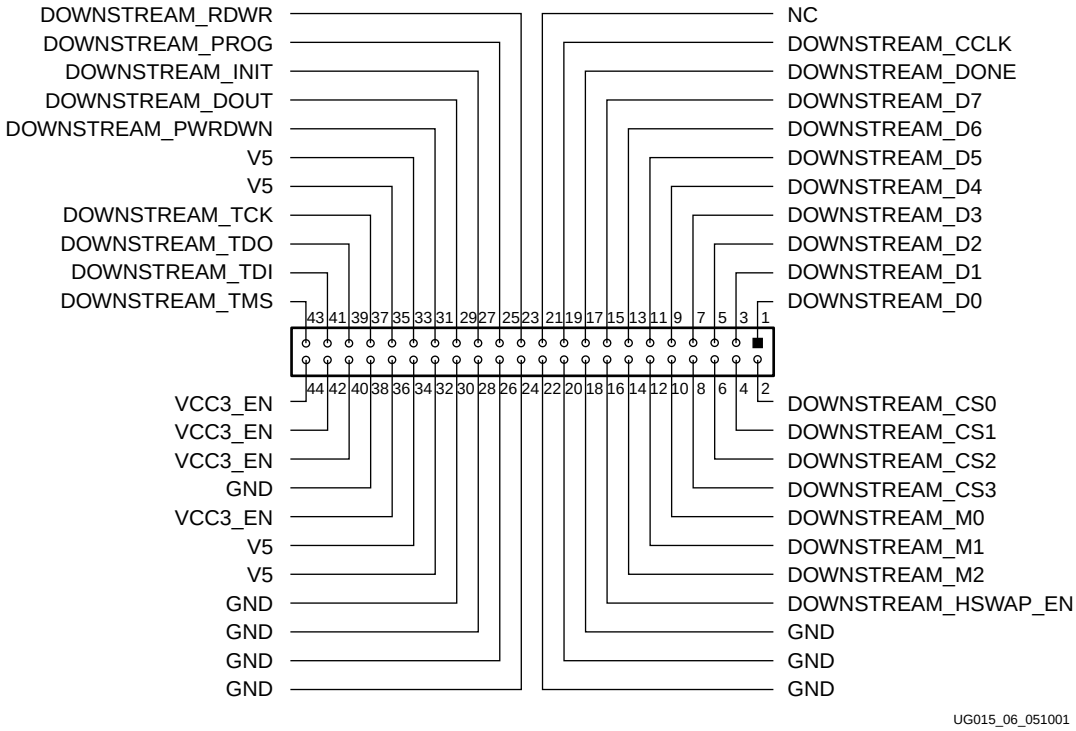

Figure 6: **Downstream Configuration Interface Connector, 44-Pin Male**

6. JTAG Control Switch

The JTAG control switch is functional only when the configuration mode switch is set to JTAG (position 5). The JTAG control switch is used to select the order of the devices in the JTAG chain using the options shown in Table 7.

Table 7: **JTAG Control Options**

Switch Number	Mode	Description
0	DUT	DUT only in chain
1	PROM	User PROM only in chain
2	DUT → PROM	DUT first, PROM second in chain
3	PROM → DUT	PROM first, DUT second in chain
4	Feedthrough	Allows a board to be switched out of the JTAG chain without physically removing it

Note:

1. The Service FPGA and its supporting Service PROM are not part of the JTAG chain.
2. Since all of the JTAG signals are routed in and out of the Service FPGA multiple times, use caution to not run the JTAG bus too fast.

7. Chip Select Switch

The chip select switch assigns a unique identification (ID) to each DUT in a select map configuration chain. This switch may be set from 0 to 3, allowing up to four devices to be configured/read back in a select map chain. During readback, each board in the chain must have a unique ID, otherwise more than one device will drive the data bus. However, multiple DUTs may be set to the same ID for "Select Map Mode" configuration. Pins on the configuration connectors correspond to each ID. The **CS** pin on the DUT will be connected to the **CS** pin on the configuration connector that corresponds to its chip select switch.

The **CS** pin on the DUT is set to zero, by default, when the configuration mode is set to Master Select Map PROM. Otherwise, its value is dependent on the value of the **UPSTREAM_CS[3:0]** pins.

8. User PROM Socket

The user PROM socket can be used to configure the Virtex-II device in master serial mode. The socket accepts XC17V01-V04 and XC18V01-V04 series configuration PROMs in VQ44 packages. The PROM port can also be used to reprogram the PROM using JTAG. (Consult the Xilinx data book, http://www.xilinx.com/partinfo/databook.htm, for selecting the appropriate PROM device for each particular Virtex-II device.)

9. JTAG Interface, Service PROM, and FPGA Header

In addition to the user PROM, the board has a dedicated XC18V01 serial PROM that configures the Service FPGA. The Service PROM and the Service FPGA are not part of the user configuration chain. Only the DUT and its related configuration PROM are part of the configuration chain.

Warning! Do not use the JTAG Interface Service PROM and FPGA header. This can cause the board to malfunction. This header is for internal use only.

10. PROM Daughter Card Interface

This header is located near the User PROM socket so that the PROM may be substituted with a daughter board, permitting daisy-chaining of PROMs and experimentation with other configuration methods.

Note: PROM substitution is dependent upon configuration and JTAG switch settings.

11. Service FPGA

In addition to the DUT FPGA, the board contains a Service FPGA. The Service FPGA acts as a switch matrix to control the routing of all of the configuration signals on the board. This enables simple rotary switches (rather than jumpers) to control the board, minimizing training and errors. The Service FPGA is configured by a dedicated Service PROM. The Service FPGA and the Service PROM are not part of the user configuration chain. Only the DUT and its related configuration PROM are part of the configuration chain.

Warning! Do not use the JTAG Interface Service PROM and FPGA header. This can cause the board to malfunction. This header is for internal use only.

12. Prototyping Area

The prototyping area accommodates 0.10" spaced ICs. The kit contains headers that can be soldered to the breakout area, if desired. Power and ground buses are located at the top and bottom, respectively, of the prototyping area.

13. V_{CCO} Supply Jumpers

Virtex-II series devices have eight SelectIO banks, labeled 0 through 7, each with a V_{CCO} supply. VCCO_EN supply jumpers can connect each bank to one of the three on-board supplies, V_{CCINT}, V_{CCO}, or externally from V_{IO}. These jumpers must be installed for the Virtex-II device to function normally.

14. VBATT

An on-board battery holder is connected to the VBATT pin of the DUT. If an external power supply is used, the associated jumper must be removed. Select a 12 mm lithium coin battery (3V), such as part numbers BR1216, CR1216, and BR1225 from Panasonic or any other appropriate 12 mm lithium coin battery (3V).

15. Oscillator Sockets

The prototype board has two crystal oscillator sockets, both wired for standard LVTTL-type oscillators. These sockets connect to the DUT clock pads as shown in Table 8. On-board termination resistors can be changed by the user. The oscillator sockets accept both half- and full-sized oscillators and are powered by the 3.3V power supply.

Table 8: **OSC Clock Pin Connections**

Label	FG256		FG456		FG676		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
OSC Socket Top	GCLK0S	D9	GCLK0S	D12	GCLK0S	F14	GCLK7P	K18
OSC Socket Bottom	GCLK3S	N9	GCLK3S	W12	GCLK3S	AA14	GCLK4P	AF18

16. Function Generator Clock Inputs

In addition to the oscillator sockets, there are two 50Ω SMB connectors that allow connection to an external function generator. These connect to the DUT clock pads as shown in Table 9.

Table 9: **SMB Clock Pin Connections**

Label	FG256		FG456		FG676		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
SMB Top	GCLK1P	C9	GCLK1P	E12	GCLK1P	G14	GCLK6S	J18
SMB Bottom	GCLK2P	P9	GCLK2P	Y12	GCLK2P	AB14	GCLK5S	AG18

17. Clock Enable Switches 0-7

The user has access to eight additional global clocks on the DUT. These clocks can be enabled by setting the appropriate dip switches shown in Table 10. After selecting the clock frequency, all enabled clocks run at that frequency.

Table 10: **Dip Switches and Associated Global Clocks**

Label	FG256		FG456		FG676		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
CLOCK ENABLE 0	GCLK1S	R9	GCLK1S	AA12	GCLK1S	AC14	GCLK6P	AK19
CLOCK ENABLE 1	GCLK6P	R8	GCLK6P	Y11	GCLK6P	AB13	GCLK1S	AK16
CLOCK ENABLE 2	GCLK5S	P8	GCLK5S	W11	GCLK5S	AA13	GCLK2P	AG17
CLOCK ENABLE 3	GCLK4P	N8	GCLK4P	V11	GCLK4P	Y13	GCLK3S	AF17
CLOCK ENABLE 4	GCLK7P	D8	GCLK7P	D11	GCLK7P	F13	GCLK0S	H16
CLOCK ENABLE 5	GCLK6S	C8	GCLK6S	C11	GCLK6S	E13	GCLK1P	H17
CLOCK ENABLE 6	GCLK5P	B8	GCLK5P	B11	GCLK5P	D13	GCLK2S	E16
CLOCK ENABLE 7	GCLK2S	B9	GCLK2S	F13	GCLK2S	H15	GCLK5P	E19

The frequency of each of these clocks can be doubled by setting the CLK_DOUBLE switch, shown in Table 11. Clock doubling is achieved by the DLL in the Service FPGA. However, setting this switch doubles the frequency of all enabled clocks.

The remaining four FPGA global clocks are accessible through the header pins surrounding the DUT.

Note:

1. When LED 7 is lighted before configuration, it implies that the DLL is locked.
2. The above 12 global clocks are not available through the breakout area test points.

18. Clock Enable Switches 8-12

The remaining four clock enable switches are described in Table 11.

Table 11: **Dip Switches 8-12**

Label	Function
CLK_DOUBLE	Doubles the frequency of all enabled clocks
HSWAP_EN	Controls user I/O pullups before configuration
DOWNSTREAM_TDO_TERM	Connects TDO of last device back to the feedback chain
(not used)	

Note: For more information about HSWAP, see the Xilinx Data Book available at: http://www.xilinx.com/partinfo/databook.htm.

19. DUT Socket

The DUT socket contains the user FPGA, referred to as the Device Under Test.

The device must be oriented using the P1 indicator on the board. Failure to insert the device to the proper orientation can damage the device. To avoid pin damage, always use the vacuum tool provided when inserting or removing the Virtex-II device. When using BGA packages, do not apply pressure to the device while activating the vacuum tool lever. Doing so can damage the socket and/or the device.

20. Pin Breakout

The pin breakout area is used to monitor or apply signals to each of the DUT pins. Headers can be soldered to the breakout area to use with certain types of oscilloscope probes, for either connecting function generators or wiring pins to the pin breakout area. Clocks in the pin breakout area that connect to the DUT clock pads are shown in Table 12.

Table 12: **Breakout Clock Pin Connections**

Label	FG256		FG456		FG676		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
Breakout Area 1	GCLK3P	A9	GCLK3P	F12	GCLK3P	H14	GCLK4S	E18
Breakout Area 2	GCLK4S	A8	GCLK4S	A11	GCLK4S	C13	GCLK3P	E17
Breakout Area 3	GCLK7S	T8	GCLK7S	AA11	GCLK7S	AC13	GCLK7S	AK18
Breakout Area 4	GCLK0P	T9	GCLK0P	AB12	GCLK0P	AD14	GCLK0P	AK17

21. User LEDs (Active-High)

There are eight active-high user LEDs on the board. Before configuration, the LEDs reflect the status of the configuration mode switch. During configuration, the LEDs are in a high-impedance condition. After configuration, the LEDs are available to the user and reflect the status of pins **D0-D7** (corresponding to LED 0-LED 7). The LED assignments are shown in Table 13.

Table 13: **LED Assignments and Corresponding I/O**

Configuration Mode Status				Pin Number For Package Type			
LED	Before and During Configuration	After Configuration	Status Pin	FG256	FG456	FG676	FF1152
LED 0	Master Serial PROM	Available as user LEDs	D0	P13	V18	Y20	AG10
LED 1	Master Serial UPSTREAM		D1	R13	V17	Y19	AH11
LED 2	Master Select MAP PROM		D2	N12	W18	AA20	AK7
LED 3	Master Select Map UPSTREAM		D3	P12	Y18	AB20	AK8
LED 4	Slave Serial		D4	P5	Y5	AB7	AK28
LED 5	JTAG		D5	N5	W5	AA7	AL29

Table 13: **LED Assignments and Corresponding I/O *(Continued)***

Configuration Mode Status				Pin Number For Package Type			
LED	**Before and During Configuration**	**After Configuration**	**Status Pin**	**FG256**	**FG456**	**FG676**	**FF1152**
LED 6	Select Map		D6	R4	AB4	AD6	AG24
LED 7	DLL Locked Status		D7	P4	AA4	AC6	AG25

22. Program Switch

The active-low program switch, when pressed, grounds the program pin on the DUT. This switch is driven indirectly by the Service FPGA.

23. Reset Switch (Active-Low)

The reset switch connects (indirectly through the Service FPGA) to the **INIT** pin on the DUT, allowing the user, after configuration, to reset the logic within the DUT. Before and during configuration of the DUT, the **INIT** pin has no function. After configuration, the **INIT** pin becomes a regular I/O. When pressed, this switch grounds the **INIT** pin.

24. DONE LED

The DONE LED indicates the status of the **DONE** pin on the DUT. This LED lights when **DONE** is high or if power is applied to the board without a part in the socket.

25. INIT LED

The INIT LED lights during initialization.

User Programmable Pins

Table 14 shows the user hardware that corresponds to available DUT package types.

Table 14: **User Hardware and Corresponding I/Os**

Label	Pin Number For Package Type			
	FG256	FG456	FG676	FF1152
RESET (INIT)	T13	AA19	AC21	AL5
D0/LED 0	P13	V18	Y20	AG10
D1/LED 1	R13	V17	Y19	AH11
D2/LED 2	N12	W18	AA20	AK7
D3/LED 3	P12	Y18	AB20	AK8
D4/LED 4	P5	Y5	AB7	AK28
D5/LED 5	N5	W5	AA7	AL29
D6/LED 6	R4	AB4	AD6	AG24
D7/LED 7	P4	AA4	AC6	AG25

Note: Refer to the **readme.txt** file for implementation of these user pins.

Table 15 shows the clock pins and corresponding I/Os.

Table 15: **Clock Pins and Corresponding I/Os**

Clock Pins	FG256		FG456		FG676		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
CLOCK ENABLE 0	GCLK1S	R9	GCLK1S	AA12	GCLK1S	AC14	GCLK6P	AK19
CLOCK ENABLE 1	GCLK6P	R8	GCLK6P	Y11	GCLK6P	AB13	GCLK1S	AK16
CLOCK ENABLE 2	GCLK5S	P8	GCLK5S	W11	GCLK5S	AA13	GCLK2P	AG17
CLOCK ENABLE 3	GCLK4P	N8	GCLK4P	V11	GCLK4P	Y13	GCLK3S	AF17
CLOCK ENABLE 4	GCLK7P	D8	GCLK7P	D11	GCLK7P	F13	GCLK0S	H16
CLOCK ENABLE 5	GCLK6S	C8	GCLK6S	C11	GCLK6S	E13	GCLK1P	H17
CLOCK ENABLE 6	GCLK5P	B8	GCLK5P	B11	GCLK5P	D13	GCLK2S	E16
CLOCK ENABLE 7	GCLK2S	B9	GCLK2S	F13	GCLK2S	H15	GCLK5P	E19
OSC Socket Top	GCLK0S	D9	GCLK0S	D12	GCLK0S	F14	GCLK7P	K18
OSC Socket Bottom	GCLK3S	N9	GCLK3S	W12	GCLK3S	AA14	GCLK4P	AF18
SMB Top	GCLK1P	C9	GCLK1P	E12	GCLK1P	G14	GCLK6S	J18
SMB Bottom	GCLK2P	P9	GCLK2P	Y12	GCLK2P	AB14	GCLK5S	AG18
Breakout Area 1	GCLK3P	A9	GCLK3P	F12	GCLK3P	H14	GCLK4S	E18
Breakout Area 2	GCLK4S	A8	GCLK4S	A11	GCLK4S	C13	GCLK3P	E17

Table 15: **Clock Pins and Corresponding I/Os *(Continued)***

Clock Pins	FG256		FG456		FG676		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
Breakout Area 3	GCLK7S	T8	GCLK7S	AA11	GCLK7S	AC13	GCLK7S	AK18
Breakout Area 4	GCLK0P	T9	GCLK0P	AB12	GCLK0P	AD14	GCLK0P	AK17