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Virtex-II LVDS Demonstration Board

User Guide

UG019 (1.0.2) September 14, 2005

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Virtex-II LVDS Demonstration Board

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The following table shows the revision history for this document.

Date	Version	Revision
12/06/01	1.0	Initial Xilinx release.
09/22/01	1.0.1	Updated links to: **http://www.xilinx.com/bvdocs/userguides/ug019.zip** file.
09/14/05	1.0.2	Updated link to DS031: **http://direct.xilinx.com/bvdocs/publications/ds031.pdf**

Contents

Chapter 1

LVDS High-Speed Serial I/O Demonstration Board

Summary

This document describes the Virtex™-II LVDS high-speed serial I/O demonstration board.

General Description

The Virtex-II LVDS High-Speed Serial I/O demonstration board is a compact board for testing of different LVDS and high speed serial applications. The board has an LCD display, several LEDs, switches, and connectors to work with different demonstration designs. The board can demonstrate LVDS solutions at 840 Mb/s over high-speed serial I/O using fiber-optic or cable media. Figure 1-1 shows the PCB overview drawing.

LVDS

LVDS is a popular and powerful high-speed interface used in many systems applications. Virtex-II I/Os are designed to comply with the IEEE 1596.3 electrical specification for LVDS, making system and board design easier. The LVDS board is designed to demonstrate two different solutions: a 16-bit data, one-clock LVDS over cable and a 16-bit data, one-clock LVDS over PCB traces.

High-Speed Serial I/O

To demonstrate high-speed serial I/O, the demonstration board includes a TLK2501 SerDes device. By using the SerDes device, serial communications of up to 2.5 Gb/s are possible. These speeds are available over optical fiber and copper wire.

Edge Connection

An extra connector is available to host daughter boards to demonstrate other possible applications.

- High-speed serial communication board using SerDes device
- Separate memory device board

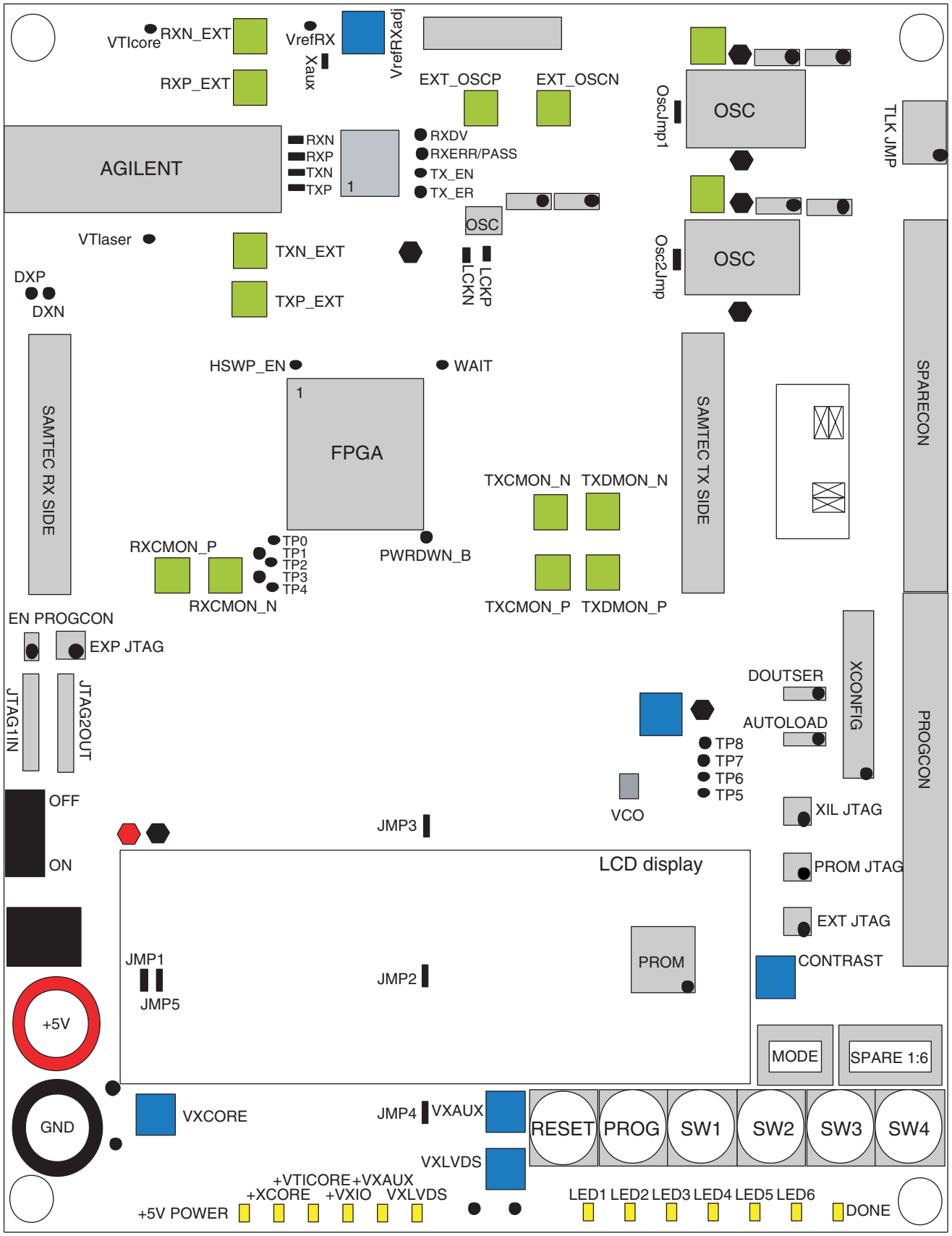

Figure 1-1: **PCB Overview Drawing**

Power Supply

The external board power supply is +5 VDC ± 10%. An AC-DC switching power supply is connected with either a jack connector or a banana connector from lab power supply. Several regulators are used on the board to provide the different voltages needed by various components.

- 1.5 V for the core voltage of the FPGA (VXICORE)
- 3.3 V for the auxiliary supply of the FPGA I/Os. (VXAUX3.3V)
- 3.3 V for the input/output supply of the FPGA I/Os. (VXIO3.3V)
- 3.3 V for the LVDS input and output supply of the FPGA I/Os. (VXLVDS3.3V)
- 5V for the LCD, and as input voltage for all the other regulators
- 2.5V for the TLK2501. The regulator (IC12) providing this voltage is closely located to the high speed serial device TLK2501.
- 3.3V for the Agilent Laser. The regulator (IC11) providing this voltage is closely located to the laser device Agilent HFBR5010E.

Each power supply is adjustable with a potentiometer and has a state indicator LED and a test point. The popular LM1117TX-adj is used as a device regulator. Further information on the power supply is available in Chapter 2.

LCD Panel

The PowerTip PC2002LRU-LSO-H 20-character LCD display is a two-line display with a 5 x 8 dot matrix plus a cursor. The LCD panel is mounted on top of the voltage regulators and flash serial PROM. The LCD connection to the demonstration board is made with a flex-strip connection. A flex-strip connection makes it easy to remove the LCD while under power. In this way, different types of LCD panels can be easily connected. Table 1-1 lists the LCD pin descriptions and FPGA connections.

Table 1-1: **LCD Pin Descriptions and FPGA Connections**

Pin Number	Symbol	Function	FPGA Pin	Schematic
1	V_{SS}	Power Supply (GND)		GND
2	V_{DD}	Power Supply (+5 V)		+5 V
3	V_O	Contrast Adjust		CON
4	RS	Register Selection	U11	UISEL
5	R/W	Read / Write Selection		GND
6	E	Read / Write Enable	U10	UIEN
7 - 10	$DB_0 – DB_3$	Data Bus	AB8, AA8, AB7, AA7	UID0 – UID3
11- 14	$DB_4 – DB_7$	Data Bus	AB6, AA6, AB5, AA5	UID4 – UID7
-	A	LED Backlight (+)		
-	K	LED Backlight (-)		

The information needed to build the steering design for the LCD panel is provided below. The LCD write diagram is shown in Figure 1-2. Table 1-2 lists the LCD write timing. Table 1-3 lists the display commands. Figure 1-3 shows the display initialization sequence, and Figure 1-4 is the LCD panel character set.

Write Cycle for the LCD

Reading from the LCD panel memory is not implemented on this demonstration board.

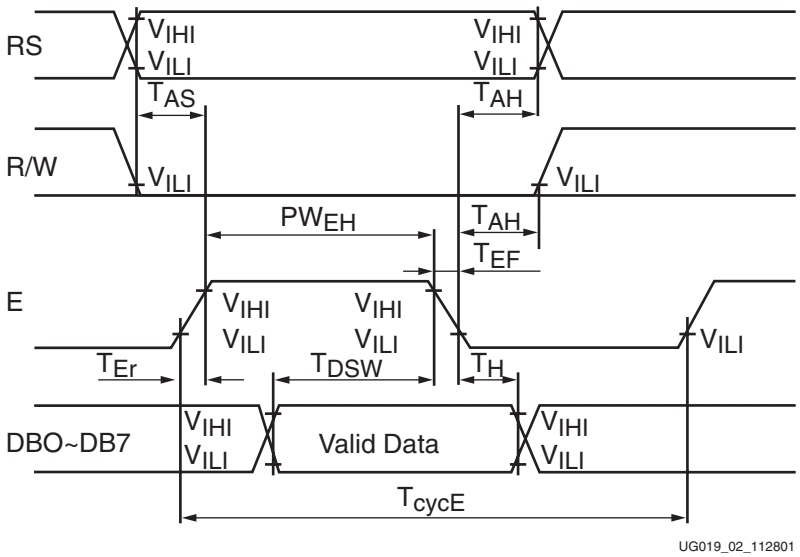

Figure 1-2: **LCD Write Diagram**

Table 1-2: **LCD Write Timing**

Item	Symbol	MIN	TYP	MAX	Units
Enable cycle timing	T_{CYCLE}	1.0			µs
Enable pulse width	P_{WEN}	450			ns
Enable rise/fall time	t_{ER}, t_{EF}			25	ns
RS, R/W setup time		140			ns
Data delay time	t_{DDR}			320	ns
Data setup time	t_{DSW}	195			ns
Hold time	t_H	20			ns
Input High voltage	V_{IH}		2.2		V
Input Low voltage	V_{IL}		0.6		V

Display Commands

Table 1-3 provides display commands. Notes to the table are given on the next page.

Table 1-3: **Display Commands**

Instruction	Code										Description (Notes 2 and 3)	Maximum Execution Time (Note 1)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets Data Display Ram (DDR) address 0 in address counter.	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DDR address 0 in address counter. Also returns display being shifted to original position. DDR contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40 µs
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DDR contents.	40 µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L), and character fonts (F).	40 µs
Set CG RAM Address	0	0	0	1	ACG						Sets Character Generator RAM (CGR) address. CGR data is sent and received after this setting.	40 µs
Set DD RAM Address	0	0	1	ADD							Sets DDR address. CGR data is sent and received after this setting.	40 µs
Read Busy Flag and Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 µs
Write Data to CG or DDR	1	0	Write Data								Writes data into DDR or CGR.	40 µs

Notes:

1. Maximum execution time is when f_{cp} or f_{osc} is 250 kHz. Execution time changes when frequency changes.

   Example: When f_{cp} or f_{osc} is 270 kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

2. DD RAM: Display data RAM
   CG RAM: Character generator RAM
   ACG: CG RAM address
   ADD: DDR address - corresponds to cursor address
   AC: Address counter used for both DDR and CG RAM address.

I/D = 1: Increment or I/D = 0: Decrement
S = 1: Accompanies display shift
S/C = 1: Display shift or S/C = 0: Cursor move
R/L = 1: Shift to the right or R/L = 0: Shift to the left
DL = 1: 8 bits or DL = 0: 4 bits
N = 1: 2 lines or N = 0: 1 lines
F = 1: 5 x 10 dots or F = 0: 5 x 7 dots
FB = 1: Internally operating or FB = 0: Can accept instruction

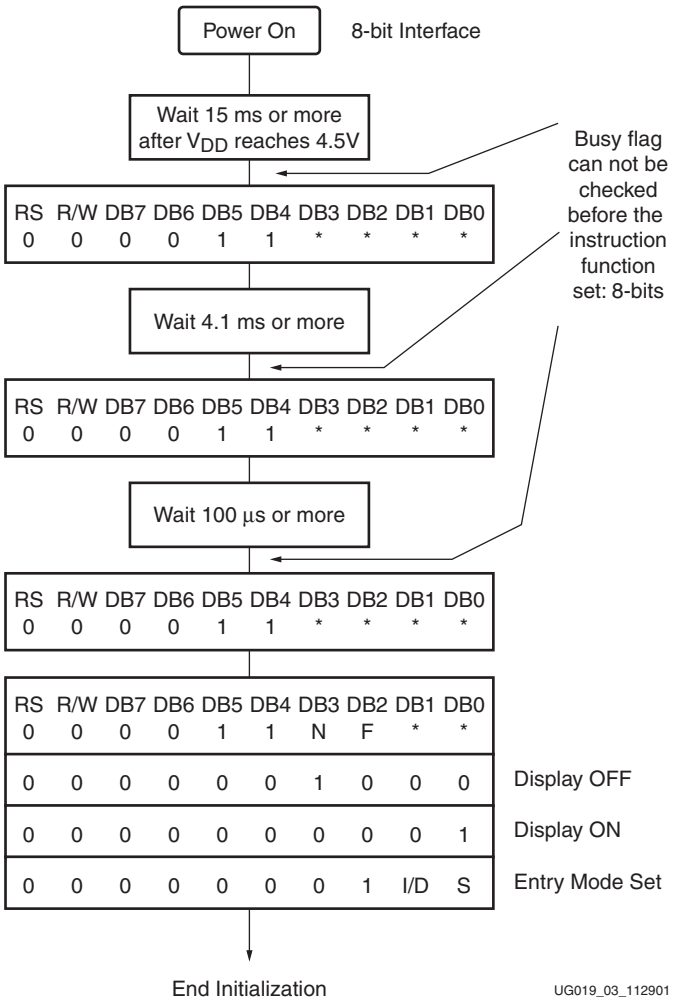

Figure 1-3: **Display Initialization Sequence**

LCD Panel Character Set

Higher 4 bit / Lower 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)												
xxxx0001	(2)												
xxxx0010	(3)												
xxxx0011	(4)												
xxxx0100	(5)												
xxxx0101	(6)												
xxxx0110	(7)												
xxxx0111	(8)												
xxxx1000	(1)												
xxxx1001	(2)												
xxxx1010	(3)												
xxxx1011	(4)												
xxxx1100	(5)												
xxxx1101	(6)												
xxxx1110	(7)												
xxxx1111	(8)												

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Figure 1-4: **LCD Panel Character Set**

Switches, LEDs, and Test Points

Switches

Four active Low push-button switches are located on the bottom side of the PCB. Figure 1-1 shows the PCB and Table 1-4 lists the switch locations.

Reset Switch

This switch functions, in most cases, as a reset switch for the FPGA logic or serial download cable. When using as reset switch, remember that it is an active Low push-button. This switch can also be used as a general-purpose switch.

Program Switch

This switch is connected to the PROGRAM pin of the FPGA. In cases where the ISP PROM has been programmed via the JTAG port, the FPGA can be reconfigured in Master Slave or Select Map mode with this switch.

Spare Jumpers

The board has two slide switch blocks; DipSwitch DIP 1, switch number 4, and DipSwitch DIP 2, all six switches are available for designers to use. The three remaining switches of DipSwitch DIP 1 are the FPGA's mode selection switches.Table 1-4 lists the locations for the jumpers.

Table 1-4: **Switch and Jumper Location**

Switch	Net Name	FPGA Pin
Reset	UIRES	AB10
Program	UIPRG	A2
Spare 1	UISPB1	AA10
Spare 2	UISPB2	AB9
Spare 3	UISPB3	V11
Spare 4	UISPB4	V9
Spare Jmp 1	UISPJ1	E11
Spare Jmp 2	UISPJ2	E10
Spare Jmp 3	UISPJ3	C10
Spare Jmp 4	UISPJ4	D10
Spare Jmp 5	UISPJ5	C9
Spare Jmp 6	UISPJ6	D9
Mode Switch 4	MODEX	A17

LEDs

Six surface mount LEDs of different colors are available for test purposes. They are located on the bottom side of the PCB (Figure 1-1). All of the LEDs are active High and can be used as general-purpose LEDs, although some of the LEDs also are connected to a test point. Table 1-5 lists the LED parameters.

Table 1-5: **LED Test Point Location**

LED	Net Name	Color	FPGA Pin	Test Point
LED 1	UILED1	Yellow	AA9	TP5
LED 2	UILED2	Yellow	W8	TP6
LED 3	UILED3	Green	Y7	
LED 4	UILED4	Red	W7	
LED 5	UILED5	Green	Y6	TP7
LED 6	UILED6	Red	W6	TP8

Test Points

Test points for instrumentation are available on the PCB. For the exact location of the test points, view the PCB overview in Figure 1-1. Table 1-6 lists the FPGA pin numbers connected to a test point.

Table 1-6: **Test Point Connections**

Test Point	FPGA Pin	LED	Net Name
TP0	V6	–	UI_TP8
TP1	V7	–	UI_TP9
TP2	V8	–	UI_TP10
TP3	V9	–	UI_TP11
TP4	V10	–	UI_TP12
TP5	AA9	LED6	UILED 1
TP6	W8	LED5	UILED 2
TP7	Y6	LED3	UILED 5
TP8	W6	LED4	UILED 6

Jumper Settings

Table 1-7 lists the jumper settings of the complete PCB.

Table 1-7: **Jumper Settings**

PCB Stubs	Name	Description
J1	EN PROGCON	Allows the PROGCON connector to be used as a JTAG input
J3	XILINX JTAG	Include the FPGA into the JTAG chain
J4	JTAG1 IN	JTAG input connector
J5	JTAG2 OUT	JTAG output connector
J8		Oscillator 1 enable
J9	AUTOLOAD	Use the PROM to program the FPGA
J10		Oscillator 2 enable

Table 1-7: **Jumper Settings *(Continued)***

PCB Stubs	Name	Description
J11	PROM JTAG	Include the PROM into the JTAG chain
J21		Differential oscillator enable
J24	EXTBRDJTAG	Put the PROGCON connector in the JTAG loop
J25	OSC1 Supply	Power supply selection for oscillator 1
J26	OSC2 Supply	Power supply selection for oscillator 2
J27	XPAND JTAG	Put JTAG2 OUT connector in the JTAG loop
J32	DOUTSER	Use DOUT or IO
J33	XTO5 SUPPLY	Power supply selection for differential oscillator
JMP1		Selection, solder, jumper on 1.5 V core power supply
JMP2		Selection, solder, jumper on auxiliary 3.3 V power supply
JMP3		Selection, solder, jumper on 3.3V I/O power supply
JMP4		Selection, solder, jumper on LVDS 3.3V power supply
JMP5		Selection, solder, jumper of 5V power supply
JMP6	TXP	Selection, solder, jumper on high-speed serial I/O output
JMP7	TXN	Selection, solder, jumper on high-speed serial I/O output
JMP8	RXP	Selection, solder, jumper on high-speed serial I/O input
JMP9	RXN	Selection, solder, jumper on high-speed serial I/O input
JMP10	CLK2	Oscillator selection, solder jumper
JMP11	LCKN	Differential oscillator selection, solder jumper.
JMP12	CLK1	Oscillator selection, solder jumper
JMP13	XAUX	2.5 V power supply selection jumper for TLK part
JMP14	LCKP	Differential oscillator selection, solder jumper.

Connector Settings

Table 1-8 lists the connector information of the complete PCB.

Table 1-8: **Connector Settings**

PCB Stubs	Name	Description
J2		5 V power jack connector input
J7		LCD connector, located under the LCD device
J12	PROGCON	Connector with JTAG and spare I/O connections
J22	XCONFIG	Connector for serial or SelectMap programming of the FPGA
J31	SPARECON	Connector with spare I/O pins of the FPGA

Table 1-8: **Connector Settings *(Continued)***

PCB Stubs	Name	Description
J20	TLK2501 JMP	Permanent settings for the TLK2501
J38	TLK SPARE	Spare I/O in the TLK banks on the FPGA
J29	TX SIDE	SAMTEC connector at the LVDS TX side of the FPGA
J30	RX SIDE	SAMTEC connector at the LVDS RX side of the FPGA
J36	RXCMON_P	Clock monitor at RX side of LVDS
J37	RXCMON_N	Clock monitor at RX side of LVDS
J23	TXCMON_P	Clock monitor at TX side of LVDS
J28	TXCMON_N	Clock monitor at TX side of LVDS
J34	TXDMON_P	Data monitor at TX side of LVDS
J35	TXDMON_N	Data monitor at TX side of LVDS
J6	EXT OSC 1	Input for external oscillator
J13	EXT OSC 2	Input for external oscillator
J15	EXT OSCP	Input for external differential oscillator
J14	EXT OSCN	Input for external differential oscillator
J18	RXP_EXT	Receiver side of SerDes
J19	RXN_EXT	Receiver side of SerDes
J16	TXP_EXT	Transmitter side of SerDes
J17	TXN_EXT	Transmitter side of SerDes

Configuration

The demonstration board has very flexible programming options. There are five different ways to program the Virtex-II FPGAs.

- Program the FPGA via slave-serial mode through the XCONFIG header with a MultiLINX or other cable.
- Use the SelectMap mode, with a MultiLINX cable, through the PROGCON connector.
- Use JTAG to program the FPGA, with MultiLINX or parallel download cable.
- Program the on-board PROM via JTAG and then let the FPGA configure itself via the SelectMap mode
- Program the on-board PROM via JTAG and then let the FPGA configure itself via the Serial Master mode.

These FPGA programming modes are set with the mode lines (M0, M1, M2) by means of jumpers as shown in Table 1-9.

Table 1-9: **Configuration Modes Supported on the LVDS Board**

Mode	M2	M1	M0	CCLK	Data Width	Serial DOUT
Master Serial	0	0	0	Out	1	yes
Slave Serial	1	1	1	In	1	yes
JTAG	1	0	1	N/A	1	no
Master SelectMap	0	1	1	Out	8	no
Slave SelectMap	1	1	0	In	8	no

An LED on the DONE pin adds a visual aid to detect a good FPGA configuration. If the LED is ON, the FPGA configuration is complete.

JTAG

The JTAG chain contains two on-board devices (FPGA and PROM). An external device can be included using two possible connections: the PROGCON connector and the JTAG2 OUT connector.

There is a JTAG input (JTAG1 IN) and a JTAG output (JTAG2 OUT) connector. The JTAG input connector is the start of the JTAG chain. The JTAG output can be used to connect the on-board JTAG chain to other board JTAG chains, as either a second demonstration board or a daughter card. Each chip can be isolated from the complete JTAG chain by the use of jumpers that are located close to each device in the chain. Figure 1-5 shows how to build a JTAG chain.

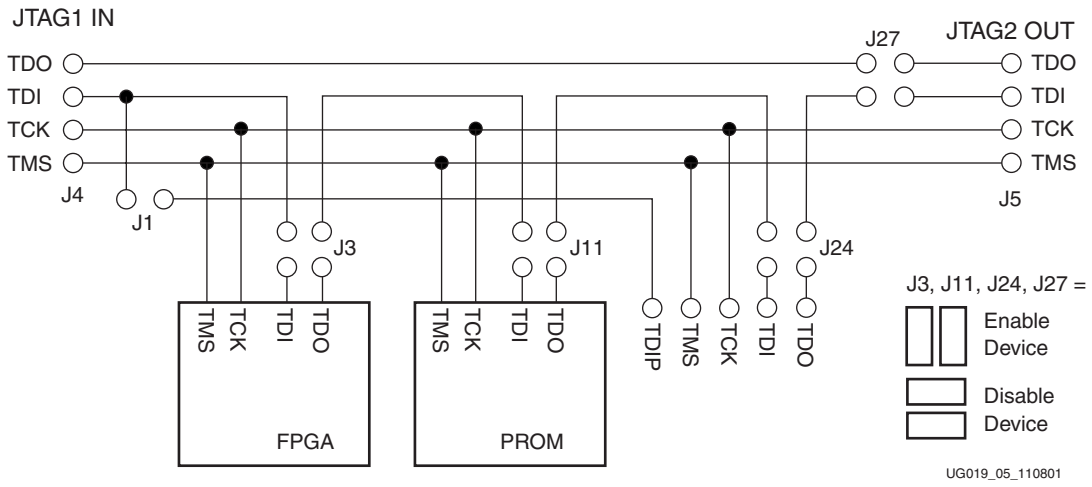

Figure 1-5: **JTAG Chain**

A JTAG connection is integrated in the PROGCON connector. This makes it easy for adding daughter cards into the JTAG chain, programming on daughter card devices using JTAG, or having the daughter board program the FPGA on the motherboard using JTAG.

Figure 1-6 shows the JTAG input and output connector.

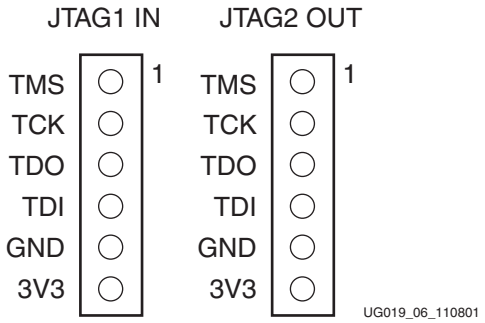

Figure 1-6: **JTAG I/O Connector**

PROM

The LVDS demonstration board uses is a XC18V04VQ44C PROM. As an ISP Flash memory, it is programmable and reprogrammable through the JTAG chain. The PROM can program the FPGA in either serial or parallel mode.

SelectMap

A Virtex-II FPGA is programmable in parallel mode, also called SelectMap mode. In this mode, two possibilities of programming exist:

- Master mode: The FPGA delivers the CCLK download clock.
- Slave mode: The FPGA must receive the CCLK clock from an external device.

The demoboard can use both modes via pins of the PROGCON connector. Slave mode can be used to program the FPGA on the demoboard from a MultiLINX cable, while Master mode can be used when a daughter card is plugged into the PROGCON connector.

The connector (PROGCON), used for SelectMap programming, also carries the upper bits of the spare I/O of the SPARECON connector. Together, this becomes a 36-bit bus. Both connectors are lined up and can carry a daughter card or flat cables. When SelectMap is not used, the SelectMap pins can also be used as normal I/O and the available bus can be extended. Figure 1-7 shows the layout of the SelectMap part of the connector (PROGCON).

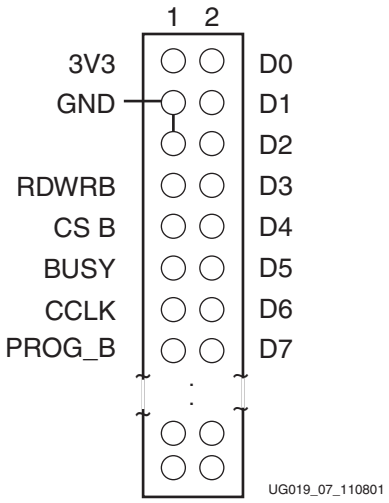

Figure 1-7: **PROGCON Connector**

Place a jumper on the D_{OUT}/Busy line. For a parallel download, the jumper must be set in position A; for a serial download, the jumper must be set in position B. If the jumper is set in position B, then D_{OUT} is taken to the Virtex configuration jumpers and can be monitored. Jumper and connector locations are outlined in Table 1-7.

Serial

Serial programming of the FPGA can be done using a Serial download cable (MultiLINX or another serial cable) or by using an ISP Flash PROM (e.g., XC18V04VQ44C). It is very important to set the D_{OUT} jumper to position B to monitor the signal on D_{OUT}. Figure 1-8 shows the connections used for programming the FPGA with a serial cable.

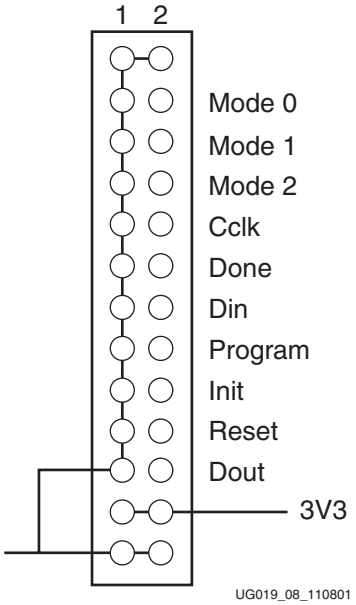

Figure 1-8: **XCONFIG Jumpers**

Spare Connectors

There are two spare I/O connectors located on the right edge side of the PCB, SPARECON and PROGCON. A few uses for these spare connectors are for flat cable connection or daughter card connection.

The second spare connector, PROGCON, has built-in signals for the SelectMap bus and JTAG bus. Daughter cards can be designed for JTAG or SelectMap configuration.

Figure 1-9 shows the spare I/O connectors with FPGA pin connections. Figure 1-10 shows the second spare connector.

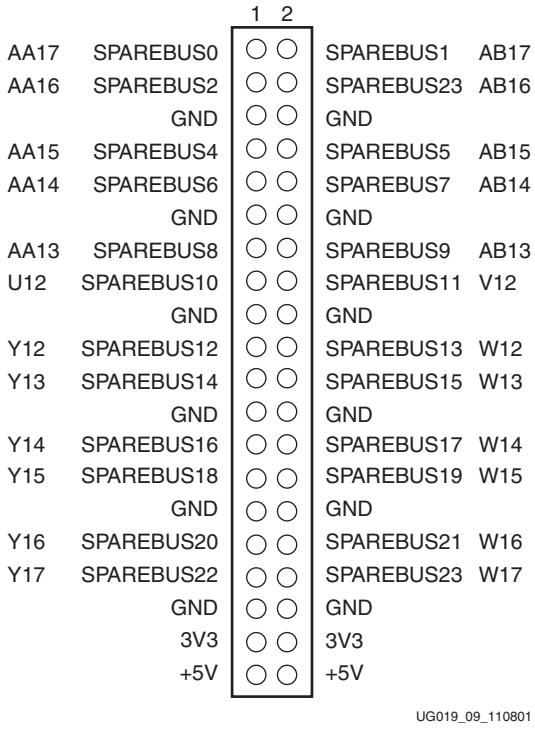

Figure 1-9: **SPARECON Connector**

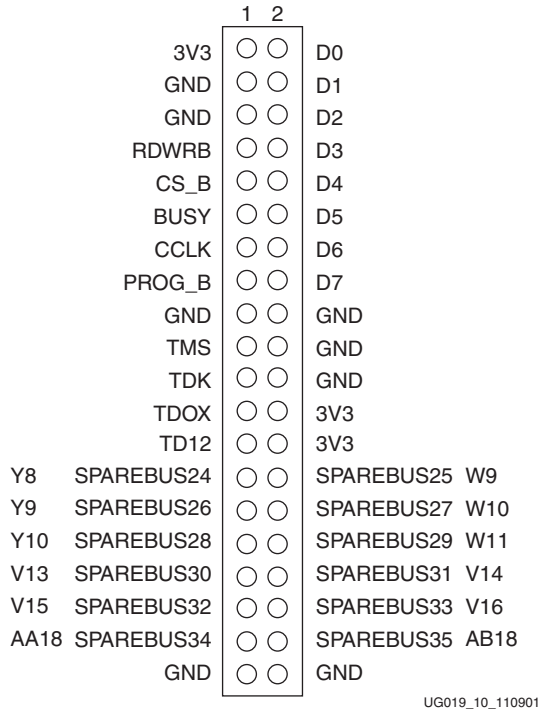

Figure 1-10: **PROGCON Connectors**

Oscillators

The demonstration board has three oscillators and a VCO.

- 156.26 MHz oscillator used for the LVDS design in the FPGA.
- 125 MHz oscillator used by the FPGA as transmitter clock for the TLK SerDes device
- 410 MHz differential oscillator is also used for the LVDS design in the FPGA.

All oscillators can be disabled. An external oscillator can be applied to the on-board SMB plugs. To apply an external clock waveform:

- Disable the oscillator by replacing the jumper.
- Fill the solder jumper in order to connect the external oscillator device to the clock line. The exact location of these jumpers is shown on the PCB overview schematic in Figures 1-1.
- Connect a signal wire to the SMB connector.

Various oscillator foot prints are designed on the board, along with the different oscillator power supplies.

More information on the demonstration board oscillators is available in Chapter 3. Figure 1-11 shows the oscillators.

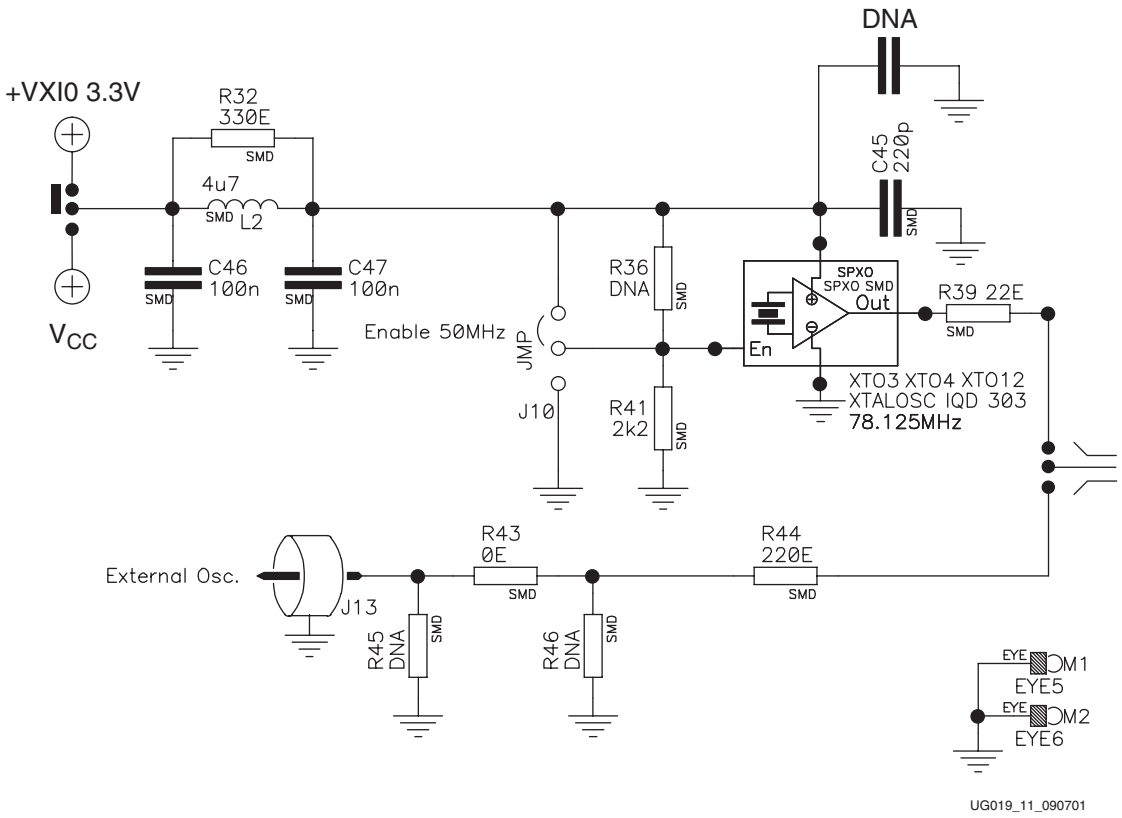

Figure 1-11: **Oscillator**

LVDS Interface

The LVDS interface on this demonstration board is a popular low-voltage differential signaling interface used for high-speed back panel and other interconnections. Figure 1-12 outlines the setup for the demonstration board, which contains two 16-bit data, one clock and one synchronous LVDS buses. Pin location information for both LVDS buses is given in the **Pin Locking .ucf File** section of this document.

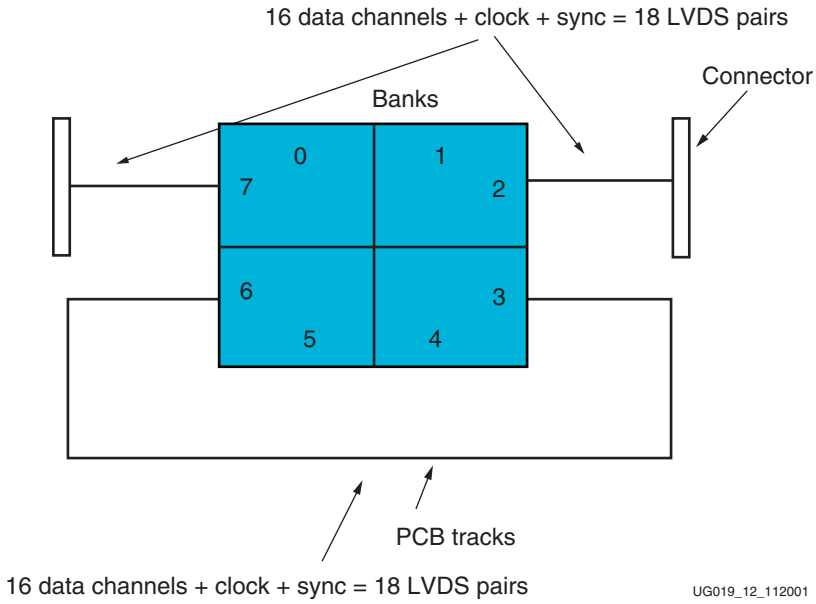

Figure 1-12: **LVDS Interface Setup**

Bus 1

Bus 1, a 16-bit bus, is routed to and from connectors placed on the board. Its purpose is to run LVDS signals over a longer distance using cable connections. FPGA I/O banks 2 and 7 are used for this purpose. When the connectors are mounted, the probing of the LVDS bus, can be done when soldering wires or putting probes to/on the solder islands of the non-mounted resistors close to the connectors. FPGA I/O Bank 2 is the transmission side of this bus, while FPGA I/O bank 7 is the receive side. SAMTEC QSE-type connectors are used on the board. The cable is custom made by Precision-Interconnect and is built using SAMTEC QTE connectors and 50 Ω AWG36 coax flat cable. QSE and QTE connectors are specially designed for high-speed differential signal routing. Figure 1-13 and Table 1-10 show the connector and cable details.

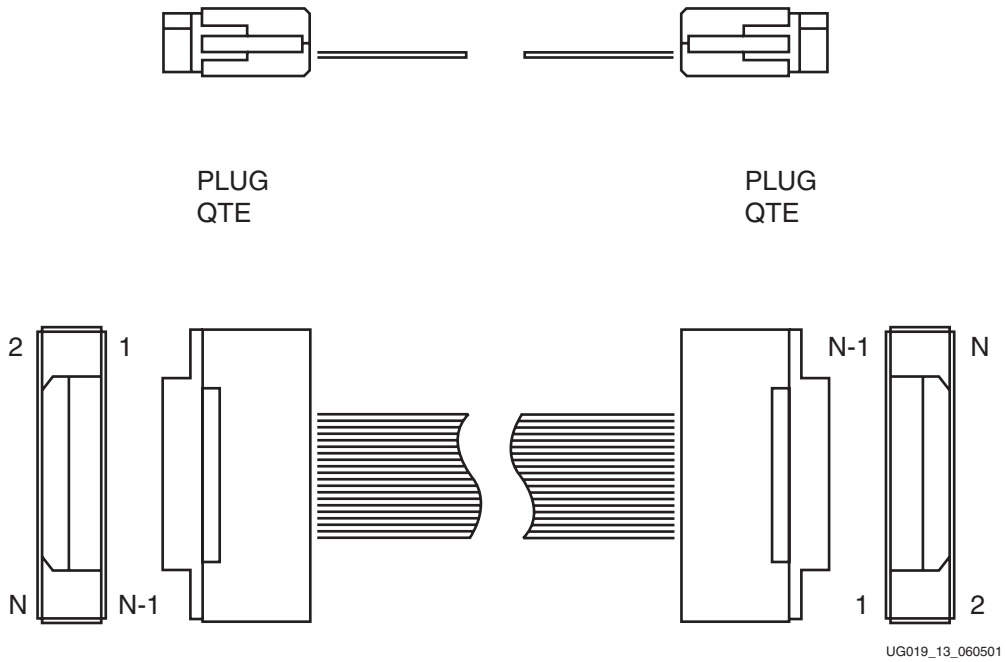

Figure 1-13: **Cable**

Table 1-10: **Cable Details**

Side 1	Side 2
1	N
2	N – 1
N – 1	2
N	1

- Board Connector: SAMTEC QSE-040—1-L-D-A
  Specifications are available at:
  http://www.samtec.com
  http://www.samtec.com/suddenspecs/techspec.asp?series=QSE
- Technical specifications can be found at:
  http://www.samtec.com/suddenspecs/techspec_test.asp?series=QSE
- Cable assembly: Precision Interconnect 023850080030JL20

More information about the characteristics of this cable are available in Chapter 6.

Bus 2

LVDS Bus 2 is laid-out entirely on the demonstration PCB. FPGA I/O bank 3 is the transmission side of this LVDS bus, while FPGA I/O bank 6 is the receive side. Bus 2 starts in bank 3 as a 16-bit, one clock, one SYNC signal and arrives in bank 6 as a 16-bit, one-clock, one SYNC signal bus.

High Speed Serial Interface

The TLK2501 is a member of the transceiver family of gigabit transceivers used in high-speed bi-directional point-to-point data transmission systems. There are three family members:

- The TLK2501 has an effective serial interface speed of 1.6 to 2.5 Gb/s. The TLK2501 is pin-for-pin compatible with the TLK2500.
- The TLK1501 has an effective serial interface speed of 0.6 to 1.6 Gb/s. It is both pin-for-pin compatible with and functionally identical.
- The TLK3101 has an effective serial interface speed of 2.5 to 3.125 Gb/s.

This approach provides a wide range of performance solutions with no board layout changes required. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable.

This device can also replace parallel data transmission architectures, as in traditional back planes, by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals.

Parallel data loaded into the transmitter is delivered to the receiver over a serial channel. It is then reconstructed into its original parallel format. Significant power reduction and cost savings are offered, as well as scalability for future (higher) data rates.

The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (GTX_CLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8B/10B) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTX_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the extracted reference clock (RX_CLK). It then decodes the 20-bit wide data using the 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data terminals (RXD0-15). The outcome is an effective data payload of 1.28 Gb/s to 2.0 Gb/s (16-bit data times the GTX_CLK frequency).

- The TLK2501 is housed in a high performance, thermally enhanced, 64-pin VQFP PowerPAD package. Solder the TLK2501 PowerPAD to the thermal land on the board.
- The TLK2501 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, allowing the protocol device a functional self-check of the physical interface.
- The TLK2501 is designed to be hot-plug capable. An on-chip power-on reset circuit holds the RX_CLK Low and forces DOUTTXP, DOUTTXN, and the parallel side output signal terminals into a high impedance state during power up.
- The TLK2501 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock.
- The TLK2501 allows users to implement redundant ports by connecting receive data bus terminals from two TLK2501 devices together. Deasserting the LCKREFN Low causes the receive data bus terminals, RXD[0:15], RX_CLK, and RX_ER, RX_DV/LOS to go into a high-impedance state. This places the device in a transmit-only mode since the receiver is not tracking the data.
- The TLK2501 uses a 2.5V supply. The I/O section is 3V compatible. With the 2.5V supply, the chipset is very power-efficient, consuming less than 360 mW typical.

The PowerPAD™ package is a trademark of Texas Instruments.

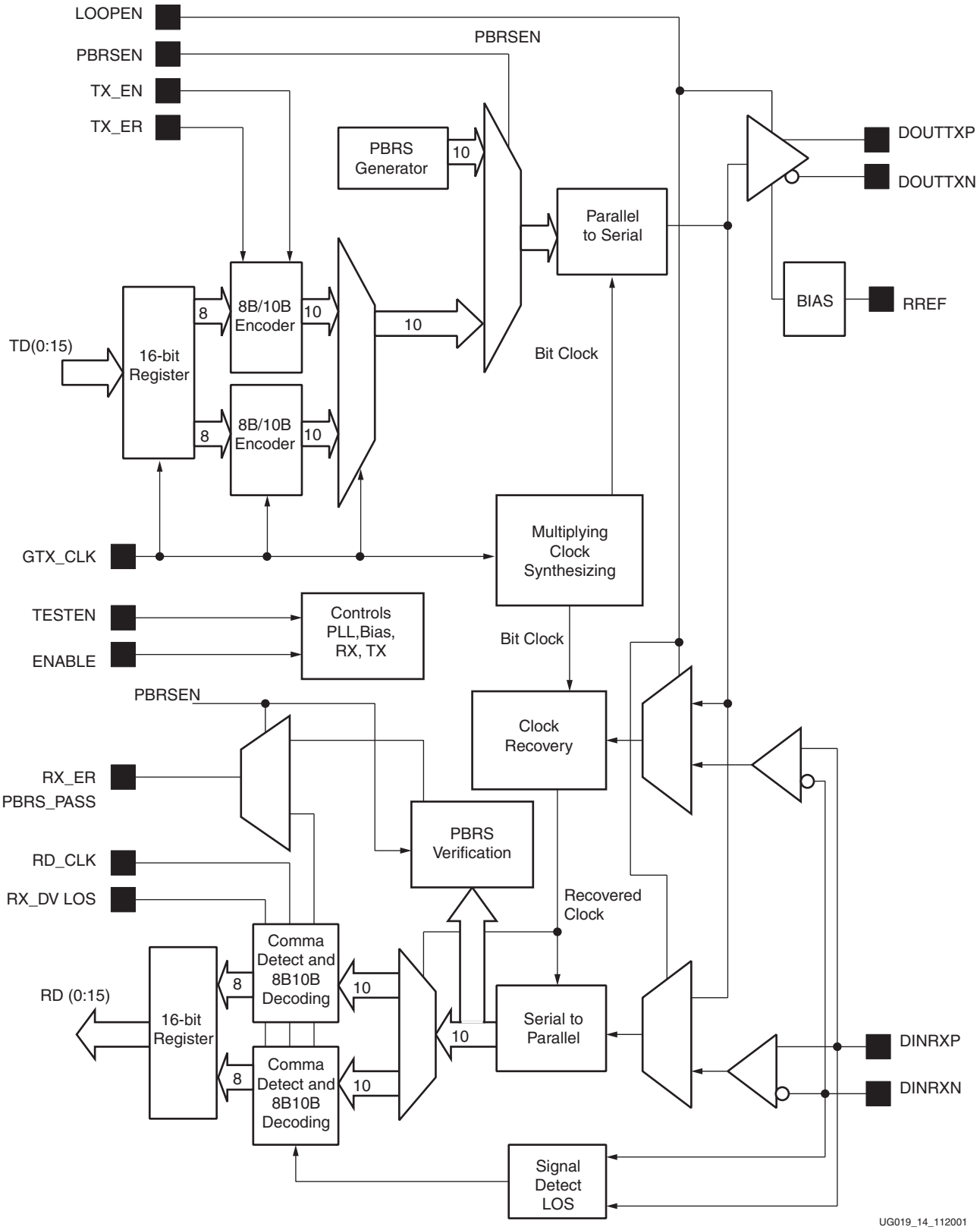

Figure 1-14: **TLK2501 Block Diagram**

FPGA to TLK2501 Connections

To demonstrate the capabilities of both devices, the FPGA is connected to the TLK device. The high-speed data connections require precautions during layout of the demonstration board. Appendix A has more information on TLK2501 functionality and discusses the layout precautions. The following are connections between the FPGA and the TLK2501 device:

- 16-bit transmit bus from normal LVTTL I/O (2.5V) of the FPGA
- 16-bit receive bus to normal LVTTL I/O (2.5V) of the FPGA
- Recovered clocks are connected to the dedicated clock inputs of the FPGA.
- The reference clock (GTX_CLK) is coming from an oscillator (OSC2 of 125 MHz.)
- Status signal TX_EN and TX_ER are coming from the FPGA to the transmitter sections of the Serdes device..
- PBRS_PASS and RX_DV are routed to normal FPGA I/O.
- Jumpers on "TLK SPARE HEADER" to signals LCKREFN, ENABLE, PRBSN, and LOOPEN can be connected to normal FPGA I/O or these signals are connected to a header "TLK JMP SETTINGS" and become static signals.
- Serial connections of the TLK2501 device are routed to an Agilent optical transceiver or to coax SMB connectors using PCB "to-solder" traces.

TLK2501 Jumper Setting

The jumpers are used to set some default settings for the SerDes device (Figure 1-15). These settings can also be dynamically controlled using the FPGA. Then the jumper bank "TLK JMP SETTINGS" must be left unconnected and jumpers must be placed om jumper bank "TLK SPARE HEADER". Chapter 5 defines the TLK2501 pins.

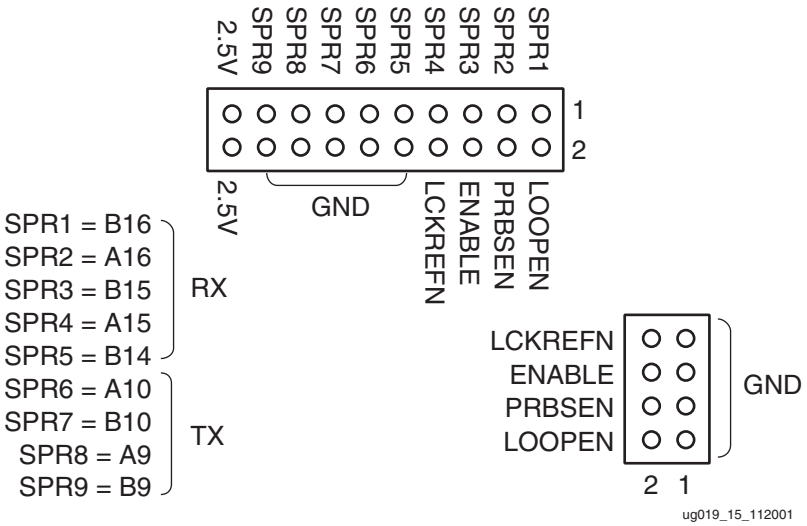

Figure 1-15: **TLK2501**

The SerDes device can be connected to the external world via a coax or optical interface. Selection of the media used is made with solder jumpers JMP6 to JMP9. These jumpers are located between the TLK2501 and the Agilent optical transceiver. A small solder connection is used to connect to the appropriate physical interface. Exact location of the solder jumpers are shown on Figure 1-1, page 6 and Figure 1-16.

Selection of Physical Interface

There are two physical interfaces on the board, an optical interface and a cable interface. The optical interface is an Agilent laser transceiver. The cable interface uses a coax connection.

The interface is selected on the PCB using solder jumps. Select one of the interfaces and place a solder jump on the correct pads. The jumpers are located between the Agilent transceiver and the TLK2501 device, as shown in Figure 1-16.

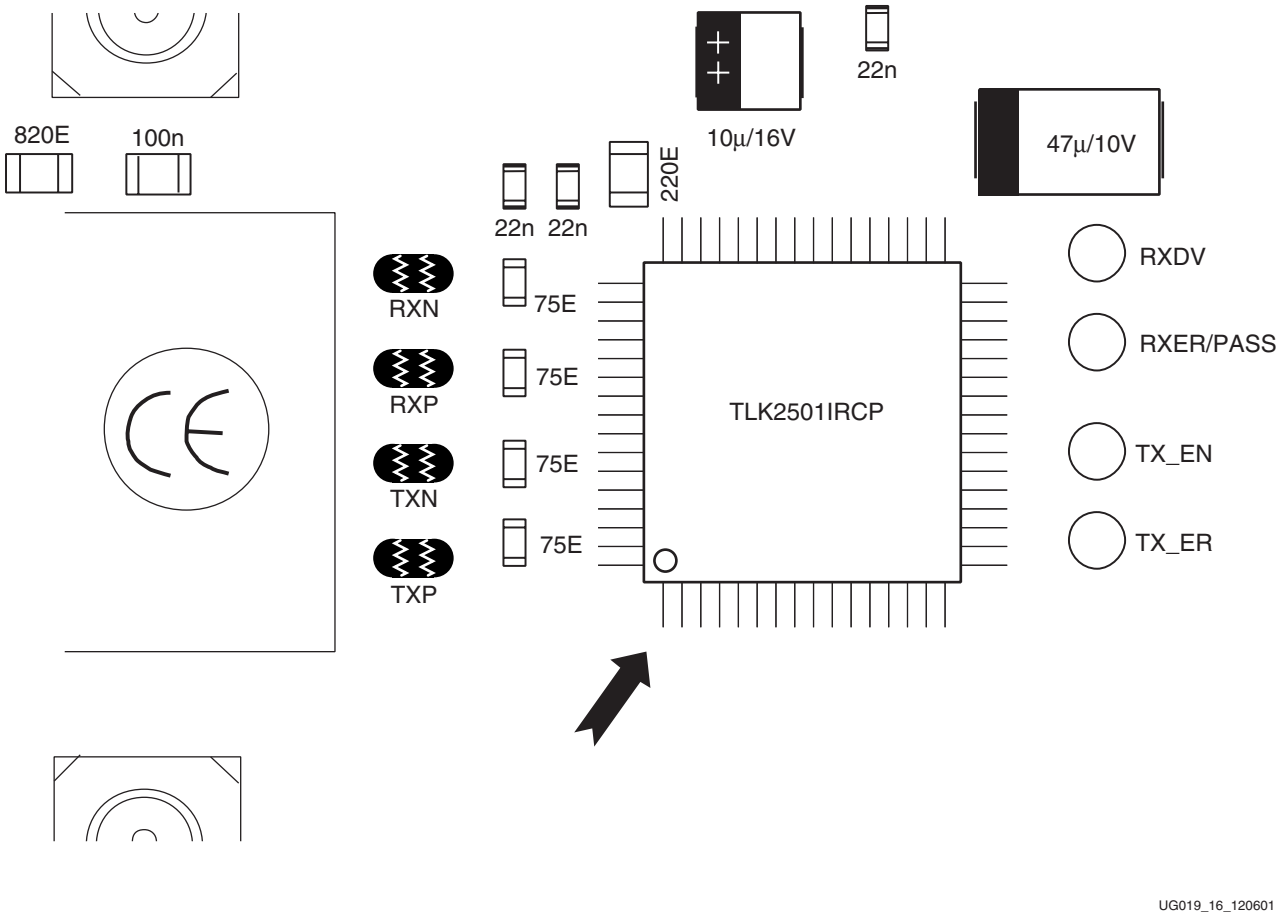

Figure 1-16: **Physical Jumpers**

The cables can be ordered through Pasternack Enterprises (http:/www.pasternack.com).

- Optical cable example order number:

  MTRJ to MTRJ (multimode): PE300028-L (L= length 1, 2, 3, or 5 meters)

- Coax cables example order number:

SMB right angle to SMB right angle: PE3656-L (L= length in inches)

A 50 W, low loss, teflon COAX capable of handling +2 GHz RF signal should be used. The connector material be similarly specified.

Agilent HFBR5910E/HFBR5912E

The Agilent HFBR-5910E/5912E transceiver allows a designer to implement a range of solutions or multimode and single mode Fibre Channel applications. The transceivers are

configured in the new multi-sourced industry standard 2 x 5 dual-in-line package with an integral MT-RJ fiber connector.

Transmitter Section

The transmitter section of the HFBR-5910E consists of an 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) in an optical subassembly (OSA), which mates to the fiber cable. The OSA is driven by a custom silicon bipolar IC, which accepts differential PECL logic signals (ECL referenced to a +3.3 V supply) and provides bias and modulation control for the laser.

Receiver Section

The receiver section of the HFBR-5910E includes a GaAs PIN photo diode mounted together with a custom, silicon bipolar transimpedance preamplifier IC in an OSA. This OSA is mated to a custom silicon bipolar circuit that provides post-amplification and quantization. The post-amplifier also includes a Signal Detect circuit that provides a TTL logic-high output upon detection of an optical signal.

Package Footprint

The Agilent transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multi-source announcement which defined the 2 x 5 package style. This drawing is reproduced in Figure 1-17 with the addition of ANSI Y14.5M-compliant dimensioning to be used as a guide in the mechanical layout of the circuit board.

Transmit Enable

Toggling the transmit disable allows an attempted turn-on of the transmitter. If fault occurs, the transmitter stays disabled. The HFCT-5910E utilizes an optical subassembly consisting of a short piece of single mode fiber along with a current limiting circuit to guarantee eye safety. It is intrinsically eye safe and does not require shutdown circuitry.

Signal Detect

The Signal Detect circuit provides a TTL low output signal when the optical link is broken or when the transmitter is off. The Signal Detect threshold is set to transition from a high to low state between the minimum receiver input optional power and –30 dBm average input optical power indicating a definite optical fault (e.g. unplugged connector for the receiver or transmitter, broken fiber, or failed far-end transmitter or data source). A Signal Detect indicating a working link is functional when receiving characters. The Signal Detect does not detect receiver data error or error-rate.

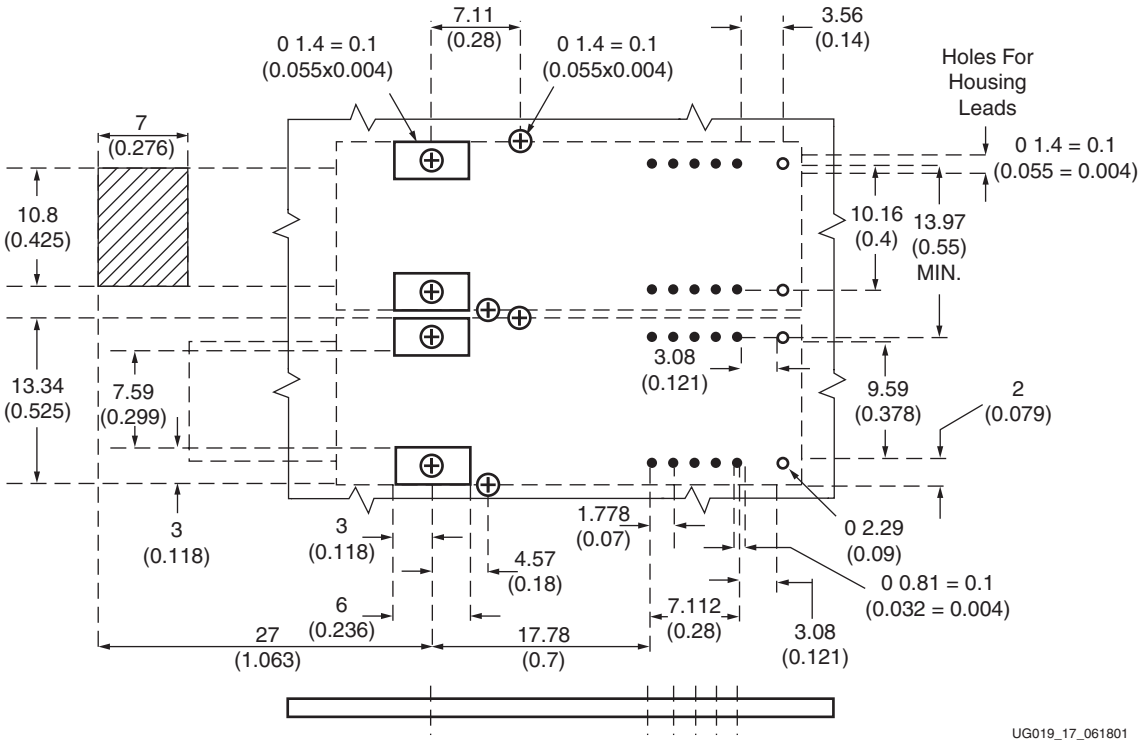

Figure 1-17: **Agilent Transceiver Mechanics**

Eye Safety

These laser-based transceivers are classified as AEL Class I (U.S. 21 CFR(J) and AEL Class 1 per EN 60825-1 (+A11). They are eye safe when used within the data sheet limits per the Center for Devices and Radiological Health (CDRH). They are also eye safe under normal operating conditions and under all reasonably foreseeable single-fault conditions per EN60825-1. Agilent has tested the transceiver design for compliance with the requirements listed below under normal operating conditions and under single-fault conditions where applicable. TUV Rheinland has granted certification to these transceivers for laser eye safety and use in EN 60950 and EN 60825-2 applications. Their performance enables the transceivers to be used without concern for eye safety up to 5.0 V transmitter V_{CC}.

Coax

This is a simple interface with SMB coax connectors for the transmit and receive sides

Pin Locking .ucf File

A .zip file available at: http://www.xilinx.com/bvdocs/userguides/ug019.zip contains a complete .ucf file, which is provided as an Adobe Acrobat (.pdf) document.

In Acrobat reader, select the Select Text Button  and highlight the complete .ucf file syntax. Push [CTRL] "C" and then perform a paste function in the text editor used for making the .ucf file.

LVDS Banking/Pinning

The following figures provide an overview of the pins per bank using an XC2V1000-FG456 as an example. For more details, refer to the Virtex-II data sheet at:

http://direct.xilinx.com/bvdocs/publications/ds031.pdf

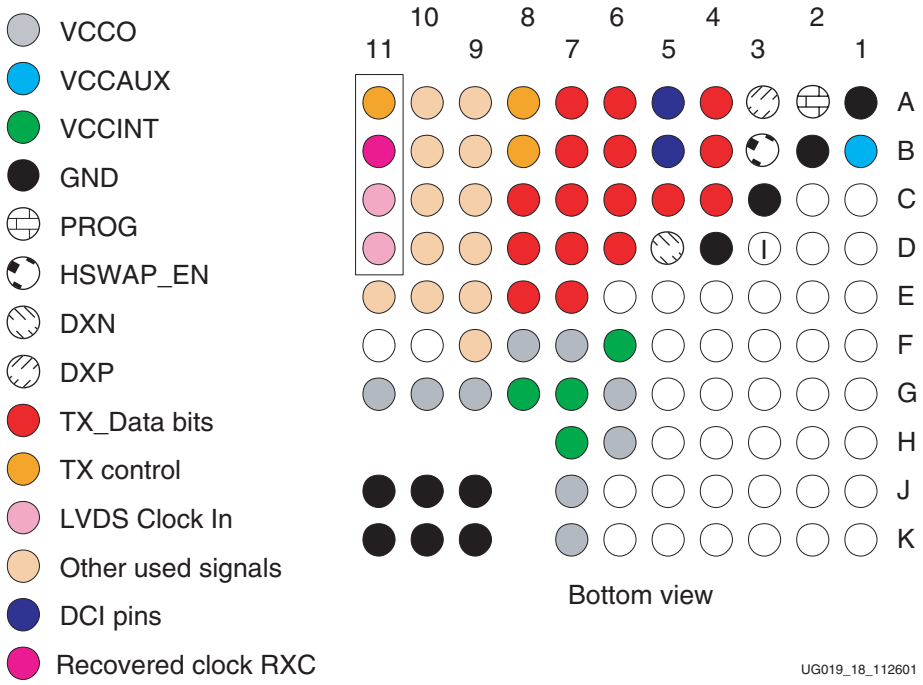

Figure 1-18: **Bank 0 - TLK2501 TX Bus**

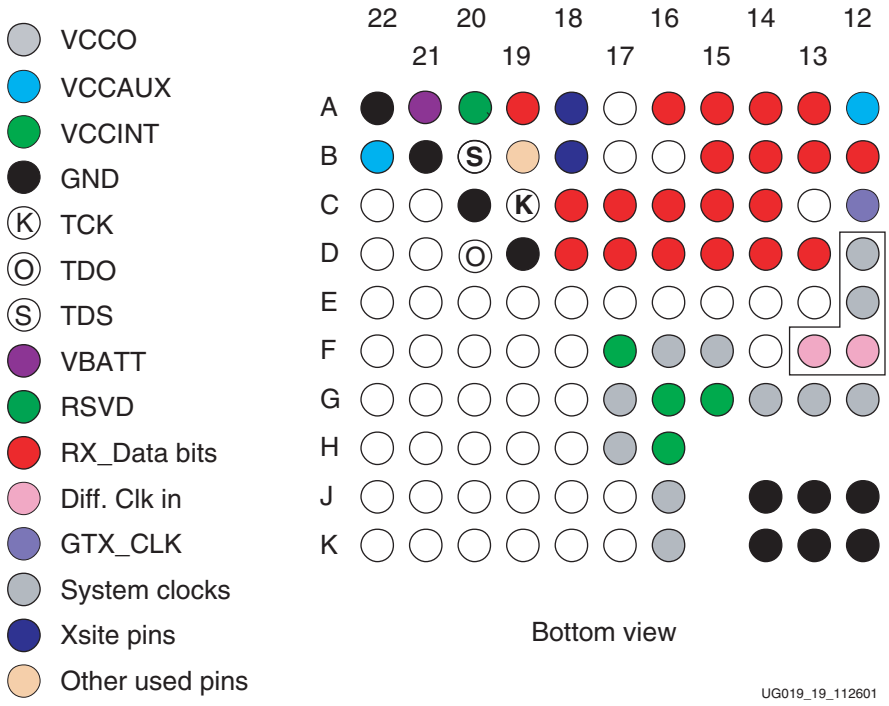

Figure 1-19: **Bank 1 - TLK2501 RX Bus**

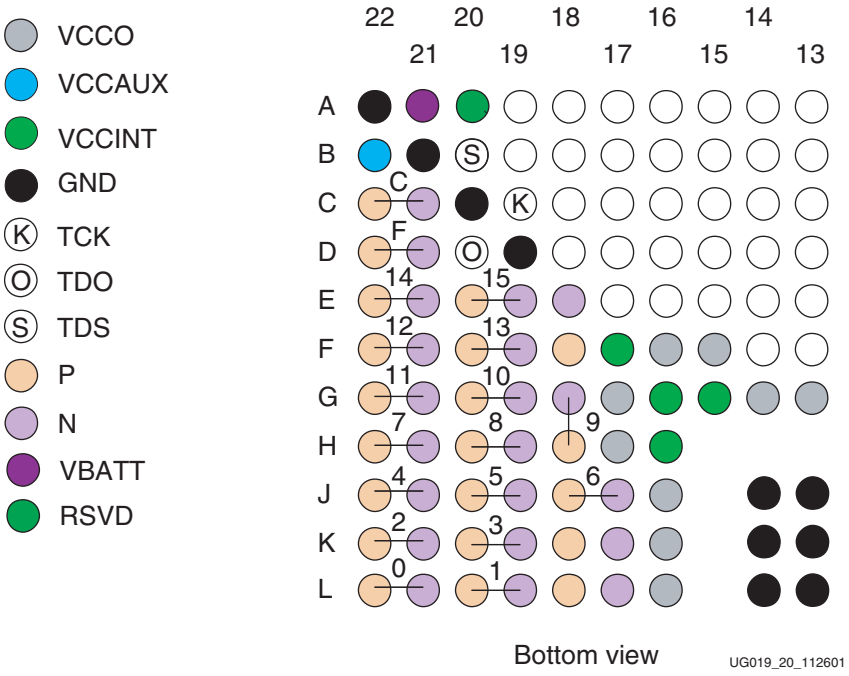

Figure 1-20: **Bank 2 - LVDS Connector**

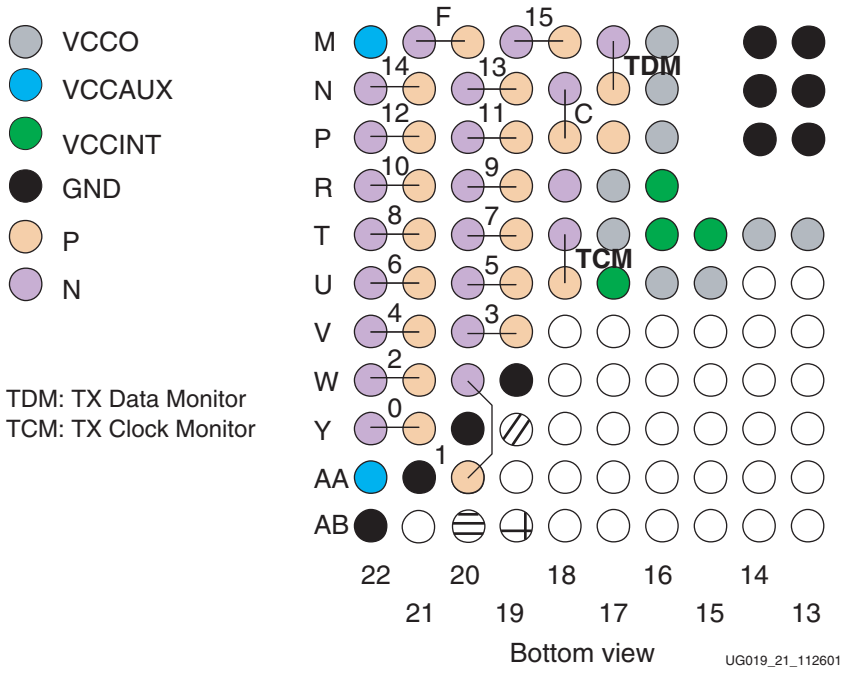

Figure 1-21: **Bank 3 - LVDS Backplane**

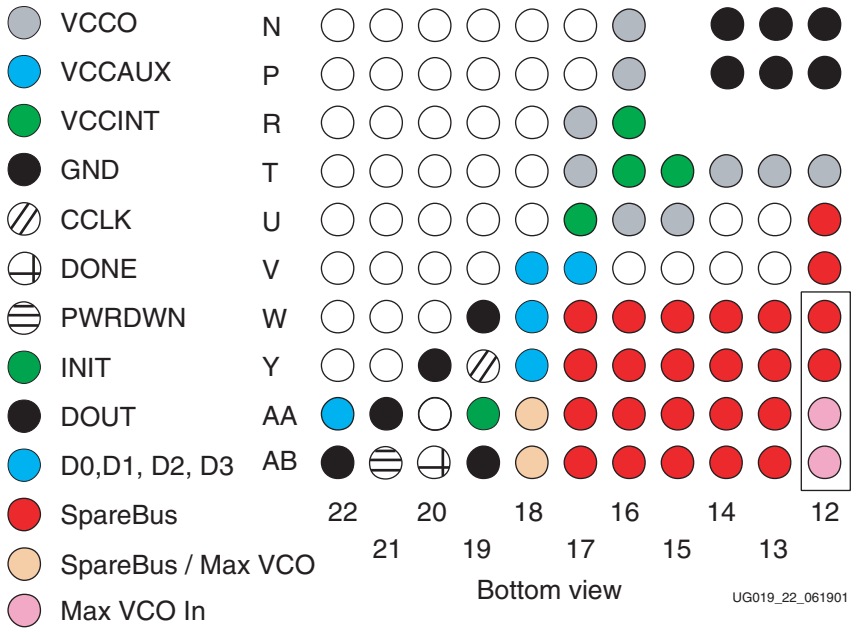

Figure 1-22: **Bank 4 - SpareCon**

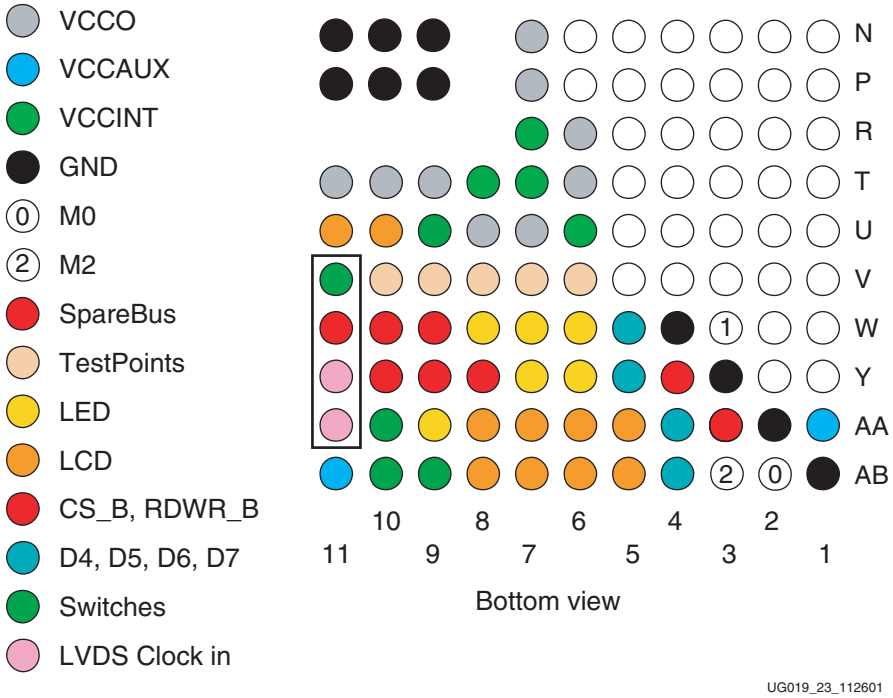

Figure 1-23: **Bank 5 - UI_BUS**

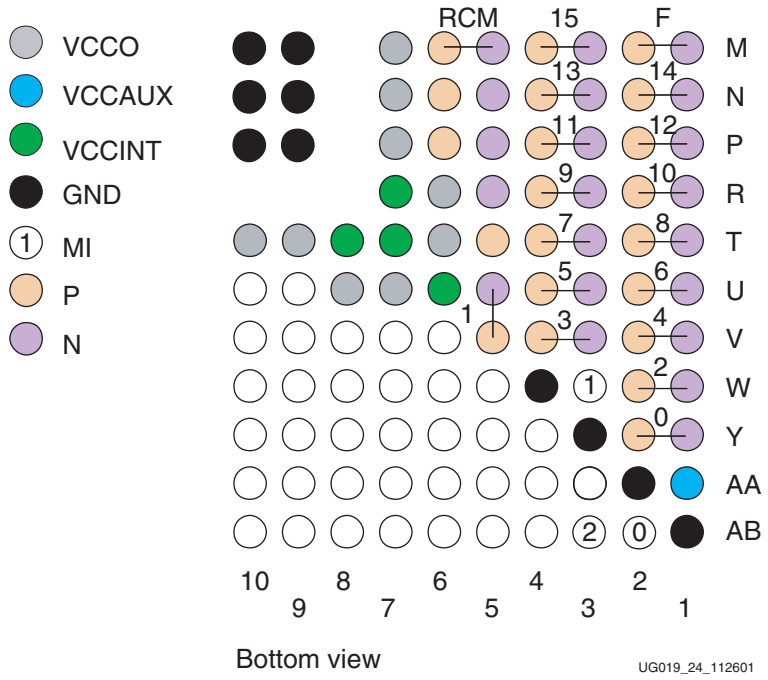

Figure 1-24: **Bank 6 - LVDS Backplane**

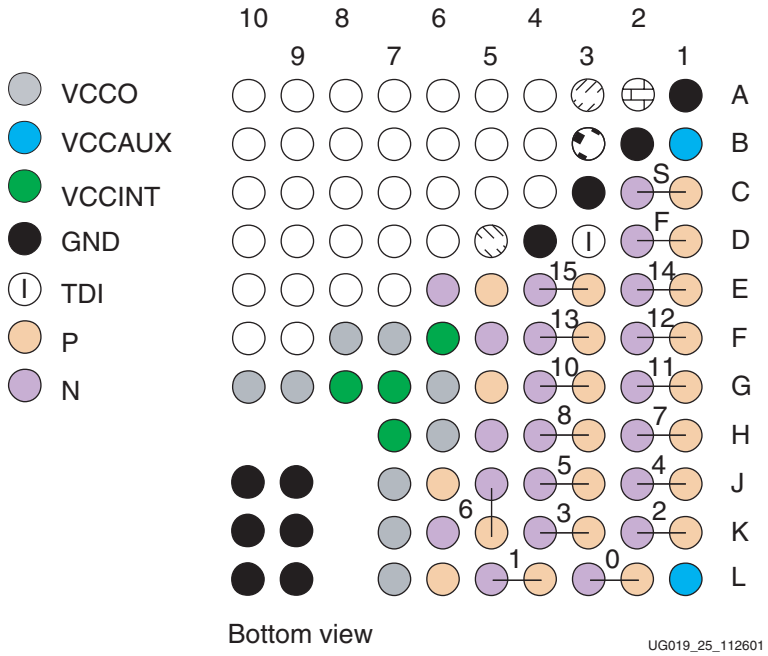

Figure 1-25: **LVDS Connector**

Schematics, Layouts, and Bill of Materials

A .zip file available at: http://www.xilinx.com/bvdocs/userguides/ug019.zip contains the following schematic files, example layouts, and a Bill of Materials (BOM) for the LVDS demonstration board:

- Component localization scheme (silk screen) for both sides of the PCB
- Board Power Supply
- FPGA and PROM programming and clock circuitery
- TI SerDes and Laser Circuitry
- LVDS data loop
- LVDS data Loop to SAMTEC Connectors
- User I/O and spare signals

Chapter 2

Power Supply

Power Supply

Input Section

- The input voltage for the board is 5V ± 10 %. The input connection is from either banana plugs or from a jack.
- The input section has all the elements to protect the board from
  - a short circuit (FUSE 1)
  - a noisey supply (R3, FIL1, C6, and C7)
- HF filter to keep supply noise from the board.
  - Power supply inversion (D3)
- Dual high-speed Schottky diodes.
- Test clips and a LED indication are designed as control elements of the input section of the power supply.

Back sections

- There are six different power supplies on the board, every component has a specific power supply.
- When needed, these supply voltages are adjustable.
- This makes it also possible, in the lab, to measure and test the behavior of the component under different supply voltage conditions.
- The component used to make the appropriate voltages is the popular LM1117TX-adj.
- Each supply can be disconnected from the board through a solder jumper. An LED shows the status of the power supply.

Table 2-1 shows the power supply connections.

Table 2-1: **Power Supply**

VX_{ICORE}	1.5 V	JMP21	Adjustable	1.35 V ... 1.65 V	LED 4
VX_{AUX}	3.3 V	JMP 2	Adjustable	3.0 V ... 3.6 V	LED 5
VX_{IO}	3.3 V	JMP 3	Fixed		LED 6
VX_{LVDS}	3.3 V	JMP 4	Adjustable	3.0 V .. 3.6 V	LED 7
V_{CC}	5 V	JMP 5	Fixed		LED 2
Vlaser	3.3 V		Fixed		
VT_{Icore}	2.5 V	JMP 13	Fixed		LED 14

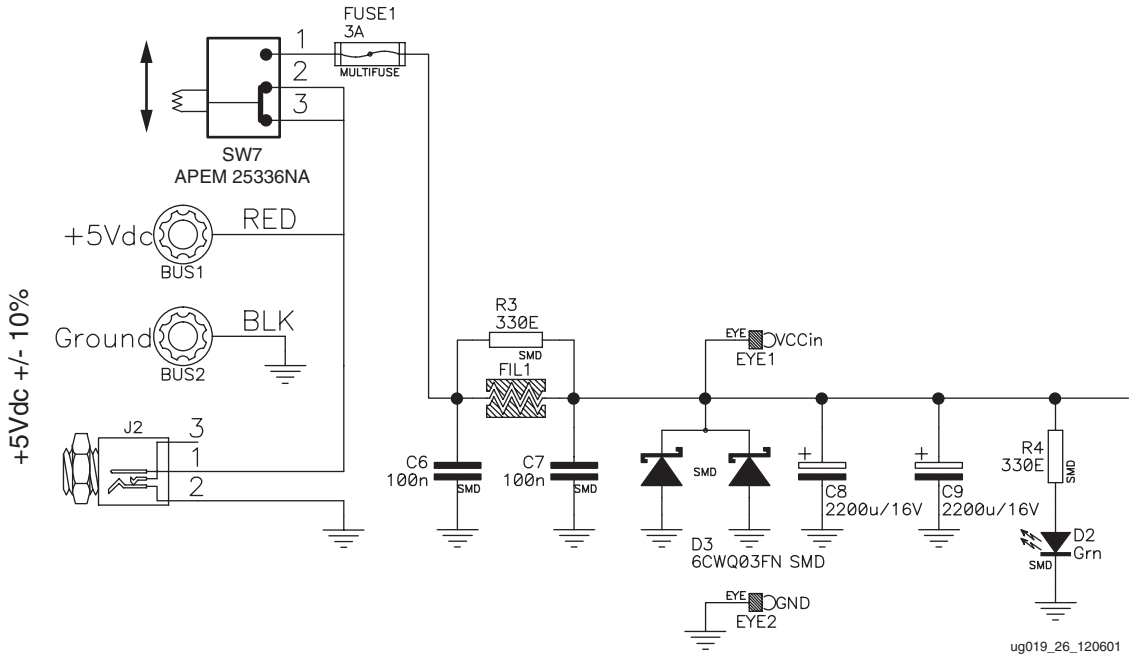

Figure 2-1: **Power Supply In**

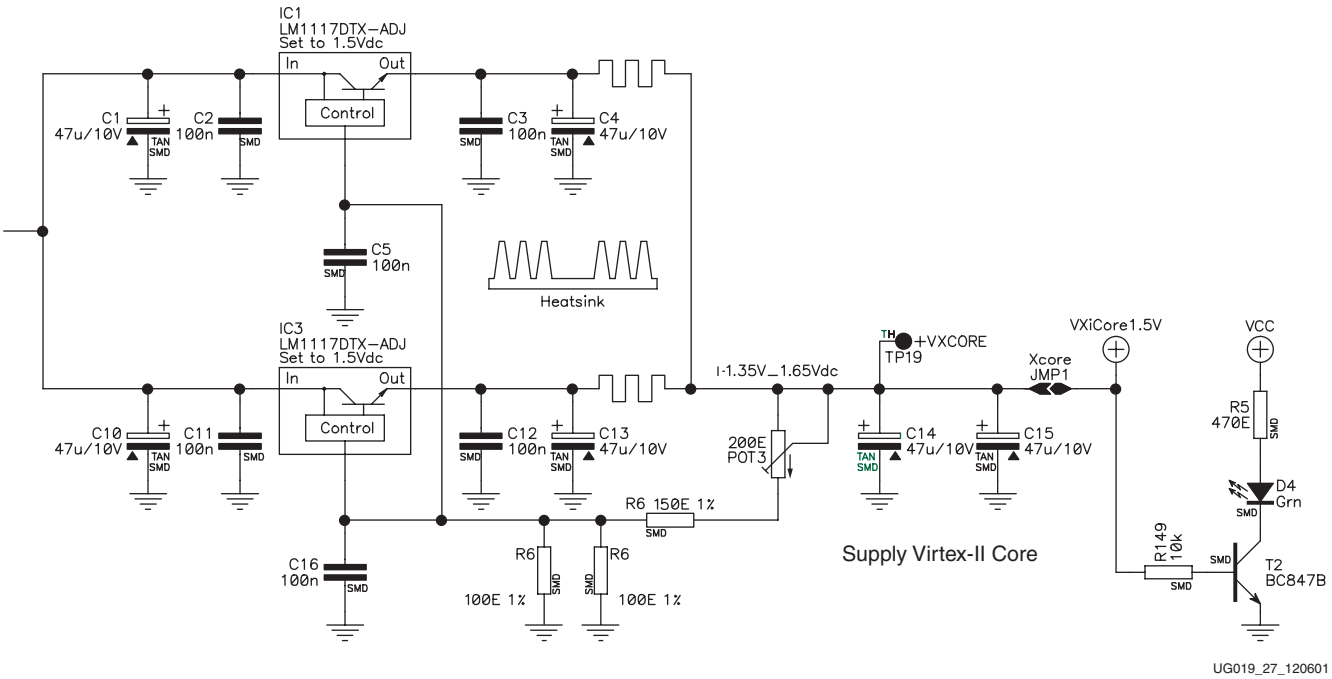

Figure 2-2: **Power Supply 1.5**

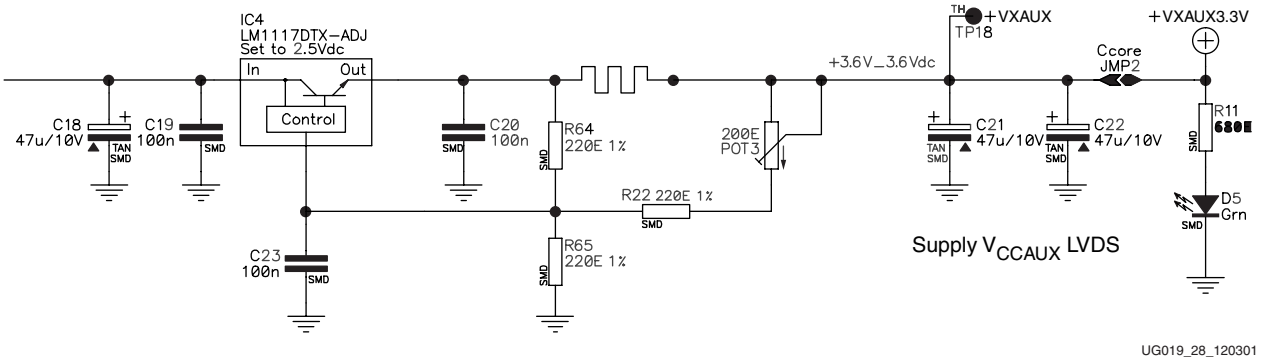

Figure 2-3: **Power Supply Other**

Voltage Regulator

The LM1117TX-Adj is the voltage regulator for all voltages on the LVDS demonstration board. This device can deliver 800 mA. To double the output current for the core voltage, two of these voltage regulators are placed in parallel.

a. Two very small 0.1 Ω resistors levels out the possible differences in the regulator outputs, which allows use of the same feedback path for both regulators.

b. All voltage regulators, except those for VT_RX and VT_TX of the SerDes, are on a heatsink.

c. For all voltages, a trace jumper is available to allow disconnecting one of the voltages. Disconnecting a power supply means cutting a trace on the board.

d. An LED display shows the voltage level.

Chapter 3

Oscillators

Components

There are three oscillators on the demonstration board.

Two single ended oscillators:

- 156.25 MHz; General purpose oscillator.
- 125 MHz; Oscillator for the TLK2501

One differential oscillator

- 420 MHz; used for LVDS.

For each oscillator, With the exception of the differential oscillator, there is room for 14-pin DIL, 8-pin DIL, or SMD oscillators. This allows customization with self-selected oscillators.

The board comes with pre-installed oscillators.

- 156.25 MHz; 5 V, DIL package, VITE
- 125 MHz; 3.3 V, SMD package, VITE
- 420 MHz; 3.3 V, SMD package, SEIKO

- An HF π-filter on the power supply, placed closely to each oscillator circuit, ensures that no power supply noise can disturb the generated clock signal.
- A jumper placed on the enable input of the oscillator allows connection of an external generated clock to the SMB input connector.
- For maximum flexibility, a power supply jumper is available for each oscillator. The jumper can be set to 5V or 3.3V.
- Ground connections are designed close to each oscillator for easy measurement purposes.
- A solder jumper is located in the clock trace on the PCB to easily disconnect from the oscillator.
- This SMB for external clock input is nicely matched to 50 Ω.
- The 5.0 V oscillators connected to the FPGA gives a 3.3 V signal through a 22 Ω divider circuit with a matched 12-mil wide, 100 mil. trace.
- All high-speed signals are on the top and bottom layers of the PCB. This is the easiest way to control trace impedance. Impedance discontinuities are at one side of the signal only (the board side).
- In Figure 3-1, the high-speed signal traces are laid without corners. All edges are avoided and replaced by circular direction changes.
- A guard ring is around the oscillator output signals for:
  - Good decoupling against GND.
  - No cross talk possible from traces close to the clock signals.
  - Distance between signal trace and guarded GND trace is 2x the signal trace width.

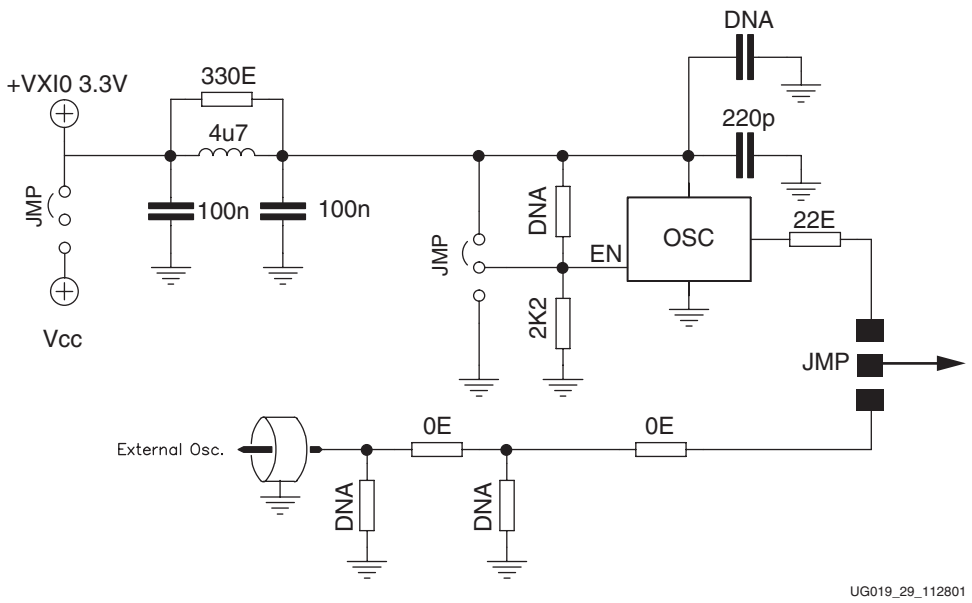

Figure 3-1: **Oscillator Components**

Routing and Placement

Figure 3-2 shows the routing and placement of an oscillator circuit on the PCB.

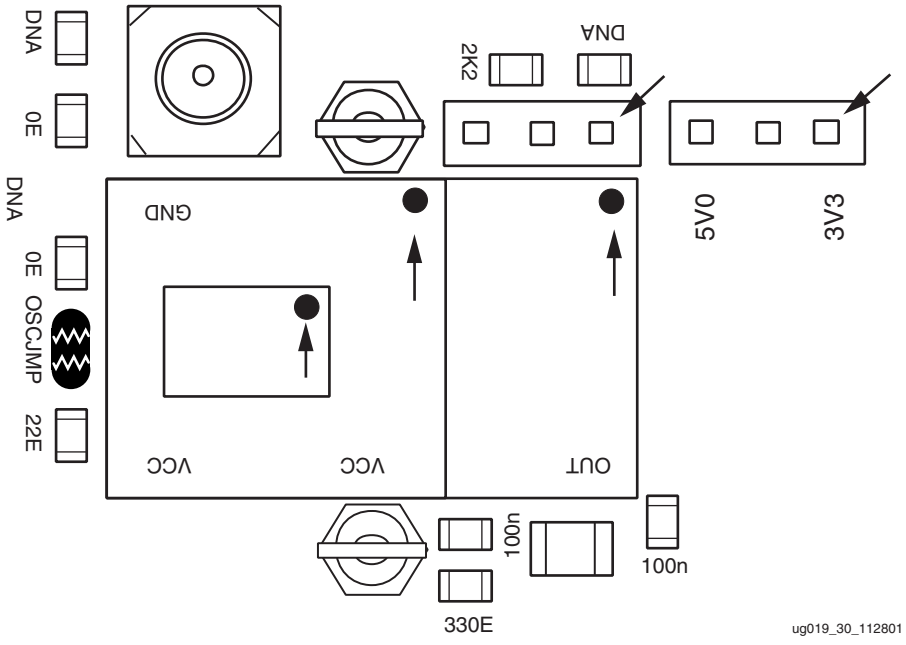

Figure 3-2: **Oscillator Placement**

Chapter 4

Optical Transceiver and Coax Routing

Optical Transceiver

The serial output of the SerDes can be routed to SMB coax buses or to an Agilent optical transceiver device. The default of an on-board jumper is routed through the Agilent device. The SerDes is connected to the optical transceiver through AC coupling.

Although not necessarily mounted, resistors and capacitors are on the PCB for added filters and termination. These items are available to change to a different transceiver or other uses.

The PCB traces from the SerDes to the SMB connectors or to the optical transceiver are already optimized for speed and impedance.

The length of the traces is not longer than 14 mm (center of the SerDes to center of SMB or transceiver) and the impedance is matched to 100 Ω.

Coax

The SerDes to coax connection is not longer than 14 mm.

The board routes are matched to each other at 100 Ω. A guard ring is placed along these high-speed traces. Close to each SMB coax connector a matching π-filter is placed.

In Figure 4-1, the traces are matched with a loosely coupled 100 Ω, 7-mil wide, and 13-mil long, up to the 100 Ω, 1% termination resistor. The trace is then separated and widened to 12 mil with a matched at 50 Ω resistor. Two capacitors assure good DC decoupling.

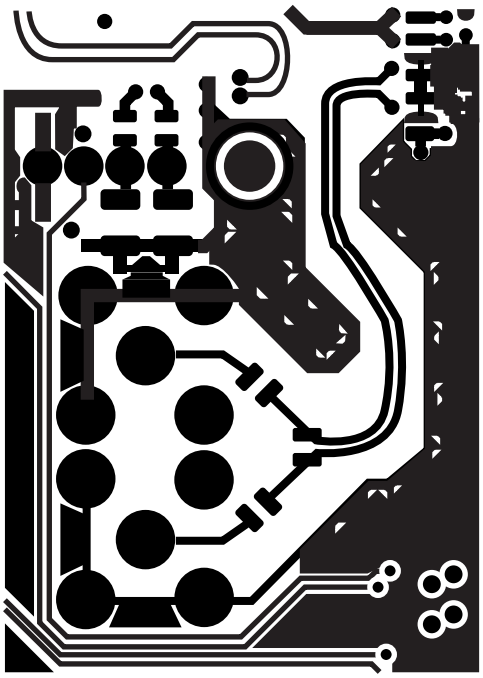

Figure 4-1: **SerDes Coax Tracks**

Figure 4-2 shows the setup of the SerDes, Coax SMB connectors, and optical transceiver. In this figure, SerDes setting is shown for the accompanying components.

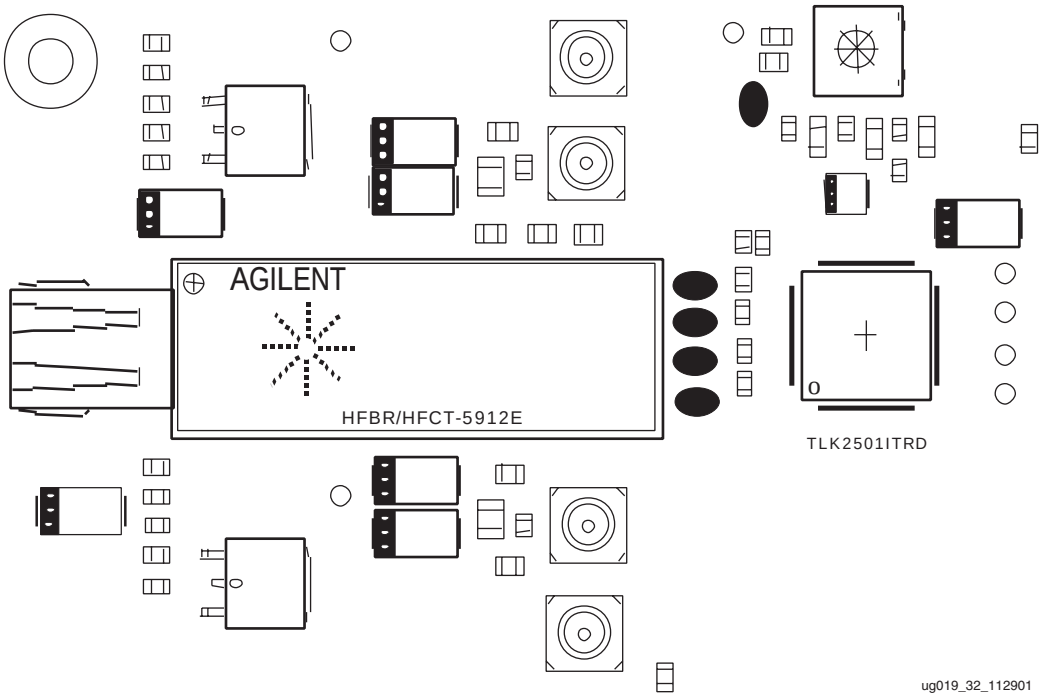

Figure 4-2: **Agilent Silkscreen**

Chapter 5

TLK2501 Device

Interface

Transmit Interface

The bus interface to TX input side of the SerDes accepts 16-bit single-ended LVTTL parallel data at the TXD[0:15] terminals. Data is valid on the rising edge of the GTX_CLK when the TX_EN is High and the TX_ER is Low.

The GTX_CLK is used as the word clock. The data, enable, and clock signals must be properly aligned as shown in Figure 5-1.

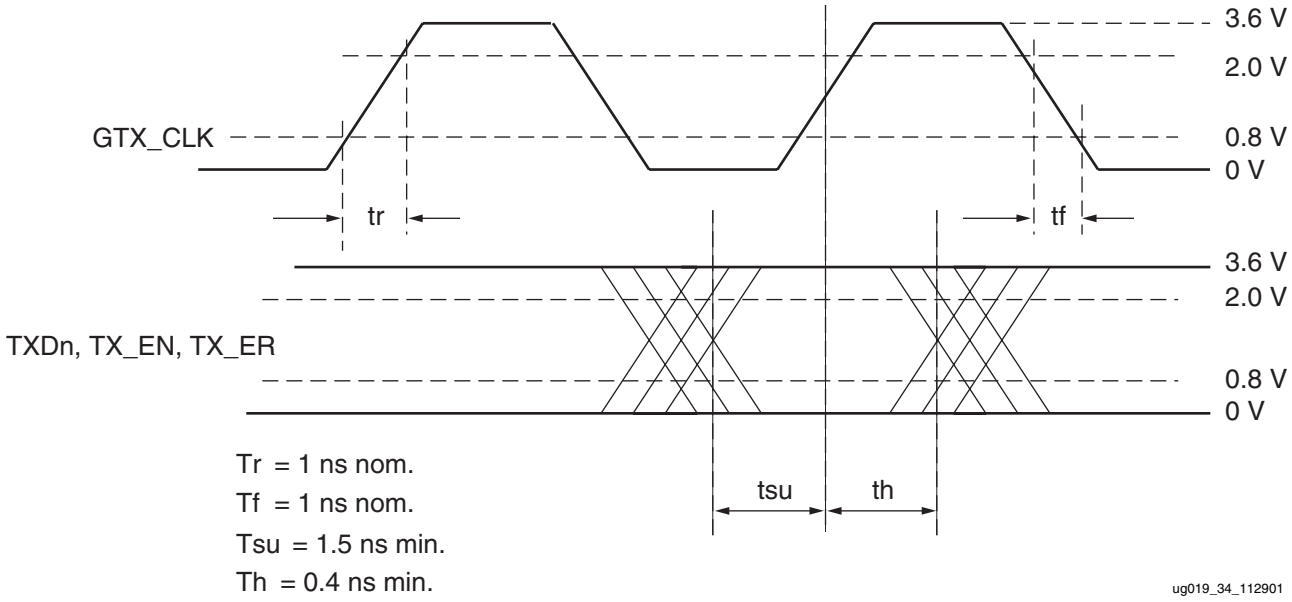

Figure 5-1: **Transmit Waveform**

When the TX word is latched into the SerDes, a transmission latency exist before data arrives at the differential outputs of the transmitter of the component.

The data transmission latency is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0.

Figure 5-2 illustrates the timing relationship between the transmit data bus, the GTX_CLK and serial transmit terminals.

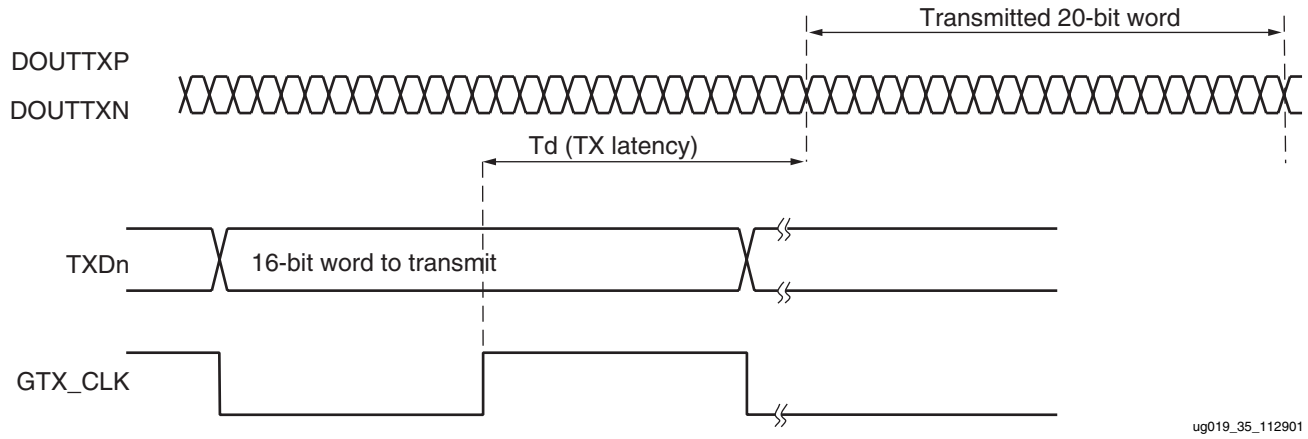

Figure 5-2: **Transmitter Latency**

Receive Interface

The receive bus interface drives 16-bit wide single-ended LVTTL parallel data on the RXD[0:15] terminals. Data is valid on the rising edge of the RX_CLK when the RX_DV/LOS is asserted High and the RX_ER is deasserted Low. The RX_CLK is used as the recovered word clock. The data, enable, and clock signals are aligned as shown in Figure 5-3.

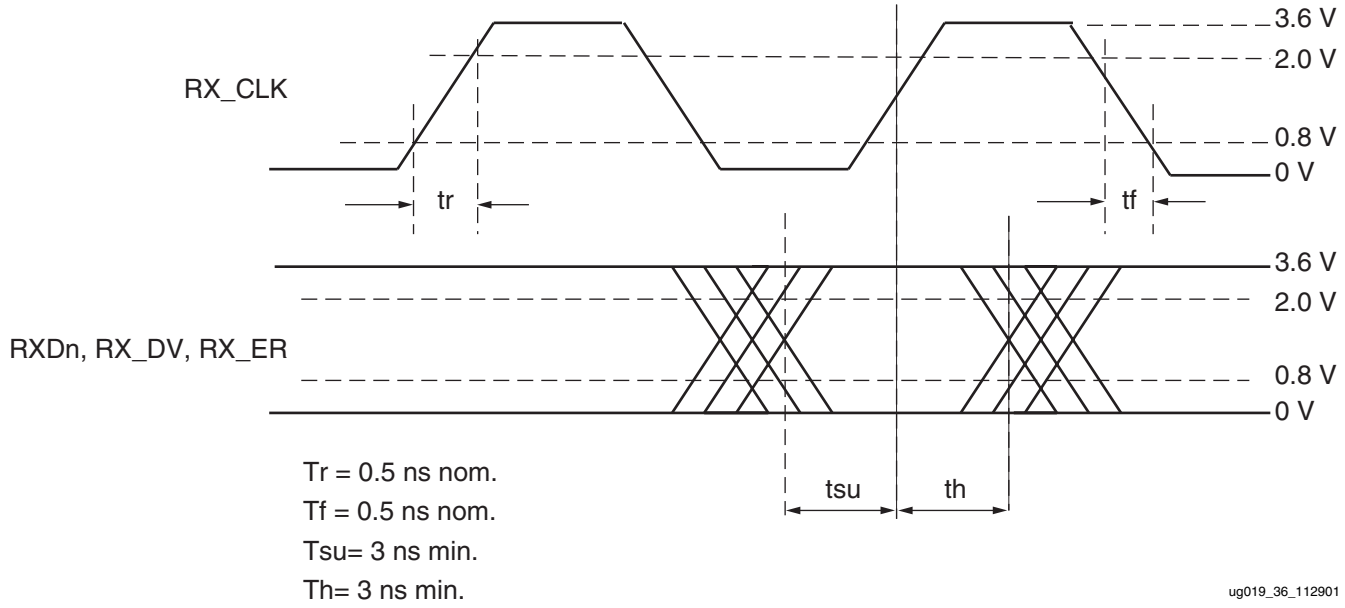

Figure 5-3: **Receive Waveform**

There is a receiver latency between the incoming differential serial data and the parallel bus output RXD. The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output as the aligned parallel word with RXD0 received as first bit.

Figure 5-4 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RX_CLK), and the receive data bus.

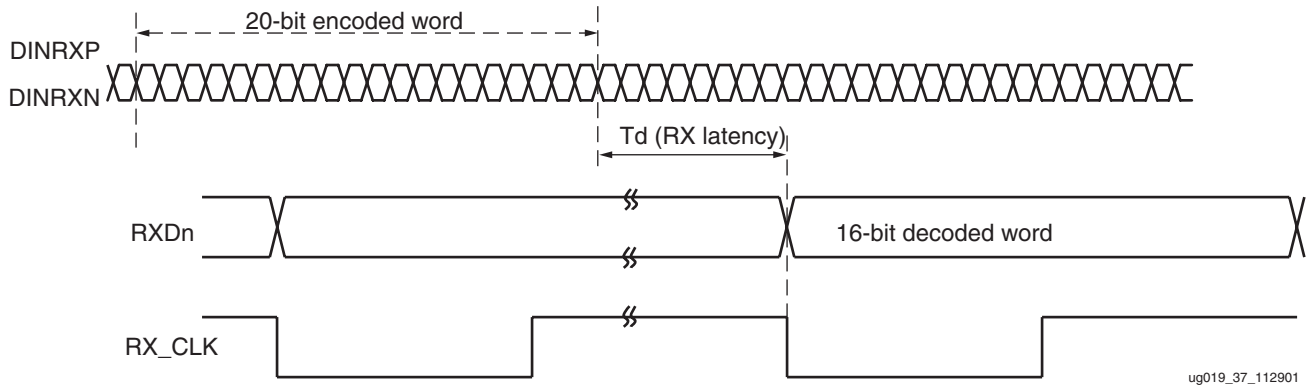

Figure 5-4: **Receiver Latency**

Latency

Transmit and receiver latency are fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum transmit latency ($T_{latency}$) is 34-bit times; the maximum is 38-bit times. The minimum receive latency ($R_{latency}$) is 76-bit times; the maximum is 107-bit times.

8B/10B Encoding and 10B/8B Decoding

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiver has a minimal number of transitions to stay locked. The encoding scheme at the same time maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking.

This popular encoding/decoding scheme is 8B/10B. The TLK family uses the 8-bit/10-bit encoding algorithm, that is also used by the fibre channel and the gigabit Ethernet interfaces. The TLK2501 internally encodes and decodes the data such that the user reads and writes actual 16-bit data and the encoding/decoding is hidden (user transparent).

The 8-bit/10-bit encoder, transmitter side, converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. The TLK2501 has a 16-bit wide interface, the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependant upon two additional input signals, the TX_EN and TX_ER.

When the TX_EN is High and the TX_ER is Low then the data bits TXD[0:15] are encoded and data is transmitted normally. When the TX_EN is Low and TX_ER is High the encoder will generate a carrier extend output signal consisting of two K23.7 codes. If the TX_EN and the TX_ER are both asserted, then the encoder generates K30.7 codes.

Table 5-1 provides the transmit data control decoding.

Table 5-1: **TxDataCode**

TX_EN	TX_ER	Encoded 20-Bit Output
0	0	IDLE (<K28.5,D5.6> or <K28.5, D16.2>)
0	1	Carrier extend (K23.7, K23.7)
1	0	Normal Data Character
1	1	Transmit error propagation (K30.7, K30.7)

Notes:
1. Data is transmitted in 20-bit serial words, K codes indicating carrier extend and transmit error propagation are transmitted as two consecutive 10-bit K-codes.

When no payload data is available to be sent, the encoder inserts the IDLE character set. IDLE consists of a K28.5 (BC) code and either a D5.6 (C5) or a D16.2 (50) character.

At the receiver side there are two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10-bit encoded data (half of the 20-bit received word) into 8-bits. The comma detect circuit is designed to provide byte synchronization to an 8-bit/10-bit transmission code.

When parallel data is clocked into a parallel-to-serial converter, at the transmitter side, the byte boundary with the parallel data is lost in the serialization of the data. When the serial data is received and converted to parallel format a way must be provided to recognize the byte boundary. Normally this is accomplished through the use of a synchronization pattern. This pattern is generally a unique sequence of 1s and 0s that cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8-bit/10-bit encoding contains the comma (`b0011111` or `b1100000`), a character used by the comma detect circuit to align the received serial data back to its original byte boundary.

When the decoder detects the K28.5 comma, a synchronization signal aligning the data to their 10-bit boundaries for decoding will be generated. It then converts the data back into 8-bit data, removing the control words. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RX_CLK) and output valid on the rising edge of the RX_CLK.

The RX_DV/LOS and RX_ER control signals are generated along with the decoded 16-bit data output on the RXD[0:15] terminals. The output status signals are asserted as shown in Table 5-2. When normal data is decoded the outputs will reflect that data on RXD[0:15] while RX_DV/LOS will be a logic High and RX_ER is a logic Low. When the TLK2501 decodes a K23.7 code (F7F7) indicating carrier extend, RX_DV/LOS transitions Low and RX_ER transitions High. If the decoded data is not a valid 8-bit/10-bit code, an error is reported by the assertion of both RX_DV/LOS and RX_ER. If the error was due to an error propagation code, the RXD bits outputs hex FEFE. If the error was due to an invalid pattern, the data output on RXD is undefined. When the TLK2501 decodes an IDLE code, both RX_DV/LOS and RX_ER are deasserted and a K28.5 (BC) code followed by either a D5.6 (C5) or D16.2 (50) code are output on the RXD terminals.

It is possible that a data pattern is interpreted as a comma due to a single bit error. If the erroneous comma is taken as the new byte boundary, all subsequent data will be improperly decoded until a properly aligned comma is detected. To prevent miss interpretation of data as a comma, the comma word alignment circuit is turned off after receiving a properly aligned comma after the link is established. The link is established after three idle patterns or one valid data pattern is properly received. The comma alignment circuit is re-enabled when the synchronization state machine detects a loss of synchronization condition (see synchronization and initialization). Loss of synchronization occurs when four or more invalid words are received in a short period of time.

Table 5-2: **RXDataControl**

Received 20-Bit Data	RX_DV/LOS	RX_ER
IDLE (<K28.5,D5.6> or <K28.5, D16.2>)	0	0
Carrier extend (K23.7, K23.7)	0	1
Normal Data Character (Dx.y)	1	0
Receive error propagation (K30.7, K30.7)	1	1

Extra Functionality of the SerDes

PRBS Generation / Verification

The SerDes has a built-in 2^{7-1} PRBS (pseudorandom bit stream) function. When the PRBSEN input is forced High, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register of the transmitter and data from the normal input source is ignored. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another TLK2501, or can be looped back to the receive input. Errors will be reported by forcing the RX_ER/PRBSPASS terminal Low at the receiver side.

Loopback Functionality

The loopback functionality provides for a full speed testing capability of the transmit/receive circuitry. The transceiver can provide this test function by enabling (LOOPEN) the internal loopback path this causes serial-transmitted data to be routed internally back into the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held during this function in a high-impedance state during the loopback testing.) By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RX_ER/PRBS_PASS terminal.

Loss of Signal Detection

A loss of signal detection circuit is provided for conditions where the incoming signal no longer has sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The TLK2501 reports this condition by asserting, the RX_DV/LOS, RX_ER and RXD all to a High state. As long as the signal is above 200 mV in differential magnitude, the LOS circuit does not signal an error condition.

Power down mode

When the ENABLE terminal is Low, the TLK2501 goes into a power-down mode. In the power-down mode, the serial transmit terminals (DOUTTXP, DOUTTXN), the receive data bus terminals, and the RX_ER goes into a high-impedance state. The signal detection circuit is still active and the RX_DV/LOS terminal acts as an output. If the signal detection circuit detects valid differential signal amplitude of >200 mV on the serial receive terminals (DINRXP, DINRXN), the RX_DV/LOS is driven Low. If no signal of sufficient amplitude is detected, the signal detection circuit indicates a loss of signal by driving the RX_DV/LOS High. In the power-down condition, the signal detection circuit draws less than 15 mW. When the TLK2501 is in the power-down mode, the clock signal on the GTX_CLK terminal must be provided at all times.

Chapter 6

LVDS On-Board Connectors

The LVDS connectors used on the demonstration board are QTE and QSE type connectors from SAMTEC.

The SAMTEC web site should be consulted for more detailed and complete information.

Reference Documents

The following documents are from SAMTEC. They have been included in a .zip file available at: http://www.xilinx.com/bvdocs/userguides/ug019.zip.

- QTEQSECC.pdf gives details about the current carrying and ground plane capacity.
- QTEQSER.pdf gives detailed information on the RF characterization of the 5 mm stack height, 50 Ω system.

Table 6-1: **QTE/QSE Summary**

0.8 mm Pitch (QTE/QSE)	10 MHz	100 MHz	500 MHz	1 GHz	Units
Impedance	50.2	50.7	55.0	60.0	Ω
Voltage Standing Wave Ratio (VSWR)	1.01	1.06	1.25	1.45	
Attenuation	–0.005	–0.0305	–0.2429	–0.4607	dB
Crosstalk	–76.9	–60.6	–49.0	–39.5	dB
Propagation Delay	58.4	58.4	58.4	58.4	ps
Rise Time	99.4	99.4	99.4	99.4	%

Notes:
1. 50 Ω System, S-G-S configuration with plane grounded, 5 mm mated height

Chapter 7

LVDS Cable Details

Cable Assembly

Figure 7-1 is a summary of all possible LVDS cable assembly parameters.

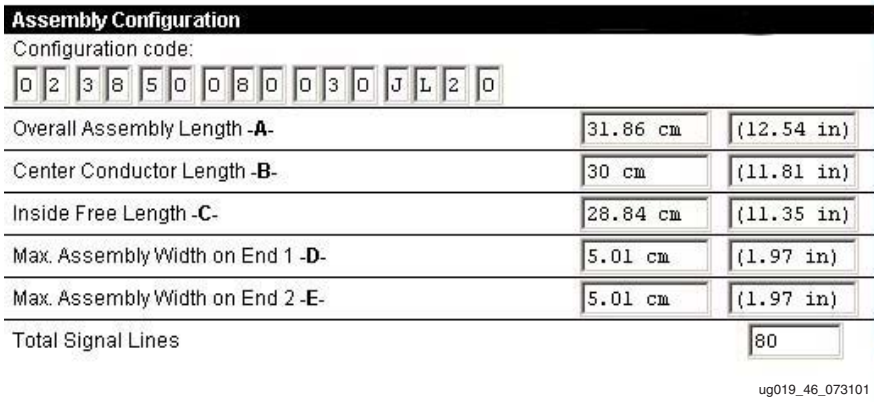

Figure 7-1: **LVDS Cable Assembly Parameters**

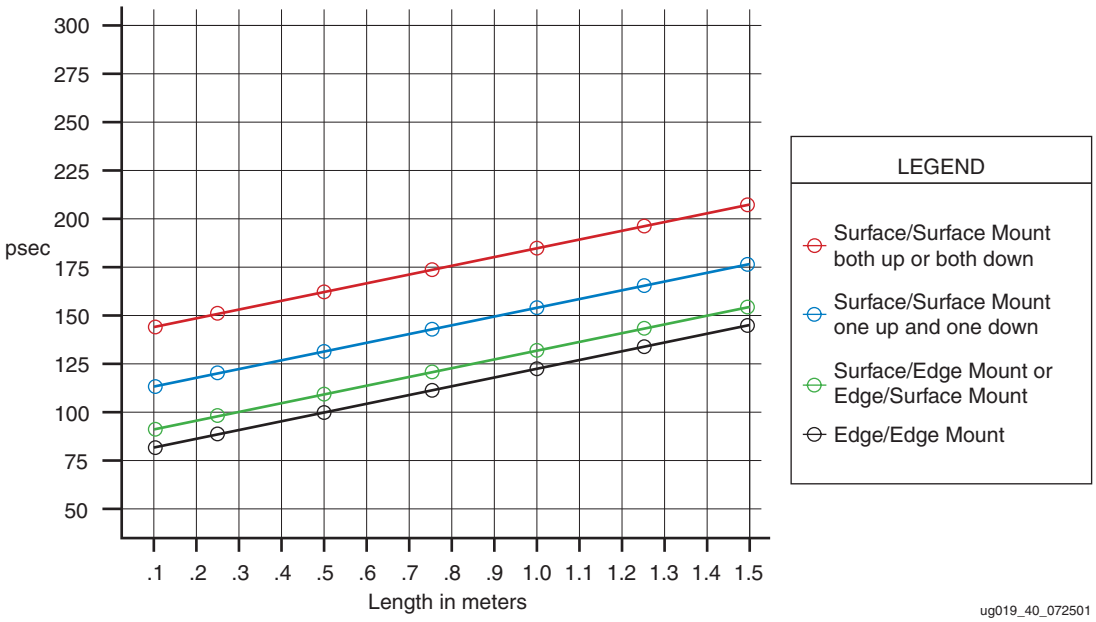

Figure 7-2: **Cable Delay**

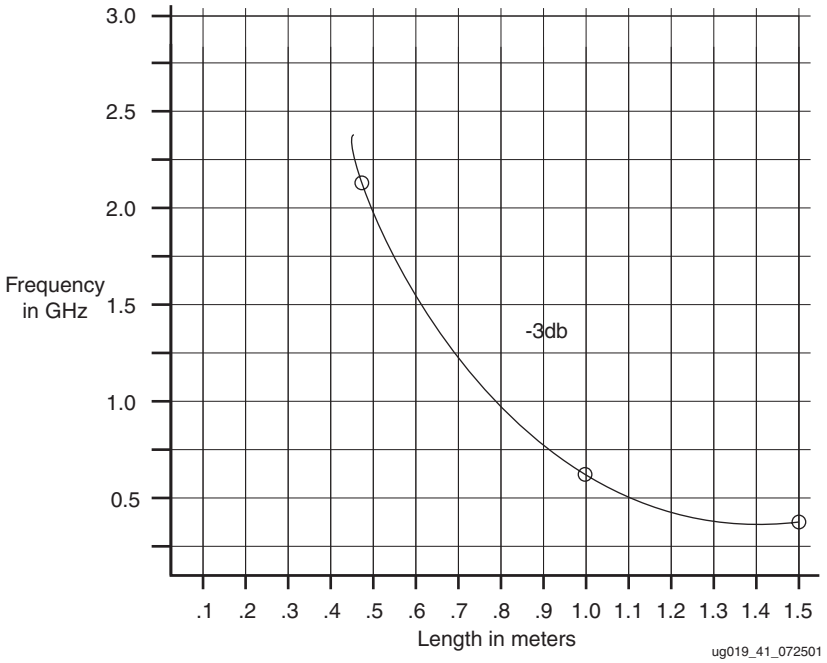

Figure 7-3: **Typical COAX Attenuation, 50 Ω, 38 AWG Blue Ribbon Cable**

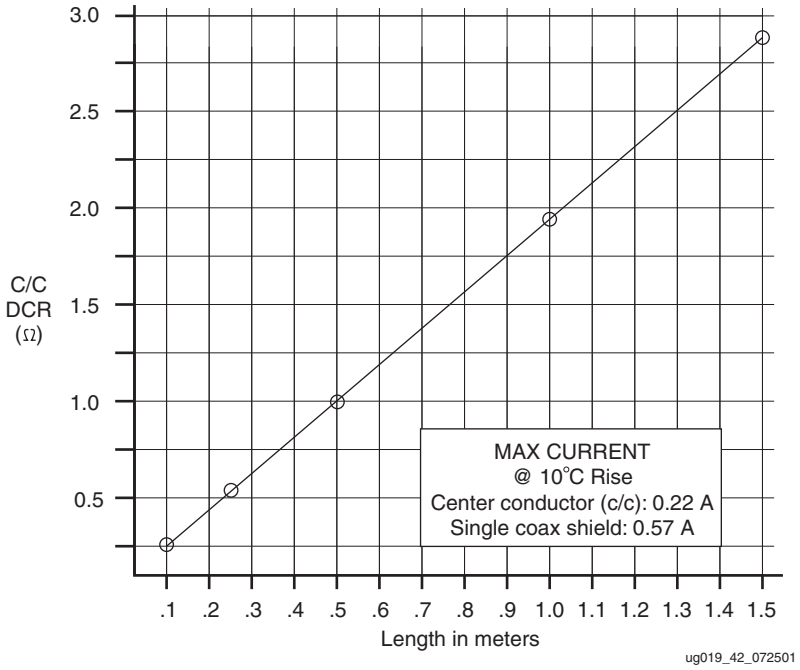

Figure 7-4: **Typical DCR and Maximum Current-Carrying Capacity**

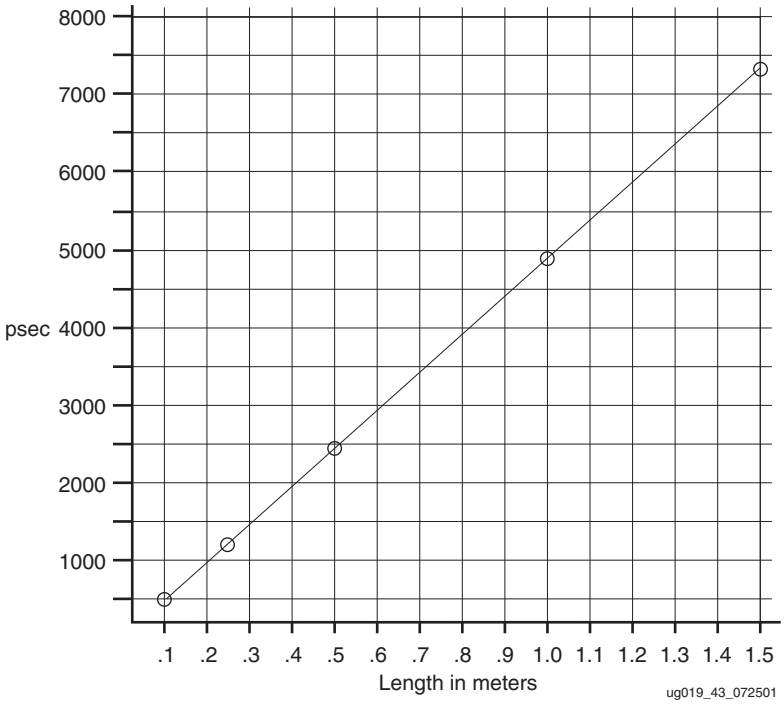

Figure 7-5: **Typical Propagation Delay**

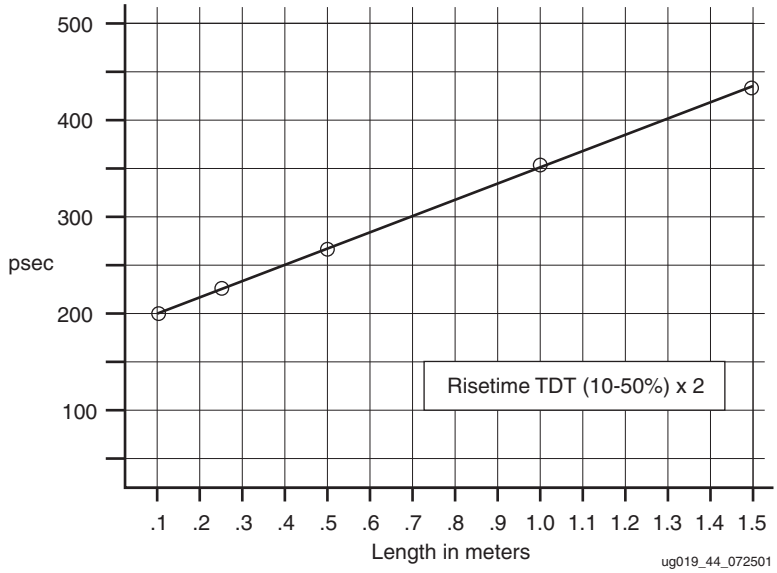

Figure 7-6: **Typical Rise Time**

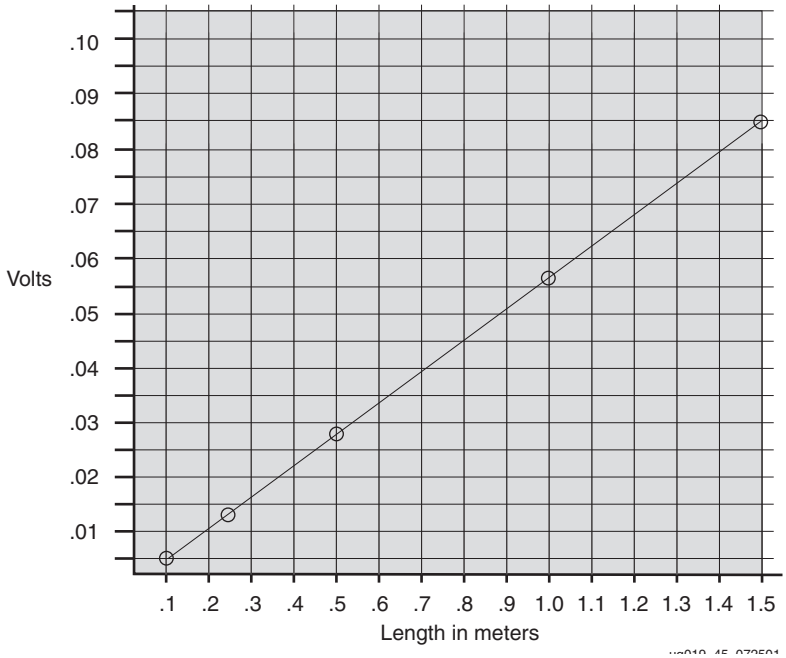

Figure 7-7: **Typical Voltage Drop at 30 mA**

Appendix A

Layout Guidelines

Printed Circuit Board

Figure A-1 shows the demonstration board's PCB layer layout. The ideal guideline is to strictly follow the 50 Ω design rules.

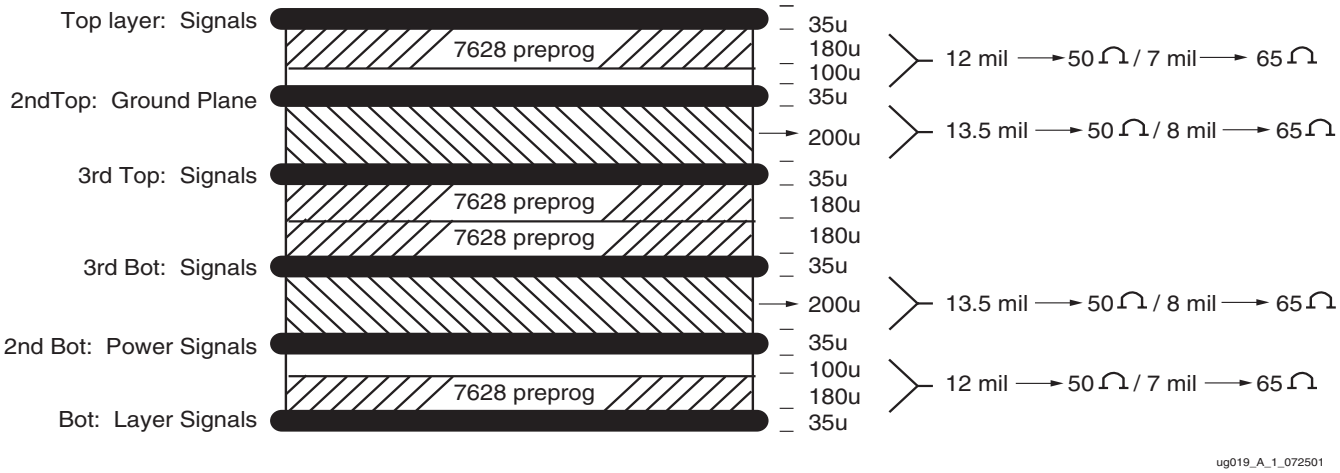

Figure A-1: **PCB Layer Layout**

FPGA - SerDes Connection

The TLK2501 device is connected to the Virtex-II device by two 16-bit buses and some control signals. Transmit and receive buses are high-speed parallel data buses crossing the board. No termination resistors are used on these buses because the XCITE function in the FPGA is used. The control signals all are more or less slow logic signals indicating statuses of the SerDes or used to control functions of the SerDes. The clock signals running between the devices have been designed as such.

- RX_CLK.
  - The recovered word clock.
  - Signal levels are LVTTL.
- GTX_CLK
  - The transmission word clock strobe.
  - Because transmitted parallel data and this clock need to be related, the oscillator that generates the GTX_CLK clock is routed to a clock input on the FPGA, and the generation of this clock is done through a normal I/O.
  - Connection between FPGA and SerDes is a clock signal and is threaded as such.

Differential Signal Routing

Differential signaling is a good way to get rid of all kind of signal disturbances like; common mode noise, etc. This is true if the differential signals follow a good and strict lay-out scheme.

- Matched in impedance, 50 Ω
- Matched in length, per pair and per bus system.
- No square corners, all route changes must have round or 45° corners.

Matching LVDS pair lengths can be quite a tedious job, especially when chips have turned so the base length distance is quite long. In that case, you need PCB space and time. Space to curl the pairs and so to match them in length and also the time to do that thoroughly. Of course, the PCB CAD tool can provide you with a total copper length calculation feature.

Another thing to look out for is the placement of connectors. For the greatest benefit, place them carefully, leaving space to move the connectors around.

Impedance Discontinuities

Impedance discontinuities in the signal path are the cause of reflections that degrade the quality of the transmitted signal. Most sources of this kind of discontinuities are vias, connectors, sharp angles, and stubs.

Vias in high-speed signals are avoided by designing these signals at the top and bottom layers of the circuit board. This is done for all high-speed signals, clocks and LVDS connections. Another reason for using the outer most layers of the PCB as high-speed planes is that edging circuit boards can cause discontinuities in the characteristic impedance of the different layers. This is something that is under less control when designing at inner layers of the PCB.

Connectors are avoided by designing the circuits in a way that connectors are not needed. In the giga data path, from SerDes to optical transceiver, the possible connector for switching between coax and optic is avoided by designing a “to cut and solder” jumper. Where a connector could not be avoided, connectors designed for this kind of high-speed application have been used in conjunction with high-speed board layout techniques.

All differential signals have been routed to match in length and to achieve a 100 Ω differential characteristic impedance.

Sharp angled traces have been avoided in the clock and giga data path connections. Not even 45° angles have been used, but nicely curved traces are laid out on the board. To further improve signal integrity, a guard ring has been designed close to these signals, and a continuous ground plane has been put under or above.

Power and Ground Design

Important in PCB design is the conception of the power/ground system. This includes proper isolation and stacking of the power/ground layers, providing bulk capacitance needs and providing decoupling/bypassing capacitors next to the different chips supply/ground pins.

In each FPGA I/O bank, a combination of 10 µF tantalum and 100 nF ceramic capacitors have been placed close to the pins, providing bulk capacitance to keep the power supply stable and filtering low frequency noise.

Two 22 nF capacitors have been placed between each V_{CC} (V_{CCO}, V_{CCINT}, and V_{CCAUX}) and ground pin combination. Most of these capacitors have been placed very close to FPGA power and ground pins. They are placed inside the pin grid of the Fine Pitch Ball array.

For the SerDes, the same technique has been applied. Each power pin has a small 22 nF capacitor to ground closely placed to the pins. Bulk tantalum capacitors of 47 µF have been foreseen for every V_{CC}. The analog supply has its own separated power plane connected to the main power supply through a ferrite bead.

The termination supplies (VT_TX and VT_RX) each have their own voltage regulator and decoupling. A voltage regulation via a potentiometer has been designed to adapt the output and input voltages to the line.

Brief PCB Guidelines

1. Make the data lines transmission lines of fixed impedance. This should be done even if the trace lengths are so short that the propagation delay of the line is small relative to the transition time of the signal. In general, routes of 50 Ω impedance should be used to help dominate parasitic effects of the board and devices on the signal quality (reflections, ringing, distortion) and minimize unwanted electrical noise.
2. Keep data lines as short as possible and of equal length to minimize pulse-width distortion of the differential data lines. Load differential lines symmetrically to prevent pulse-width distortion. Avoid sharp 90° bends in the high-speed serial data lines. Use large radius corners or make sharp bends with exterior angles of <45° where the high-speed data lines change direction.
3. Keep differential data lines in the same approximate location to prevent unbalanced crosstalk coupling.
4. Place power supply filter circuits as close as possible to the V_{CC} pins for best power supply conductive noise filtering.
5. Place data line terminations at the load end of the transmission line where the input of the receiving circuit is located.
6. Use a wide-area, continuous ground plane to provide a low-inductive impedance return path for the power supply ground currents. Minimize holes in the ground plane to allow ground currents to take direct paths to the return point.
7. If possible, distribute V_{CC} power via a plane rather than by traces. This helps minimize the inductive effect of traces on the switching logic currents supplied from V_{CC}.
8. Place V_{CC} bypass capacitors as close as possible to the V_{CC} locations that require bypassing.
9. Use high-quality, high-frequency surface-mount components for best high-frequency performance.
10. Surface mount coil inductors should have less than 0.7 Ω series resistance and a high self-resonant frequency. Ferrite beads can be substituted for coil inductors if the power supply noise is fairly quiet. The 0.1 µF capacitors used should be monolithic; ceramic capacitors and 10 µF capacitors should be tantalum.