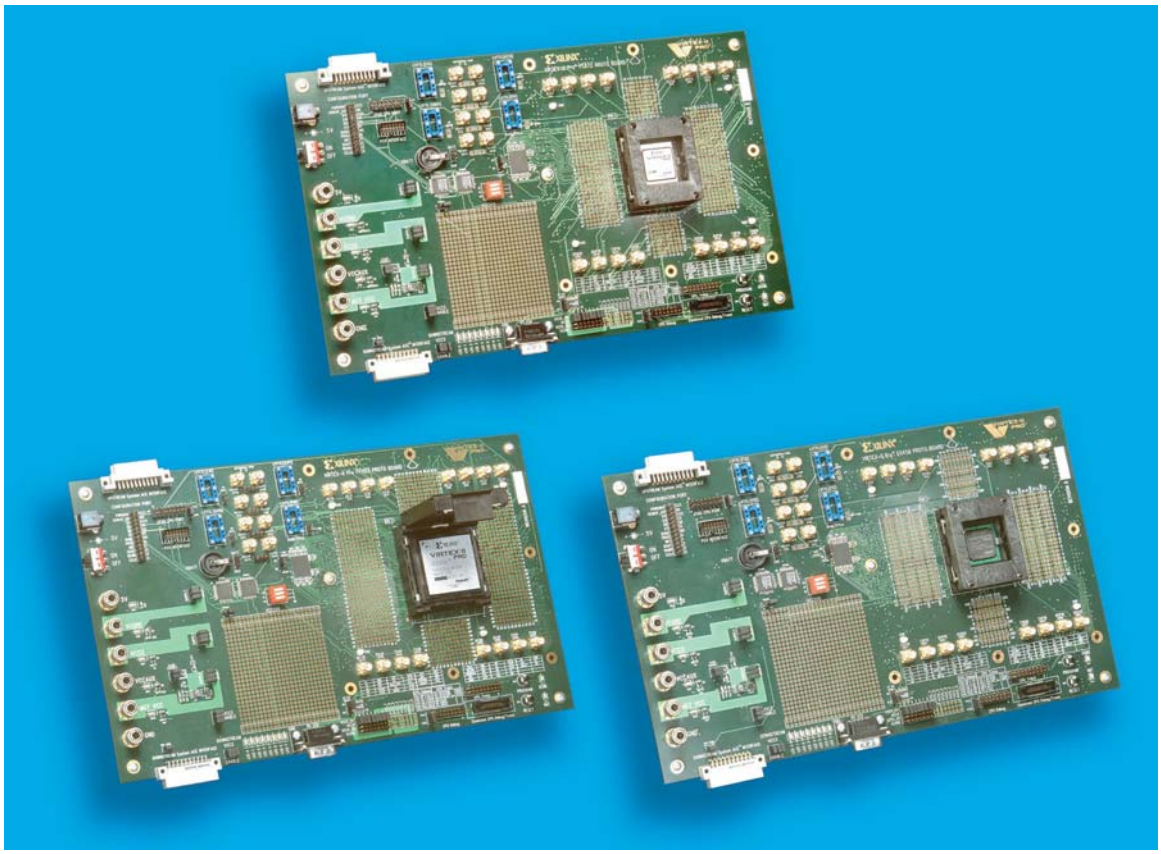
Product Not Recommended for New Designs

Virtex-II Pro Prototype Platform User Guide

UG027 / PN 0402044 (v1.6) October 25, 2002



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The following table shows the revision history for this document.

Date	Version	Revision
03/04/02	1.0	Preliminary Xilinx release.
05/29/02	1.1	Initial Xilinx release.
06/04/02	1.2	Modifications to Figure 1-1.
06/11/02	1.3	Modifications to Figure 1-2.
07/01/02	1.4	Addition of Appendix A.
07/03/02	1.5	Modifications to text and import to common user guide template.
10/25/02	1.6	Modifications to Figure 1-1 and to Table 1-11, note 4.

Preface: About This Manual

Chapter 1: Virtex-II Pro Prototype Platform

Appendix A: RISCWatch and RISCTrace Interfaces

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Preface

About This Manual

This manual contains information about the Virtex-II Pro™ Prototype Platform prototype and demonstration boards.

Manual Contents

This manual contains the following chapters:

- Chapter 1, "Virtex-II Pro Prototype Platform," describes the features and operation of the boards
- Appendix A, "RISCWatch and RISCTrace Interfaces," summarizes the interface requirements between the PPC405x3 and the RISCWatch and RISCTrace tools

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Book	Pages from *The Programmable Logic Data Book*, which contains device-specific information on Xilinx device characteristics, including readback, Boundary Scan, configuration, length count, and debugging http://support.xilinx.com/partinfo/databook.htm

Resource	Description/URL
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *`design_name`*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *`design_name`*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr ={on|off}`**
Vertical bar |	Separates items in a list of choices	**`lowpwr ={on|off}`**

Convention	Meaning or Use	Example

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *`block_name loc1 loc2 ... locn;`*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current file or in another file in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Chapter 1

Virtex-II Pro Prototype Platform

Package Contents

- Xilinx Virtex-II Pro™ Prototype Platform board
- User guide
- Device vacuum tool
- Four SMA-to-SMA coax cable assemblies
- Headers for test points
- CD-ROM
- Two low-voltage, 14-pin, dual-inline package (DIP) crystal oscillators

CD-ROM Contents

- User guide in PDF format
- Example designs
  - These designs include the Verilog source code, user constraints files (***.ucf**), documentation in PDF, and a **readme.txt** file
- Bitstream files (***.bit**) for each part type supported by the board (Bitstream synthesized using Xilinx ISE 4.2i tools)
- Full schematics of the board in both PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in ***.pho** and ***.pdf** for the PC board (There are many free or shareware Gerber file viewers available on the Web for viewing and printing these files)

Introduction

Virtex-II Pro Prototype Platforms are prototype and demonstration boards that allow designers to investigate and experiment with the features of Virtex-II Pro series FPGAs. This document describes the features and operation of the boards, including how to configure chains of FPGAs and serial PROMs. Prototype Platforms are intended strictly for evaluating the functionality of Virtex-II Pro features and are not intended for A/C characterization or high-speed I/O evaluation.

Features

- Independent power supply jacks for V_{CCINT} , V_{AUX}, V_{CCO}, and MGT_V_{CC}
- Selectable V_{CCO} for each SelectI/O™ bank
- Configuration port for use with Parallel Cable III and Parallel Cable IV cables
- Headers for CPU debug, CPU trace, and JTAG CPU port
- RS232 serial port
- 12 global clock (GCLK) inputs
  - Four differential clock pairs
  - Four LVTTL-type oscillator sockets
- Eight pairs of (TX, RX) SMA inputs for the Rocket I/O transceivers
- 8 MB (32-bit data width) SDRAM
- Power indicator LEDs
- Two onboard SPROMs (4 Mb each) for any configuration mode
- JTAG port for reprogramming the XC18Vxx series reconfigurable PROMs and the user FPGA, also known as the Device Under Test (DUT)
- Upstream and downstream System ACE and Configuration Interface connectors
- Onboard battery holder
- Two low-voltage, 14-pin, DIP crystal oscillators

The kit contains headers that can be soldered to the breakout area, if desired. These headers are useful with certain types of oscilloscope probes for either connecting function generators or wiring pins to the prototype area.

The Virtex-II Pro Prototype Platform board (referred to as "the board") contains a DUT FPGA and two in-system XC18V04 programmable SPROMs. Each SPROM can hold up to 4,194,304 bits. The DUT can be configured either from the SPROMs or from the configuration ports (Parallel III/IV cable).

In addition to the SPROMs and the configuration ports, there is an upstream connector and a downstream connector. The upstream connector can be connected to configure the DUT using the System ACE configuration solution. The downstream connector can be used to connect to another board in a chain.

The board also contains an 8-MB SDRAM chip. This chip can be used as a scratch pad or to hold programs when testing the embedded processor functionality.

Figure 1-1 shows a block diagram of the board.

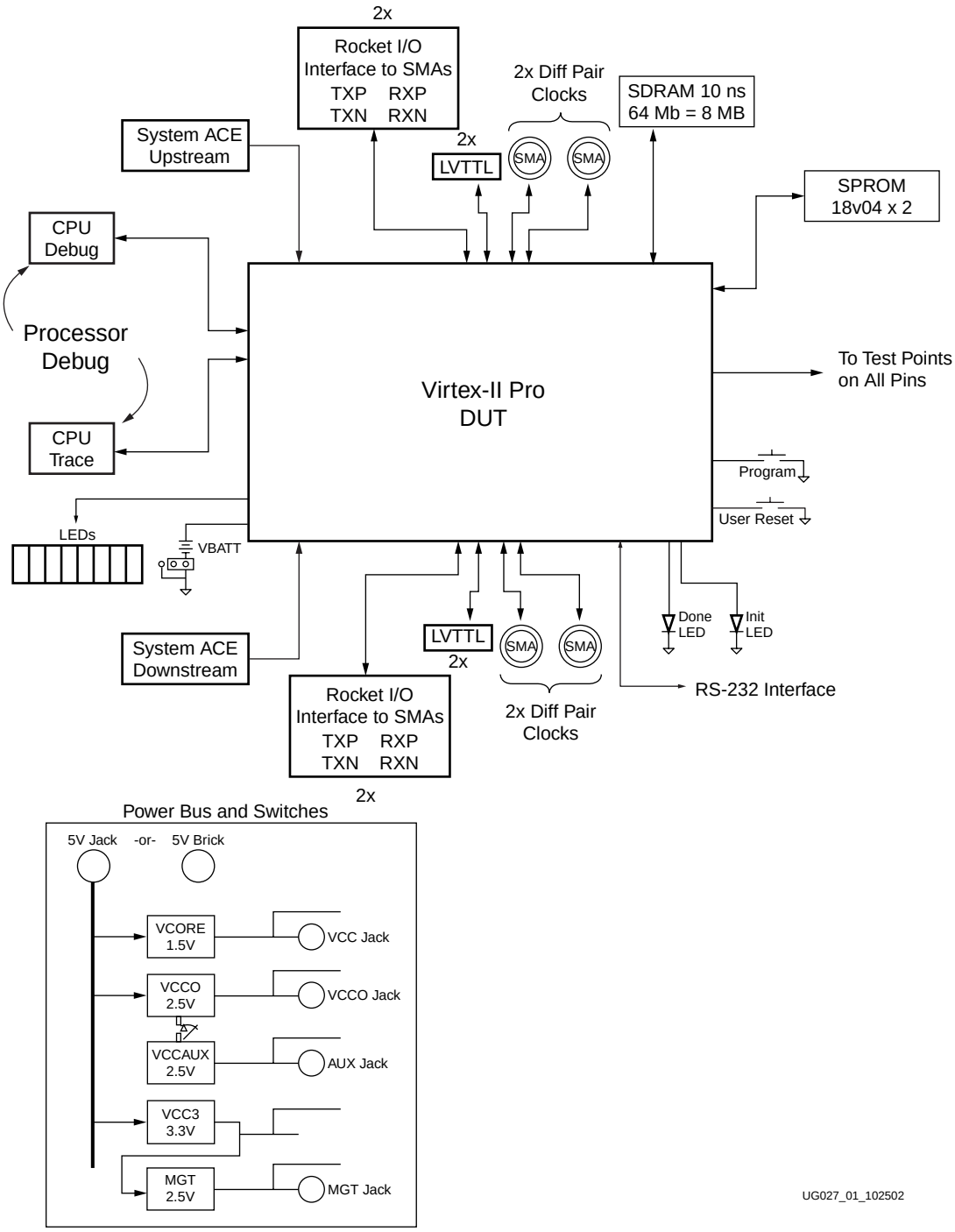

Figure 1-1: **Virtex-II Pro Prototype Platform Block Diagram**

Detailed Description

The Virtex-II Pro Prototype Platform board is shown in Figure 1-2. Each feature is detailed in the numbered sections that follow.

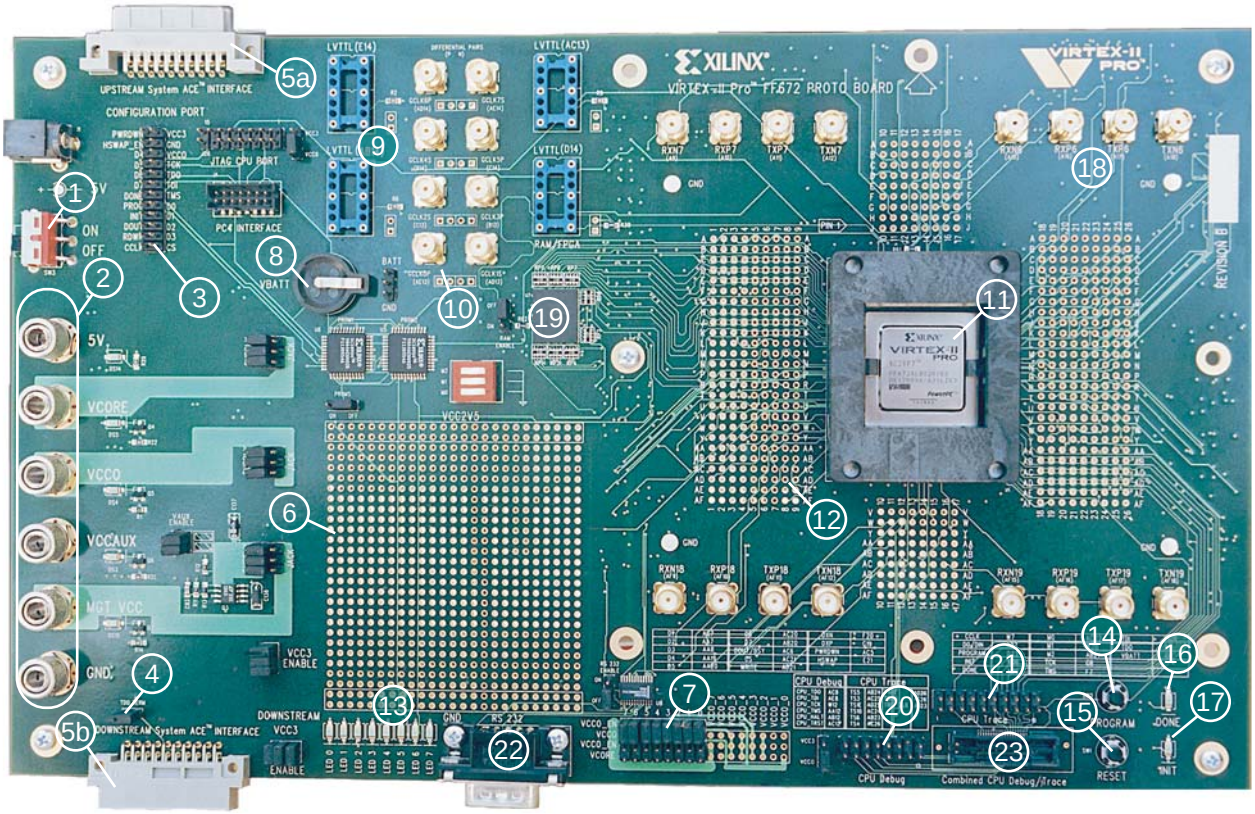

Figure 1-2: **Detailed Description of Virtex-II Pro Prototype Platform Components**

1. Power Switch

The board has an onboard power supply and an **on|off** power switch. When lit, a green LED indicates power from the power brick connector or the 5V jack.

On Position

In the on position, the power switch enables delivery of all power to the board by way of voltage regulators situated on the backside of the board. These regulators feed off a 5V external power brick or the 5V power supply jack.

The voltage regulators deliver fixed voltages. Maximum current range for each supply is 2A. Table 1-1 shows the maximum voltage for each power supply jack.

Note: To power the V_{CCAUX} pins you must jumper the pins labeled VAUX enable located next to the VCCAUX jack on the board. This action will connect the V_{CCAUX} pins on the DUT to V_{CCO}.

Table 1-1: **Voltage Ranges**

Label	Max Voltage
VCORE	1.5V
VCCO	2.5V
VCCAUX	2.5V
MGT_VCC	2.5V

Off Position

In the off position, the power switch disables all modes of powering the DUT.

Power Enable Jumpers

For each power supply there are headers marked **Supply** on one side and **Jack** on the other side. Appropriate placements of jumpers on these headers enables delivery of all power from either the onboard regulators or the four power supply jacks marked **VCORE**, **VCCO**, **VCCAUX**, and **MGT_VCC**.

2. Power Supply Jacks

One method of delivering power to the DUT is by way of the power supply jacks. (Consult the Xilinx data book, http://www.xilinx.com/partinfo/databook.htm, for the maximum voltage rating for each device you are using.) The power supply jacks are:

- VCORE
  - Supplies voltage to the core of the DUT
- VCCO
  - Supplies I/O voltages to the DUT
  - Each bank can be powered from one of two sources (V_{CCO}, V_{CCINT}) by appropriate placement of jumpers on the header
- VCCAUX
  - Supplies voltage to the V_{AUX} header and the V_{AUX} DUT pins
- MGT_VCC
  - Supplies power to the Rocket I/O transceivers on the DUT ($AV_{CC}AUX$, VTT_X, VTR_X)

3. Configuration Ports

These headers can be used to connect a Parallel Cable III or Parallel Cable IV cable to the board and support all Virtex-II Pro device configuration modes. (See Table 1-3 for connecting the cables to the Configuration Ports.)

Table 1-2: **Slave Serial Mode**

Configuration Port Header	Parallel Cable III/IV Pins
VCC3	VCC
GND	GND
CCLK	CCLK
DONE	D/P
D0	DIN
PROG	PROG
INIT	

4. JTAG Termination Jumper

The JTAG termination jumper is used to short the TDI pin of the downstream System ACE connector to the TDO pin of the upstream System ACE connector for the final board in a chain.

TCK and TMS are parallel feedthrough connections from the upstream System ACE connector to the downstream System ACE connector and drive the TCK and TMS pins of the onboard PROMs and the DUT.

> **Note:** The termination jumper must be in place on the last board in the chain to connect the TDO pin of the final device to the TDO feedback chain.

Figure 1-3 shows the setup of the JTAG chain on the board.

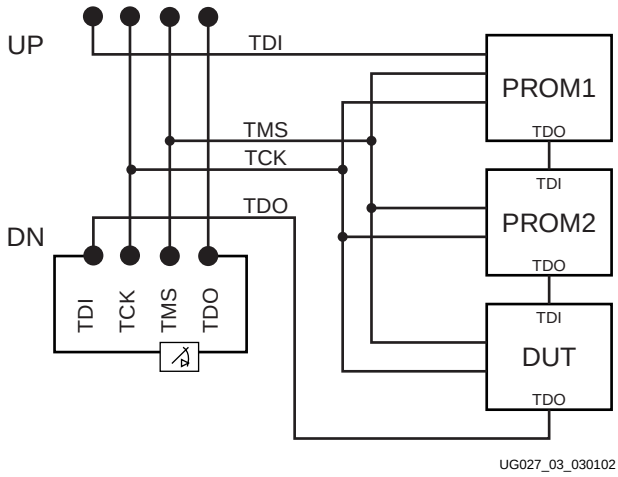

Figure 1-3: **JTAG Chain Termination**

Table 1-3: **JTAG Mode**

Configuration Port Header /Parallel IV Cable Connector	Parallel Cable III Pins	Parallel Cable IV Pins
VCC3	VCC	VCC
GND	GND	GND
TMS	TMS	TMS
TDI	TDI	TDI
TDO	TDO	TDO
TCK	TCK	TCK
INIT		INIT

5a. Upstream System ACE Connector

The Upstream System ACE connector, as shown in Figure 1-4, can be used to configure the DUT. This connector can be sourced by any JTAG configuration stream. For example, a System ACE Controller with CompactFlash can be used to generate very large JTAG streams for configuring multiple Virtex-II Pro Prototype Platforms using the Downstream System ACE connector.

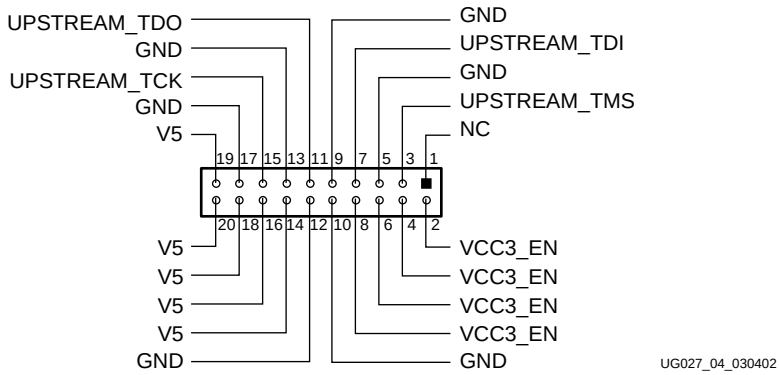

Figure 1-4: **Upstream System ACE Connector, 20-Pin Female**

5b. Downstream System ACE Connector

The Downstream System ACE connector, as shown in Figure 1-5, is used to pass configuration information to a DUT in a downstream prototype platform from sources such as a Parallel Cable III cable or an Upstream System ACE connector.

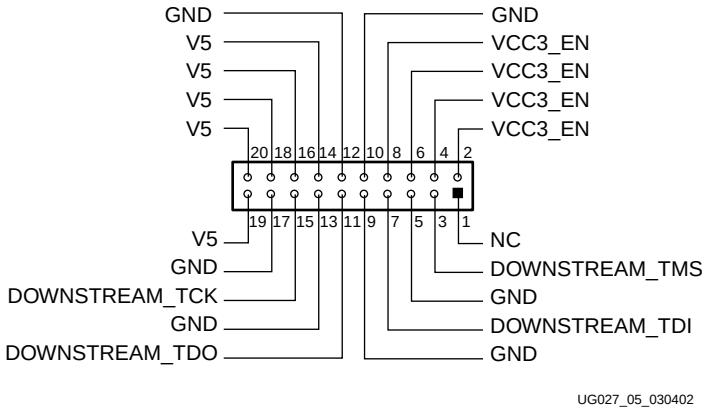

Figure 1-5: **Downstream System ACE Connector, 20-Pin Male**

6. Prototyping Area

The prototyping area accommodates 0.10" spaced ICs. The kit contains headers that can be soldered to the breakout area, if desired. Power and ground buses are located at the top and bottom, respectively, of the prototyping area.

7. V_{CCO} Enable Supply Jumpers

Virtex-II Pro series devices have eight SelectI/O banks, labeled 0 through 7, each with a V_{CCO} enable supply jumper. V_{CCO} enable supply jumpers can connect each bank to one of the two onboard supplies, V_{CCINT} or the V_{CCO} supply. These jumpers must be installed for the Virtex-II Pro device to function normally.

8. VBATT

An onboard battery holder is connected to the VBATT pin of the DUT. If an external power supply is used, the associated jumper must be removed. Select a 12 mm lithium coin battery (3V), such as part numbers BR1216, CR1216, and BR1225 from Panasonic or any other appropriate 12 mm lithium coin battery (3V).

9. Oscillator Sockets

The prototype board has four crystal oscillator sockets, all wired for standard LVTTL-type oscillators. These sockets connect to the DUT clock pads as shown in Table 1-4, page 19. Onboard termination resistors can be changed by the user. The oscillator sockets accept both half- and full-sized oscillators and are powered by a 2.5V power supply.

Table 1-4: **OSC Clock Pin Connections**

Label	FG456		FF672		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
OSC Socket Top1	GCLK0S	F12	GCLK0S	E14	GCLK0S	E18
OSC Socket Bottom 2	GCLK1P	E12	GCLK1P	D14	GCLK1P	D18
OSC Socket Bottom 1	GCLK2P	V12	GCLK2P	AB14	GCLK2P	AJ17
OSC Socket Top 2	GCLK3S	U12	GCLK3S	AC13	GCLK3S	AH18

10. Differential Clock Inputs

In addition to the oscillator sockets, there are eight 50Ω SMA connectors that allow connection to an external function generator. These connect to the DUT clock pads as shown in Table 1-5. They can also be used as differential pairs with 100Ω termination resistors. The differential clock pairings are as shown.

Table 1-5: **SMA Clock Pin Connections**

Label	FG456		FF672		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
N	GCLK1S	W12	GCLK4P	AD13	GCLK4P	AK17
P	GCLK0P	Y12	GCLK5S	AE13	GCLK5S	AL17
N	GCLK3P	C12	GCLK6P	B13	GCLK6P	H17
P	GCLK2S	D12	GCLK7S	C13	GCLK7S	J17
N	GCLK7S	Y11	GCLK7P	AE14	GCLK7P	AL18
P	GCLK6P	W11	GCLK6S	AD14	GCLK6S	AK18
N	GCLK5P	D11	GCLK5P	C14	GCLK5P	J18
P	GCLK4S	C11	GCLK4S	B14	GCLK4S	H18

Notes:

1. Use these differential clock pairs for the Rocket I/O transceivers. They have been optimized for the transceivers.
2. These global clocks are not available through the breakout area test points.

11. DUT Socket

The DUT socket contains the user FPGA, referred to as the Device Under Test.

The device must be oriented using the P1 indicator on the board. Failure to insert the device to the proper orientation can damage the device. To avoid pin damage, always use the vacuum tool provided when inserting or removing the Virtex-II Pro device. When

using BGA packages, do not apply pressure to the device while activating the socket. Doing so can damage the socket and/or the device.

12. Pin Breakout

The pin breakout area is used to monitor or apply signals to each of the DUT pins. Headers can be soldered to the breakout area to use with certain types of oscilloscope probes, for either connecting function generators or wiring pins to the pin breakout area. Clocks in the pin breakout area that connect to the DUT clock pads are shown in Table 1-6.

Table 1-6: **Breakout Clock Pin Connections**

Label	FG456		FF672		FF1152	
	Clock Name	Pin Number	Clock Name	Pin Number	Clock Name	Pin Number
Breakout Area 1	GCLK3S	V11	GCLK5S	AC14	GCLK5S	AJ18
Breakout Area 2	GCLK4P	U11	GCLK3S	AB13	GCLK3S	AH17
Breakout Area 3	GCLK7P	F11	GCLK1P	D13	GCLK1P	D17
Breakout Area 4	GCLK6S	E11	GCLK0S	E13	GCLK0S	E17

13. User LEDs (Active-High)

There are eight active-high user LEDs on the board. Before configuration, the LEDs reflect the status of the configuration mode switch. During configuration, the LEDs are in a high-impedance condition. After configuration, the LEDs are available to the user and reflect the status of pins **D0-D7** (corresponding to LED 0- LED 7). The LED assignments are shown in Table 1-7

Table 1-7: **LED Assignments and Corresponding I/O**

LED	After Configuration	Status Pin	Pin Number For Package Type		
			FG456	FF672	FF1152
LED 0	Available as user LEDs	D0	V17	AB7	AG9
LED 1		D1	V16	AC7	AH9
LED 2		D2	W16	AA7	AK6
LED 3		D3	Y16	AA8	AK7
LED 4		D4	Y7	AA19	AK28
LED 5		D5	W7	AA20	AK29
LED 6		D6	V7	AC20	AH26
LED 7		D7	V6	AB20	AG26

14. Program Switch

The active-low program switch, when pressed, grounds the program pin on the DUT.

15. Reset Switch (Active-Low)

The reset switch connects to the **INIT** pin on the DUT, allowing the user, after configuration, to reset the logic within the DUT. Before and during configuration of the DUT, the **INIT** pin has no function. After configuration, the **INIT** pin becomes a regular I/O. When pressed, this switch grounds the **INIT** pin.

Table 1-8 shows the **INIT** pin locations for the available DUT package types.

Table 1-8: **User Hardware and Corresponding I/Os**

Label	Pin Number For Package Type		
	FG456	FF672	FF1152
RESET (INIT)	W17	AD6	AL6

Note: Refer to the **readme.txt** file for implementation of this user pin.

16. DONE LED

The DONE LED indicates the status of the **DONE** pin on the DUT. This LED lights when **DONE** is high or if power is applied to the board without a part in the socket.

17. INIT LED

The INIT LED lights during initialization.

User Programmable Pins

18. Rocket I/O Transceiver Pins

Table 1-9 shows the TX/RX pin pair locations of the Rocket I/O multi-gigabit transceiver (MGT) for the available DUT package types.

Table 1-9: **MGT TX and RX Pin Pairs**

	Pin Pair	FG456 (P, N)	FF672 (P, N)	FF1152 (P, N)
TX	1	A8, A7	A10, A9	A16, A17
	2	AB14, AB13	AF16, AF15	AP20, AP21
	3	A14, A13	A16, A15	A20, A31
	4	AB8, AB7	AF10, AF9	AP16, AP17
RX	1	A9, A10	A11, A12	A15, A14
	2	AB15, AB16	AF17, AF18	AP19, AP18
	3	A15, A16	A17, A18	A19, A18
	4	AB9, AB10	AF11, AF12	AP15, AP14

19. SDRAM Pins

The system clock that enables proper communication between the SDRAM and the DUT is GCLK1P. Table 1-10 shows the system clock pin locations for the available DUT package types.

Table 1-10: **System Clock for SDRAM and DUT**

SDRAM Pin	FG456	FF672	FF1152
CLK	E12	D14	D18

Table 1-11 shows the pin mapping from the SDRAM to the available DUT package types.

Table 1-11: **SDRAM to FPGA Pin Mapping**

SDRAM Pin	FG456	FF672	FF1152
DQ0	T2	H3	N8
DQ1	T3	J4	N9
DQ2	T1	H4	N10
DQ3	R1	G4	M6
DQ4	R2	G3	N4
DQ5	N2	E3	M4
DQ6	U2	J3	N7
DQ7	N1	E4	M7
DQ8	Y1	N4	AB2
DQ9	M3	K4	W10
DQ10	W2	N3	AA3
DQ11	V1	M3	Y6
DQ12	V2	M4	AA2
DQ13	N4	L3	Y7
DQ14	M4	K3	W9
DQ15	N3	L1	W8
DQ16	K4	N2	L4
DQ17	H1	G1	M3
DQ18	K3	L2	L5
DQ19	K1	J1	P7
DQ20	K2	K1	L6
DQ21	J2	J2	P8
DQ22	H3	H2	M2
DQ23	J1	H1	N1
DQ24	F2	E2	K1
DQ25	G1	E1	L3
DQ26	F1	D1	K2

Table 1-11: **SDRAM to FPGA Pin Mapping *(Continued)***

SDRAM Pin	FG456	FF672	FF1152
DQ27	E1	C2	K4
DQ28	E3	C1	L7
DQ29	D2	B1	K5
DQ30	G2	F1	L1
DQ31	D1	A2	F5
A0	J4	R3	N3
A1	J3	T3	N2
A2	F4	P3	P2
A3	F3	V3	AA4
A4	G3	W2	AB3
A5	G4	Y3	W5
A6	K5	U1	AA1
A7	G5	W3	Y9
A8	P2	U3	AA6
A9	L2	T2	Y3
A10	H4	R2	R3
DQM0	P3	V4	W6
DQM1	M2	W1	AC1
DQM2	H5	P4	L8
DQM3	E4	V1	AA5
RAS#	J6	W4	W11
CAS#	M5	T4	R9
WE#	U3	U4	W7
CKE	L3	T1	Y1
BA0	K6	R4	R10
BA1	L4	P2	V11

Notes:

1. For proper operation of the SDRAM, use the LVCMOSDCI25 voltage standard on the FPGA pins.
2. CS # is tied to the jumper labeled **RAM_ENABLE/RAM_DISABLE**.
3. Disable the SDRAM when using the DUT pins as standard I/O pins.
4. The SDRAM is a Samsung K4S64323LF-S(D)G/S75. For information on its operation, see: http://www.samsungelectronics.com/semiconductors/DRAM/Mobile_SDRAM/64M_bit/K4S64323LF/ds_k4s64323lf-s(d)g_s.pdf

20. CPU Debug Pins

Figure 1-6 shows the location of the CPU debug pins on the debug connector.

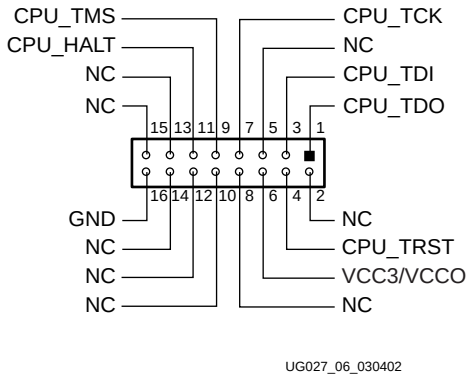

Figure 1-6: **CPU Debug Connector, 16-Pin Male**

Table 1-12 shows the CPU debug pin locations for the available DUT package types.

Table 1-12: **CPU Debug Pins**

Pin	FG456	FF672	FF1152
CPU_TDO	L20	AC8	AC31
CPU_TDI	L21	AE8	AC32
CPU_TCK	M21	W12	AA25
CPU_TMS	M20	AA12	AA26
CPU_HALT	M19	AB12	AD31
CPU_TRST	M18	AC12	AB29

For details on CPU debug pins, refer to **Appendix A, "RISCWatch and RISCTrace Interfaces."**

21. CPU Trace Pins

Figure 1-7 shows the location of the CPU trace pins on the trace connector.

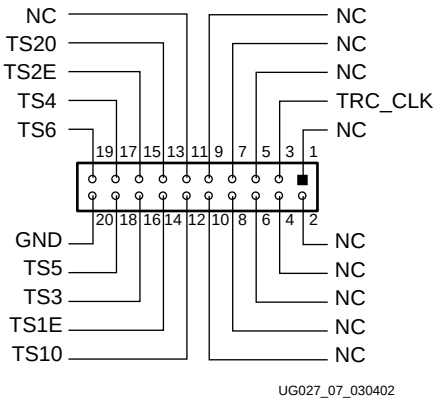

Figure 1-7: **CPU Trace Connector, 20-Pin Male**

Table 1-13 shows the CPU trace pin locations for the available DUT package types.

Table 1-13: **RISC Trace Pins**

Pin	FG456	FF672	FF1152
TS5	V22	AB24	AE34
TS3	V21	AC25	AF33
TS1E	V20	AD25	AF32
TS10	V19	AC24	AL33
TS6	W21	AB23	AD34
TS4	Y22	AC26	AE33
TS2E	Y21	AD26	AG33
TS20	AA22	AE26	AK31
TRC_CLK	AB21	AD23	AL34

For details on CPU debug pins, , refer to **Appendix A, "RISCWatch and RISCTrace Interfaces."**

22. RS232 Port Pins

Table 1-14 shows the RS232 port pin locations for the available DUT package types.

Table 1-14: **RS232 Port Pins**

Pin	FG456	FF672	FF1152
T1IN	Y2	AC1	AF10
T2IN	T4	AC2	AH10
R1OUT	U4	AD2	AE11
R2OUT	V4	AD1	AG10

23. Mictor Connector

Figure 1-8 shows the location of the pins on the Mictor connector.

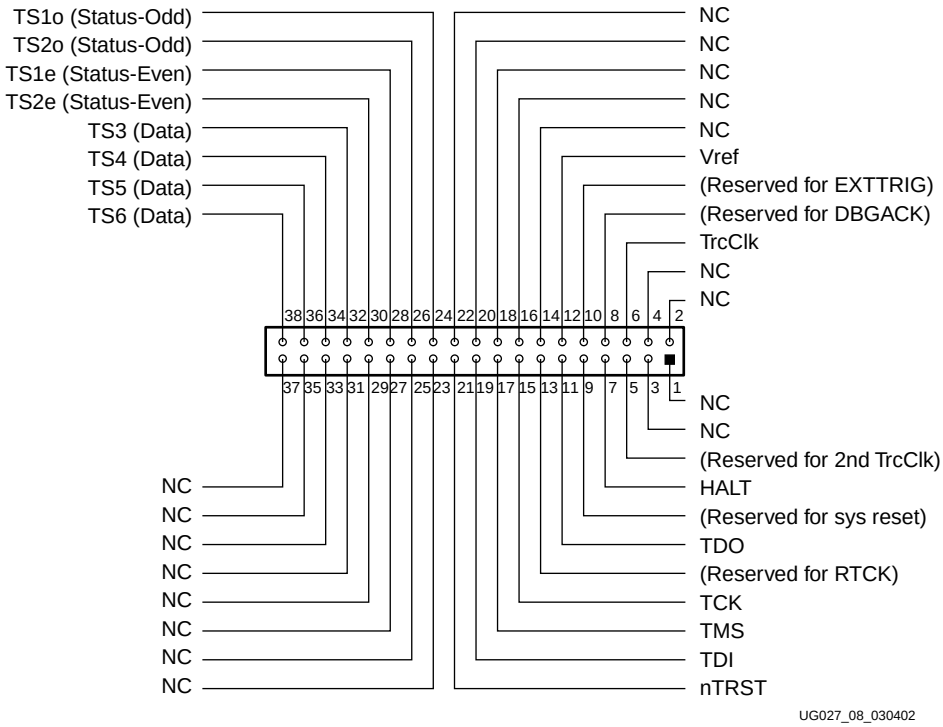

Figure 1-8: **38-Pin Mictor Connector**

Appendix A

RISCWatch and RISCTrace Interfaces

This appendix summarizes the interface requirements between the PPC405x3 and the RISCWatch and RISCTrace tools.

The requirement for separate JTAG and trace connectors is being replaced with a single Mictor connector to improve the electrical and mechanical characteristics of the interface. Pin assignments for the Mictor connector are included in the signal-mapping tables.

RISCWatch Interface

The RISCWatch tool communicates with the PPC405x3 using the JTAG and debug interfaces. It requires a 16-pin, male 2x8 header connector located on the target development board. The layout of the connector is shown in Figure A-1 and the signals are described in Table A-1. A mapping of PPC405x3 to RISCWatch signals is provided in Table A-2. At the board level, the connector should be placed as close as possible to the processor chip to ensure signal integrity. Position 14 is used as a connection key and does not contain a pin.

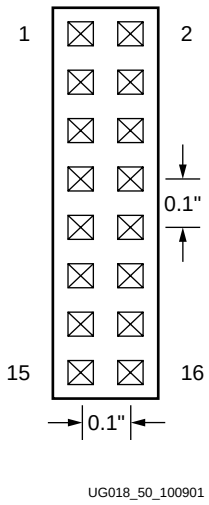

Figure A-1: **JTAG-Connector Physical Layout**

Table A-1: **JTAG Connector Signals for RISCWatch**

Pin	RISCWatch		Description
	I/O	Signal Name	
1	Input	TDO	JTAG test-data out.
2	No Connect	Reserved	
3	Output	TDI[1]	JTAG test-data in.
4	Output	TRST	JTAG test reset.
5	No Connect	Reserved	
6	Output	+Power[2]	Processor power OK
7	Output	TCK[3]	JTAG test clock.
8	No Connect	Reserved	
9	Output	TMS	JTAG test-mode select.
10	No Connect	Reserved	
11	Output	HALT	Processor debug halt mode.
12	No Connect	Reserved	
13	No Connect	Reserved	
14	KEY	No pin should be placed at this position.	
15	No Connect	Reserved	
16		GND	Ground

Notes:

1. A 10KΩ pull-up resistor should be connected to this signal to reduce chip-power consumption. The pull-up resistor is not required.
2. The +POWER signal, is provided by the board, and indicates whether the processor is operating. This signal does not supply *power* to the debug tools or to the processor. A series resistor (1KΩ or less) should be used to provide short-circuit current-limiting protection.
3. A 10KΩ pull-up resistor must be connected to these signals to ensure proper chip operation when these inputs are not used.

Table A-2: **PPC405x3 to RISCWatch Signal Mapping**

PPC405x3		RISCWatch		JTAG Connector Pin	Mictor Connector Pin
Signal	I/O	Signal	I/O		
C405JTGTDO[1]	Output	TDO	Input	1	11
JTGC405TDI	Input	TDI	Output	3	19
JTGC405TRSTNEG	Input	$\overline{\text{TRST}}$	Output	4	21
JTGC405TCK	Input	TCK	Output	7	15
JTGC405TMS	Input	TMS	Output	9	17
DBGC405DEBUGHALT[2]	Input	$\overline{\text{HALT}}$	Output	11	7

Notes:

1. This signal must be driven by a tri-state device using C405JTGTDOEN as the enable signal.
2. This signal must be inverted between the PPC405x3 and the RISCWatch.

RISCTrace Interface

The RISCTrace tool communicates with the PPC405x3 using the trace interface. It requires a 20-pin, male 2x10 header connector (3M 3592-6002 or equivalent) located on the target development board. The layout of the connector is shown in Figure A-2 and the signals are described in Table A-3. A mapping of PPC405x3 to RISCTrace signals is provided in Table A-4. At the board level, the connector should be placed as close as possible to the processor chip to ensure signal integrity. An index at pin one and a key notch on the same side of the connector as the index are required.

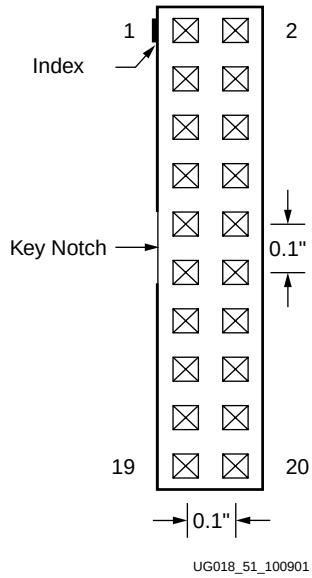

Figure A-2: **Trace-Connector Physical Layout**

Table A-3: **Trace Connector Signals for RISCTrace**

Pin	RISCTrace		Description
	I/O	Signal Name	
1	No Connect	Reserved	
2	No Connect	Reserved	
3	Output	TrcClk	Trace cycle.
4	No Connect	Reserved	
5	No Connect	Reserved	
6	No Connect	Reserved	
7	No Connect	Reserved	
8	No Connect	Reserved	
9	No Connect	Reserved	
10	No Connect	Reserved	
11	No Connect	Reserved	
12	Output	TS1O	Execution status.

Table A-3: **Trace Connector Signals for RISCTrace *(Continued)***

Pin	RISCTrace		Description
	I/O	Signal Name	
13	Output	TS2O	Execution status.
14	Output	TS1E	Execution status.
15	Output	TS2E	Execution status.
16	Output	TS3	Trace status.
17	Output	TS4	Trace status.
18	Output	TS5	Trace status.
19	Output	TS6	Trace status.
20		GND	Ground

Table A-4: **PPC405x3 to RISCTrace Signal Mapping**

PPC405x3		RISCTrace		Trace Connector Pin	Mictor Connector Pin
Signal	I/O	Signal	I/O		
C405TRCCYCLE	Output	TrcClk	Input	3	6
C405TRCODDEXECUTIONSTATUS[0]	Output	TS1O	Input	12	24
C405TRCODDEXECUTIONSTATUS[1]	Output	TS2O	Input	13	26
C405TRCEVENEXECUTIONSTATUS[0]	Output	TS1E	Input	14	28
C405TRCEVENEXECUTIONSTATUS[1]	Output	TS2E	Input	15	30
C405TRCTRACESTATUS[0]	Output	TS3	Input	16	32
C405TRCTRACESTATUS[1]	Output	TS4	Input	17	34
C405TRCTRACESTATUS[2]	Output	TS5	Input	18	36
C405TRCTRACESTATUS[3]	Output	TS6	Input	19	38