ML365 Virtex-II Pro QDR II SRAM (200 MHz) Memory Board User Guide

UG066 (v1.0) June 29, 2004

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The following table shows the revision history for this document.

	Version	Revision
06/29/04	1.0	Initial Xilinx Release

Preface

About This Guide

This document describes the design of the ML365 Virtex-II Pro™ QDR II SRAM (200 MHz) Memory Board, which connects a Virtex-II Pro FPGA to Quad Data Rate (QDR) memories.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction," describes the purpose of the ML365 board and provides its key features.
- Chapter 2, "Architecture," provides a block diagram of the memory board and describes the key components.
- Chapter 3, "Electrical Requirements," lists the electrical specifications for the memory board.
- Chapter 4, "Signal Integrity Recommendations and Simulations," provides information on termination, transmission lines, and duty cycles. It also gives the results of several IBIS simulations.
- Chapter 5, "Board Layout Guidelines," provides information on decoupling capacitors, ground signals, and PCB layout.
- Appendix 1, "Related Documentation," lists data sheet and external website references specific to the ML365 components.
- Appendix 2, "FPGA Pinout," provides the pinout of the Virtex-II Pro FPGA.
- Appendix 3, "Memory Board Schematics and Characterization Results" shows the schematics for the board.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging: http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records: http://support.xilinx.com/xlnx/xil_ans_browser.jsp

Resource	Description/URL
Application Notes	Descriptions of device-specific design techniques and approaches: http://support.xilinx.com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging: http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues: http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment: http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Italic font	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it *overlaps* the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

Introduction

Overview

The ML365 Virtex-II Pro QDR II SRAM Memory Board provides a communications platform between a Virtex-II Pro FPGA and high-speed, quad data-rate (QDR) memories with operating speeds up to 200 MHz. The ML365 has three major functions:

- Test and verify the interoperability of Virtex-II Pro devices with high-speed QDR II SRAM memories
- Serve as a development platform for Xilinx and its customers to use for building memory interfaces
- Provide a means by which Xilinx can demonstrate high-speed QDR II SRAM memory interoperability

This document describes the functional blocks within the ML365. It also provides various recommendations and requirements for usage of the board, including electrical requirements, logic analyzer requirements, and signal integrity issues. Simulation results using IBIS also are included.

Figure 1-1 shows a simplified block diagram of the ML365 memory interfaces.

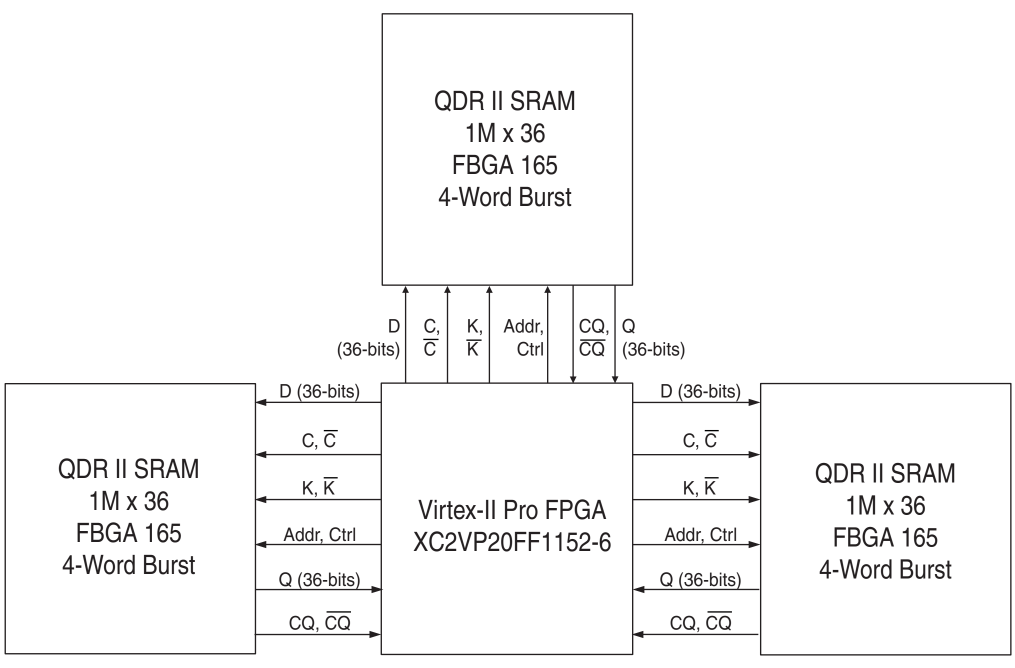

Figure 1-1: **Simplified Block Diagram of Memory Board Interface**

The ML365 demonstrates a 36-bit interface to a 36 MByte, 200 MHz QDR II SRAM component. There are three independent 36-bit interfaces on the board; one on the left side of the FPGA, the second on the right side of the FPGA, and the third on top of the FPGA.

Features

The key features of the ML365 are summarized as follows:

- One Virtex-II Pro FPGA (XC2VP20FF1152)
- Three QDR II SRAM Components (Samsung K7R323684M or NEC UPD44165364F5)
  - 18 MBytes
  - 36-bit Data interface
- Three separate controllers for each 36-bit memory interface
- Characterized 200 MHz clock operation for interfaces A (interface to the FPGA on the right side, U5) and B (interface to the FPGA on the left side, U11)
- One additional memory interface on the top banks of the FPGA (interface C, U12)

Chapter 2

Architecture

This chapter provides functional descriptions of the major blocks within the ML365 board design. For additional detailed information on the design, refer to the schematics, which are located at http://www.xilinx.com/bvdocs/userguides/ug066.zip.

ML365 Board Block Diagram

Figure 2-1 shows a block diagram of the ML365 board. Refer to "Block Descriptions" for additional information on the major blocks.

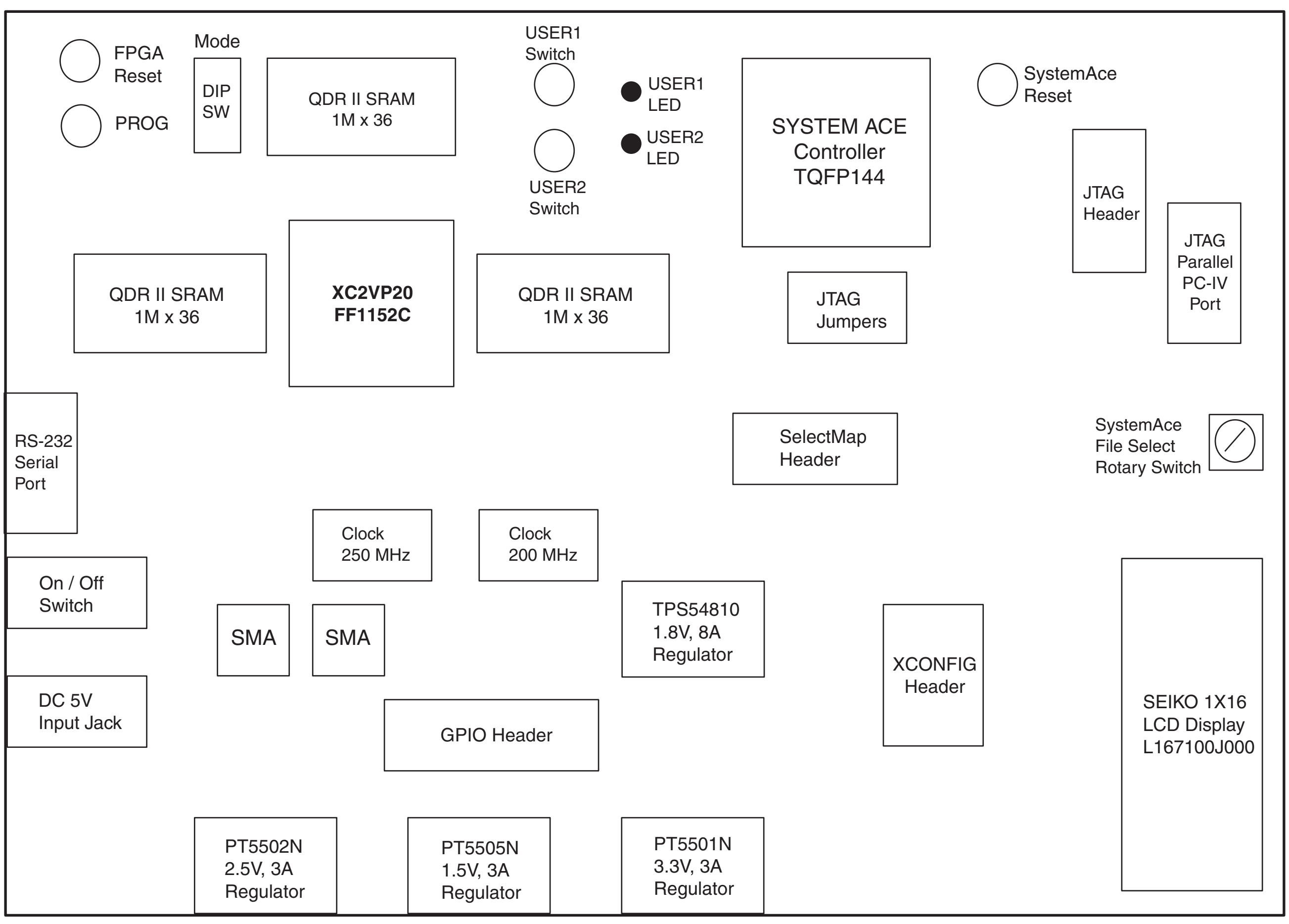

Figure 2-1: **ML365 Board Block Diagram**

Block Descriptions

This section describes the major blocks of the ML365 board.

FPGA

The ML365 uses a Xilinx XC2VP20FF1152C-6 Virtex-II Pro device. This device is packaged in a 1152-pin BGA package with a -6 speed grade. Refer to Appendix 2, “FPGA Pinout,”for a complete pinout of the Virtex-II Pro device.

Memories

The ML365 board supports three types of memories in two speed grades.

QDR II SRAM (U5, Banks 6 and 7)

The QDR II SRAM component connected to FPGA I/O banks 6 and 7 is a 165-pin, 200 MHz Samsung K7R323684M or NEC UPD44165364F5 SRAM in a Ball Grid Array package. This component has a 36-bit wide data interface.

QDR II SRAM (U11, Banks 2 and 3)

The QDR II SRAM component connected to FPGA I/O banks 2 and 3 is a 165-pin, 200 MHz Samsung K7R323684M or NEC UPD44165364F5 SRAM. This component has a 36-bit wide data interface.

QDR II SRAM (U12, Banks 0 and 1)

The QDR II SRAM component connected to FPGA I/O banks 0 and 1 is a 165-pin, 250 MHz Samsung K7R323684M or NEC UPD44165364F5 SRAM. This component has a 36-bit wide data interface.

RS232 (J5)

The ML365 board provides an RS232 serial interface using a Maxim MAX3316ECUP device. The maximum speed of this device is 460 Kb/s. The RS232 interface is accessible through a male DB9 serial connector.

Clocks

The ML365 board has 200 MHz and 250 MHz LVPECL (2.5 V) clock oscillators on board. It also has two SMA connectors for external differential clock inputs.

200 MHz LVPECL Clock (Y1)

The LVPECL clock is an Epson EG-2121CA-200 MHz oscillator with a differential output. The oscillator runs at 200 MHz ±100 PPM with an operating voltage of 2.5 V ±5%. It is terminated at the FPGA with a 50 ohm resistor. FPGA pins AH17 and AJ17 in Bank 4 serve as the OSC_200M_N and OSC_200M_P inputs, respectively.

250 MHz LVPECL Clock (Y2)

The LVPECL clock is an Epson EG-2121CA-250 MHz clock oscillator with a differential output. This oscillator runs at 250 MHz ±100 PPM with an operating voltage of 2.5 V ±5%.

FPGA pins AK17 and AL17 in Bank 4 serve as the OSC_250M_N and OSC_250M_P inputs, respectively.

SMA Clock Connectors

Two SMA connectors are provided for the input of an off-board differential clock. The traces from the SMAs are run as a pair to the FPGA where they are terminated with a 50 ohm resistor. AK18 serves as the EXTCLK1_P input, and AL18 serves as the EXTCLK1_N input for the SMA connector pair.

User I/Os

This subsection describes the devices that connect to the User I/Os of the ML365 board.

GPIO (P19)

The ML365 board contains 16 General-Purpose I/Os (GPIOs) that are accessible through a 2 x 16 .100" pin header (P19). The odd-numbered pins on each header are connected to an FPGA pin, and the even-numbered pins on each header are connected to GND (refer to Table 2-1). The GPIO header pins are accessed through I/Os in Bank 0. The header pins each have a pull-down resistor of 51 ohms.

Table 2-1: **GPIO Header Pins**

GPIO Header Pin #	FPGA I/O Pin	GPIO Header Pin # Ground Connections
G1	AL13	G2
G3	AL12	G4
G5	AD16	G6
G7	AE16	G8
G9	AM14	G10
G11	AM13	G12
G13	AF16	G14
G15	AG16	G16
G17	AH15	G18
G19	AJ15	G20
G21	AD17	G22
G23	AE17	G24
G25	AH16	G26
G27	AJ16	G28
G29	AK16	G30
G31	AF17	G32

DIP Switch (SW3)

One 3-position DIP switch (SW3) is connected to the FPGA I/O as shown in Table 2-2. These switches are used to set the FPGA configuration mode pins M0, M1, and M2.

Table 2-2: **DIP Switch Connections**

DIP Switch Input	FPGA I/O Pin #
DIP1	AF26 (M0)
DIP2	AE26 (M1)
DIP3	AE25 (M2)

LEDs

Eleven surface-mounted blue LEDs are installed as status indicators. Refer to Table 2-3, Table 2-4, and Table 2-5.

Table 2-3: **Power-On Status**

Status Indication	FPGA I/O Pin #
5.0V on	D9
2.5V on	D7
3.3V on	D5
1.8V on	D8
1.5V on	D6

Table 2-4: **FPGA Configuration Status**

Configuration INIT	D3
Configuration DONE	D4

Table 2-5: **SystemAce Configuration Status**

System Ace LEDs	Error	D2
	Status	D1
User LEDs	USER1	AF15
	USER2	AE15

Push Buttons

The ML365 board contains five momentary push buttons. Their functions are as follows:

- Program the FPGA
- Reset FPGA
- Reset SystemAce
- USER1
- USER2

Rotary Switch

The ML365 board contains one eight-position rotary switch used to select the SystemAce file address. One of eight configuration file images is loaded from the Compact Flash card present in the socket.

Power On or Off Slide Switch

The power on or off slide switch is a DPST slide switch used to apply 5V input power to the board.

Jumper Settings

Table 2-6 lists the jumper settings for the complete PCB.

Table 2-6: **Jumper Settings**

Pin #	Purpose	Jumper Position	
		1 - 2	**2 - 3**
P6	QDR II U5 DLL enable	DLL enable	DLL bypass
P7	QDR II U5 ZQ select	Minimum Z mode	0.2RQ = 50 ohm
P20	QDR II U11 DLL enable	DLL enable	DLL bypass
P21	QDR II U11 ZQ select	Minimum Z mode	0.2RQ = 50 ohm
P22	QDR II U12 DLL enable	DLL enable	DLL bypass
P23	QDR II U12 ZQ select	Minimum Z mode	0.2RQ = 50 ohm
P2	System Ace	On = Disable after reset Off = Enable after reset	

Grounded I/Os

Unused I/Os are connected to GND in all FPGA banks. This was done to improve power dissipation and SSO ground bounce. Users **must not** drive any unused I/Os that are connected to GND.

Liquid Crystal Display

The Seiko L167100J000 Liquid Crystal Display (LCD) is a 5V, 1-line X16 character display without a backlight. The LCD is connected to the PCB using two rows of 1 x 16 pin SIP headers placed 31 mm. apart. The LCD interfaces uses bank 5 of the FPGA. The LCD pin descriptions and FPGA pinouts are listed in Table 2-7.

Table 2-7: **LCD Pin Descriptions and PFGA Connections**

Symbol	Function	FPGA Pin #
V_{SS}	Power supply (GND)	N/A
V_{DD}	Power supply (+5V)	N/A
V_O	Contrast adjustment	N/A
RS	Register selection	AF22
R/W	Read / Write selection	AG22
E	Read / Write enable	AE22
DB (0-7)	Data bus	AF25 (DB0), AL28, AM28, AE24, AF24, AG25, AH25, AK27 (DB7)

The information needed to control the LCD panel is provided in the following figures and tables. Figure 2-2 shows the LCD write timing diagram, and Table 2-8 lists the LCD write timing parameters.

Table 2-9 shows the instruction codes for the LCD. Figure 2-3 shows the Display Initialization Sequence, and Figure 2-7, the LCD panel character set. For complete information, refer to the manufacturer's data sheet.

Write Cycle for the LCD

Reading from the LCD panel memory is not implemented on this demonstration board.

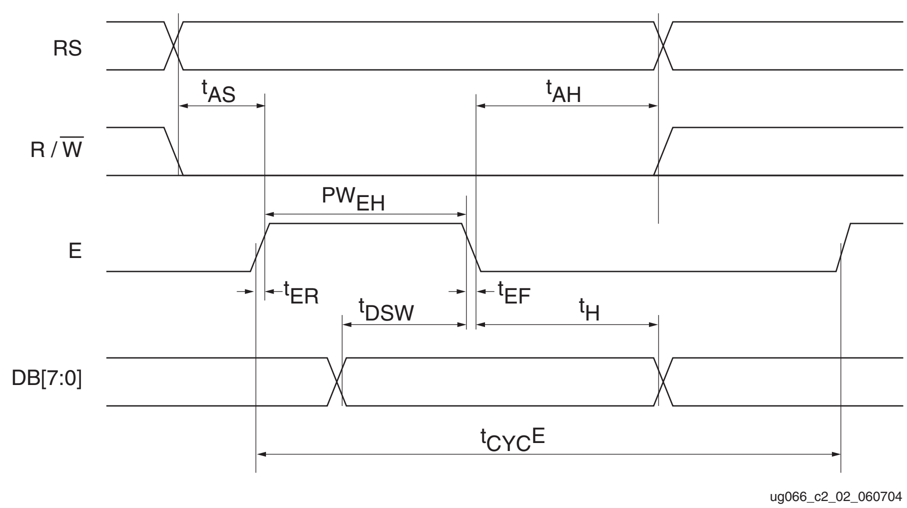

Figure 2-2: **LCD Write Timing Diagram**

Table 2-8: **LCD Write Timing Parameters**

Item	Symbol	Standard		Unit
		Minimum	Maximum	
Enable cycle time	$t_{CYC}E$	500		ns
Enable pause width / High Level	PW_{EH}	230		ns
Enable rise and fall time	t_{ER}, t_{EF}		20	ns
Address setup time / RS, R/W - E	t_{AS}	40		ns
Address hold time	t_{AH}	10		ns
Data setup time	t_{DSW}	80		ns
Data hold time	t_H	10		ns

Display Commands

Table 2-9 provides display commands or instruction code for the LCD. Refer to the Table Notes for additional information.

Table 2-9: **Instruction Code**

Instruction	Code										Description (Notes 2 and 3)	Maximum Execution Time (Note 1)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets Data Display RAM (DDR) address 0 in the address counter.	82 µs - 1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DDR address 0 in the address counter. Also returns display being shifted to original position. DDR contents remain unchanged.	40 µs - 1.6 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40 µs – 1.64 ms
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 µs

Table 2-9: **Instruction Code**

Instruction	Code										Description (Notes 2 and 3)	Maximum Execution Time (Note 1)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DDR contents.	40 µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L), and character fonts (F).	40 µs
Set CG RAM Address	0	0	0	1	A_{CC}						Sets Character Generator RAM (CGR) address. CGR data is sent and received after this setting.	40 µs
Set DD RAM Address	0	0	1	A_{DD}							Sets DDR address. CGR data is sent and received after this setting.	40 µs
Read Busy Flag and Address	0	1	BF	A_C							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1 µs
Write Data to CG or DDR	1	0	Write Data								Writes data into DDR or CGR.	40 µs

*Not applicable

Notes:

1.Maximum execution time is when f_{cp} or f_{osc} is 250 kHz. Execution time changes when frequency changes.

2.DD RAM: Display data RAM

CG RAM: Character generator RAM

A_{CG}: CG RAM address

A_{DD}: DDR address - corresponds to cursor address

A_C: Address counter used for both DDR and CG RAM address

I/D = 1: Increment or I/D = 0: Decrement

S = 1: Display shift or S = 0: No Display shift

D = 1: Display ON or D = 0: Display OFF

C = 1: Cursor ON or C = 0: Cursor OFF

B = 1: Blink ON or B = 0: Blink OFF

S/C = 1: Display shift or S/C = 0: Cursor move

R/L = 1: Shift to the right or R/L = 0: Shift to the left

DL = 1: 8 bits or DL = 0: 4 bits

N = 1: 2 lines

F = 0: 5 x 7 dots

BF = 1: Internally operating or BF = 0: Can accept instruction

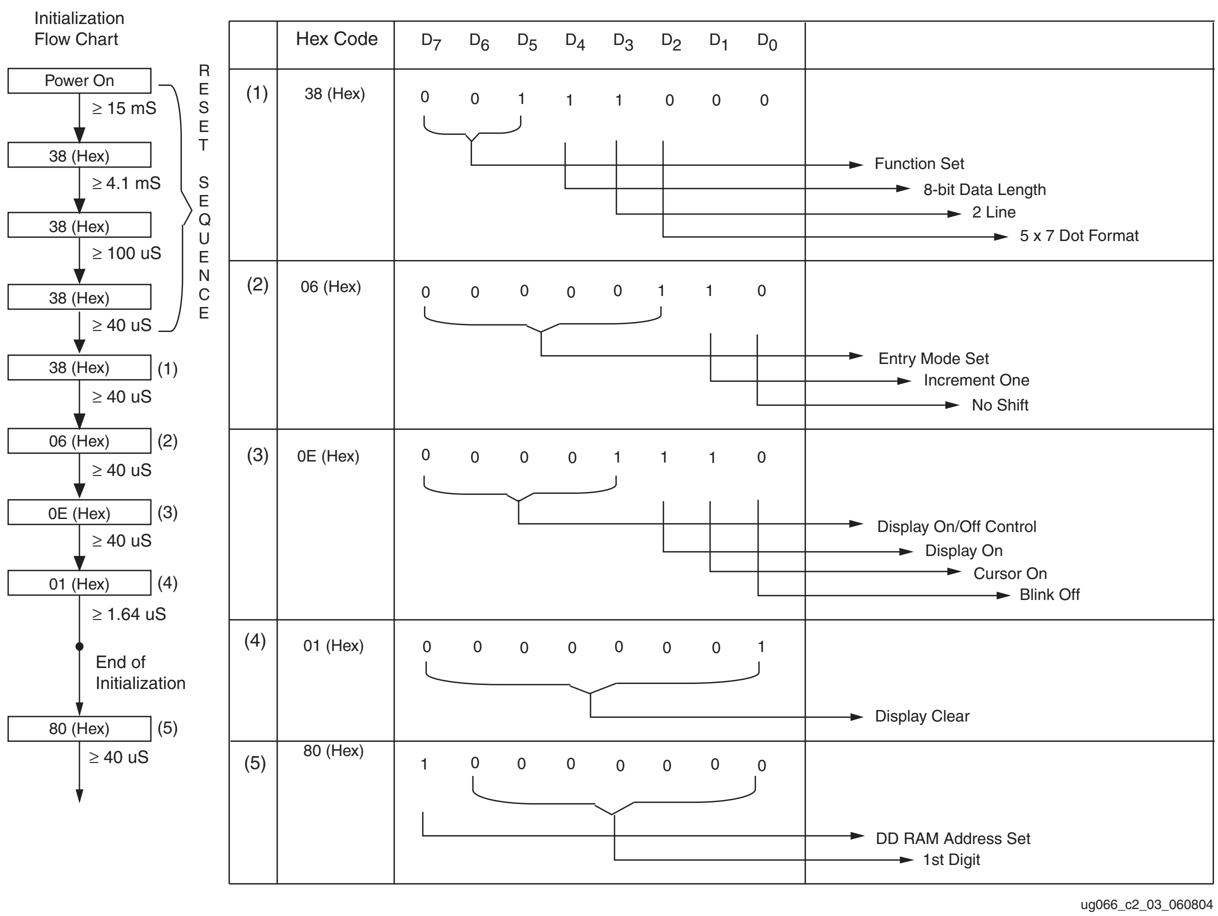

Figure 2-3: **Display Initialization Sequence**

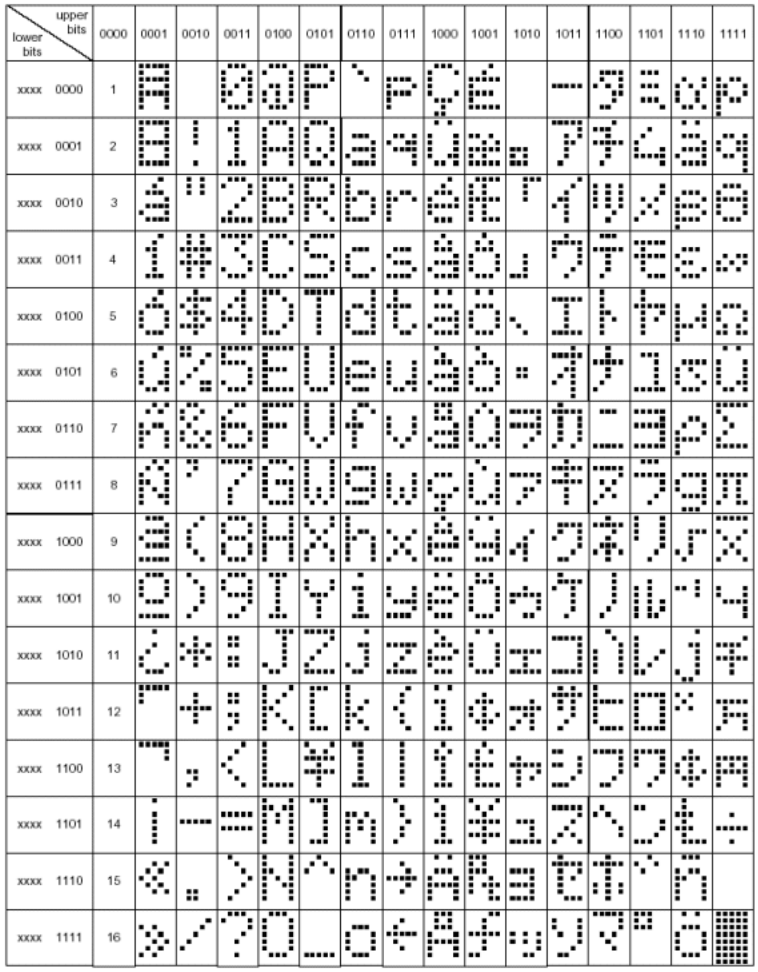

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Figure 2-4: **LCD Panel Character Set**

Power

Power Distribution

The ML365 board uses a 5V +/- 10% input voltage source to generate all the on-board voltages (1.5V, 1.8V, 2.5V, and 3.3V).

Input Voltage

The input voltage is specified at 5 V @ 6.5 A. The recommended power supply is a CUI Inc. DTS050650UTC-PSP-SZ. The jack used is a 2 mm. barrel jack. The slide switch turns the power on or off. Four regulators on the board provide different voltages required by various components on the board.

3.3 V Generation

The Texas Instruments PT5501N voltage regulator generates the 3.3 V @ 3 A power. This power regulator is packaged in a 5-pin, thermally-efficient copper case that is solderable, and provides the auxiliary supply for some of the FPGA I/Os (V_{CCO}).

2.5 V Generation

The Texas Instruments PT5502N voltage regulator generates the 2.5 V @ 3 A power. This power regulator is packaged in a 5-pin, thermally-efficient copper case that is solderable. It supplies the clock oscillators, System Ace device, LCD Display unit, and for some of the FPGA I/Os (V_{CCAUX}).

1.8 V Generation

The Texas Instruments TSP54810 voltage regulator generates the 1.8 V @ 8 A power. This power regulator has a thermally-enhanced 28-pin TSSOP package, and supplies the memory devices.

1.5 V Generation

The Texas Instruments PT5505N voltage regulator generates the 1.5 V @ 3 A power. This power regulator is packaged in a 5-pin, thermally-efficient copper case that is solderable, and provides the core voltage to the FPGA (V_{CCINT}).

FPGA Configuration

The demonstration board FPGA programming options are very flexible (refer to the following five configuration modes). For a detailed explanation of the basic Virtex-II configurations, refer to the Virtex-II Platform FPGA User Guide. The five Virtex-II configuration modes are:

- Master Serial mode (not used on QDR II Demo Board)
- Slave Serial / SystemAce mode (QDR II Demo Board default)
- Master SelectMap mode
- Slave SelectMap mode
- JTAG mode

Selecting the Configuration Mode

The FPGA programming modes are set with the mode lines (M0, M1, M2) by means of the 3-pole DIP switch (SW5). Table 2-10 shows the programming modes.

Table 2-10: **Configuration Modes Supported on the QDR II SRAM Demonstration Board**

Mode	M2	M1	M0	CCLK	Data Width	Data DOUT
Master Serial(1)	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
SystemAce(2)	1	1	1	N/A	N/A	N/A
Master SelectMap	0	1	1	Out	8	No
Slave SelectMap	1	1	0	In	8	No
JTAG	1	0	1	N/A	1	No

1. Not used on QDR II Demonstration Board.
2. SystemAce is a Slave Serial configuration mode, and is the default for the QDR II Demonstration Board.

An LED on the Done pin adds a visual aid to detect a good FPGA configuration. If the LED is “on”, the FPGA configuration is complete.

Serial Configuration

The Virtex-II is programmable in serial mode in one of two ways:

Master Serial Mode

This mode is not used in the QDR II Demonstration Board.

Slave Serial Mode

In Slave Serial Mode, the FPGA CCLK pin is driven by an external source. The FPGA is configured by loading one bit per CCLK cycle in the DIN pin.

SystemAce Configuration (Default Mode)

SystemAce is a Slave Serial configuration mode, and is the default mode for the QDR II Demonstration Board.

If the SystemAce Controller (U2) detects a Compact Flash card present in socket P2, it attempts to load a configuration file from the Compact Flash card into the FPGA. Table 2-11 shows the allowable correct jumper positions.

Table 2-11: **Jumper Positions for SystemAce Configuration**

Pins Jumpered	Function
P1.4 to P113	TCK from SystemAce connected to TCK input of the FPGA
P1.7 to P114	TMS from SystemAce connected to TMS input of the FPGA
P1.5 to P1.6	SystemAce TDO connected to the TDI input of the FPGA

1. Recommended SW5 switch setting for the SystemAce mode is 111; refer to Table 2-10.

SelectMap Configuration

The Virtex-II FPGA is programmable using SelectMap, a parallel configuration mode. In this mode, two possibilities of programming exist:

- Master Mode: FPGA delivers the CCLK download clock
- Slave Mode: FPGA must receive the CCLK clock from the external device

The demonstration board can be programmed in both modes using the SelectMap connectors; P99 and P111. The FPGA on the demonstration board can be programmed in slave mode using a MultiLINX cable, or in Master mode when an external device is plugged into these connectors.

The SelectMap connector P99 carries FPGA bits [7:0]. When SelectMap is not used, the SelectMap connector pins can also be used as normal I/O.

Figure 2-5 shows the layout of the SelectMap connectors P99 and P111.

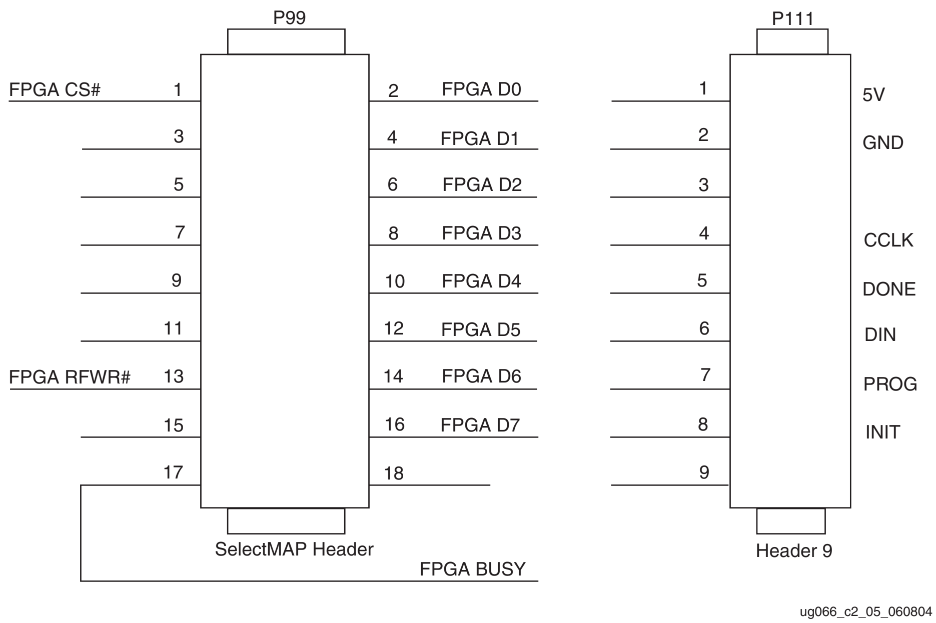

Figure 2-5: **SelectMap Connectors P99 and P111**

JTAG Configuration

The Virtex-II FPGA is programmable in JTAG mode. The JTAG chain contains two on-board devices (FPGA and SystemAce).

The JTAG input connector is P103, wired to the TSTCFG pins of the SystemAce Controller U2. The JTAG input connector is the start of the JTAG chain. The configuration output port of the SystemAce Controller is wired to the FPGA via P1, P113, and P114 pins as shown in Table 2-11. The FPGA can be isolated from the JTAG chain by removing the jumper blocks from the P1 pins as specified in Table 2-11. Figure 2-6 shows how to build the JTAG chain, and Table 2-12 shows the connections for the JTAG connector P1.

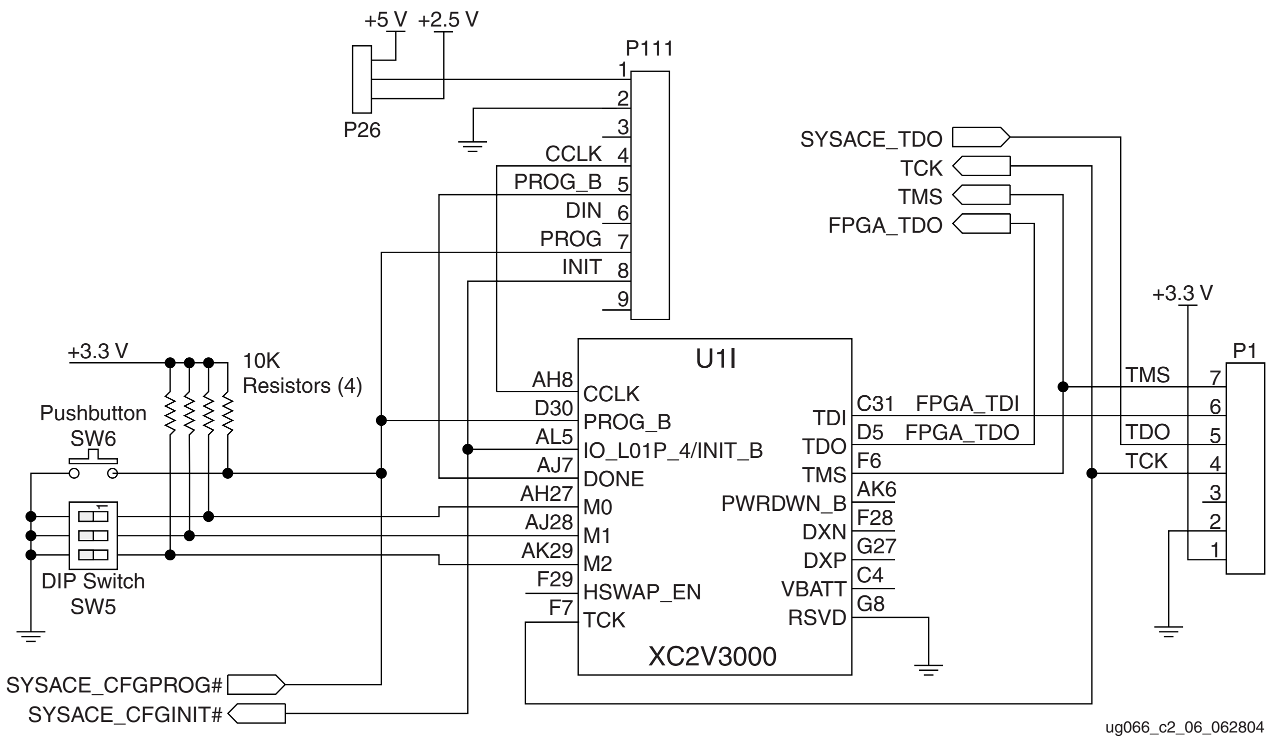

Figure 2-6: **SystemAce and JTAG Connectors**

Table 2-12: **JTAG Connector Pins (P1)**

Pin Number	Function
1	3.3 Volts
2	GND
3	N/C
4	TCK
5	TDO
6	FPGA_TDI
7	TMS

Figure 2-7 shows the JTAG connector P103.

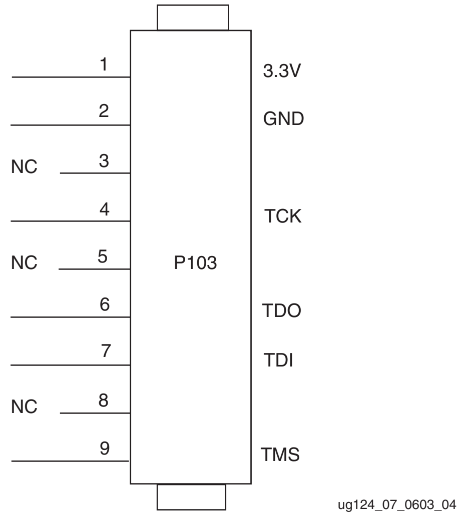

Figure 2-7: **JTAG I/O Connector P103**

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Chapter 3

Electrical Requirements

Power Consumption

Table 3-1 lists the operating voltages, maximum currents, and power consumption used by the ML365 board devices. Refer to Appendix 1, "Related Documentation," for more information on the source material.

Table 3-1: **ML365 Power Consumption**

Device	Quantity	Voltage (V)	Current (mA)	Power (W)	Source
Total Available Power					
Power Supply	1	5	6500	32.5	
FPGA Power (Based on Design)					
FPGA (XC2VP20-6 FF1152)	1			6.87	Power Estimator Tool
Board Power					
Static Power-on Termination Resistors (Split 100 ohms)	402 [1]	1.8	7236	13	*Virtex-II Pro User Guide*
QDR SRAM (108-bit interface)	3	1.8	800	4.32	Samsung QDR SRAM Data Sheet
200 MHz LVPECL Clock Oscillator	2	4	80	0.64	EPSON EG2121CA Data Sheet
16-pin GPIO Header	2	2.6	160	.42	Average 10 mA * 16 pins
LEDs	11	—	—	0.5	LED Circuits
DIP Switch	1	—	—	.06	Eight 3.3 kohm pullups
RS232 Serial Port	1	3.3	40	0.13	Maxim MAX3316ECUP Data Sheet
LCD	—	2.5 / 3.3	100	0.33	LCD Datasheet
System Ace Compact Flash	—	2.5 / 3.3	150	.049	SystemACE Datasheet
Worst Case Power Consumption:				**23.0**	

1. The resistor count is distributed as follows per devices, and multiplied by the number of devices (3):
   - data bus D: 36 (x2 (split termination))
   - clocks: CQ, C, K: 6 (x2 (split termination))
   - address bus A: 18 (x2 (split termination))
   - R_n_int: 1 (x2 (split termination))
   - Control signals: 6 (x2 (split termination))

FPGA Internal Power Budget

The following tables show the power consumption values inside the FPGA based on the complete QDR design. These results are derived using the Xilinx Power Estimator tool. Block Select RAM, Block Multiplier, Processor, and MGT Power tables are not included in this section as they are not used in this application.

- Table 3-2, "XC2VP20FF1152 Estimated Power Consumption," page 30
- Table 3-3, "XC2VP20FF1152 Temperature Specifications," page 30
- Table 3-4, "Device Quiescent Power," page 30
- Table 3-5, "CLB Logic Power," page 31
- Table 3-6, "Digital Clock Manager Power," page 31
- Table 3-7, "Input/Output Power," page 31

Table 3-2: **XC2VP20FF1152 Estimated Power Consumption**

Parameter	Value	Units
Total Estimated Design Power	6500	mW
Estimated Design VCC_{INT} 1.5 V Power	3500	mW
Estimated Design VCC_{AUX} 2.5 V Power	417	mW
Estimated Design VCCO 3.3 V Power	100	mW
Estimated Design VCCO 2.5 V Power	173	mW
Estimated Design VCCO 1.8V Power	7859	mW
Estimated Design VCCO 1.5 V Power	0	mW
Estimated Design VCCO 1.2 V Power	0	mW

Table 3-3: **XC2VP20FF1152 Temperature Specifications**

Parameter	Value	Units
Ambient Temperature	25	°C
Air Flow	0	LFM
Junction Temperature	107	°C

Table 3-4: **Device Quiescent Power**

VCC_{INT} Subtotal (mW)	VCC_{AUX} Subtotal (mW)
450	417

Table 3-5: **CLB Logic Power**

Name	Frequency (MHz)	Total Number of CLB Slices	Total Number of Flip/Flop or Latches	Total Number of Shift Register LUTs	Total Number of Select RAM LUTs	Average Toggle Rate %	Amount of Routing Used	VCC_{INT} Subtotal (mW)
User Module 1	200	1299	1302	0	544	40%	High	1220
User Module 2	0	0	0	0	0	0%	Low	0
							Total	**1220**

Table 3-6: **Digital Clock Manager Power**

Name	Clock Input Frequency (MHz)	DCM Frequency Mode	VCC_{INT} Subtotal (mW)
User DCM 1	200	Low	6
User DCM 2	200	Low	6
		Total	**12**

Table 3-7: **Input/Output Power**

Name	Frequency (MHz)	I/O Standard Type	Total Number of Inputs	Total Number of Outputs	Average IOB Toggle Rate %	Average Output Enable Rate %	Average Output Load (pF)	IOB Registers	VCC_{INT} Subtotal (mW)	VCCO Subtotal (mW)
CLK200	200	LVDS_25	1	0	100%	100%	15	DDR	2	8
CLK200_N	200	LVDS_25	1	0	100%	100%	35	DDR	2	8
GPIO	200	LVDCI_25 (50)	0	16	10%	100%	35	DDR	14	157
D/mem_R_n_ext	200	HSTL_II (1.8v)	0	111	25%	100%	35	DDR	11	752
Q/mem_R_n_int	200	HSTL_II_DCI (1.8v)	111	0	25%	0%	35	DDR	258	3662
Mem Addr/Control	200	HSTL_II_DCI (1.8v)	0	66	10%	100%	35	SDR	18	2431
Mem K/C	200	HSTL_II_DCI (1.8v)	0	12	25%	100%	35	DDR	13	536
Mem CQ	200	HSTL_II_DCI (1.8v)	6	0	25%	0%	35	DDR	25	260
A_R/W, C_R/W	200	HSTL_II (1.8v)	0	12	10%	100%	35	SDR	1	41
								Total	**344**	**7859**

Chapter 4

Signal Integrity Recommendations and Simulations

This chapter provides the following information:

- Summary of the termination schemes for various signals (refer to "Termination and Transmission Line Summaries," page 33).
- IBIS simulations and duty cycle measurements (refer to "IBIS Simulations," page 35).

Termination and Transmission Line Summaries

Table 4-1 summarizes the terminations for the three QDR II SRAM components for both the FPGA and memory.

Table 4-1: **QDR SRAM Terminations**

Number	Signal	Drivers at the FPGA	Termination at FPGA	Termination at Memory
1	Data (D)	HSTL_18_C2_DCI	No termination	50 ohm pull-up to 0.9 V
2	Data (Q)	HSTL_18_C1	No termination	No termination
3	Data Strobe (CQ, $\overline{\text{CQ}}$)	HSTL_18_C2	50 ohm pull-up to 1.3V	50 ohm pull-up to 0.9 V
4	Clock (K, $\overline{\text{K}}$)	HSTL_18_C2	50 ohm pull-up to 1.3V	No termination
5	Address (A)	HSTL_18_C2	No termination	100 ohm parallel split termination pull-up to 1.8 V
6	Control ($\overline{\text{R}}$, $\overline{\text{W}}$, $\overline{\text{BW}}$)	HSTL_18_C2	No termination	100 ohm parallel split termination pull-up to 1.8 V

Terminations and Transmission Lines for QDR Components

Data and Clock Signals (D, Q, CQ, $\overline{\text{CQ}}$, and CLK)

For the QDR signals included in the data bus D, the terminations consist of a 50 ohm parallel termination pulled-up to 0.9 Volts. As DCI is used in the FPGA, no termination is required.

Use 50 ohm transmission lines with less than ±1% tolerance on the transmission line impedance. The recommendations for the transmission line lengths are:

- All the data and clock signals are point-to-point from the FPGA to each QDR component. The flight time of the signals going to one individual QDR II SRAM component need to be matched with respect to the other signals with a ±2% tolerance.
- All signals going to the memory component have been matched within a 200 ps. window. This timing requirement includes the FPGA internal package skew (available in Appendix 2, "FPGA Pinout") and the skew between the ball of the FPGA to the resistor pack as well as the length of the actual trace.
- The IBIS simulation provided in "IBIS Simulations," page 35 have been processed using the actual PCB characteristics, from the PCB layout tool and the memory and FPGA driver IBIS models.

Address and Control Signals (A, $\overline{\text{R}}$, $\overline{\text{W}}$, $\overline{\text{BW}}$)

For the address and control signals, no termination is required at the FPGA. At memory, a 50 ohm resistor pulled up to 0.9 V is used to terminate the transmission line.

Use 50 ohm transmission lines with ± 5% tolerance from the FPGA to all the memory components. The recommendations for the transmission line lengths are as follows:

- All the data and clock signals are point-to-point from the FPGA to each QDR component. The flight time of the signals going to one individual QDR II SRAM component need to be matched with respect to to the other signals with a ± 2% tolerance.
- All signals going to the memory component have been matched within a 200 ps. window. This timing requirement includes the FPGA internal package skew (available in Appendix 2, "FPGA Pinout") and the skew between the ball of the FPGA to the resistor pack as well as the length of the actual trace.
- The IBIS simulation provided in "IBIS Simulations," page 35 have been processed using the actual PCB characteristics, from the PCB layout tool and the memory and FPGA driver IBIS models.

IBIS Simulations

This section summarizes the various simulations run on the ML365 Board using IBIS. The simulations have been completed using the Cadence SPECCTRAQuest tool. These simulations account for specific PCB characteristics, ensuring high fidelity waveforms. For each waveform presented in this section, the results of the test conditions are provided.

The simulations have been divided into the following categories:

Data Signal Simulations

- Data signals from the FPGA to the QDR II SRAM, U11, Component B, Data D, Bit 4
  - Typical Case
  - Slow Weak Case
  - Fast Strong Case
  - Eye Diagram
- Data signals from the QDR II SRAM to the FPGA, U11, Component B, Data Q, Bit 4
  - Typical Case
  - Slow Weak Case
  - Fast Strong Case
  - Eye Diagram

Clock Signal Simulations

- Clock signals from the FPGA to the QDR II SRAM, U11, Component B
  - Typical Case
  - Slow Weak Case
  - Fast Strong Case

Address and Control Signal Simulations

- Address and control signals from the FPGA to the QDR II SRAM Memory Component
  - QDR II SRAM, U11, Component B, Address Bit 4 (Typical, Slow / Weak, and Fast / Strong Cases)

Notes on the Simulation Results

The provided waveforms show the results of each simulation. The signals in these waveforms are color-coded:

- Purple signal: Typical driver
- Green signal: Fast / strong driver
- Blue signal: Slow / weak driver

For the eye diagram, the typical drivers are used.

Data Signal Simulations

All of the data signal simulation use the following test conditions for typical, slow / weak, and fast / strong cases:

- Topology for data signals: 50-ohm transmission lines
- Transmit:
  - At the memory: 100-ohm parallel split termination pulled-up to V_{dd} = 1.8 V (equivalent to a 50-ohm termination pulled up to V_{ref} = 0.9V)
  - At the FPGA: HSTL_18_C2 drivers
- Receive:
  - At the FPGA: HSTL_18_C1_DCI receivers (internal termination, VRP, and VRN pins connected to reference resistors)

Figure 4-1 shows signal terminations for transmitted and received data.

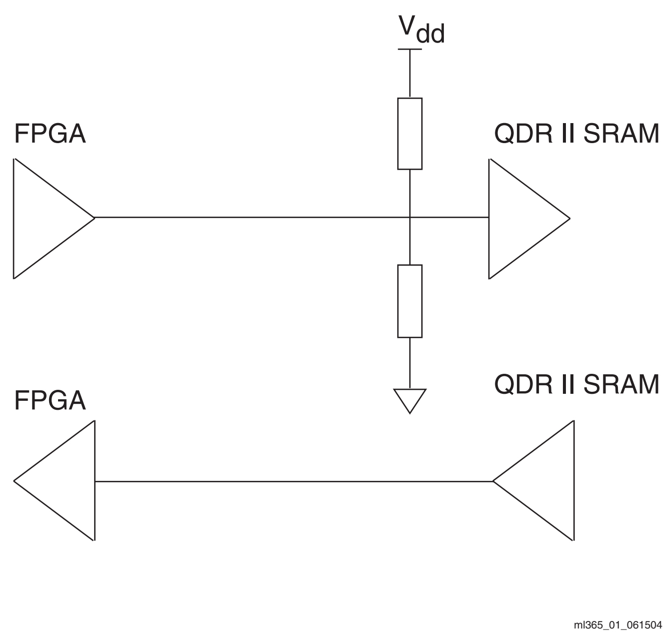

Figure 4-1: **Signal Terminations for Transmitted and Received Data**

Data Signals from the FPGA to the Memory (HSTL_18_C2 at FPGA)

The simulations in this subsection test the data signals from the FPGA to the memory. Simulations were performed for the following cases: typical, slow / weak, and fast / strong (refer to Figure 4-2).

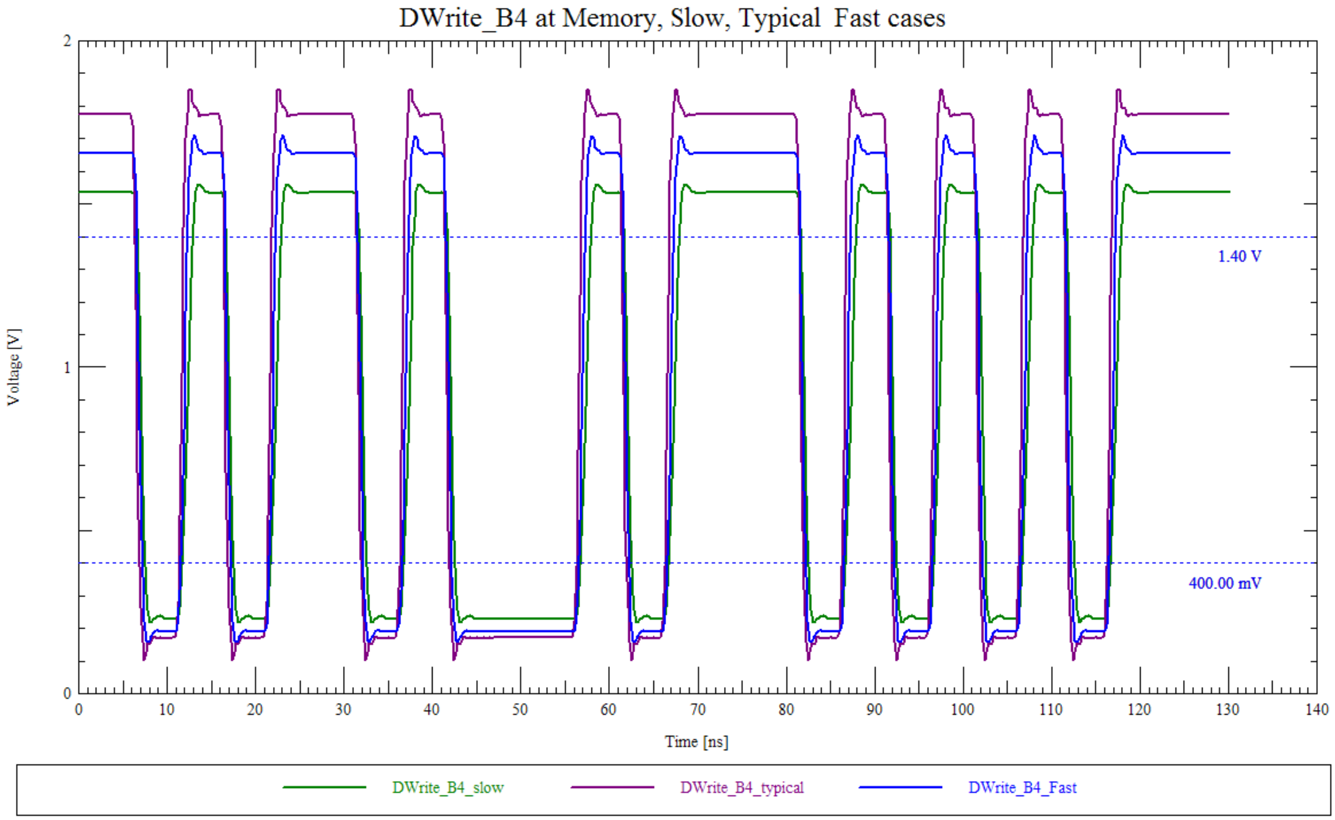

Figure 4-2: **Data Signal Bit 4 from the FPGA to the Memory (Typical Case)**

An eye diagram is provided as well (refer to Figure 4-3).

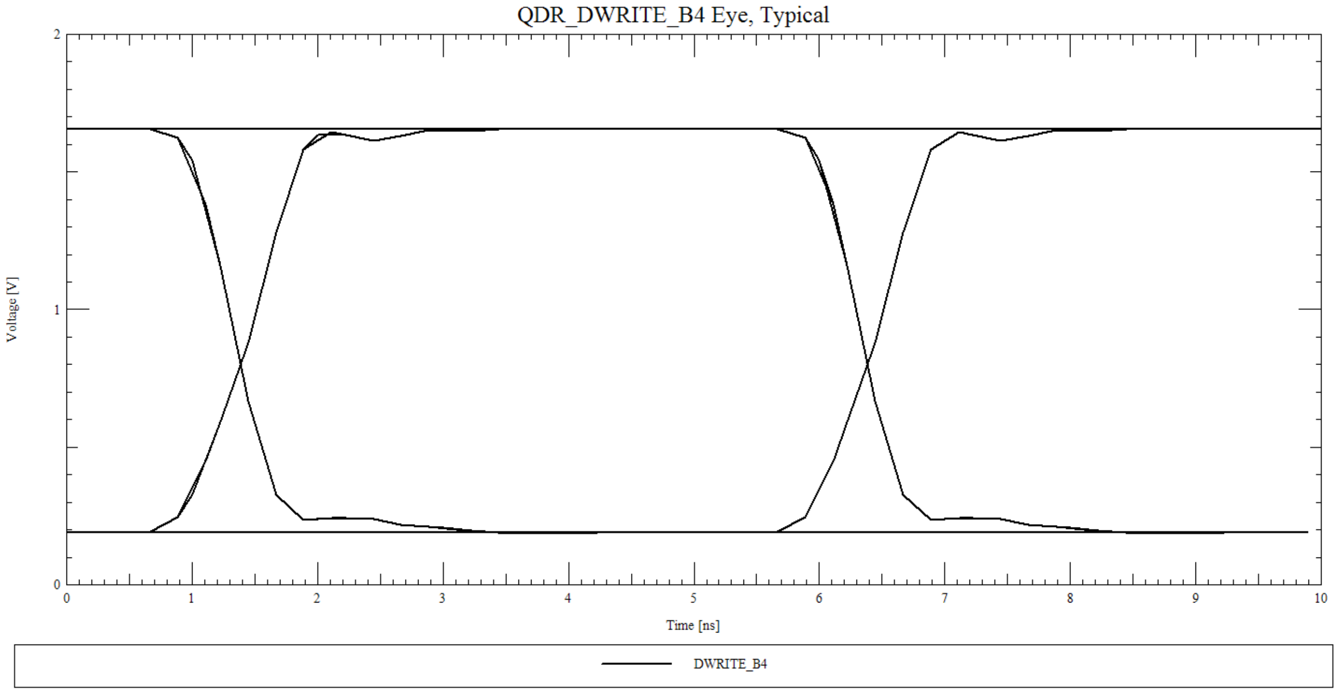

Figure 4-3: **Eye Diagram for Data Bit 4 from the FPGA to the QDR II SRAM, U11**

Data Signals from the QDR II SRAM, Component U11 to the FPGA Measured at the FPGA

The simulations in this subsection test the data signals from the last memory component to the FPGA. Simulations were performed for the following cases: typical, slow / weak, and fast / strong. An eye diagram is provided as well (refer to Figure 4-5).

Figure 4-4 shows the simulation waveforms for this case.

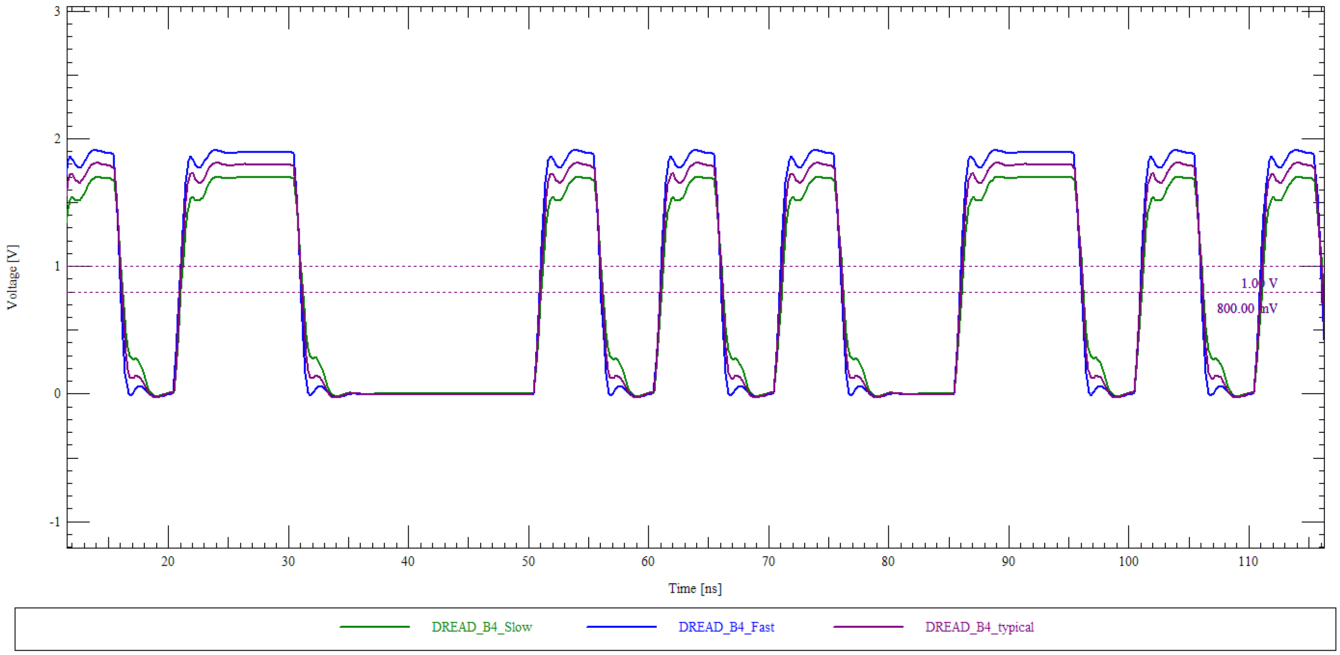

Figure 4-4: **Data Signals from the QDR II SRAM U11 at the FPGA (Typical, Slow/Weak and Fast/Strong Cases)**

Eye Diagram for the Component U11, Bit 4 Signal Measured at the FPGA

Figure 4-5 shows the eye diagram for the data signals from the FPGA to the last memory component.

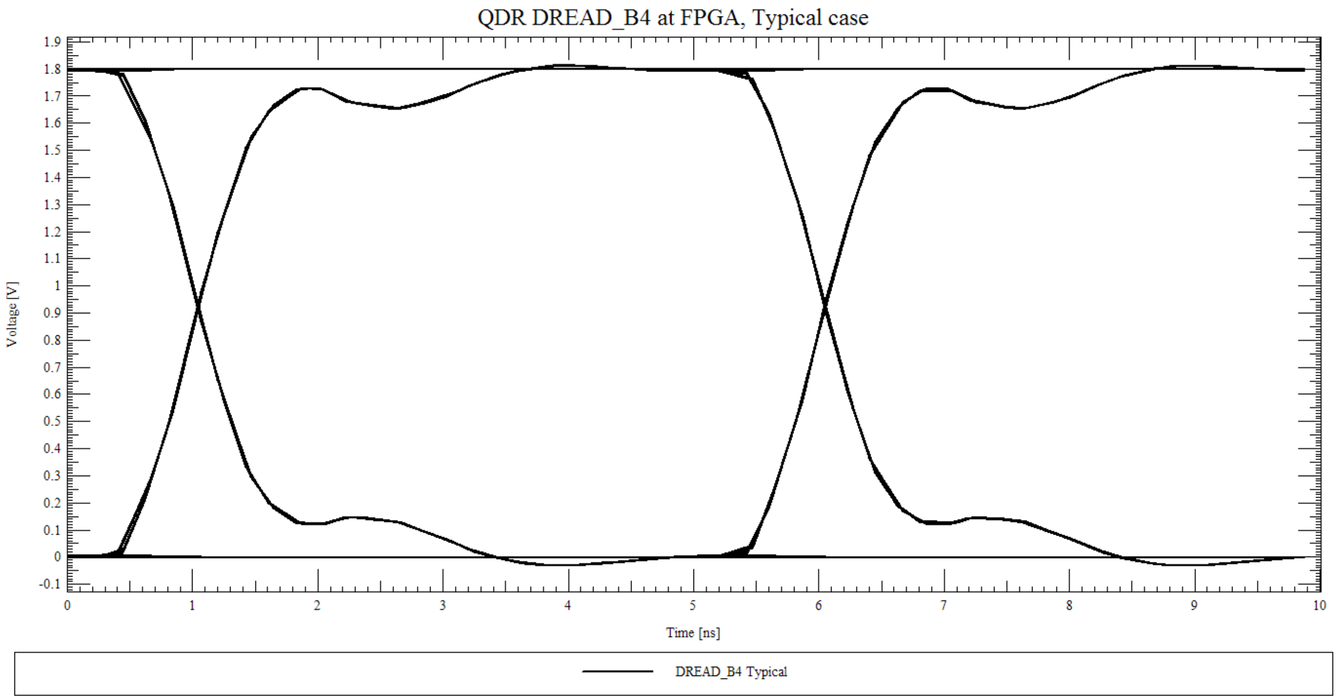

Figure 4-5: **Eye Diagram for Data Bit 4 at the FPGA from Component U11**

Clock Signal Simulations

The simulations in this subsection test the uni-directional Clock K signal from the FPGA to the QDR II SRAM, Component B. Simulations were performed for the following cases: typical, slow / weak, and fast / strong. All of the clock signal simulations use the following test conditions for typical, slow / weak, and fast / strong cases (refer to Figure 4-6).

- Topology for clock signals: 50-ohm transmission lines
- Clock K
  - ♦ At the memory: 100-ohm parallel split termination pulled-up to V_{dd} = 1.8 V (equivalent to a 50-ohm termination pulled up to V_{ref} = 0.9V)
  - ♦ At the FPGA: HSTL_18_C2 drivers
- CQ Clock
  - ♦ At the FPGA: HSTL_18_C1 receivers, 100-ohm parallel split termination pulled-up to V_{dd} = 1.8 V (equivalent to a 50-ohm termination pulled up to V_{ref} = 0.9V)

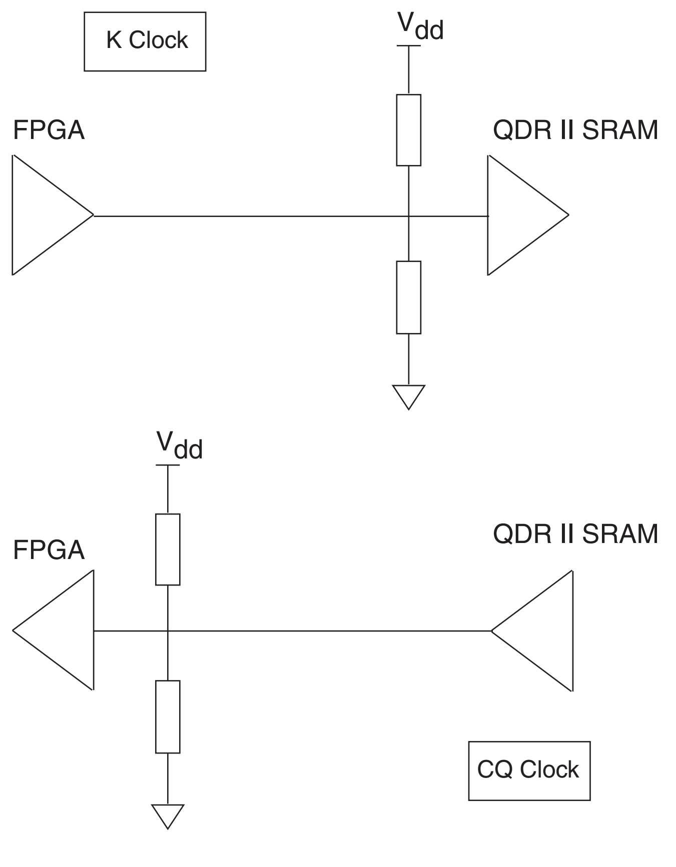

Figure 4-6: **Clock Signal Terminations**

Typical, Slow, and Fast Cases for Clock Signals

Figure 4-7 shows the simulation waveforms for this case.

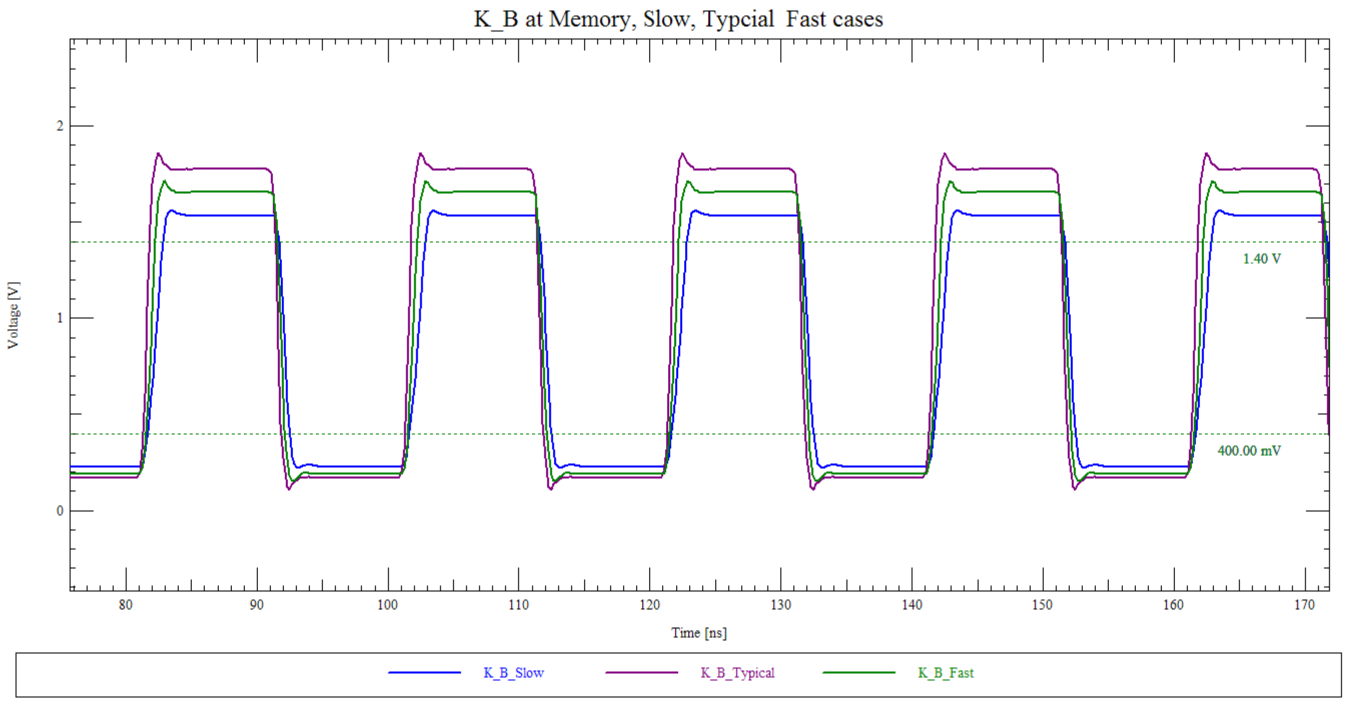

Figure 4-7: **Clock K Signal from the FPGA to the QDR II SRAM, Component U11**

Figure 4-8 shows the simulation waveforms for the Clock K Signal from the FPGA to the QDR II SRAM, Component U11.

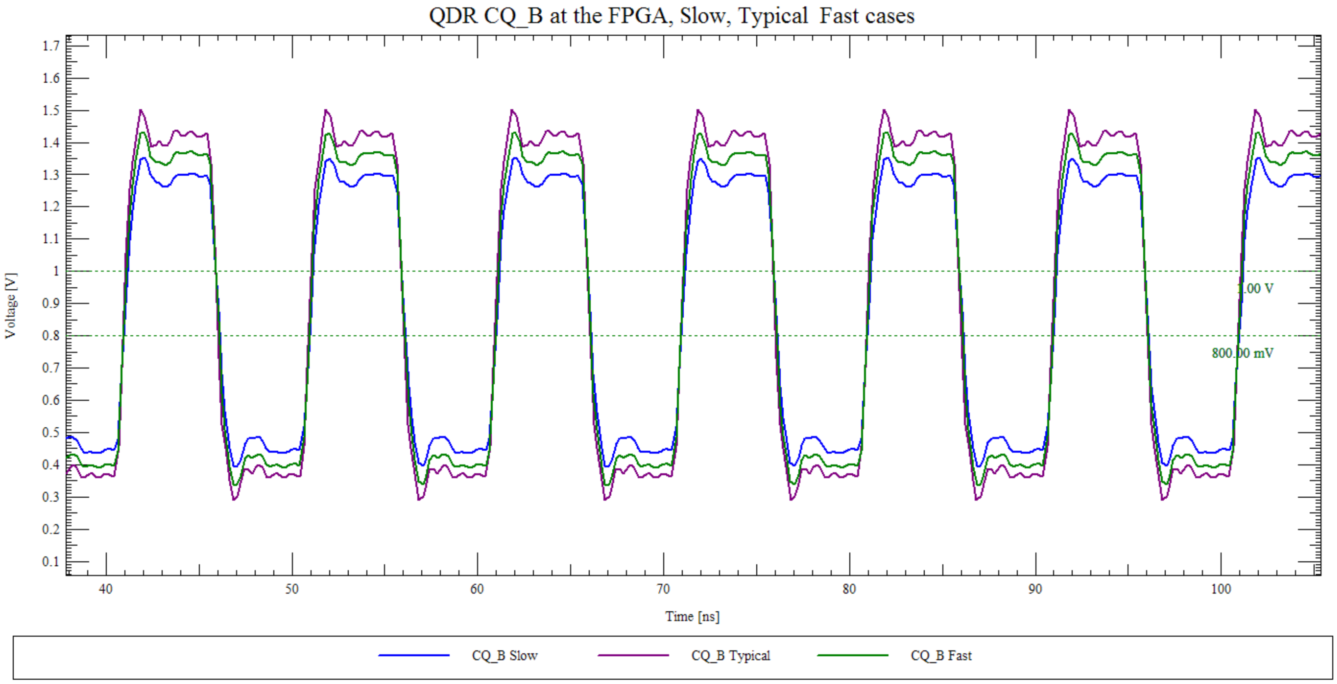

Figure 4-8: **Clock CQ Signal from the FPGA to the QDR II SRAM Component U11**

Address and Control Signal Simulations

The simulations in this subsection test the uni-directional address and control signals from the FPGA to the QDR II SRAM, Component B, U11, Bit 4. Simulations were performed for typical, slow / weak, and fast / strong driver cases.

All of the clock signal simulations use the following test conditions for typical, slow weak, and fast strong cases

- Topology for data signals: 50-ohm Transmission lines
- At the memory: 100-ohm parallel split termination pulled up to Vdd = 1.8 V (equivalent to 50-ohm termination pulled up to Vref = 0.9V)
- At the FPGA: HSTL_18_C2 drivers

Figure 4-9 shows address and control signal terminations.

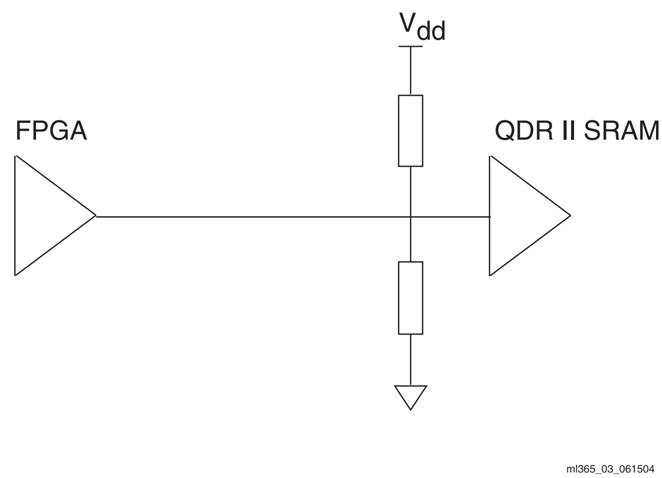

Figure 4-9: **Address and Control Signal Terminations**

Typical Case Simulation at All Memory Components

Figure 4-10 shows the typical case simulation waveforms for the QDR II SRAM, Component B, Bit 4.

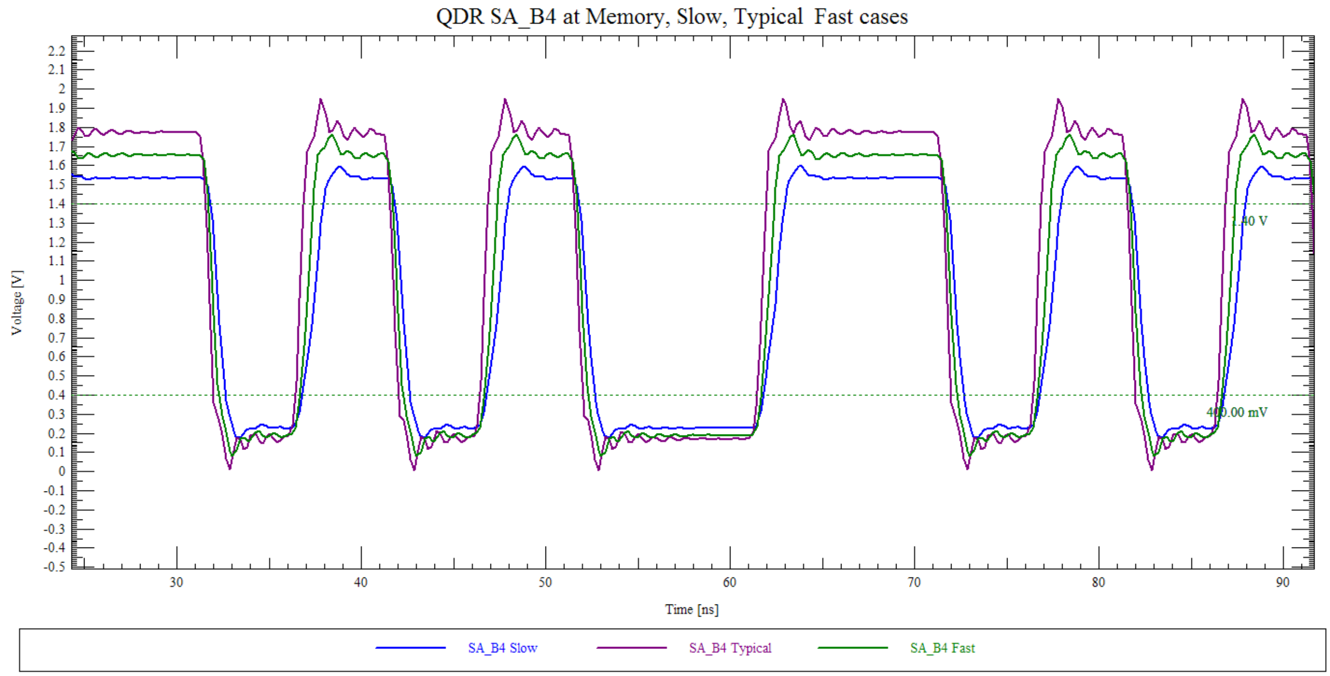

Figure 4-10: **Address/Control Signals for the QDR II SRAM, Component U11, Bit 4**

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Chapter 5

Board Layout Guidelines

This chapter provides information on decoupling capacitors, ground signals, and PCB layout.

Decoupling Guidelines

This section lists the decoupling capacitors used with the major components of the ML365 board. Refer to the board schematics for the exact placement.

Table 5-1 lists the decoupling capacitors for the Virtex-II Pro FPGA and the QDR II SRAM. VAUX and VDD are common to these two devices. Refer to the Xilinx application note XAPP623 for the implementation methodology. A balanced decoupling network is implemented for each bank, VCCINT, VAUX, and VREF.

Table 5-1: **Decoupling Capacitor Recommendations**

Decoupling Capacitors Pin(s)	Capacitor Value	Distribution
VCC 5V LCD, RS232	0.01µF ceramic capacitor, X7R, C0402	8
	0.047µF ceramic capacitor, X7R , C0603	4
	2.2µF ceramic capacitor, X7R, C1206	4
	33µF ceramic capacitor, 10V, C7343	0
	330µF solid tantalum capacitor, 10V, C7343	3
3.3V System ACE	0.01µF ceramic capacitor, X7R, C0402	14
	0.047µF ceramic capacitor, X7R , C0603	7
	2.2µF ceramic capacitor, X7R, C1206	7
	33µF ceramic capacitor, 10V, C7343	1
	330µF solid tantalum capacitor, 10V, C7343	4

Table 5-1: **Decoupling Capacitor Recommendations**

Decoupling Capacitors Pin(s)	Capacitor Value	Distribution
VAUX 2.5V 1 capacitor per pin, in a balanced decoupling network.	0.01µF ceramic capacitor, X7R, C0402	31
	0.047µF ceramic capacitor, X7R , C0603	14
	2.2µF ceramic capacitor, X7R, C1206	7
	33µF ceramic capacitor, 10V, C7343	4
	330µF solid tantalum capacitor, 10V, C7343	2
VCCO 1.8V HSTL 1.8V electrical standard	0.01µF ceramic capacitor, X7R, C0402	76
	0.047µF ceramic capacitor, X7R , C0603	38
	2.2µF ceramic capacitor, X7R, C1206	23
	33µF ceramic capacitor, 10V, C7343	9
	330µF solid tantalum capacitor, 10V, C7343	7
VCCINT 1.5V 1 capacitor per pin, in a balanced decoupling network.	0.01µF ceramic capacitor, X7R, C0402	30
	0.047µF ceramic capacitor, X7R , C0603	11
	2.2µF ceramic capacitor, X7R, C1206	11
	33µF ceramic capacitor, 10V, C7343	8
	330µF solid tantalum capacitor, 10V, C7343	6
VTT 0.9V HSTL 1.8V / 2 for FPGA Vref inputs	0.01µF ceramic capacitor, X7R, C0402	5
	0.047µF ceramic capacitor, X7R , C0603	1
	2.2µF ceramic capacitor, X7R, C1206	4
	33µF ceramic capacitor, 10V, C7343	0
	330µF solid tantalum capacitor, 10V, C7343	0
VTT 0.9V HSTL 1.8V / 2 for memory Vref inputs	0.01µF ceramic capacitor, X7R, C0402	13
	0.047µF ceramic capacitor, X7R , C0603	9
	2.2µF ceramic capacitor, X7R, C1206	0
	33µF ceramic capacitor, 10V, C7343	0
	330µF solid tantalum capacitor, 10V, C7343	0

Providing Additional Ground Pins

Unused and No Connect pinscan be connected to ground to improve the thermal dissipation through the metal planes in the Printed Circuit Board. Since DCI can be used in the FPGA, the heat resulting from its use can be significant.

Board Stackup Guidelines

Table 5-2 shows a suggested stackup for a 12-layer board (4 signal layers, 6 dedicated planes, 2 layers with both signals and ground planes). Figure 5-1 shows the top layer of the ML365 (Revision 1.0b) board, and Figure 5-2 shows the bottom layer of the board.

Table 5-2: **Suggested Stackup for a 12-layer board**

12-Layer Board Stackup#	Type	Layer	Trace / Spacing	Comments
1	Plane	GND	Gnd 1 / Sig 1	Ground plane, some memory traces
2	Plane	+2.5V / +5V	Pwr 1	Carve out two power planes on this layer
3	Signal	+1.8V / +2.5V	Sig 2	Some HSTL traces to the memory on this layer
4	Signal	+1.8V / +2.5V	Sig 3	Some HSTL traces to the memory on this layer
5	Plane	GND	Gnd 2	Ground plane
6	Plane	+1.5V	Pwr 2	1.5V power plane
7	Plane	+0.9V	Pwr 3	0.9V reference plane
8	Plane	GND	Gnd 3	Ground plane
9	Signal	+1.8V / +2.5V	Sig 4	Some HSTL traces to the memory on this layer
10	Signal	GND	Sig 5	Ground plane
11	Plane	+1.8V & +3.3V	Pwr 4	Carve out two power planes on this layer
12	Plane	GND	Gnd 4 / Sig 6	Ground plane, some memory traces

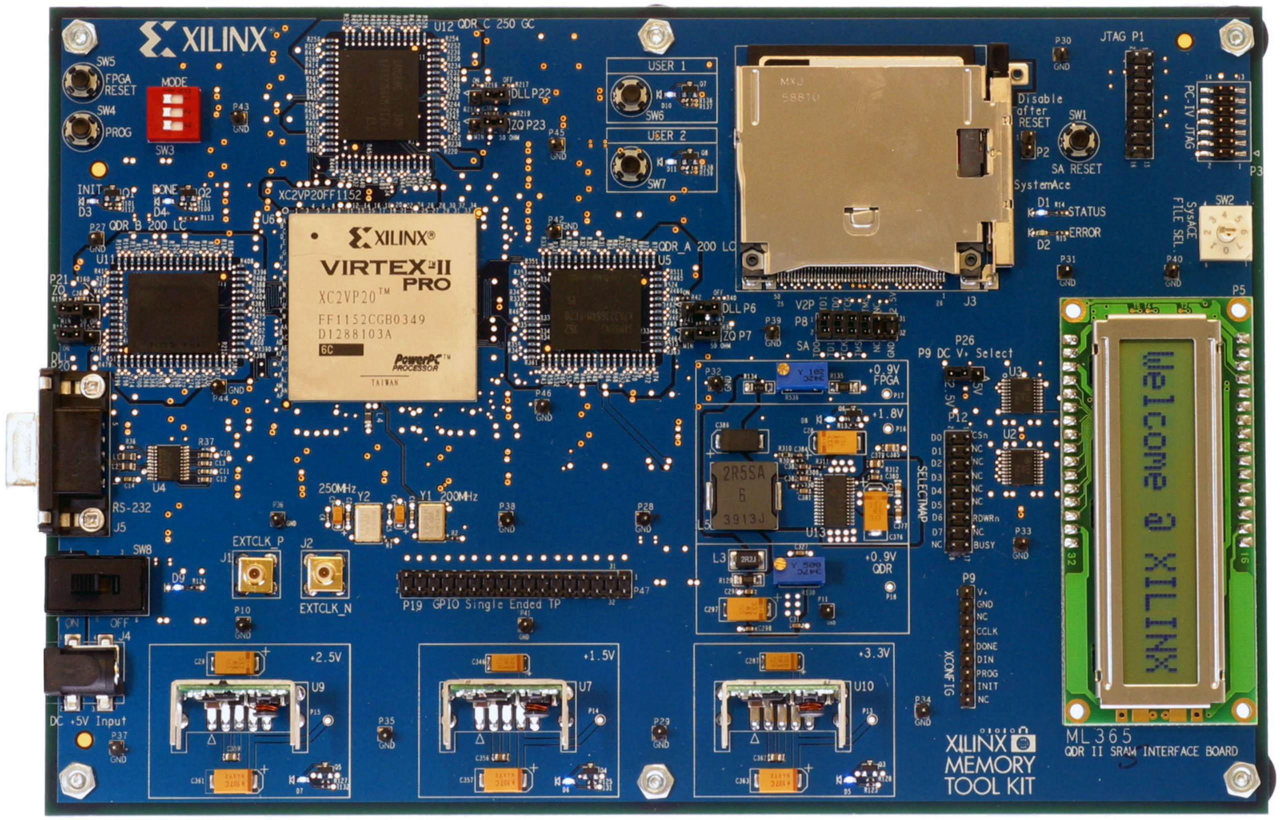

Figure 5-1: **Picture of the Top Layer of the ML365 Revision 1.0b Board**

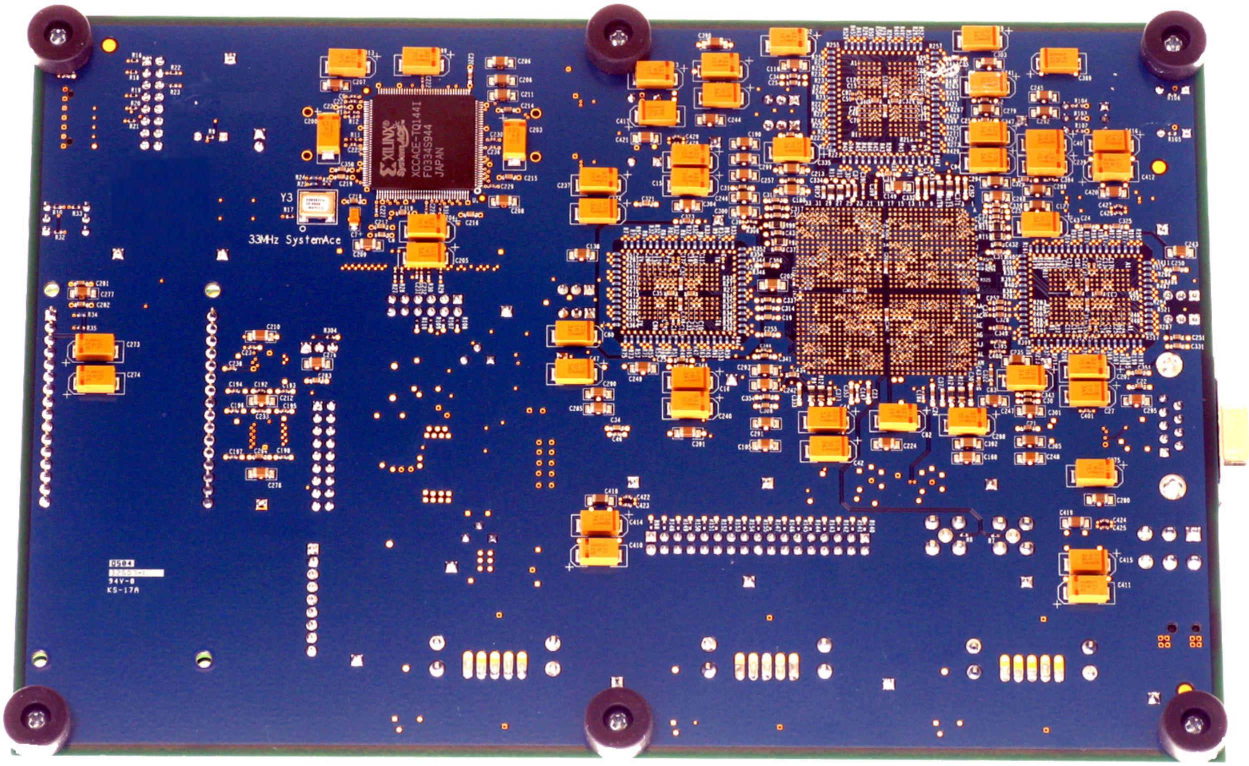

Figure 5-2: **Picture of the Bottom Layer of the ML365 Revision 1.0b Board**

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Appendix 1

Related Documentation

This appendix provides references to documents and web pages for components on the ML365 board.

- Xilinx, Inc.
  - ♦ Virtex-II Pro X™ Platform FPGAs
    http://www.xilinx.com/bvdocs/publications/ds083.pdf
  - ♦ System ACE CompactFlash Solution
    http://direct.xilinx.com/bvdocs/publications/ds080.pdf
- Texas Instruments
  - ♦ TI PT5505N 1.5Vout 3Amp 3.3V/5V-Input Adjustable Step-Down ISR
    http://focus.ti.com/docs/prod/folders/print/pt5505.html
  - ♦ TI PT5502N 2.5Vout 3Amp 3.3V/5V-Input Adjustable Step-Down ISR
    http://focus.ti.com/docs/prod/folders/print/pt5502.html
  - ♦ TI PT5501A 3.3Vout 3Amp 5V-Input Adjustable Step-Down ISR
    http://focus.ti.com/docs/prod/folders/print/pt5501.html
  - ♦ TPS54810PWP 5V Input 8A Synchronous Buck Converter with Adjustable Output Voltage (1.8V)
    http://focus.ti.com/docs/prod/folders/print/tps54810.html
  - ♦ Maxim MAX3316ECUP RS232 Interface
    http://pdfserv.maxim-ic.com/en/ds/MAX3316E-MAX3319E.pdf
- Samsung
  - ♦ Samsung QDR II SRAM Components
    http://www.samsung.com/Products/Semiconductor/SRAM/SyncSRAM/QDRI_II/36Mbit/K7R323684M/ds_k7r323684m.pdf
- Epson
  - ♦ Epson EG-2121CA 2.5V PECL Osc., EG2121CA-200.0000M-PHPAB
    Epson EG-2121CA 2.5V PECL Osc., EG2121CA-250.0000M-PHPAB
    http://www.epson-ed.info/FOE2003/e_prdct/EG2121CA.html
- Agilent Technologies
  - ♦ Logic Analyzer: *Agilent Technologies 16753/54/55/56 Logic Analyzer*
    http://cp.literature.agilent.com/litweb/pdf/5988-9043EN.pdf
  - ♦ Logic Analyzer Probes: *Agilent Technologies Connector-based Probes*
    http://cp.literature.agilent.com/litweb/pdf/16760-97012.pdf

Appendix 2

FPGA Pinout

Table 2-1 summarizes the pinout of the XC2VP20FF1152-6 FPGA in the ML365 board.

I/O pin names marked as *GND* refer to unused I/Os that are directly connected to GND. I/O pin names marked as *PULLDOWN* refer to unused I/Os that are connected to GND through a zero ohm resistor. The zero ohm resistor can be removed to use the corresponding I/O for any test purposes.

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X1Y111	E29	0	IO_L01N_0/VRP_0	R114/C430	11097.26
X1Y111	E28	0	IO_L01P_0/VRN_0	R117/C370	10150.32
X1Y111	H26	0	IO_L02N_0	QDR_DREAD_C0	6327.18
X1Y111	G26	0	IO_L02P_0	QDR_DREAD_C1	7905.95
X3Y111	H25	0	IO_L03N_0	QDR_DREAD_C2	5691.71
X3Y111	G25	0	IO_L03P_0/VREF_0	Vref(0.9V)	6996.94
X5Y111	J25	0	IO_L05_0/No_Pair	QDR_DREAD_C3	5273.75
X5Y111	K24	0	IO_L06N_0	QDR_DREAD_C4	3344.34
X5Y111	J24	0	IO_L06P_0	QDR_DREAD_C5	4601.94
X7Y111	F26	0	IO_L07N_0	QDR_DREAD_C6	9207.2
X7Y111	E26	0	IO_L07P_0	QDR_DREAD_C7	10718.03
X7Y111	D30	0	IO_L08N_0	QDR_DREAD_C8	15834.96
X7Y111	D29	0	IO_L08P_0	QDR_DREAD_C9	14848.81
X9Y111	K23	0	IO_L09N_0	QDR_DREAD_C10	3066.04
X9Y111	J23	0	IO_L09P_0/VREF_0	Vref(0.9V)	4323.64
X11Y111	H22	0	IO_L37N_0	QDR_DREAD_C11	4727.82
X11Y111	G22	0	IO_L37P_0	QDR_DREAD_C12	5923
X11Y111	D26	0	IO_L38N_0	QDR_DREAD_C13	15218.77
X11Y111	C26	0	IO_L38P_0	QDR_DREAD_C14	15469.57
X13Y111	K21	0	IO_L39N_0	QDR_DREAD_C15	5505.04
X13Y111	J21	0	IO_L39P_0	QDR_DREAD_C16	4965.14

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X19Y111	F22	0	IO_L43N_0	QDR_DREAD_C17	7541.44
X19Y111	E22	0	IO_L43P_0	QDR_DREAD_C18	8910.89
X19Y111	E25	0	IO_L44N_0	QDR_DREAD_C19	12735.3
X19Y111	D25	0	IO_L44P_0	QDR_DREAD_C20	13832.18
X21Y111	H21	0	IO_L45N_0	QDR_DREAD_C21	6364.26
X21Y111	G21	0	IO_L45P_0/VREF_0	Vref(0.9V)	7704.24
X23Y111	D22	0	IO_L46N_0	QDR_DREAD_C22	9988.1
X23Y111	D23	0	IO_L46P_0	QDR_DREAD_C23	11050.72
X23Y111	D24	0	IO_L47N_0	QDR_DREAD_C24	12302.96
X23Y111	C24	0	IO_L47P_0	QDR_DREAD_C25	13516.13
X25Y111	K20	0	IO_L48N_0	QDR_DREAD_C26	3126.3
X25Y111	J20	0	IO_L48P_0	QDR_DREAD_C27	4150.17
X27Y111	F21	0	IO_L49N_0	QDR_DREAD_C28	7682.05
X27Y111	E21	0	IO_L49P_0	QDR_DREAD_C29	8634.04
X27Y111	C21	0	IO_L50_0/No_Pair	QDR_DREAD_C30	13499.9
X29Y111	C22	0	IO_L53_0/No_Pair	QDR_DREAD_C31	15061.08
X29Y111	L19	0	IO_L54N_0	QDR_DREAD_C32	2263.39
X29Y111	K19	0	IO_L54P_0	QDR_DREAD_C33	3226.4
X31Y111	G20	0	IO_L55N_0	QDR_DREAD_C34	6227.05
X31Y111	F20	0	IO_L55P_0	QDR_DREAD_C35	7549.54
X31Y111	D21	0	IO_L56N_0	R_n_int_C	10983.43
X31Y111	D20	0	IO_L56P_0	GND	10275.3
X33Y111	J19	0	IO_L57N_0	GND	3969.14
X33Y111	H19	0	IO_L57P_0/VREF_0	Vref(0.9V)	5173.85
X35Y111	G19	0	IO_L67N_0	GND	6064.32
X35Y111	F19	0	IO_L67P_0	GND	8063.93
X35Y111	E19	0	IO_L68N_0	GND	9549.27
X35Y111	D19	0	IO_L68P_0	GND	10957.97
X37Y111	L18	0	IO_L69N_0	GND	2444
X37Y111	K18	0	IO_L69P_0/VREF_0	Vref(0.9V)	3320.11
X43Y111	G18	0	IO_L73N_0	GND	5890.16
X43Y111	F18	0	IO_L73P_0	GND	7223.69
X45Y111	E18	0	IO_L74N_0/GCLK7P	QDR_CQ_C	8692.96
X45Y111	D18	0	IO_L74P_0/GCLK6S	QDR_CQ_n_C	9819.09

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X45Y111	J18	0	IO_L75N_0/GCLK5P	GND	3858.95
X45Y111	H18	0	IO_L75P_0/GCLK4S	GND	5131.43
X47Y111	H17	1	IO_L75N_1/GCLK3P	GND	5131.43
X47Y111	J17	1	IO_L75P_1/GCLK2S	GND	3858.95
X47Y111	D17	1	IO_L74N_1/GCLK1P	GND	10242.07
X47Y111	E17	1	IO_L74P_1/GCLK0S	GND	8752.34
X49Y111	F17	1	IO_L73N_1	GND	7223.69
X49Y111	G17	1	IO_L73P_1	GND	5890.16
X55Y111	K17	1	IO_L69N_1/VREF_1	Vref(0.9V)	3320.11
X55Y111	L17	1	IO_L69P_1	QDR_DWRITE_C0	2444
X57Y111	D16	1	IO_L68N_1	QDR_DWRITE_C1	10931.46
X57Y111	E16	1	IO_L68P_1	QDR_DWRITE_C2	9549.27
X57Y111	F16	1	IO_L67N_1	QDR_DWRITE_C3	8063.93
X57Y111	G16	1	IO_L67P_1	QDR_DWRITE_C4	6064.32
X59Y111	H16	1	IO_L57N_1/VREF_1	Vref(0.9V)	5173.85
X59Y111	J16	1	IO_L57P_1	QDR_DWRITE_C5	3969.14
X61Y111	D15	1	IO_L56N_1	QDR_DWRITE_C6	10275.3
X61Y111	D14	1	IO_L56P_1	QDR_DWRITE_C7	10983.43
X61Y111	F15	1	IO_L55N_1	QDR_DWRITE_C8	7549.54
X61Y111	G15	1	IO_L55P_1	QDR_DWRITE_C9	6227.05
X63Y111	K16	1	IO_L54N_1	QDR_DWRITE_C10	3226.4
X63Y111	L16	1	IO_L54P_1	QDR_DWRITE_C11	2263.39
X63Y111	C13	1	IO_L53_1/No_Pair	QDR_DWRITE_C12	15102.5
X65Y111	C14	1	IO_L50_1/No_Pair	QDR_DWRITE_C13	13541.32
X65Y111	E14	1	IO_L49N_1	QDR_DWRITE_C14	8634.04
X65Y111	F14	1	IO_L49P_1	QDR_DWRITE_C15	7682.05
X67Y111	J15	1	IO_L48N_1	QDR_DWRITE_C16	4150.17
X67Y111	K15	1	IO_L48P_1	QDR_DWRITE_C17	3084.88
X69Y111	C11	1	IO_L47N_1	QDR_DWRITE_C18	13513.12
X69Y111	D11	1	IO_L47P_1	QDR_DWRITE_C19	12295.94
X69Y111	D12	1	IO_L46N_1	QDR_DWRITE_C20	11050.72
X69Y111	D13	1	IO_L46P_1	QDR_DWRITE_C21	9988.1
X71Y111	G14	1	IO_L45N_1/VREF_1	Vref(0.9V)	7704.24

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X71Y111	H14	1	IO_L45P_1	QDR_DWRITE_C22	6364.26
X73Y111	D10	1	IO_L44N_1	QDR_DWRITE_C23	13570.63
X73Y111	E10	1	IO_L44P_1	QDR_DWRITE_C24	12296.5
X73Y111	E13	1	IO_L43N_1	QDR_DWRITE_C25	8910.89
X73Y111	F13	1	IO_L43P_1	QDR_DWRITE_C26	7591.45
X79Y111	J14	1	IO_L39N_1	QDR_DWRITE_C27	4903.25
X79Y111	K14	1	IO_L39P_1	QDR_DWRITE_C28	5404.41
X81Y111	C9	1	IO_L38N_1	QDR_DWRITE_C29	15339.71
X81Y111	D9	1	IO_L38P_1	QDR_DWRITE_C30	14631.43
X81Y111	G13	1	IO_L37N_1	QDR_DWRITE_C31	5923
X81Y111	H13	1	IO_L37P_1	QDR_DWRITE_C32	4727.82
X83Y111	J12	1	IO_L09N_1/VREF_1	Vref(0.9V)	4323.64
X83Y111	K12	1	IO_L09P_1	QDR_DWRITE_C33	3066.04
X85Y111	D6	1	IO_L08N_1	QDR_DWRITE_C34	15105.89
X85Y111	D5	1	IO_L08P_1	QDR_DWRITE_C35	16085.61
X85Y111	E9	1	IO_L07N_1	QDR_C_n_C	10718.03
X85Y111	F9	1	IO_L07P_1	QDR_C_C	9223.77
X87Y111	J11	1	IO_L06N_1	QDR_K_n_C	4601.94
X87Y111	K11	1	IO_L06P_1	QDR_K_C	3344.34
X87Y111	J10	1	IO_L05_1/No_Pair	QDR_W_n_C	5273.75
X89Y111	G10	1	IO_L03N_1/VREF_1	Vref(0.9V)	6996.94
X89Y111	H10	1	IO_L03P_1	QDR_R_n_C	5691.71
X91Y111	G9	1	IO_L02N_1	R_n_ext_C	7905.95
X91Y111	H9	1	IO_L02P_1		6327.18
X91Y111	E7	1	IO_L01N_1/VRP_1	R116/C431	10150.32
X91Y111	E6	1	IO_L01P_1/VRN_1	R115/C371	11097.26
X91Y111	D2	2	IO_L01N_2/VRP_2	R119/C432	7113.13
X91Y110	D1	2	IO_L01P_2/VRN_2	R118/C375	4624.16
X90Y111	F8	2	IO_L02N_2	QDR_SA_C0	3390.64
X90Y110	F7	2	IO_L02P_2	QDR_SA_C1	5566.52
X90Y109	E4	2	IO_L03N_2	QDR_SA_C2	6738.57
X90Y108	E3	2	IO_L03P_2	QDR_SA_C3	14050.12
X91Y107	E2	2	IO_L04N_2/VREF_2	Vref(0.9V)	15547.77

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X91Y106	E1	2	IO_L04P_2	QDR_SA_C4	15132.61
X90Y107	J8	2	IO_L05N_2	QDR_SA_C5	6469.14
X90Y106	J7	2	IO_L05P_2	QDR_SA_C6	7292.33
X90Y105	F5	2	IO_L06N_2	QDR_SA_C7	10666.81
X90Y104	F4	2	IO_L06P_2	QDR_SA_C8	11858.77
X91Y103	H2	2	IO_L31N_2	QDR_SA_C9	12137.04
X91Y102	H1	2	IO_L31P_2	QDR_SA_C10	13451.41
X90Y103	M10	2	IO_L32N_2	QDR_SA_C11	3062.48
X90Y102	M9	2	IO_L32P_2	QDR_SA_C12	4123.3
X90Y101	K5	2	IO_L33N_2	QDR_SA_C13	8267.43
X90Y100	K4	2	IO_L33P_2	QDR_SA_C14	9537.04
X91Y99	J2	2	IO_L34N_2/VREF_2	Vref(0.9V)	12149.07
X91Y98	K2	2	IO_L34P_2	QDR_SA_C15	11352.59
X90Y99	L8	2	IO_L35N_2	QDR_SA_C16	5592.79
X90Y98	L7	2	IO_L35P_2	QDR_SA_C17	6793.53
X90Y97	L6	2	IO_L36N_2	GND	7367.37
X90Y96	L5	2	IO_L36P_2	GND	8143.52
X91Y95	K1	2	IO_L37N_2	QDR_BW_n_C0	12423.45
X91Y94	L1	2	IO_L37P_2	QDR_BW_n_C1	12451.17
X90Y95	N10	2	IO_L38N_2	QDR_BW_n_C2	2788.42
X90Y94	N9	2	IO_L38P_2	QDR_BW_n_C3	3972.59
X90Y93	M7	2	IO_L39N_2	GND	5610.09
X90Y92	M6	2	IO_L39P_2	GND	6975.04
X91Y91	L2	2	IO_L40N_2/VREF_2	Vref(0.9V)	11195.56
X91Y90	M2	2	IO_L40P_2	R_n_int_B	12186.54
X90Y91	N8	2	IO_L41N_2	QDR_DREAD_B0	4920.17
X90Y90	N7	2	IO_L41P_2	QDR_DREAD_B1	6104.35
X90Y89	L4	2	IO_L42N_2	QDR_DREAD_B2	9001.57
X90Y88	L3	2	IO_L42P_2	QDR_DREAD_B3	10259.17
X91Y87	M4	2	IO_L43N_2	QDR_DREAD_B4	8536.05
X91Y86	M3	2	IO_L43P_2	QDR_DREAD_B5	9772.91
X90Y87	P10	2	IO_L44N_2	QDR_DREAD_B6	2638.82
X90Y86	P9	2	IO_L44P_2	QDR_DREAD_B7	3823
X90Y85	N6	2	IO_L45N_2	QDR_DREAD_B8	6306.01

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X90Y84	N5	2	IO_L45P_2	QDR_DREAD_B9	7563.61
X91Y83	M1	2	IO_L46N_2/VREF_2	Vref(0.9V)	11667.8
X91Y82	N1	2	IO_L46P_2	QDR_CQ_n_B	11804.99
X90Y83	P8	2	IO_L47N_2	GND	4770.58
X90Y82	P7	2	IO_L47P_2	GND	5954.75
X90Y81	N4	2	IO_L48N_2	GND	8437.77
X90Y80	N3	2	IO_L48P_2	GND	9778.21
X91Y79	N2	2	IO_L49N_2	QDR_DREAD_B10	10426.76
X91Y78	P2	2	IO_L49P_2	QDR_DREAD_B11	10530.82
X90Y79	R10	2	IO_L50N_2	QDR_DREAD_B12	2488.12
X90Y78	R9	2	IO_L50P_2	QDR_DREAD_B13	3672.29
X90Y77	P6	2	IO_L51N_2	QDR_DREAD_B14	6499.99
X90Y76	P5	2	IO_L51P_2	QDR_DREAD_B15	7603.44
X91Y75	P4	2	IO_L52N_2/VREF_2	Vref(0.9V)	8102.88
X91Y74	P3	2	IO_L52P_2	GND	9339.48
X90Y75	T11	2	IO_L53N_2	QDR_DREAD_B16	1247.81
X90Y74	U11	2	IO_L53P_2	QDR_DREAD_B17	1919.47
X90Y73	R7	2	IO_L54N_2	QDR_DREAD_B18	4872.84
X90Y72	R6	2	IO_L54P_2	QDR_DREAD_B19	6425.42
X91Y71	P1	2	IO_L55N_2	QDR_DREAD_B20	11291.77
X91Y70	R1	2	IO_L55P_2	QDR_DREAD_B21	11455.67
X90Y71	T10	2	IO_L56N_2	QDR_DREAD_B22	2752.93
X90Y70	T9	2	IO_L56P_2	QDR_DREAD_B23	3871.63
X90Y69	R4	2	IO_L57N_2	QDR_DREAD_B24	8013.89
X90Y68	R3	2	IO_L57P_2	QDR_DREAD_B25	9271.49
X91Y67	R2	2	IO_L58N_2/VREF_2	Vref(0.9V)	9961.47
X91Y66	T2	2	IO_L58P_2	QDR_CQ_B	10173.21
X90Y67	T8	2	IO_L59N_2	GND	4753.73
X90Y66	T7	2	IO_L59P_2	GND	5872.43
X90Y65	T6	2	IO_L60N_2	GND	6031.43
X90Y64	T5	2	IO_L60P_2	GND	7055.3
X91Y63	T4	2	IO_L85N_2	QDR_DREAD_B26	7724.5
X91Y62	T3	2	IO_L85P_2	QDR_DREAD_B27	9056.44
X90Y63	U10	2	IO_L86N_2	QDR_DREAD_B28	2340.31

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X90Y62	U9	2	IO_L86P_2	QDR_DREAD_B29	3459.01
X90Y61	U6	2	IO_L87N_2	QDR_DREAD_B30	5801.93
X90Y60	U5	2	IO_L87P_2	QDR_DREAD_B31	6851.4
X91Y59	U2	2	IO_L88N_2/VREF_2	Vref(0.9V)	9665.64
X91Y58	V2	2	IO_L88P_2	GND	10394.2
X90Y59	U8	2	IO_L89N_2	QDR_DREAD_B32	4393.22
X90Y58	U7	2	IO_L89P_2	QDR_DREAD_B33	5511.92
X90Y57	U4	2	IO_L90N_2	QDR_DREAD_B34	7649.57
X90Y56	U3	2	IO_L90P_2	QDR_DREAD_B35	8839.91
X91Y55	V3	3	IO_L90N_3	QDR_DWRITE_B0	8537.7
X91Y54	V4	3	IO_L90P_3	QDR_DWRITE_B1	7799.59
X91Y53	V7	3	IO_L89N_3	QDR_DWRITE_B2	5407.06
X91Y52	V8	3	IO_L89P_3	QDR_DWRITE_B3	4483.54
X90Y53	V5	3	IO_L88N_3	QDR_DWRITE_B4	6547.9
X90Y52	V6	3	IO_L88P_3	QDR_DWRITE_B5	5998.02
X91Y51	W2	3	IO_L87N_3/VREF_3	Vref(0.9V)	9812.03
X91Y50	Y2	3	IO_L87P_3	QDR_DWRITE_B6	10611.96
X91Y49	V9	3	IO_L86N_3	QDR_DWRITE_B7	3327.27
X91Y48	V10	3	IO_L86P_3	QDR_DWRITE_B8	2405.17
X90Y49	W3	3	IO_L85N_3	QDR_DWRITE_B9	8919.9
X90Y48	W4	3	IO_L85P_3	QDR_DWRITE_B10	8159.47
X91Y47	Y1	3	IO_L60N_3	QDR_DWRITE_B11	11148.48
X91Y46	AA1	3	IO_L60P_3	QDR_DWRITE_B12	11691.6
X91Y45	V11	3	IO_L59N_3	QDR_DWRITE_B13	1638.53
X91Y44	W11	3	IO_L59P_3	QDR_DWRITE_B14	1610.19
X90Y45	W5	3	IO_L58N_3	QDR_DWRITE_B15	6678.99
X90Y44	W6	3	IO_L58P_3	QDR_DWRITE_B16	5936.59
X91Y43	Y3	3	IO_L57N_3/VREF_3	Vref(0.9V)	8909.69
X91Y42	Y4	3	IO_L57P_3	QDR_DWRITE_B17	8145.63
X91Y41	W7	3	IO_L56N_3	QDR_DWRITE_B18	5773.96
X91Y40	W8	3	IO_L56P_3	QDR_DWRITE_B19	4826.38
X90Y41	Y6	3	IO_L55N_3	QDR_DWRITE_B20	5961.45
X90Y40	Y7	3	IO_L55P_3	QDR_DWRITE_B21	5219.05

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X91Y39	AA2	3	IO_L54N_3	QDR_DWRITE_B22	10317.88
X91Y38	AB2	3	IO_L54P_3	QDR_DWRITE_B23	11488.21
X91Y37	W9	3	IO_L53N_3	QDR_DWRITE_B24	3619.48
X91Y36	W10	3	IO_L53P_3	QDR_DWRITE_B25	2590.48
X90Y37	AA3	3	IO_L52N_3	QDR_DWRITE_B26	9502.86
X90Y36	AA4	3	IO_L52P_3	QDR_DWRITE_B27	8801.88
X91Y35	AB1	3	IO_L51N_3/VREF_3	Vref(0.9V)	12006.27
X91Y34	AC1	3	IO_L51P_3	QDR_DWRITE_B28	12342.28
X91Y33	Y9	3	IO_L50N_3	QDR_DWRITE_B29	3554
X91Y32	Y10	3	IO_L50P_3	QDR_DWRITE_B30	2606.42
X90Y33	AA5	3	IO_L49N_3	QDR_DWRITE_B31	7683.23
X90Y32	AA6	3	IO_L49P_3	QDR_DWRITE_B32	7555.89
X91Y31	AB3	3	IO_L48N_3	QDR_DWRITE_B33	9319.47
X91Y30	AB4	3	IO_L48P_3	QDR_DWRITE_B34	8556.07
X91Y29	AA7	3	IO_L47N_3	QDR_DWRITE_B35	5836.46
X91Y28	AA8	3	IO_L47P_3		4888.88
X90Y29	AB5	3	IO_L46N_3	QDR_SA_B0	7371.9
X90Y28	AB6	3	IO_L46P_3	QDR_SA_B1	6629.5
X91Y27	AC2	3	IO_L45N_3/VREF_3	Vref(0.9V)	10601.93
X91Y26	AD2	3	IO_L45P_3	QDR_SA_B2	11866.32
X91Y25	AA9	3	IO_L44N_3	QDR_SA_B3	3704.71
X91Y24	AA10	3	IO_L44P_3	QDR_SA_B4	2717.14
X90Y25	AC3	3	IO_L43N_3	QDR_SA_B5	9702.33
X90Y24	AC4	3	IO_L43P_3	QDR_SA_B6	8911.96
X91Y23	AD1	3	IO_L42N_3	QDR_SA_B7	12256.07
X91Y22	AE1	3	IO_L42P_3	QDR_SA_B8	12534.09
X91Y21	AB7	3	IO_L41N_3	QDR_SA_B9	5986.05
X91Y20	AB8	3	IO_L41P_3	QDR_SA_B10	5038.48
X90Y21	AC6	3	IO_L40N_3	QDR_SA_B11	6521.49
X90Y20	AC7	3	IO_L40P_3	QDR_SA_B12	5779.09
X91Y19	AD3	3	IO_L39N_3/VREF_3	Vref(0.9V)	9751.53
X91Y18	AD4	3	IO_L39P_3	QDR_SA_B13	9046.71
X91Y17	AB9	3	IO_L38N_3	QDR_SA_B14	3854.3
X91Y16	AB10	3	IO_L38P_3	QDR_SA_B15	2906.72

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X90Y17	AD5	3	IO_L37N_3	QDR_SA_B16	8126.55
X90Y16	AD6	3	IO_L37P_3	QDR_SA_B17	8070.54
X91Y15	AE2	3	IO_L36N_3	QDR_BW_n_B0	11537.91
X91Y14	AF2	3	IO_L36P_3	QDR_BW_n_B1	11948.48
X91Y13	AD7	3	IO_L35N_3	QDR_BW_n_B2	6675.24
X91Y12	AD8	3	IO_L35P_3	QDR_BW_n_B3	5651.11
X90Y13	AE4	3	IO_L34N_3	QDR_K_B	9342.05
X90Y12	AE5	3	IO_L34P_3	QDR_K_n_B	8811.79
X91Y11	AG1	3	IO_L33N_3/VREF_3	Vref(0.9V)	12986.31
X91Y10	AG2	3	IO_L33P_3	R_n_ext_B	12391.44
X91Y9	AC9	3	IO_L32N_3	QDR_R_n_B	4005.01
X91Y8	AC10	3	IO_L32P_3	QDR_W_n_B	3336.69
X90Y9	AF3	3	IO_L31N_3	QDR_C_B	10624.52
X90Y8	AF4	3	IO_L31P_3	QDR_C_n_B	10021.36
X91Y7	AL1	3	IO_L06N_3	GND	15821.97
X91Y6	AL2	3	IO_L06P_3	GND	15583.83
X91Y5	AG7	3	IO_L05N_3	GND	9638.17
X91Y4	AH8	3	IO_L05P_3	DONE	9015.73
X90Y5	AH5	3	IO_L04N_3	GND	9452.34
X90Y4	AH6	3	IO_L04P_3	GND	9308.27
X91Y3	AK3	3	IO_L03N_3/VREF_3	Vref(0.9V)	12802.28
X91Y2	AK4	3	IO_L03P_3	GND	12761.57
X91Y1	AJ7	3	IO_L02N_3	GND	12205.75
X91Y0	AJ8	3	IO_L02P_3	GND	10415.12
X90Y1	AJ4	3	IO_L01N_3/VRP_3	R120/C433	11311.2
X90Y0	AJ5	3	IO_L01P_3/VRN_3	R121/C372	10985.88
X90Y0	AL5	4	IO_L01N_4/DOUT	FPGA_BUSY	13235.56
X90Y0	AL6	4	IO_L01P_4/INIT_B	INIT_B	12205.78
X90Y0	AG9	4	IO_L02N_4/D0	FPGA_DO	6285.75
X90Y0	AH9	4	IO_L02P_4/D1	FPGA_D1	7853.38
X88Y0	AK6	4	IO_L03N_4/D2	FPGA_D2	11359.7
X88Y0	AK7	4	IO_L03P_4/D3	FPGA_D3	11413.02
X86Y0	AF10	4	IO_l05_4/No_Pair	GND	5273.75

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X86Y0	AL7	4	IO_L06N_4/VRP_4	GND	12583.91
X86Y0	AM7	4	IO_L06P_4/VRN_4	GND	13750.42
X84Y0	AE11	4	IO_L07N_4	GND	3596.07
X84Y0	AF11	4	IO_L07P_4/VREF_4	GND	4532.67
X84Y0	AG10	4	IO_L08N_4	RS232_R1OUT	7946.43
X84Y0	AH10	4	IO_L08P_4	RS232_T1IN	8820.26
X82Y0	AK8	4	IO_L09N_4	GND	11291.37
X82Y0	AL8	4	IO_L09P_4/VREF_4	GND	11372.97
X80Y0	AE13	4	IO_L37N_4	GND	2723.68
X80Y0	AF13	4	IO_L37P_4	GND	3918.86
X80Y0	AG13	4	IO_L38N_4	USER1_PB	8007.13
X80Y0	AH13	4	IO_L38P_4	GND	8774.61
X78Y0	AJ11	4	IO_L39N_4	GND	8630.23
X78Y0	AK11	4	IO_L39P_4	GND	9736.03
X72Y0	AE14	4	IO_L43N_4	GND	3696.3
X72Y0	AF14	4	IO_L43P_4	USER2_PB	5289.64
X72Y0	AJ13	4	IO_L44N_4	GND	9198.92
X72Y0	AK13	4	IO_L44P_4	GND	10605.95
X70Y0	AL11	4	IO_L45N_4	GND	10900.17
X70Y0	AM11	4	IO_L45P_4/VREF_4	GND	12224.04
X68Y0	AE15	4	IO_L46N_4	USER2_LED	3132.45
X68Y0	AF15	4	IO_L46P_4	USER1_LED	3969.05
X68Y0	AG14	4	IO_L47N_4	GND	8129.77
X68Y0	AH14	4	IO_L47P_4	GND	9100.75
X66Y0	AL13	4	IO_L48N_4	BANK4_LA1	9870.11
X66Y0	AL12	4	IO_L48P_4	BANK4_LA2	11409.38
X64Y0	AD16	4	IO_L49N_4	BANK4_LA3	2710.75
X64Y0	AE16	4	IO_L49P_4	BANK4_LA4	3442.92
X64Y0	AJ14	4	IO_L50_4/No_Pair	GND	8953.05
X62Y0	AK14	4	IO_L53_4/No_Pair	GND	9556.17
X62Y0	AM14	4	IO_L54N_4	BANK4_LA5	12003.32
X62Y0	AM13	4	IO_L54P_4	BANK4_LA6	12348.43
X60Y0	AF16	4	IO_L55N_4	BANK4_LA7	3887.4
X60Y0	AG16	4	IO_L55P_4	BANK4_LA8	4909.89

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X60Y0	AH15	4	IO_L56N_4	BANK4_LA9	7000
X60Y0	AJ15	4	IO_L56P_4	BANK4_LA10	8217.31
X58Y0	AL14	4	IO_L57N_4	GND	10563
X58Y0	AL15	4	IO_L57P_4/VREF_4	GND	10160.18
X56Y0	AD17	4	IO_L67N_4	BANK4_LA11	2503.07
X56Y0	AE17	4	IO_L67P_4	BANK4_LA12	3464.19
X56Y0	AH16	4	IO_L68N_4	BANK4_LA13	7362.9
X56Y0	AJ16	4	IO_L68P_4	BANK4_LA14	9128.85
X54Y0	AK16	4	IO_L69N_4	BANK4_LA15	9447.56
X54Y0	AL16	4	IO_L69P_4/VREF_4	GND	10269.32
X48Y0	AF17	4	IO_L73N_4	BANK4_LA16	
X48Y0	AG17	4	IO_L73P_4	BANK4_LACLK	
X46Y0	AH17	4	IO_L74N_4/GCLK3S	OSC_200M_N	
X46Y0	AJ17	4	IO_L74P_4/GCLK2P	OSC_200M_P	
X46Y0	AK17	4	IO_L75N_4/GCLK1S	OSC_250M_N	
X46Y0	AL17	4	IO_L75P_4/GCLK0P	OSC_250M_P	
X44Y0	AL18	5	IO_L75N_5/GCLK7S	EXTCLK1_N	
X44Y0	AK18	5	IO_L75P_5/GCLK6P	EXTCLK1_P	
X44Y0	AJ18	5	IO_L74N_5/GCLK5S	GND	
X44Y0	AH18	5	IO_L74P_5/GCLK4P	GND	
X42Y0	AG18	5	IO_L73N_5	TRST#	
X42Y0	AF18	5	IO_L73P_5	HALT#	
X36Y0	AL19	5	IO_L69N_5/VREF_5	GND	
X36Y0	AK19	5	IO_L69P_5	SYSACE_MPCE#	
X34Y0	AJ19	5	IO_L68N_5	SYSACE_MPOE#	
X34Y0	AH19	5	IO_L68P_5	SYSACE_MPBIRQ	
X34Y0	AE18	5	IO_L67N_5	SYSACE_MPWE#	
X34Y0	AD18	5	IO_L67P_5	SYSACE_MPBRDY	
X32Y0	AL20	5	IO_L57N_5/VREF_5	SYSACE_CLK	
X32Y0	AL21	5	IO_L57P_5	SYSACE_MPA6	
X30Y0	AJ20	5	IO_L56N_5	SYSACE_MPA5	
X30Y0	AH20	5	IO_L56P_5	SYSACE_MPA4	
X30Y0	AG19	5	IO_L55N_5	SYSACE_MPA3	

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X30Y0	AF19	5	IO_L55P_5	SYSACE_MPA2	
X28Y0	AM22	5	IO_L54N_5	SYSACE_MPA1	
X28Y0	AM21	5	IO_L54P_5	SYSACE_MPA0	
X28Y0	AK21	5	IO_L53_5/No_Pair	SYSACE_MPD7	
X26Y0	AJ21	5	IO_L50_5/No_Pair	SYSACE_MPD6	
X26Y0	AE19	5	IO_L49N_5	SYSACE_MPD5	
X26Y0	AD19	5	IO_L49P_5	SYSACE_MPD4	
X24Y0	AL23	5	IO_L48N_5	SYSACE_MPD3	11409.38
X24Y0	AL22	5	IO_L48P_5	SYSACE_MPD2	9870.11
X22Y0	AH21	5	IO_L47N_5	SYSACE_MPD1	9029.19
X22Y0	AG21	5	IO_L47P_5	SYSACE_MPD0	8186.49
X22Y0	AF20	5	IO_L46N_5	GND	3969.05
X22Y0	AE20	5	IO_L46P_5	GND	3132.45
X20Y0	AM24	5	IO_L45N_5/VREF_5	GND	12224.04
X20Y0	AL24	5	IO_L45P_5	GND	10900.17
X18Y0	AK22	5	IO_L44N_5	GND	10795.23
X18Y0	AJ22	5	IO_L44P_5	GND	9429.62
X18Y0	AF21	5	IO_L43N_5	GND	5289.64
X18Y0	AE21	5	IO_L43P_5	MASTER_RESET#	3696.3
X12Y0	AK24	5	IO_L39N_5	GND	9736.03
X12Y0	AJ24	5	IO_L39P_5	GND	8630.23
X10Y0	AH22	5	IO_L38N_5	GND	8786.32
X10Y0	AG22	5	IO_L38P_5	LCD_R_W#	8056.83
X10Y0	AF22	5	IO_L37N_5	LCD_RS	3918.86
X10Y0	AE22	5	IO_L37P_5	LCD_E	2723.68
X8Y0	AL27	5	IO_L09N_5/VREF_5	GND	11372.97
X8Y0	AK27	5	IO_L09P_5	LCD_DB7	11420.7
X6Y0	AH25	5	IO_L08N_5	LCD_DB6	8344.01
X6Y0	AG25	5	IO_L08P_5	LCD_DB5	7652.81
X6Y0	AF24	5	IO_L07N_5/VREF_5	LCD_DB4	4532.67
X6Y0	AE24	5	IO_L07P_5	LCD_DB3	3596.07
X4Y0	AM28	5	IO_L06N_5/VRP_5	LCD_DB2	13858.11
X4Y0	AL28	5	IO_L06P_5/VRN_5	LCD_DB1	12527.75
X4Y0	AF25	5	IO_L05_5/No_Pair	LCD_DB0	

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X2Y0	AK28	5	IO_L03N_5/D4	FPGA_D4	
X2Y0	AK29	5	IO_L03P_5/D5	FPGA_D5	
X0Y0	AH26	5	IO_L02N_5/D6	FPGA_D6	
X0Y0	AG26	5	IO_L02P_5/D7	FPGA_D7	
X0Y0	AL29	5	IO_L01N_5/RDWR_B	FPGA_RDWR#	
X0Y0	AL30	5	IO_L01P_5/CS_B	FPGA_CS#	
X0Y0	AJ30	6	IO_L01P_6/VRN_6	R122/C373	10985.88
X0Y1	AJ31	6	IO_L01N_6/VRP_6	R97/C434	11321.01
X1Y0	AJ27	6	IO_L02P_6	QDR_K_n_A	10529.58
X1Y1	AJ28	6	IO_L02N_6	QDR_K_A	11720.34
X1Y2	AK31	6	IO_L03P_6	R_n_ext_A	12761.57
X1Y3	AK32	6	IO_L03N_6/VREF_6	Vref(0.9V)	12802.28
X0Y4	AH29	6	IO_L04P_6	QDR_BW_n_A0	9308.27
X0Y5	AH30	6	IO_L04N_6	QDR_BW_n_A1	9452.34
X1Y4	AH27	6	IO_L05P_6	QDR_BW_n_A2	8891.47
X1Y5	AG28	6	IO_L05N_6	QDR_BW_n_A3	9638.17
X1Y6	AL33	6	IO_L06P_6	QDR_C_n_A	15583.83
X1Y7	AL34	6	IO_L06N_6	QDR_C_A	15821.97
X0Y8	AF31	6	IO_L31P_6	QDR_W_n_A	10021.36
X0Y9	AF32	6	IO_L31N_6	QDR_R_n_A	10624.52
X1Y8	AC25	6	IO_L32P_6	GND	3336.69
X1Y9	AC26	6	IO_L32N_6	GND	4005.01
X1Y10	AG33	6	IO_L33P_6	GND	12391.44
X1Y11	AG34	6	IO_L33N_6/VREF_6	Vref(0.9V)	12986.31
X0Y12	AE30	6	IO_L34P_6	GND	8811.79
X0Y13	AE31	6	IO_L34N_6	GND	9342.05
X1Y12	AD27	6	IO_L35P_6	GND	5651.11
X1Y13	AD28	6	IO_L35N_6	QDR_DWRITE_A35	6675.24
X1Y14	AF33	6	IO_L36P_6	QDR_DWRITE_A34	11948.48
X1Y15	AE33	6	IO_L36N_6	QDR_DWRITE_A33	11537.91
X0Y16	AD29	6	IO_L37P_6	QDR_DWRITE_A32	8070.54
X0Y17	AD30	6	IO_L37N_6	QDR_DWRITE_A31	8126.55
X1Y16	AB25	6	IO_L38P_6	QDR_DWRITE_A30	2906.72

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X1Y17	AB26	6	IO_L38N_6	QDR_DWRITE_A29	3854.3
X1Y18	AD31	6	IO_L39P_6	QDR_DWRITE_A28	9046.71
X1Y19	AD32	6	IO_L39N_6/VREF_6	Vref(0.9V)	9751.53
X0Y20	AC28	6	IO_L40P_6	QDR_DWRITE_A27	5779.09
X0Y21	AC29	6	IO_L40N_6	QDR_DWRITE_A26	6521.49
X1Y20	AB27	6	IO_L41P_6	QDR_DWRITE_A25	5038.48
X1Y21	AB28	6	IO_L41N_6	QDR_DWRITE_A24	5986.05
X1Y22	AE34	6	IO_L42P_6	QDR_DWRITE_A23	12534.09
X1Y23	AD34	6	IO_L42N_6	QDR_DWRITE_A22	12256.07
X0Y24	AC31	6	IO_L43P_6	QDR_DWRITE_A21	8911.96
X0Y25	AC32	6	IO_L43N_6	QDR_DWRITE_A20	9702.33
X1Y24	AA25	6	IO_L44P_6	QDR_DWRITE_A19	2717.14
X1Y25	AA26	6	IO_L44N_6	QDR_DWRITE_A18	3704.71
X1Y26	AD33	6	IO_L45P_6	QDR_DWRITE_A17	11866.32
X1Y27	AC33	6	IO_L45N_6/VREF_6	Vref(0.9V)	10601.93
X0Y28	AB29	6	IO_L46P_6	QDR_DWRITE_A16	6629.5
X0Y29	AB30	6	IO_L46N_6	QDR_DWRITE_A15	7371.9
X1Y28	AA27	6	IO_L47P_6	QDR_DWRITE_A14	4888.88
X1Y29	AA28	6	IO_L47N_6	QDR_DWRITE_A13	5836.46
X1Y30	AB31	6	IO_L48P_6	QDR_DWRITE_A12	8556.07
X1Y31	AB32	6	IO_L48N_6	QDR_DWRITE_A11	9319.47
X0Y32	AA29	6	IO_L49P_6	QDR_DWRITE_A10	7555.89
X0Y33	AA30	6	IO_L49N_6	QDR_DWRITE_A9	7683.23
X1Y32	Y25	6	IO_L50P_6	QDR_DWRITE_A8	2606.42
X1Y33	Y26	6	IO_L50N_6	QDR_DWRITE_A7	3554
X1Y34	AC34	6	IO_L51P_6	QDR_DWRITE_A6	12342.28
X1Y35	AB34	6	IO_L51N_6/VREF_6	Vref(0.9V)	12006.27
X0Y36	AA31	6	IO_L52P_6	QDR_DWRITE_A5	8801.88
X0Y37	AA32	6	IO_L52N_6	QDR_DWRITE_A4	9502.86
X1Y36	W25	6	IO_L53P_6	QDR_DWRITE_A3	2590.48
X1Y37	W26	6	IO_L53N_6	QDR_DWRITE_A2	3619.48
X1Y38	AB33	6	IO_L54P_6	QDR_DWRITE_A1	11488.21
X1Y39	AA33	6	IO_L54N_6	QDR_DWRITE_A0	10317.88
X0Y40	Y28	6	IO_L55P_6	GND	5219.05

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X0Y41	Y29	6	IO_L55N_6	GND	5961.45
X1Y40	W27	6	IO_L56P_6	GND	4826.38
X1Y41	W28	6	IO_L56N_6	GND	5773.96
X1Y42	Y31	6	IO_L57P_6	QDR_SA_A17	8145.63
X1Y43	Y32	6	IO_L57N_6/VREF_6	Vref(0.9V)	8909.69
X0Y44	W29	6	IO_L58P_6	QDR_SA_A16	5936.59
X0Y45	W30	6	IO_L58N_6	QDR_SA_A15	6678.99
X1Y44	W24	6	IO_L59P_6	QDR_SA_A14	1610.19
X1Y45	V24	6	IO_L59N_6	QDR_SA_A13	1638.53
X1Y46	AA34	6	IO_L60P_6	QDR_SA_A12	11691.6
X1Y47	Y34	6	IO_L60N_6	QDR_SA_A11	11148.48
X0Y48	W31	6	IO_L85P_6	QDR_SA_A10	8159.47
X0Y49	W32	6	IO_L85N_6	QDR_SA_A9	8919.9
X1Y48	V25	6	IO_L86P_6	QDR_SA_A8	2405.17
X1Y49	V26	6	IO_L86N_6	QDR_SA_A7	3327.27
X1Y50	Y33	6	IO_L87P_6	QDR_SA_A6	10611.96
X1Y51	W33	6	IO_L87N_6/VREF_6	Vref(0.9V)	9812.03
X0Y52	V29	6	IO_L88P_6	QDR_SA_A5	5998.02
X0Y53	V30	6	IO_L88N_6	QDR_SA_A4	6547.9
X1Y52	V27	6	IO_L89P_6	QDR_SA_A3	4483.54
X1Y53	V28	6	IO_L89N_6	QDR_SA_A2	5407.06
X1Y54	V31	6	IO_L90P_6	QDR_SA_A1	7799.59
X1Y55	V32	6	IO_L90N_6	QDR_SA_A0	8537.7
X0Y56	U32	7	IO_L90P_7	GND	8839.91
X0Y57	U31	7	IO_L90N_7	GND	7626.14
X0Y58	U28	7	IO_L89P_7	QDR_DREAD_A0	5511.92
X0Y59	U27	7	IO_L89N_7	QDR_DREAD_A1	4393.22
X1Y58	V33	7	IO_L88P_7	GND	10394.2
X1Y59	U33	7	IO_L88N_7/VREF_7	Vref(0.9V)	9665.64
X0Y60	U30	7	IO_L87P_7	QDR_DREAD_A2	6851.4
X0Y61	U29	7	IO_L87N_7	QDR_DREAD_A3	5801.93
X0Y62	U26	7	IO_L86P_7	QDR_DREAD_A4	3459.01
X0Y63	U25	7	IO_L86N_7	QDR_DREAD_A5	2340.31

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X1Y62	T32	7	IO_L85P_7	QDR_DREAD_A6	9056.44
X1Y63	T31	7	IO_L85N_7	QDR_DREAD_A7	7724.5
X0Y64	T30	7	IO_L60P_7	GND	7055.3
X0Y65	T29	7	IO_L60N_7	GND	6031.43
X0Y66	T28	7	IO_L59P_7	GND	5872.43
X0Y67	T27	7	IO_L59N_7	GND	4753.73
X1Y66	T33	7	IO_L58P_7	QDR_CQ_A	10173.21
X1Y67	R33	7	IO_L58N_7/VREF_7	Vref(0.9V)	9961.47
X0Y68	R32	7	IO_L57P_7	QDR_DREAD_A8	9271.49
X0Y69	R31	7	IO_L57N_7	QDR_DREAD_A9	8013.89
X0Y70	T26	7	IO_L56P_7	QDR_DREAD_A10	3871.63
X0Y71	T25	7	IO_L56N_7	QDR_DREAD_A11	2752.93
X1Y70	R34	7	IO_L55P_7	QDR_DREAD_A12	11455.67
X1Y71	P34	7	IO_L55N_7	QDR_DREAD_A13	11291.77
X0Y72	R29	7	IO_L54P_7	QDR_DREAD_A14	6425.42
X0Y73	R28	7	IO_L54N_7	QDR_DREAD_A15	4872.84
X0Y74	U24	7	IO_L53P_7	QDR_DREAD_A16	1919.47
X0Y75	T24	7	IO_L53N_7	QDR_DREAD_A17	1247.81
X1Y74	P32	7	IO_L52P_7	GND	9339.48
X1Y75	P31	7	IO_L52N_7/VREF_7	Vref(0.9V)	8102.88
X0Y76	P30	7	IO_L51P_7	GND	7603.44
X0Y77	P29	7	IO_L51N_7	GND	6499.99
X0Y78	R26	7	IO_L50P_7	QDR_DREAD_A18	3672.29
X0Y79	R25	7	IO_L50N_7	QDR_DREAD_A19	2488.12
X1Y78	P33	7	IO_L49P_7	QDR_DREAD_A20	10530.82
X1Y79	N33	7	IO_L49N_7	QDR_DREAD_A21	10426.76
X0Y80	N32	7	IO_L48P_7	QDR_DREAD_A22	9778.21
X0Y81	N31	7	IO_L48N_7	QDR_DREAD_A23	8437.77
X0Y82	P28	7	IO_L47P_7	QDR_DREAD_A24	5954.75
X0Y83	P27	7	IO_L47N_7	QDR_DREAD_A25	4770.58
X1Y82	N34	7	IO_L46P_7	GND	11804.99
X1Y83	M34	7	IO_L46N_7/VREF_7	Vref(0.9V)	11667.8
X0Y84	N30	7	IO_L45P_7	GND	7563.61
X0Y85	N29	7	IO_L45N_7	GND	6306.01

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X0Y86	P26	7	IO_L44P_7	GND	3823
X0Y87	P25	7	IO_L44N_7	GND	2638.82
X1Y86	M32	7	IO_L43P_7	QDR_CQ_n_A	9772.91
X1Y87	M31	7	IO_L43N_7	GND	8536.05
X0Y88	L32	7	IO_L42P_7	QDR_DREAD_A26	10259.17
X0Y89	L31	7	IO_L42N_7	QDR_DREAD_A27	9001.57
X0Y90	N28	7	IO_L41P_7	QDR_DREAD_A28	6104.35
X0Y91	N27	7	IO_L41N_7	QDR_DREAD_A29	4920.17
X1Y90	M33	7	IO_L40P_7	GND	12186.54
X1Y91	L33	7	IO_L40N_7/VREF_7	Vref(0.9V)	11195.56
X0Y92	M29	7	IO_L39P_7	QDR_DREAD_A30	6975.04
X0Y93	M28	7	IO_L39N_7	QDR_DREAD_A31	5610.09
X0Y94	N26	7	IO_L38P_7	QDR_DREAD_A32	3972.59
X0Y95	N25	7	IO_L38N_7	QDR_DREAD_A33	2788.42
X1Y94	L34	7	IO_L37P_7	QDR_DREAD_A34	12451.17
X1Y95	K34	7	IO_L37N_7	QDR_DREAD_A35	12423.45
X0Y96	L30	7	IO_L36P_7	GND	8143.52
X0Y97	L29	7	IO_L36N_7	R_n_int_A	7340.48
X0Y98	L28	7	IO_L35P_7	GND	6793.53
X0Y99	L27	7	IO_L35N_7	GND	5592.79
X1Y98	K33	7	IO_L34P_7	GND	11352.59
X1Y99	J33	7	IO_L34N_7/VREF_7	Vref(0.9V)	12123.95
X0Y100	K31	7	IO_L33P_7	GND	9537.04
X0Y101	K30	7	IO_L33N_7	GND	8267.43
X0Y102	M26	7	IO_L32P_7	GND	4123.3
X0Y103	M25	7	IO_L32N_7	GND	3062.48
X1Y102	H34	7	IO_L31P_7	GND	13451.41
X1Y103	H33	7	IO_L31N_7	GND	12137.04
X0Y104	F31	7	IO_L06P_7	GND	11858.77
X0Y105	F30	7	IO_L06N_7	GND	10666.81
X0Y106	J28	7	IO_L05P_7	GND	7292.33
X0Y107	J27	7	IO_L05N_7	GND	6469.14
X1Y106	E34	7	IO_L04P_7	GND	15132.61
X1Y107	E33	7	IO_L04N_7/VREF_7	Vref(0.9V)	13663.12

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
X0Y108	E32	7	IO_L03P_7	GND	13396.34
X0Y109	E31	7	IO_L03N_7	GND	11802.85
X0Y110	F28	7	IO_L02P_7	GND	11146.23
X0Y111	F27	7	IO_L02N_7	GND	12438.46
X1Y110	D34	7	IO_L01P_7/VRN_7	R98/C374	15547.77
X1Y111	D33	7	IO_L01N_7/VRP_7	R99/C435	14050.12
	J26		PROG_B	PROG_B	
	K25		HSWAP_EN	HSWAP	
	K26		DXP		
	G27		DXN		
	G8		RSVD		
	K9		VBATT	GND	
	K10		TMS	JTAG_TMS	
	J9		TCK	JTAG_TCK	
	H7		DO	FPGA_TDO	
	AE9		CCLK	FPGA_CCLK	
	AF9		PWRDWN_B	PWRDWN	
	AE10		DONE	FPGA_DONE	
	AE25		M2	M2	
	AF26		M0	M0	
	AE26		M1	M1	
	H28		TDI	FPGA_TDI	
	A29		TXNPAD4		
	A28		TXPPAD4		
	A27		RXPPAD4		
	A26		RXNPAD4		
	A21		TXNPAD6		
	A20		TXPPAD6		
	A19		RXPPAD6		
	A18		RXNPAD6		
	A17		TXNPAD7		
	A16		TXPPAD7		
	A15		RXPPAD7		

Table 2-1: **FPGA Pin Out**

Slice Coordinates	Pin Numbers	Virtex-II Pro Bank Number	Package Functional Name	I/O Pin Names	Package Flight Times (In Microns)
	A14		RXNPAD7		
	A9		TXNPAD9		
	A8		TXPPAD9		
	A7		RXPPAD9		
	A6		RXNPAD9		
	AP6		RXNPAD16		
	AP7		RXPPAD16		
	AP8		TXPPAD16		
	AP9		TXNPAD16		
	AP14		RXNPAD18		
	AP15		RXPPAD18		
	AP16		TXPPAD18		
	AP17		TXNPAD18		
	AP18		RXNPAD19		
	AP19		RXPPAD19		
	AP20		TXPPAD19		
	AP21		TXNPAD19		
	AP26		RXNPAD21		
	AP27		RXPPAD21		
	AP28		TXPPAD21		
	AP29		TXNPAD21		

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Appendix 3

Memory Board Schematics and Characterization Results

This section provides schematics for the ML365 Virtex II QDR SRAM Memory Demonstration Board, as well as characterization results.

Schematics

The pages that follow show the schematics for the ML365 Memory board:

Sheet#	Rev#	Description
1	12	Notes Page
2	0	Top Hierarchical Block Diagram
3	0	Clock Sources: Epson EC2121CA OSC, SMA's
4	3	SystemAce Controller & CF Socket, JTAG Conn.
5	8	QDRII Samsung K7R323684M-FC20 SRAM 1 (A)
6	5	QDRII SRAM 1 Termination Resistors
7	8	QDRII Samsung K7R323684M-FC20 SRAM 2 (B)
8	5	QDRII SRAM 2 Termination Resistors placeholder
9	8	QDRII Samsung K7R323684M-FC25 SRAM 3 (C)
10	5	QDRII SRAM 3 Termination Resistors placeholder
11	11	XC2VP20 Bank 0 VCCo=+1.8V, VRef=+0.9V_FPGA
12	11	XC2VP20 Bank 1 VCCo=+1.8V, VRef=+0.9V_FPGA
13	11	XC2VP20 Bank 2 VCCo=+1.8V, VRef=+0.9V_FPGA
14	11	XC2VP20 Bank 3 VCCo=+1.8V, VRef=+0.9V_FPGA
15	12	XC2VP20 Bank 4 RS232 I/F & User PB/LED VCCo=+2.5V, VRef=None
16	5	XC2VP20 Bank 5 SystemACE I/F, LCD I/F, SelectMAP header VCCo=+2.5V, VRef=None
17	11	XC2VP20 Bank 6 QDRII SRAM 1 DWRITE & ADDRESS I/F VCCo=+1.8V, VRef=+0.9V_FPGA
18	11	XC2VP20 Bank 7 QDRII SRAM 1 DREAD I/F VCCo=+1.8V, Vref=+0.9V_FPGA
19	5	XC2VP20 Config Block, XCONFIG Conn., JTAG jumpers, VCCINT, VCCAUX, GND blocks
20	0	XC2VP20 MGT's not used, wired to +2.5V
21	0	XC2VP20 No Connect blocks, wired to GND
22	0	LCD I/F Connector, MC74LCX541D level shifters
23	0	RS232 I/F MAX3316ECUP 2.5V & DB9F Serial Connector
24	0	Power: +5V, +3.3V, +2.5V, +1.5V
25	5	Power: +1.8V, +0.9V_QDR, +0.9V_FPGA
26	9	Decoupling Caps for FPGA and QDR
27	10	Additional Decoupling Caps
28	12	Rev. Notes

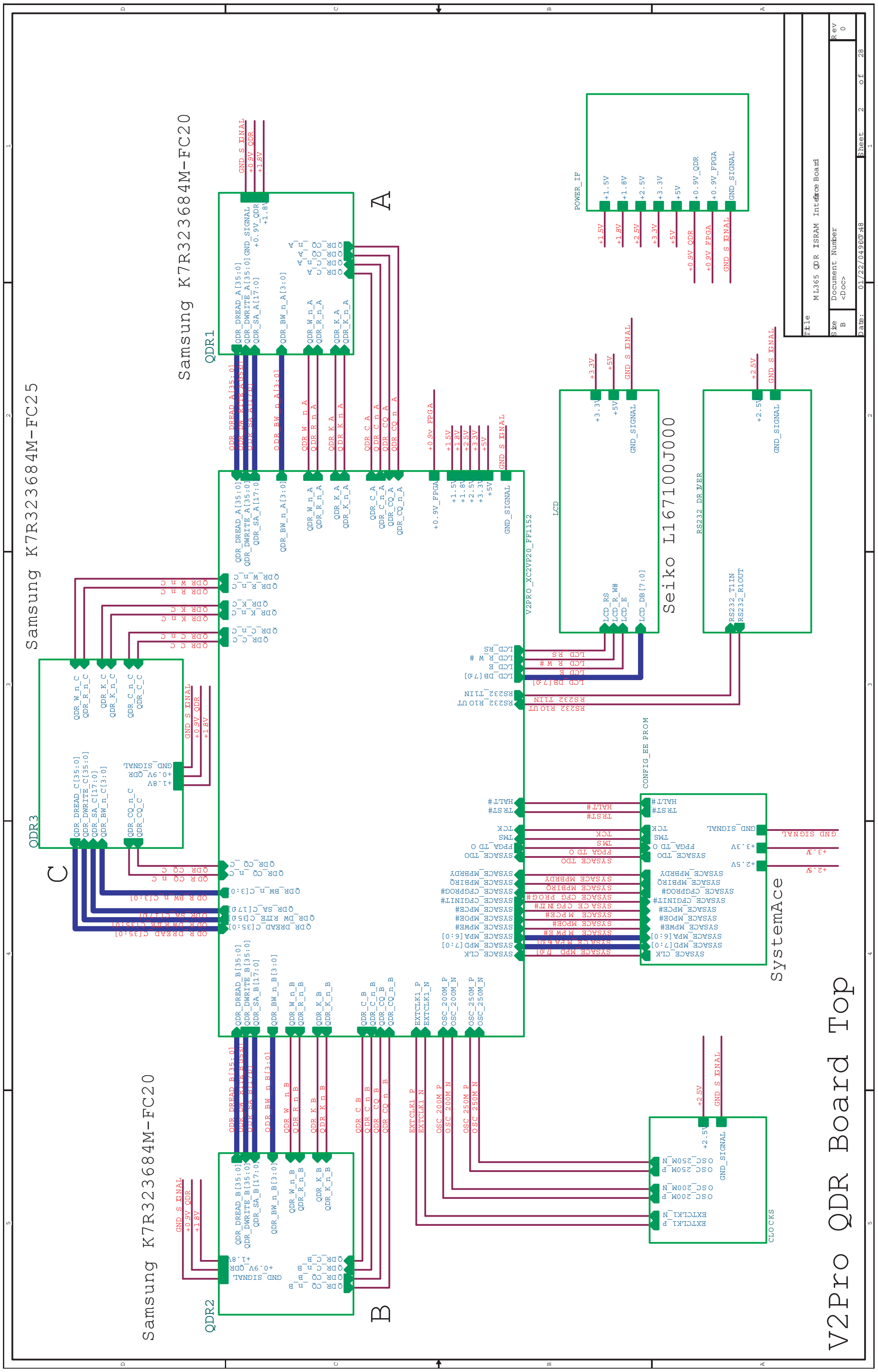
Revision Notes are on Sheet 28

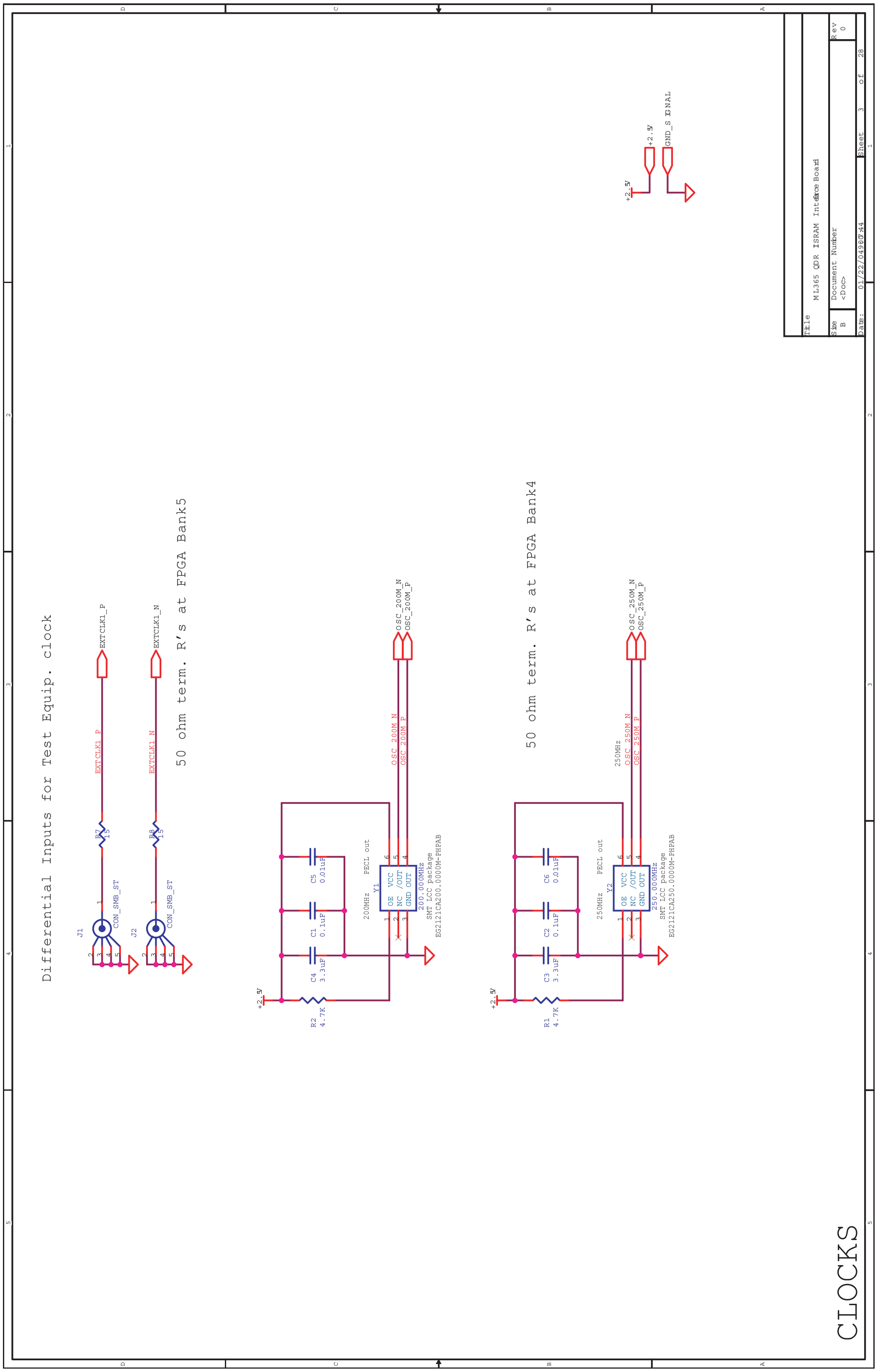
Highest Ref. Des. #:
C435
D11
J5
L5
P47
Q8
R538
SW8
U13
Y3

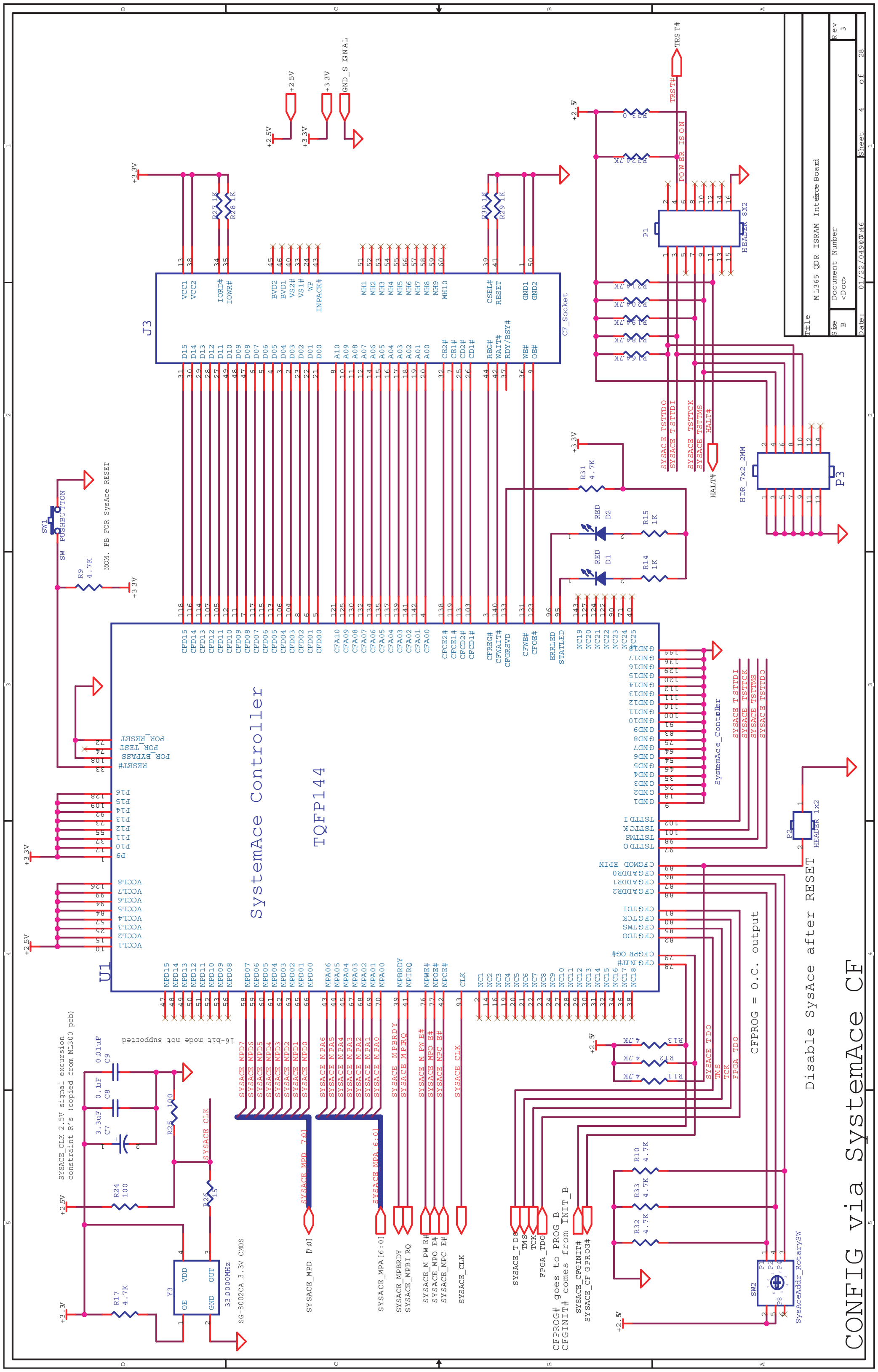
Notes Page

Latest Schematic Rev.: 12, on Date 03/15/2004

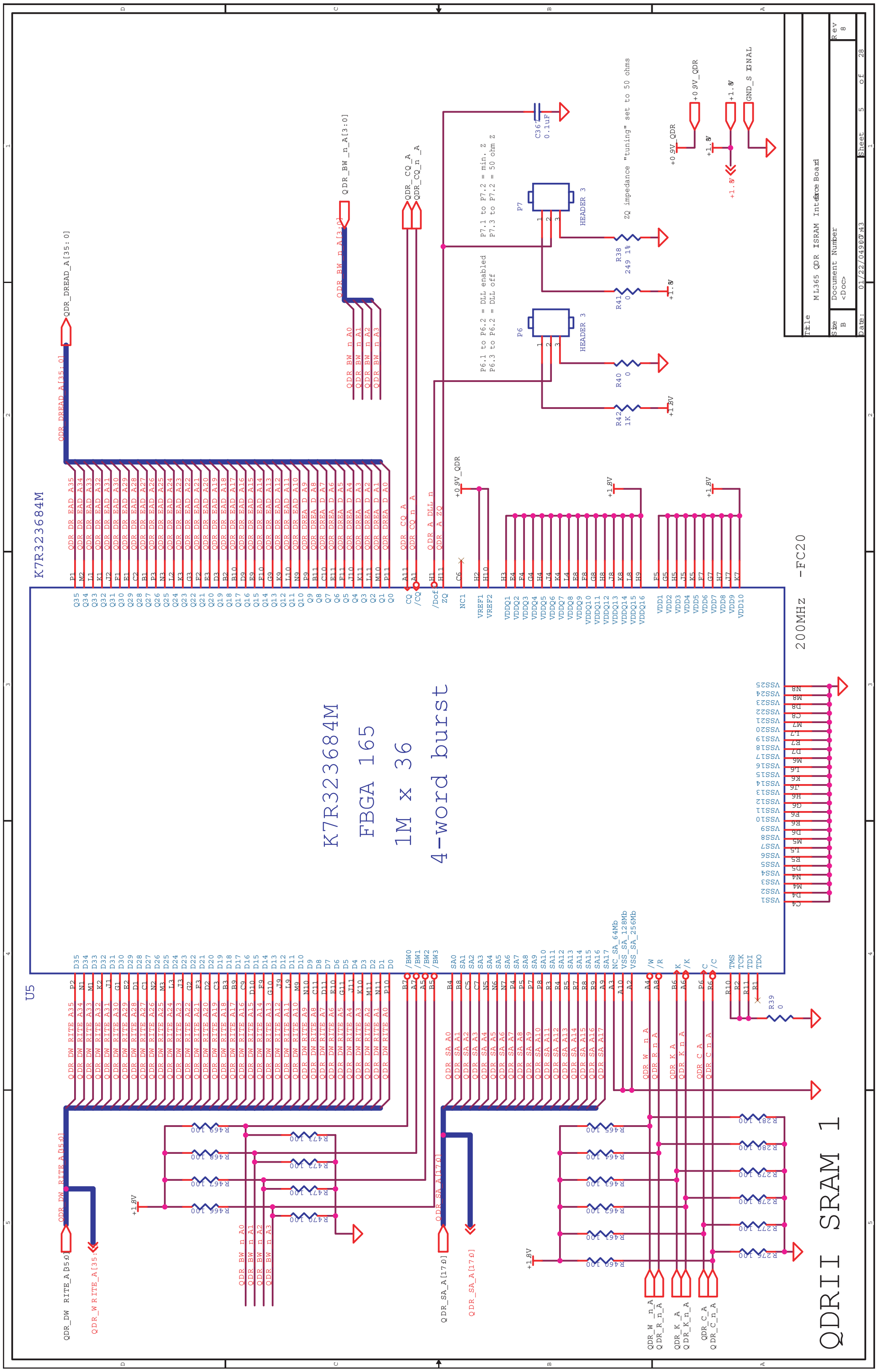
Title	ML365 QDR ISRAM Interface Board		
Size B	Document Number <Doc>		Rev 12
Date: 05/17/04		Sheet 1 of 28	


V2Pro QDR Board Top
Samsung K7R323684M-FC20
QDR1
A
Samsung K7R323684M-FC25
QDR3
C
Samsung K7R323684M-FC20
QDR2
B
V2PRO_XC2VP20_FF1152
Seiko L167100J000
LCD
RS232_DRIVER
POWER_IF
SystemAce
CONFIG_EE_PROM
CLOCKS
ML365 QDR SRAM Interface Board

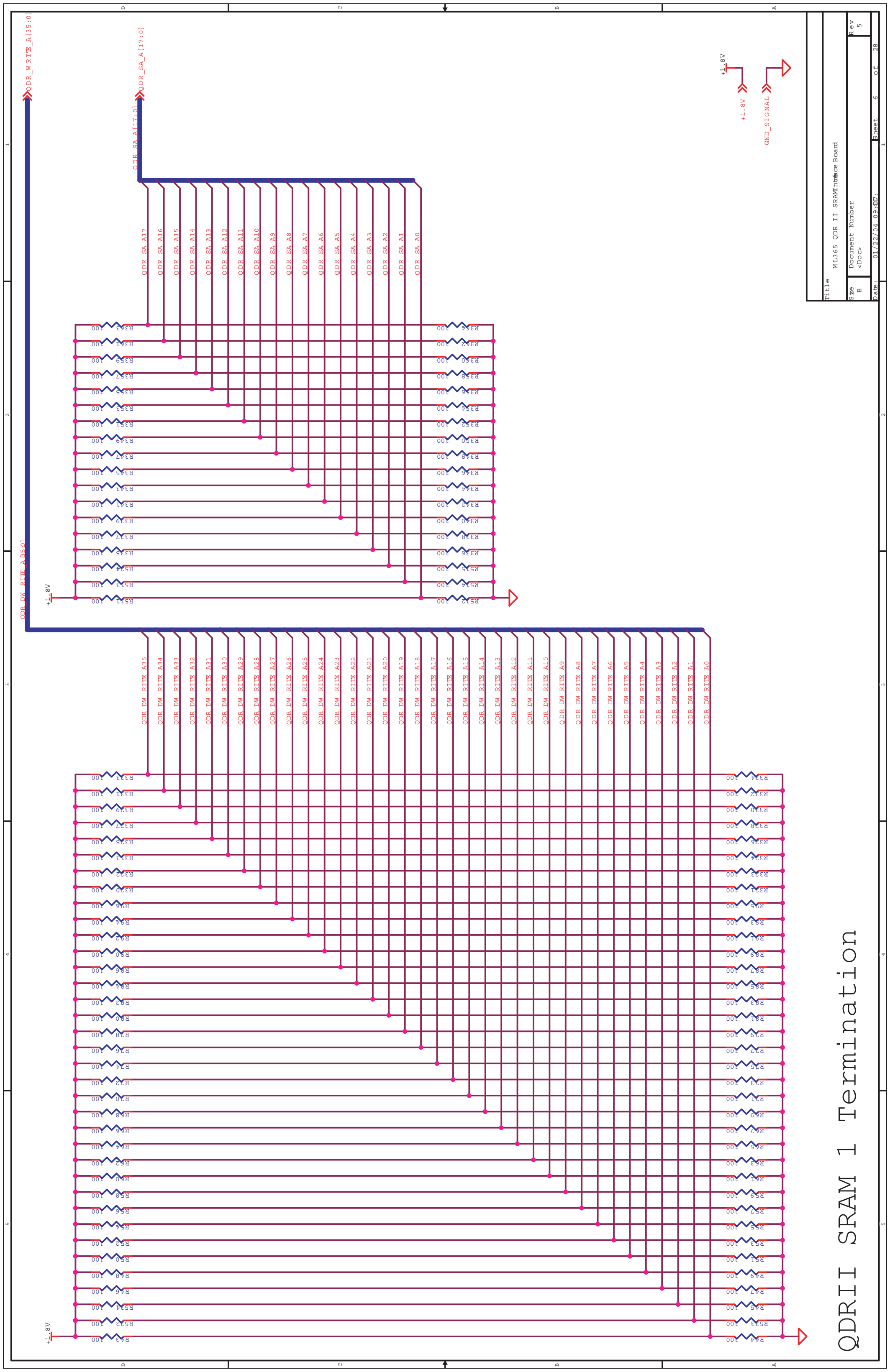

Differential Inputs for Test Equip. clock
50 ohm term. R's at FPGA Bank5
50 ohm term. R's at FPGA Bank4
EXTCLK1_P
EXTCLK1_N
OSC_200M_N
OSC_200M_P
OSC_250M_N
OSC_250M_P
ML365 QDR ISRAM Interface Board
CLOCKS

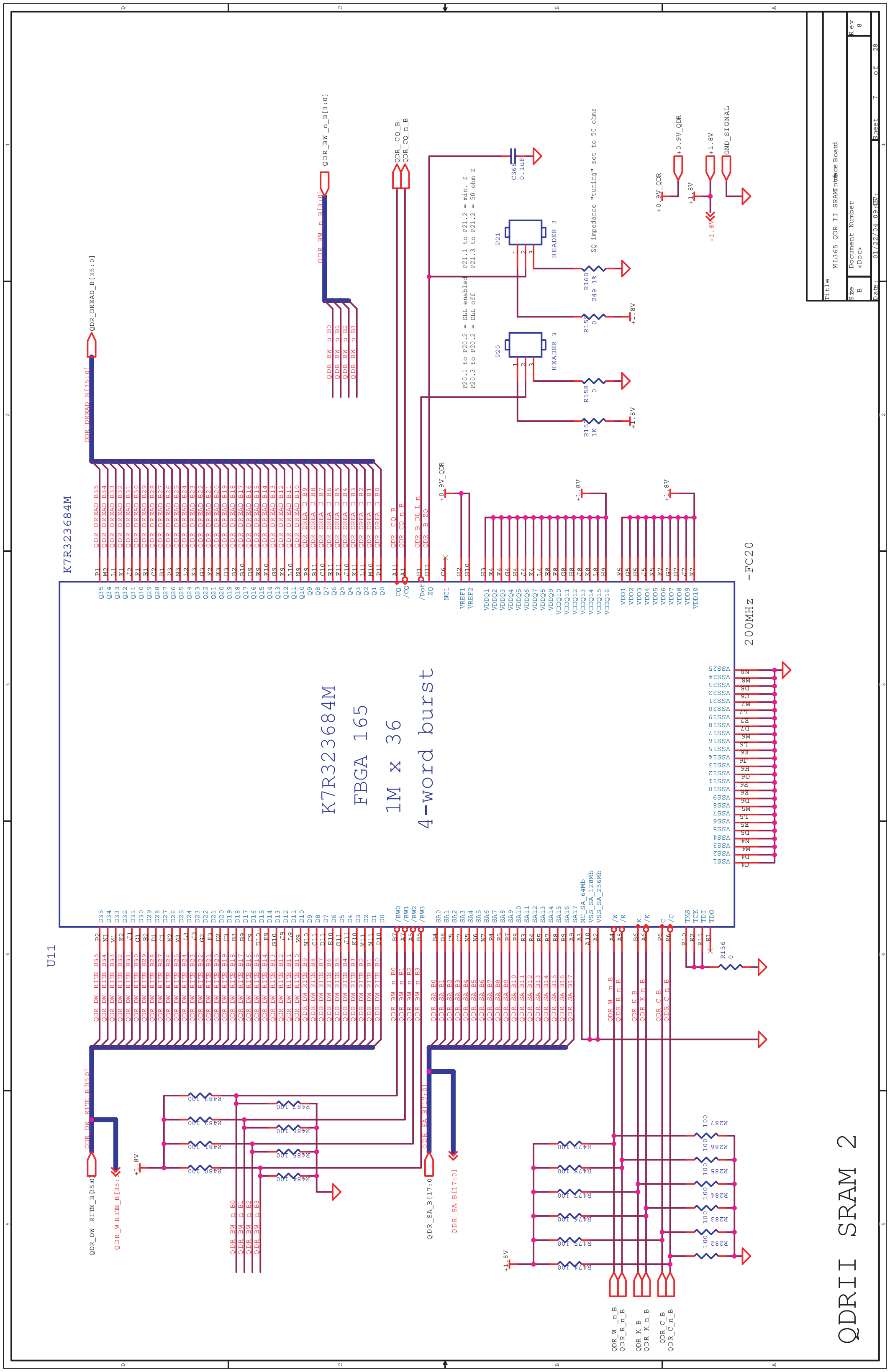


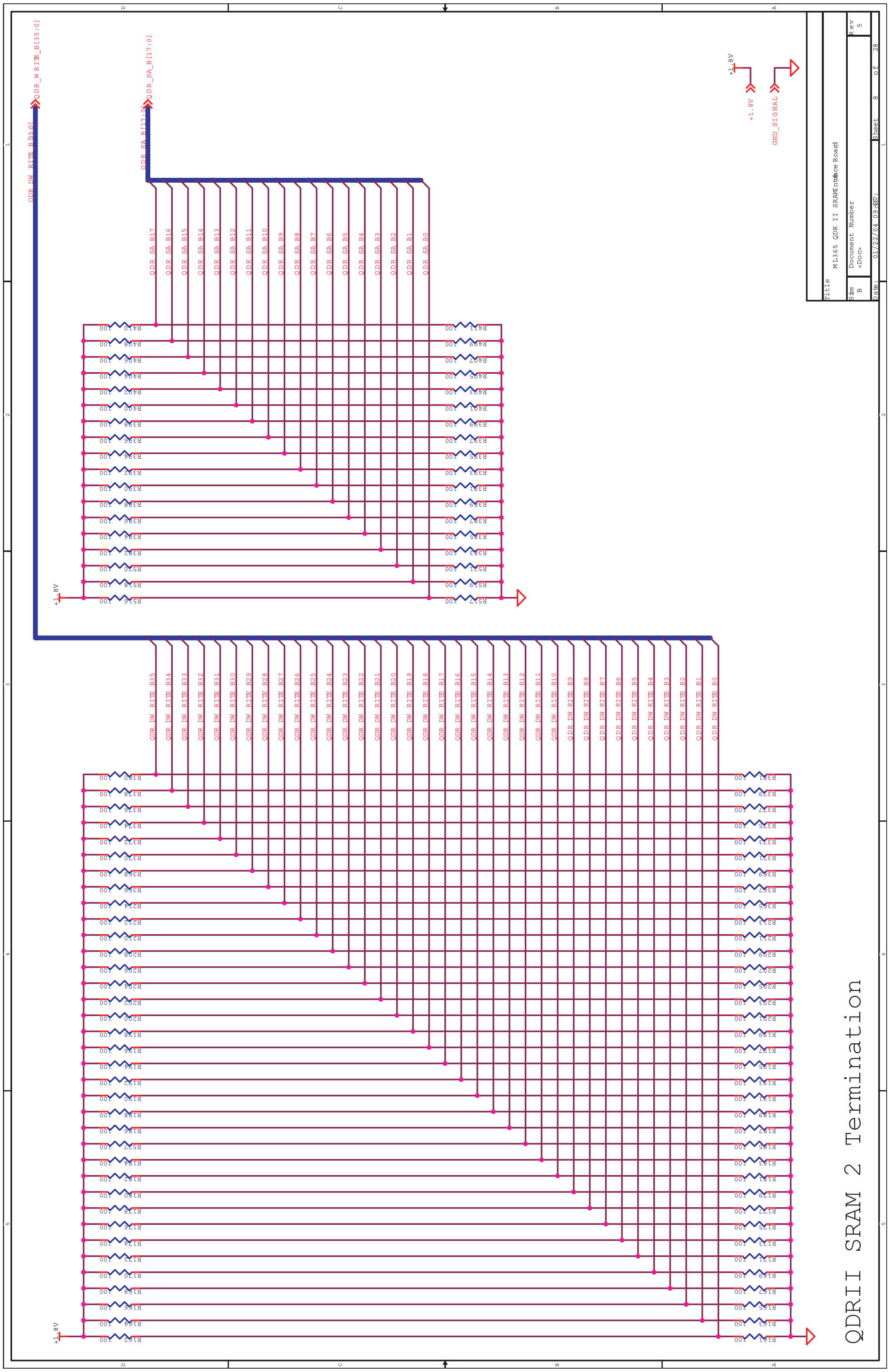
SystemAce Controller
TQFP144
U1
J3
CF_Socket
CONFIG via SystemAce CF
Disable SysAce after RESET
CFPROG = O.C. output

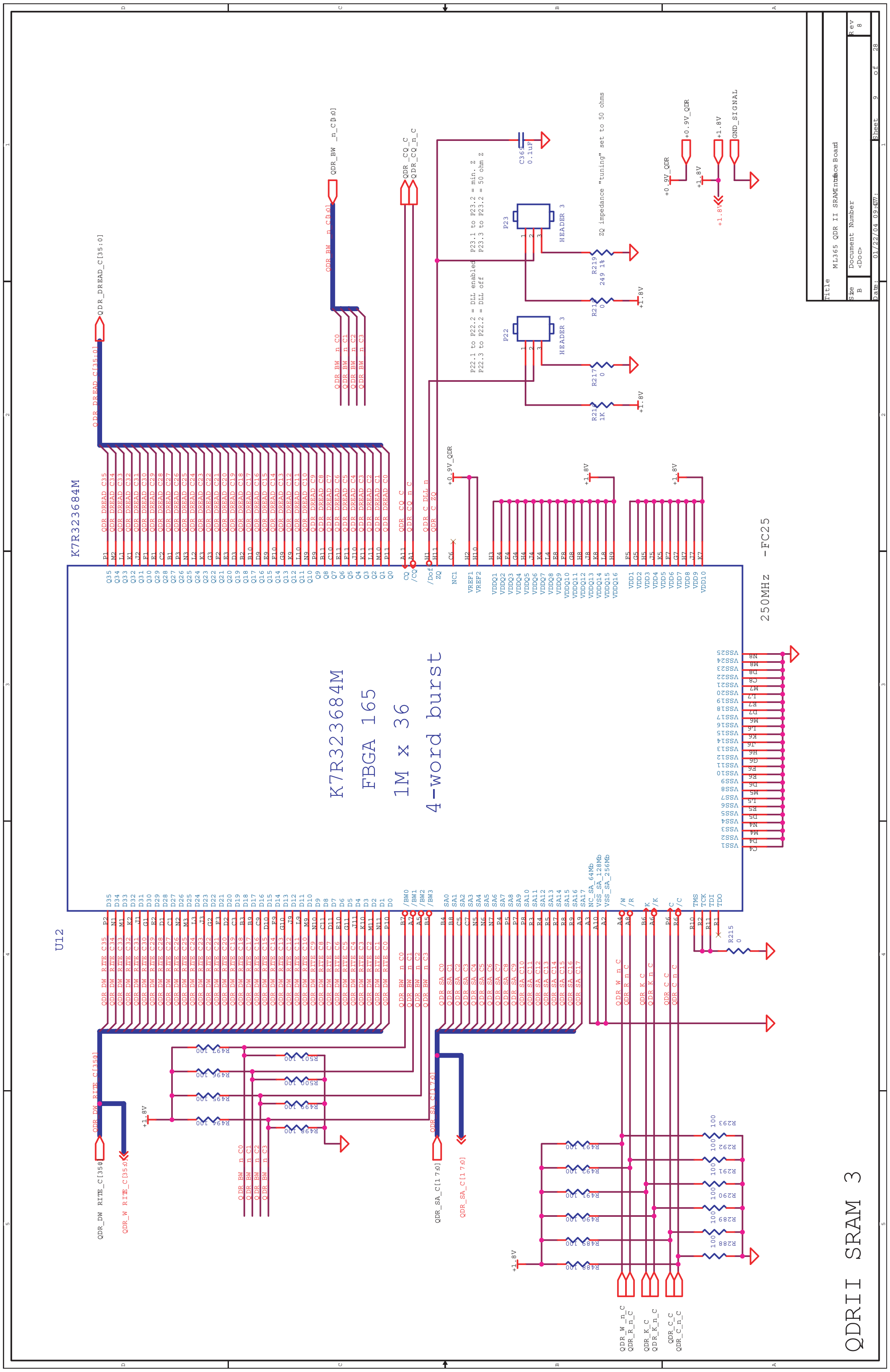


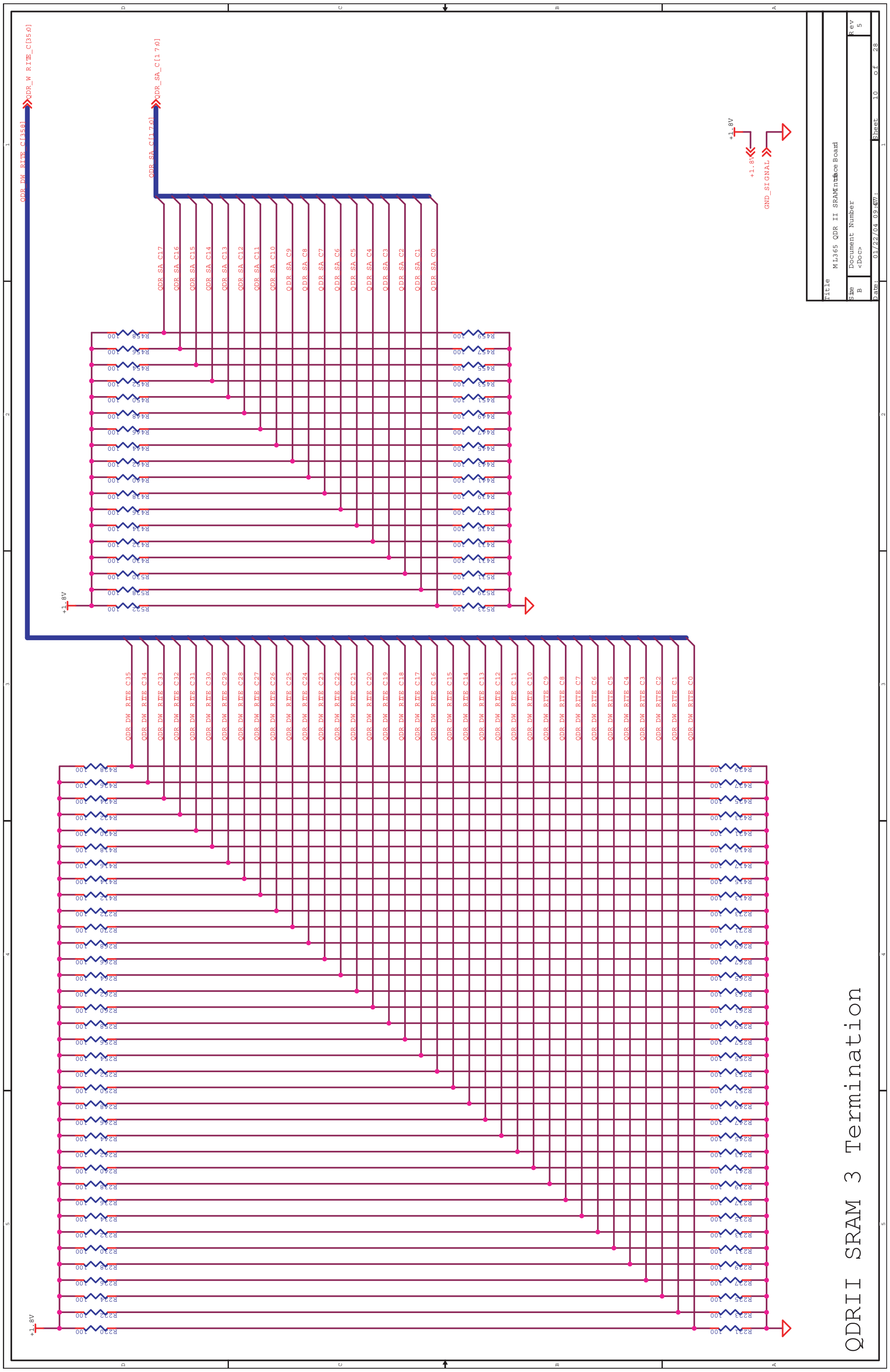
K7R323684M
FBGA 165
1M x 36
4-word burst
200MHz -FC20
QDRII SRAM 1

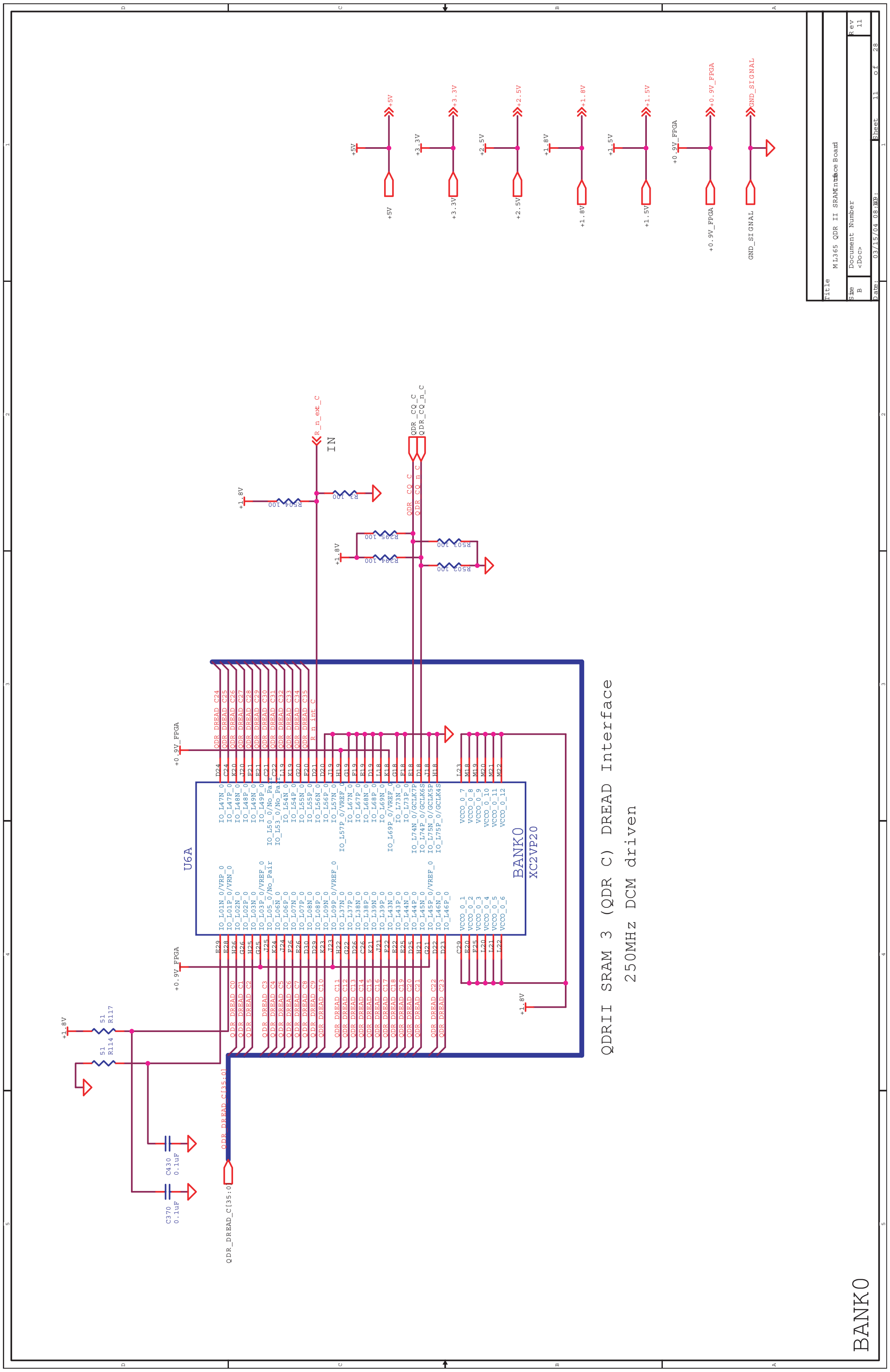

QDRII SRAM 1 Termination

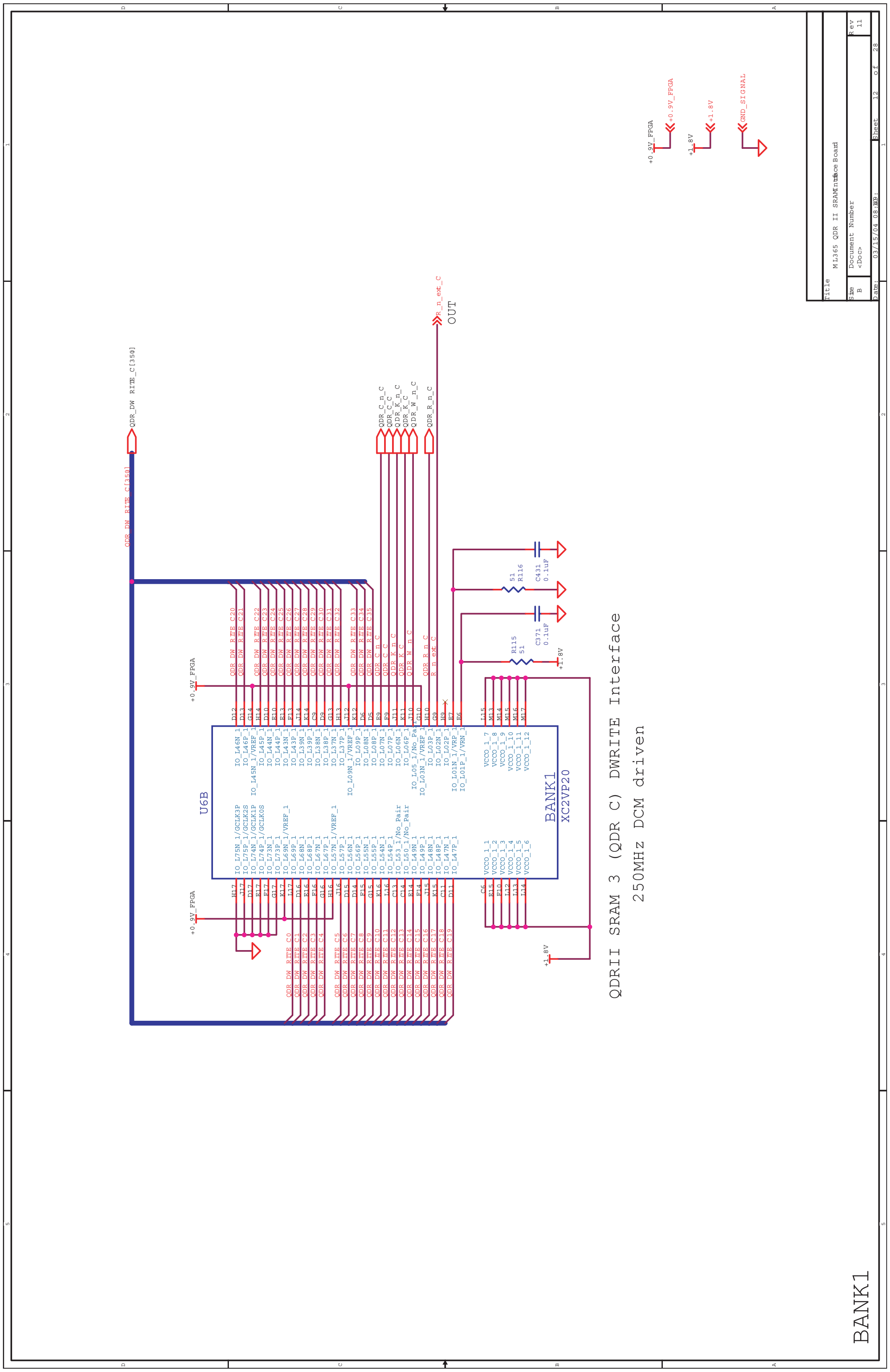

QDRII SRAM 2
K7R323684M
FBGA 165
1M x 36
4-word burst
200MHz
U11
ZQ impedance "tuning" set to 50 ohms

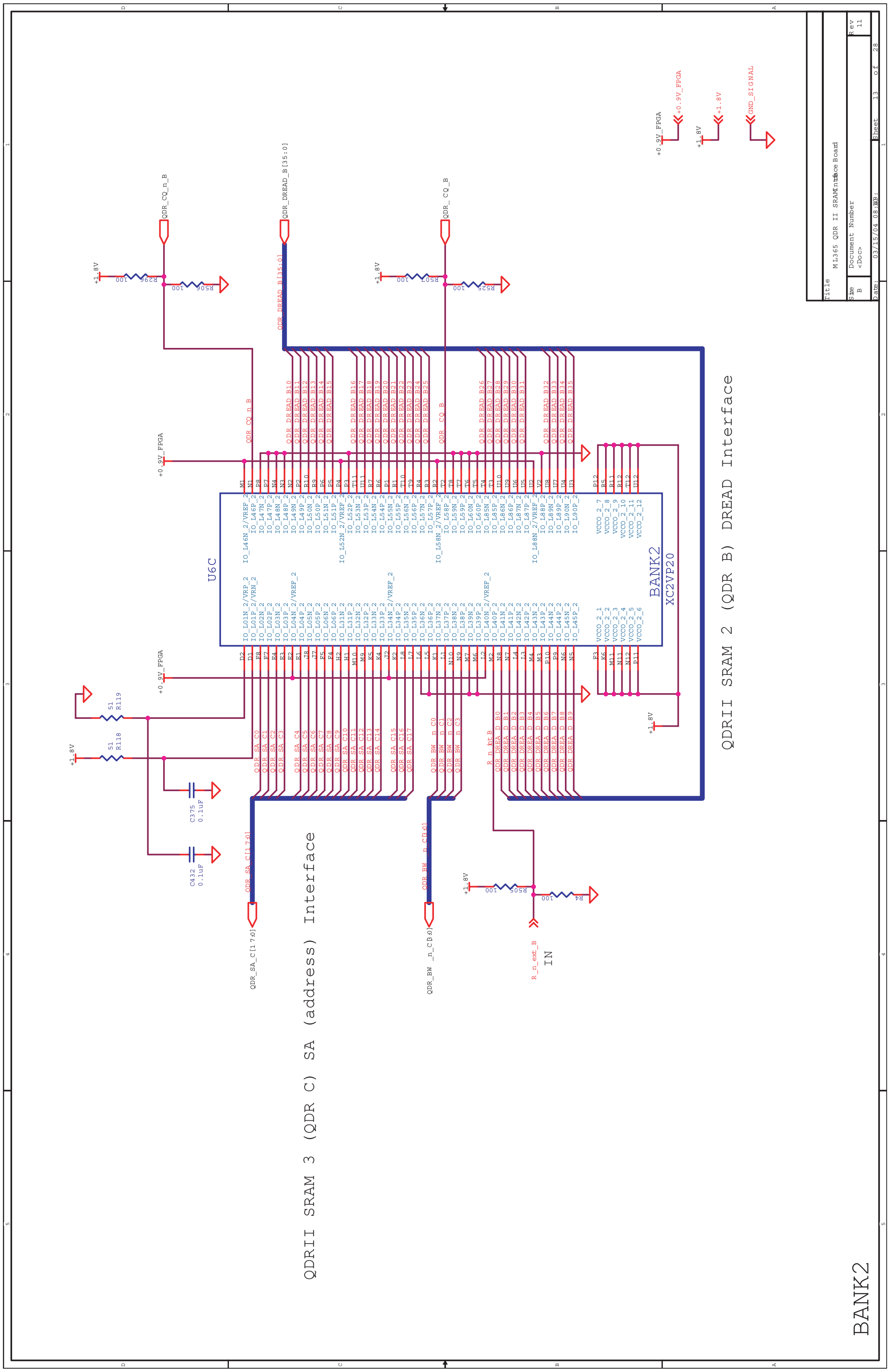

QDRII SRAM 2 Termination

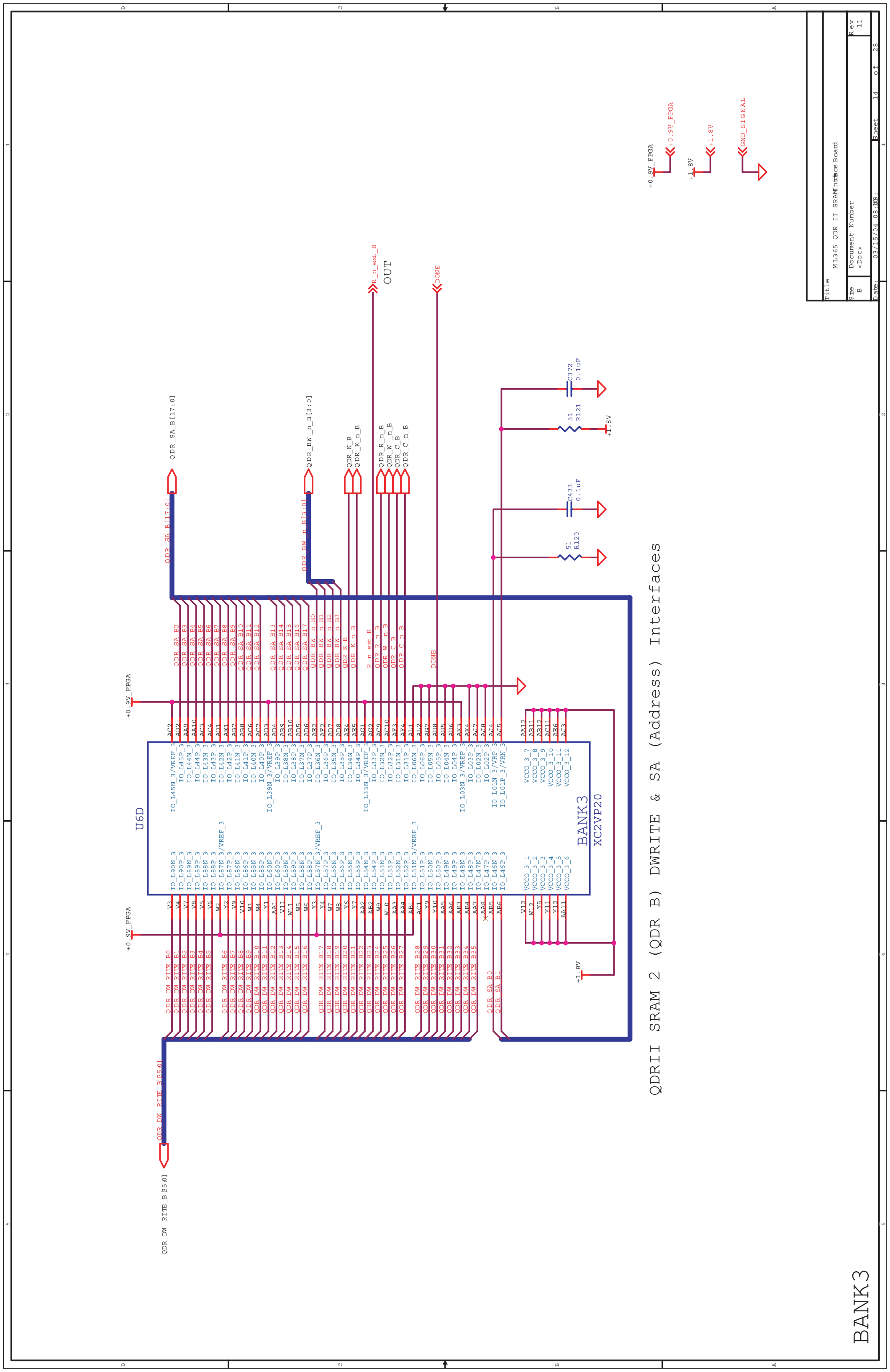

K7R323684M
FBGA 165
1M x 36
4-word burst
250MHz -FC25
QDRII SRAM 3
U12

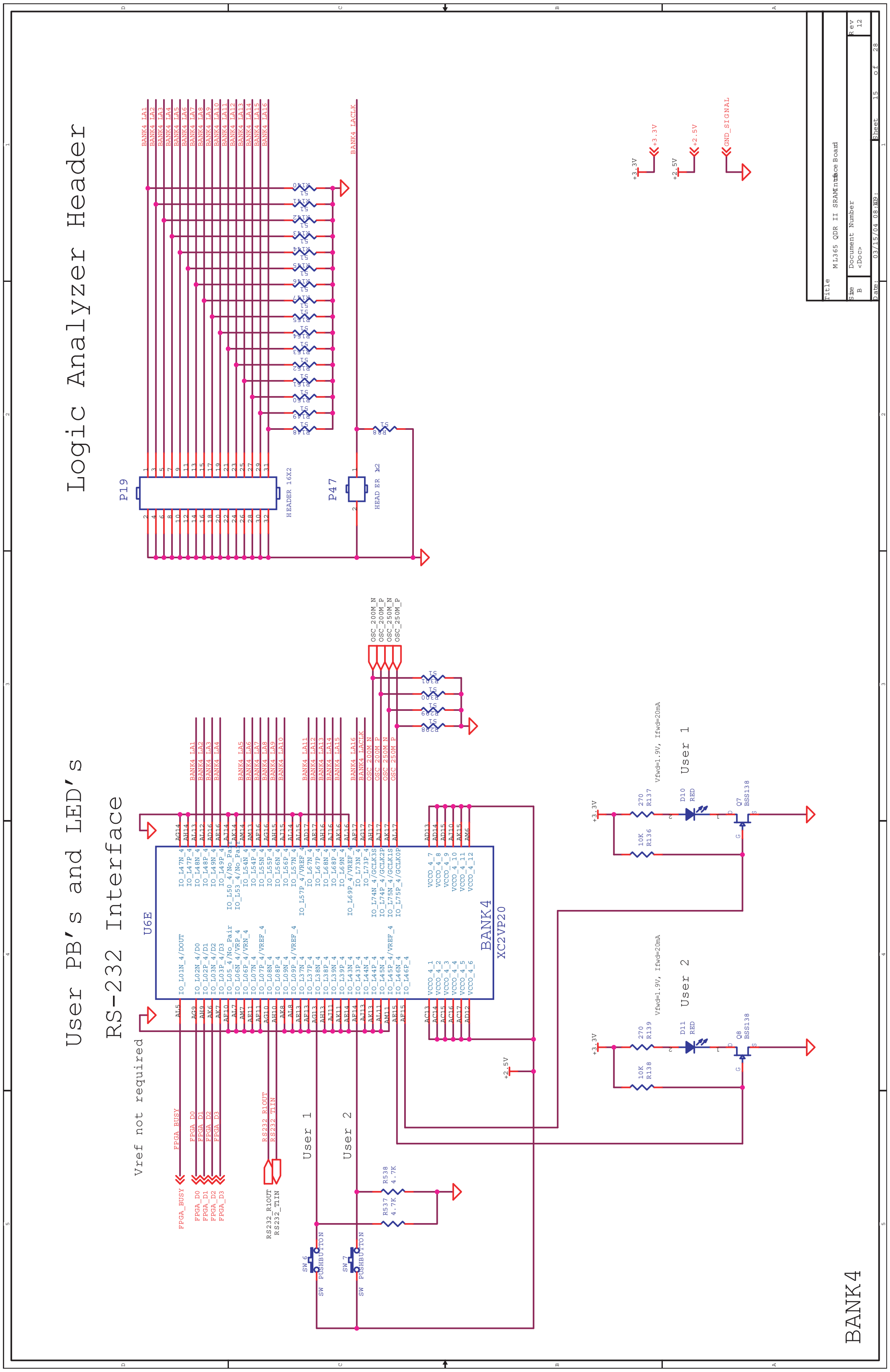

QDRII SRAM 3 Termination


QDRII SRAM 3 (QDR C) DREAD Interface
250MHz DCM driven
U6A
BANK0
XC2VP20
ML365 QDR II SRAM Interface Board

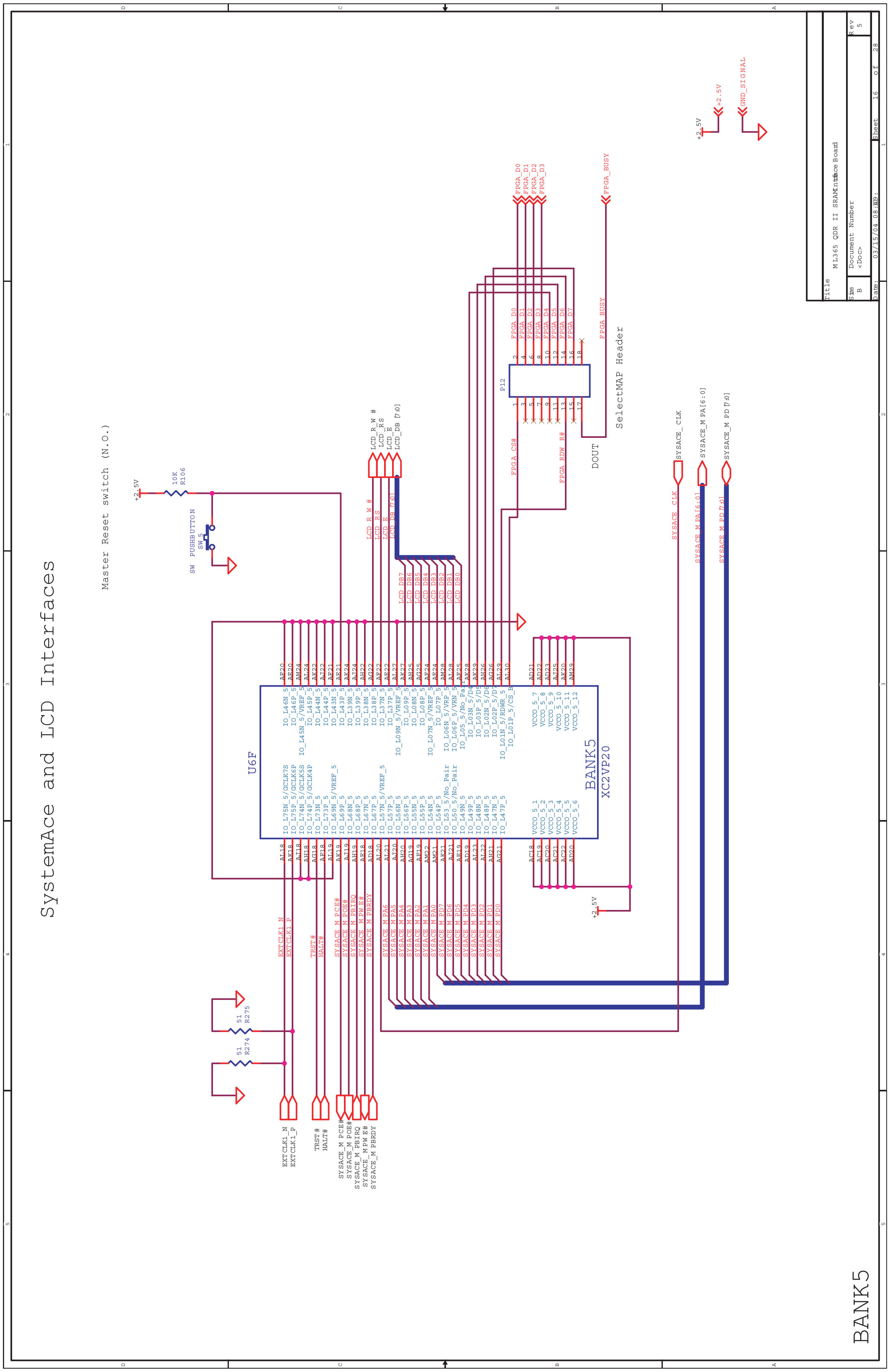

QDRII SRAM 3 (QDR C) DWRITE Interface
250MHz DCM driven
U6B
BANK1
XC2VP20
BANK1

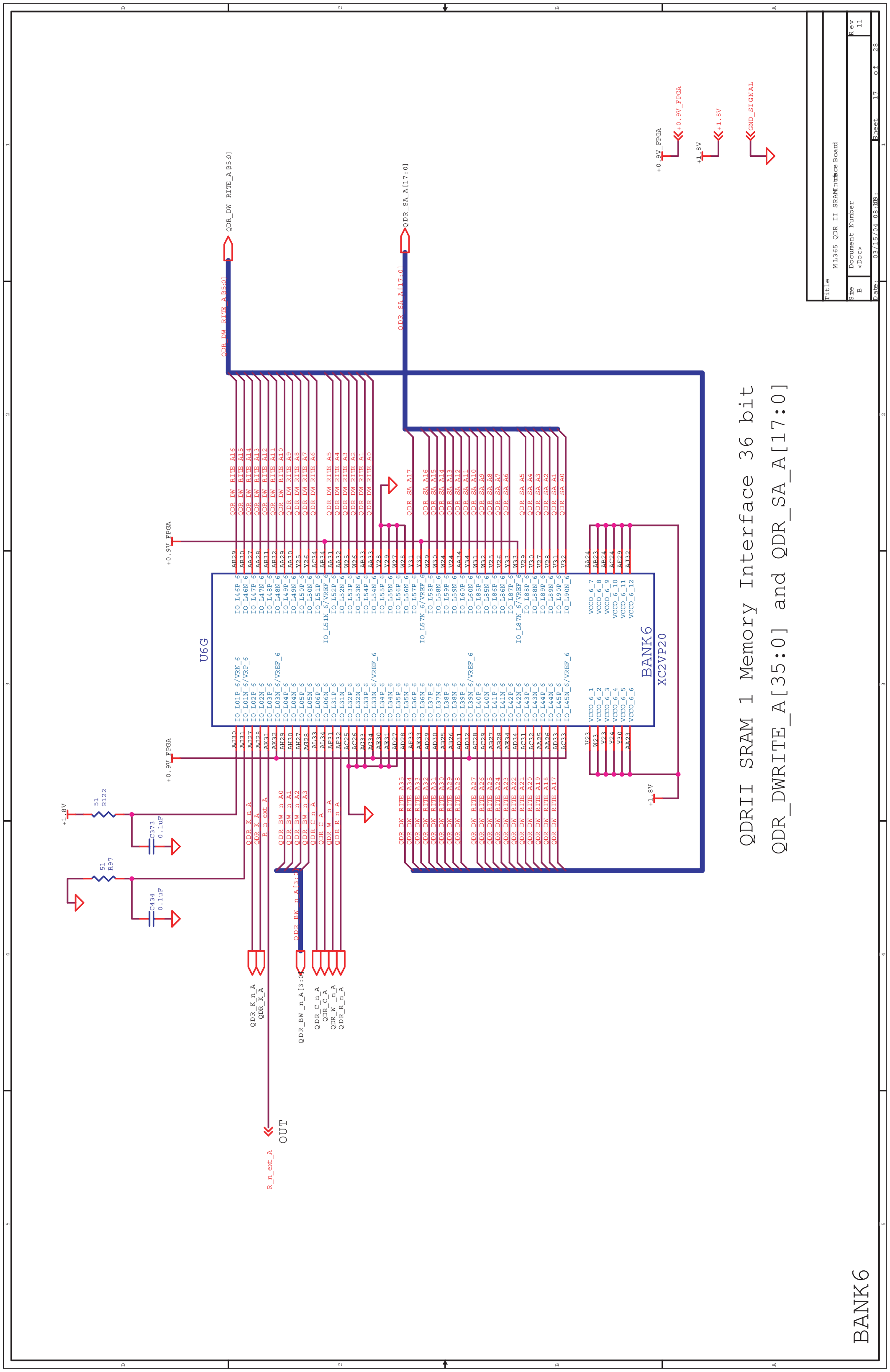

QDRII SRAM 2 (QDR B) DREAD Interface
QDRII SRAM 3 (QDR C) SA (address) Interface
U6C
BANK2
XC2VP20
BANK2

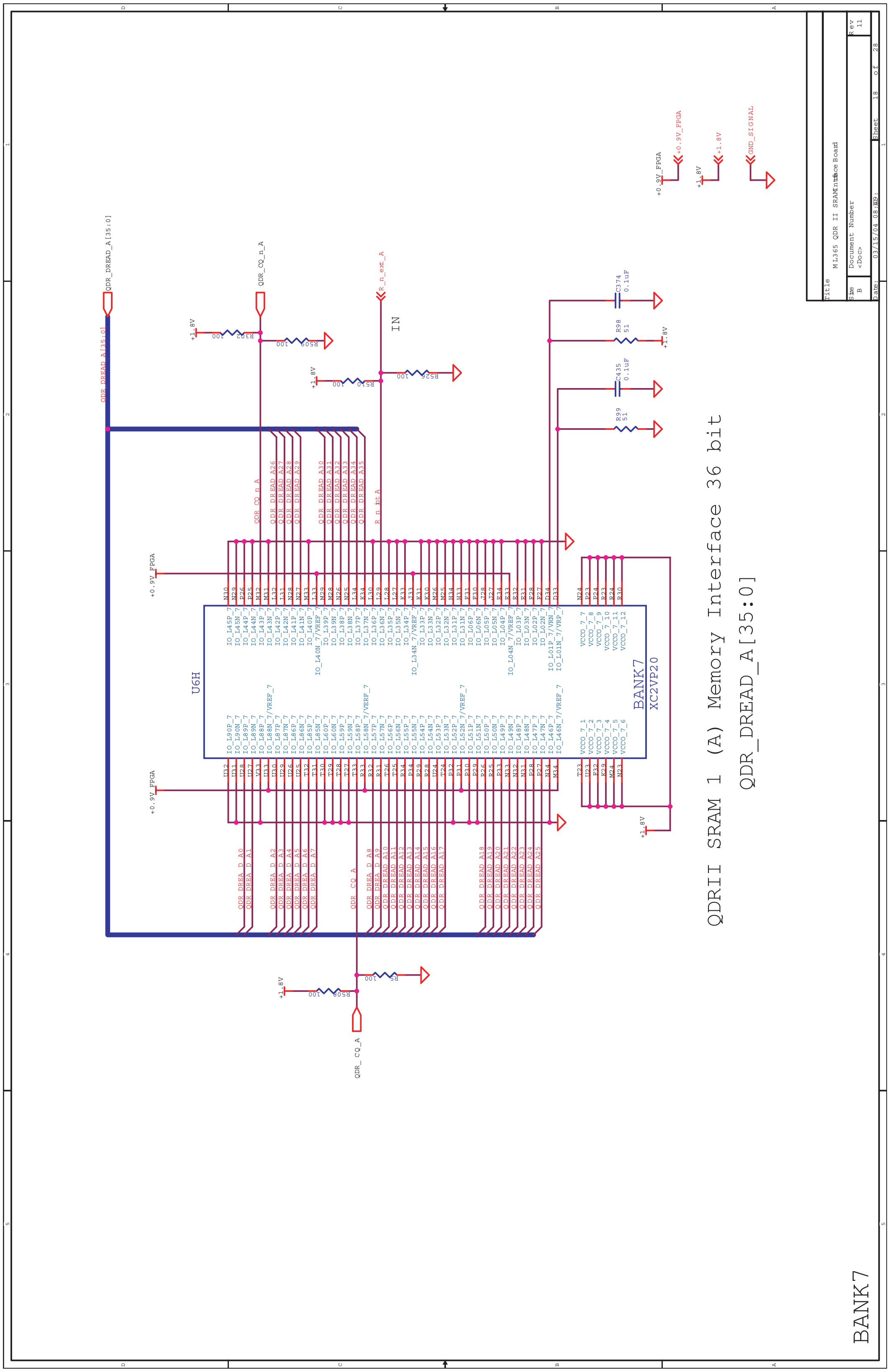


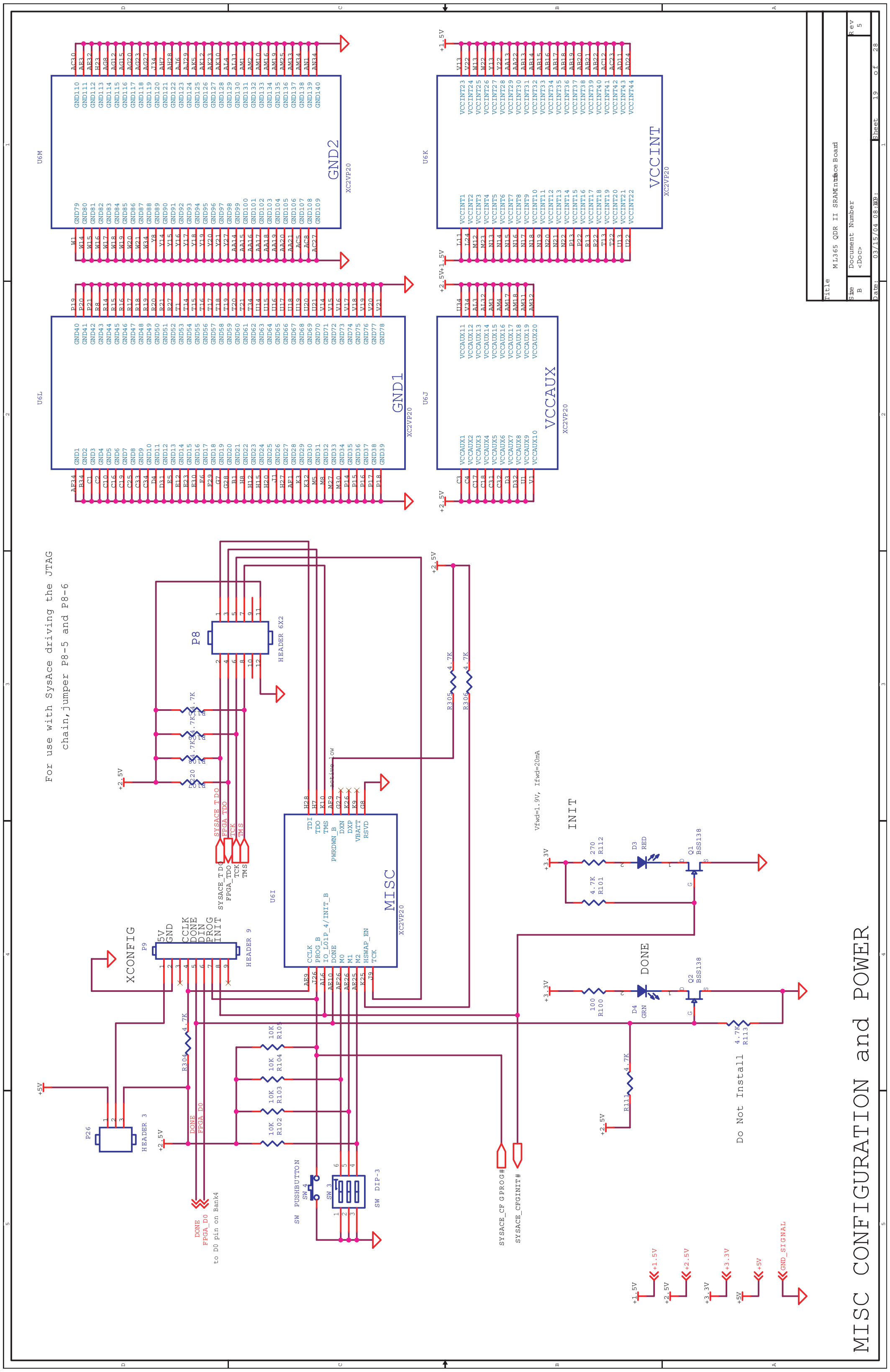


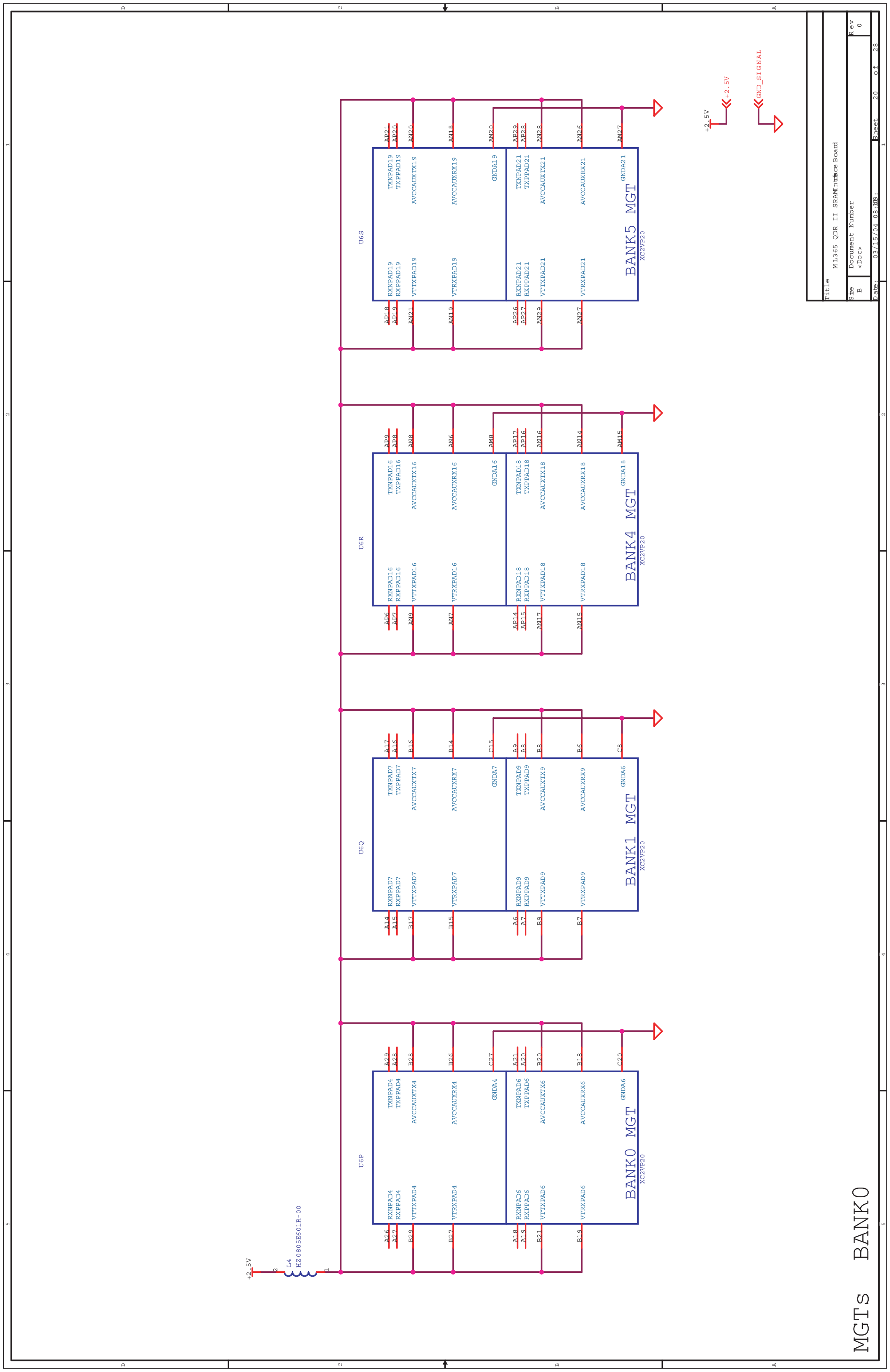
Logic Analyzer Header
User PB's and LED's
RS-232 Interface
Vref not required
BANK4
XC2VP20
User 1
User 2

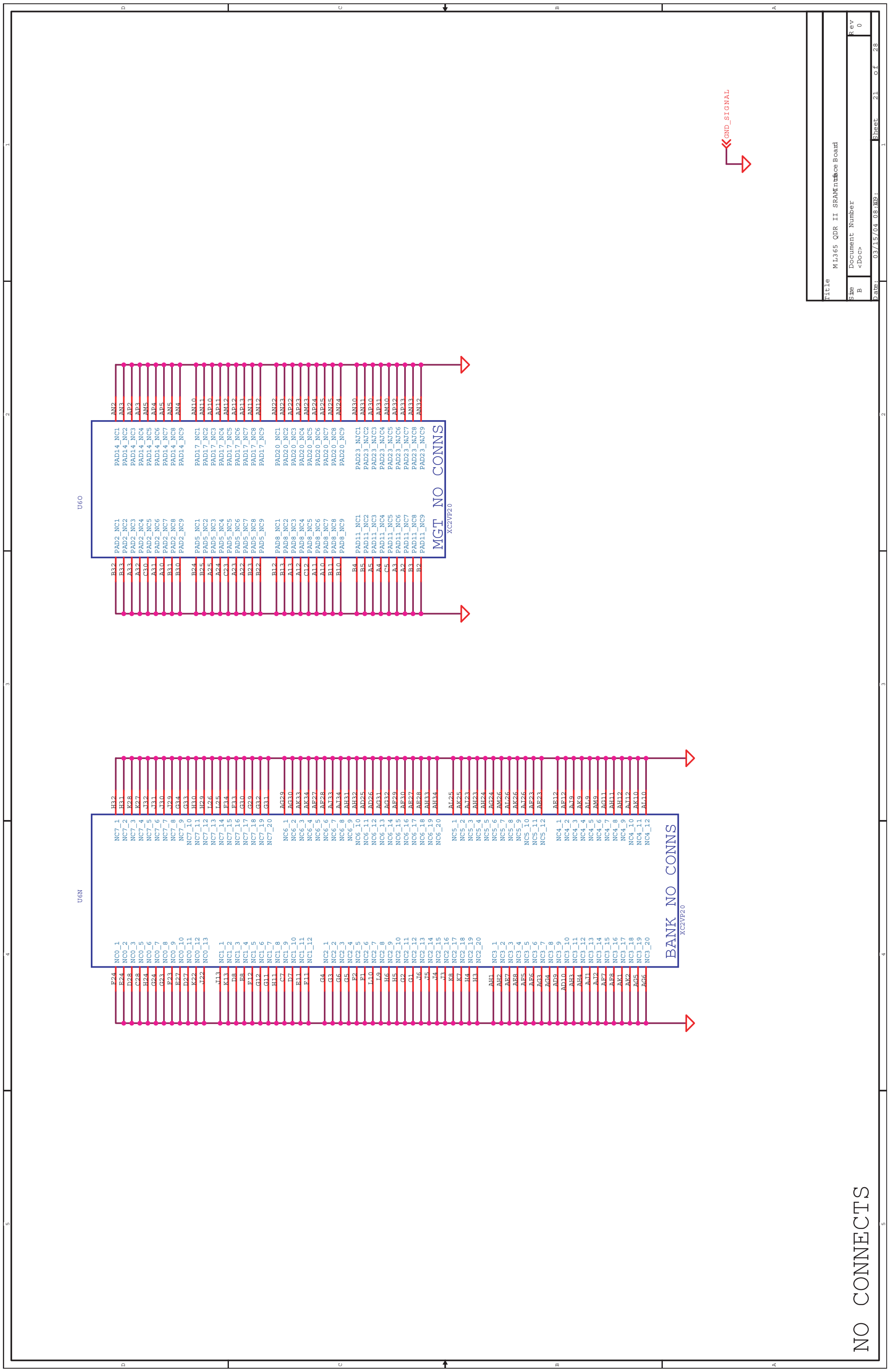

SystemAce and LCD Interfaces
Master Reset switch (N.O.)
SelectMAP Header
U6F
BANK5
XC2VP20
BANK5

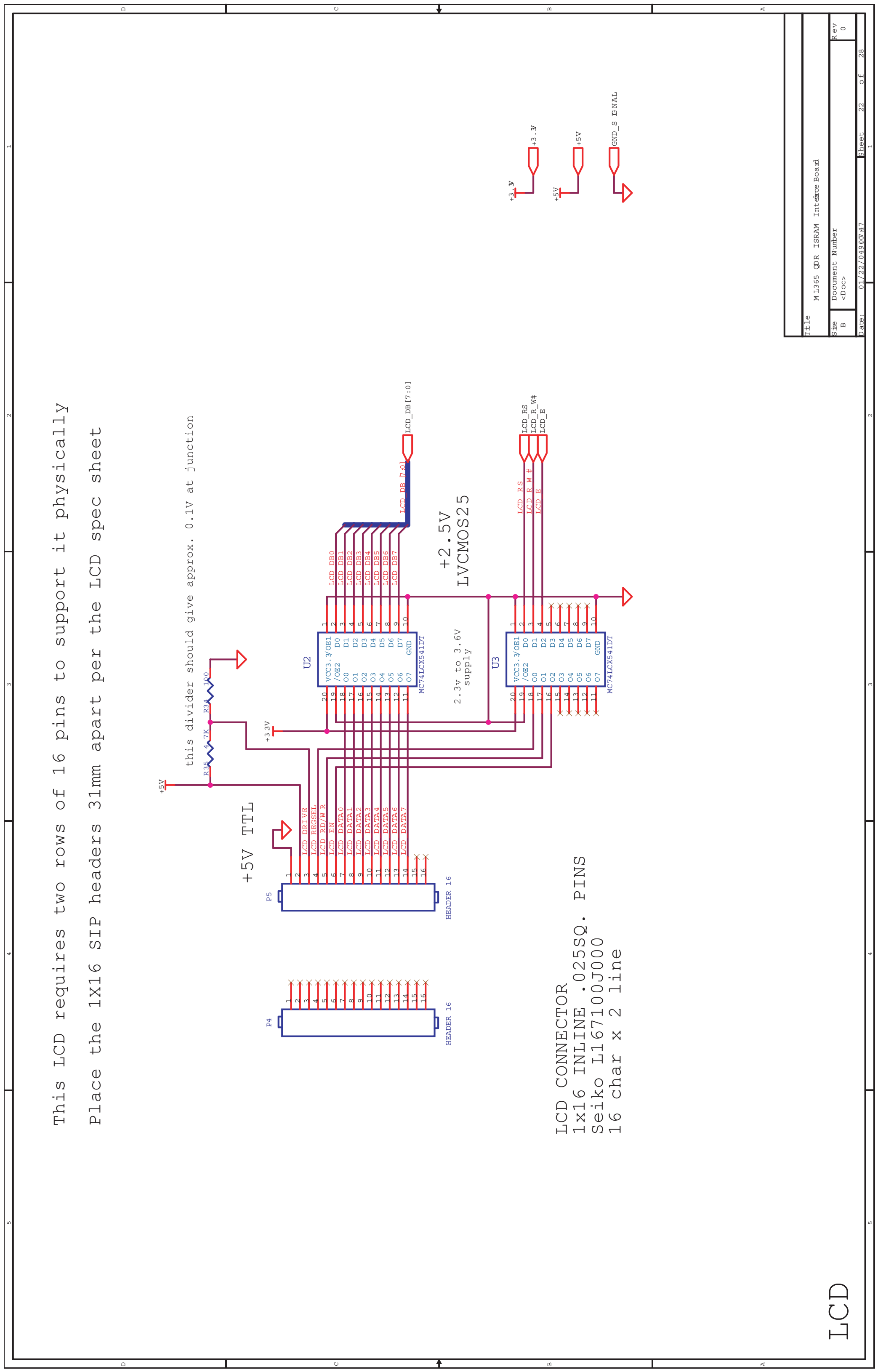

QDRII SRAM 1 Memory Interface 36 bit
QDR_DWRITE_A[35:0] and QDR_SA_A[17:0]
BANK6
XC2VP20
U6G
OUT

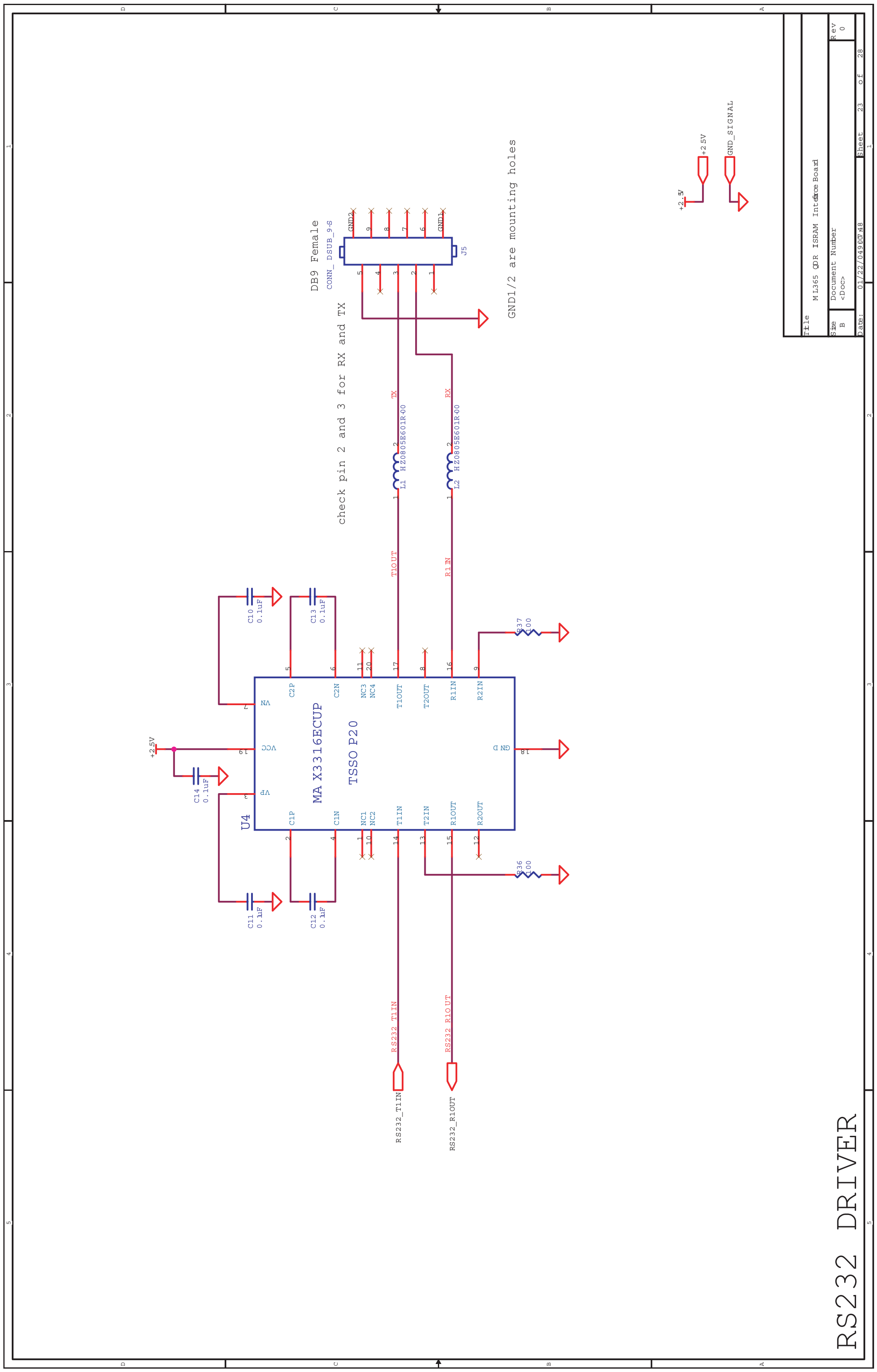

QDRII SRAM 1 (A) Memory Interface 36 bit
QDR_DREAD_A[35:0]
BANK7
XC2VP20
U6H
BANK7

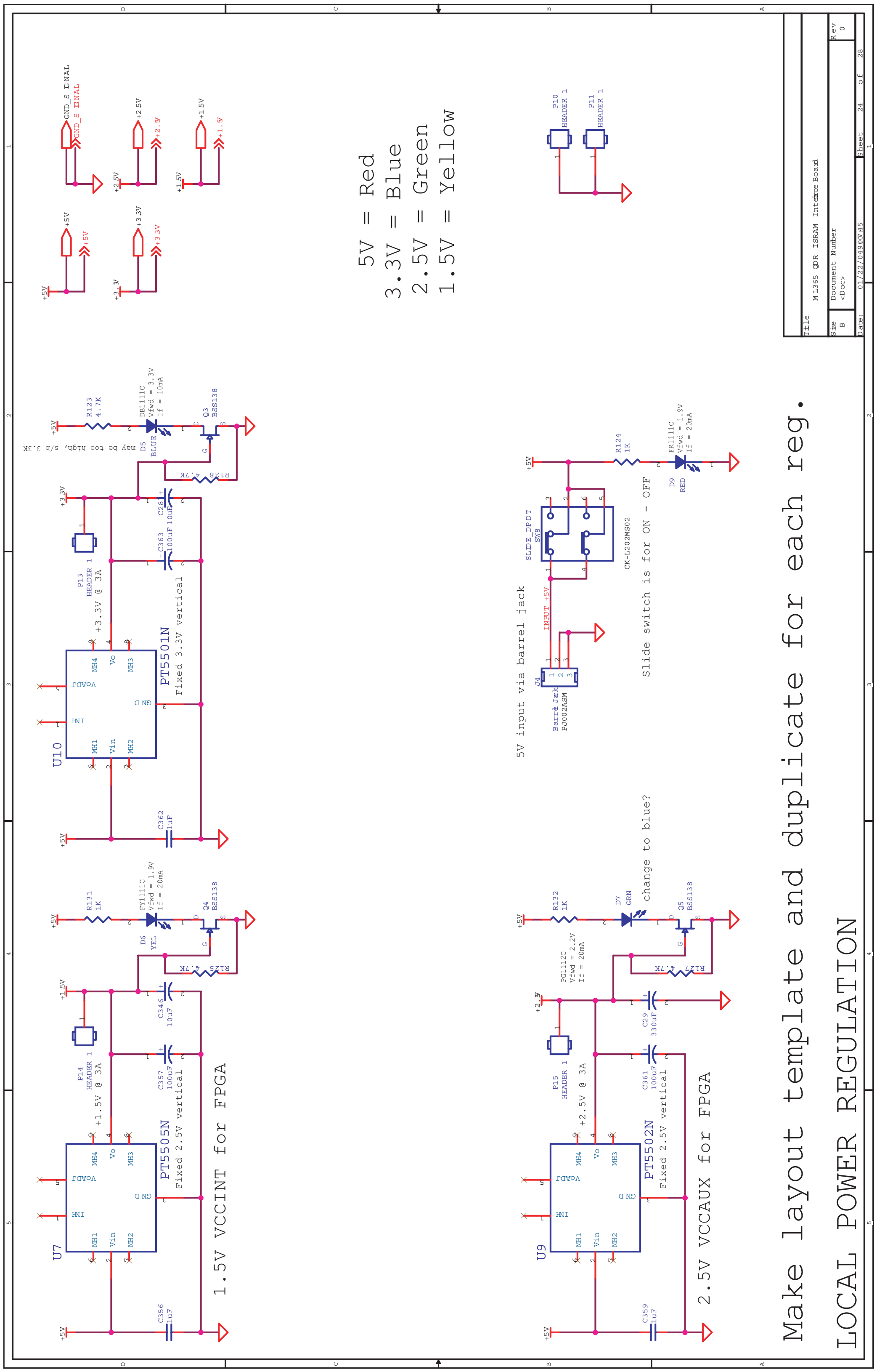

MISC CONFIGURATION and POWER
GND1
GND2
VCCAUX
VCCINT
MISC
XCONFIG
For use with SysAce driving the JTAG chain, jumper P8-5 and P8-6
Do Not Install
ML365 QDR II SRAM Interface Board


BANK5 MGT
BANK4 MGT
BANK1 MGT
BANK0 MGT
MGTs BANK0

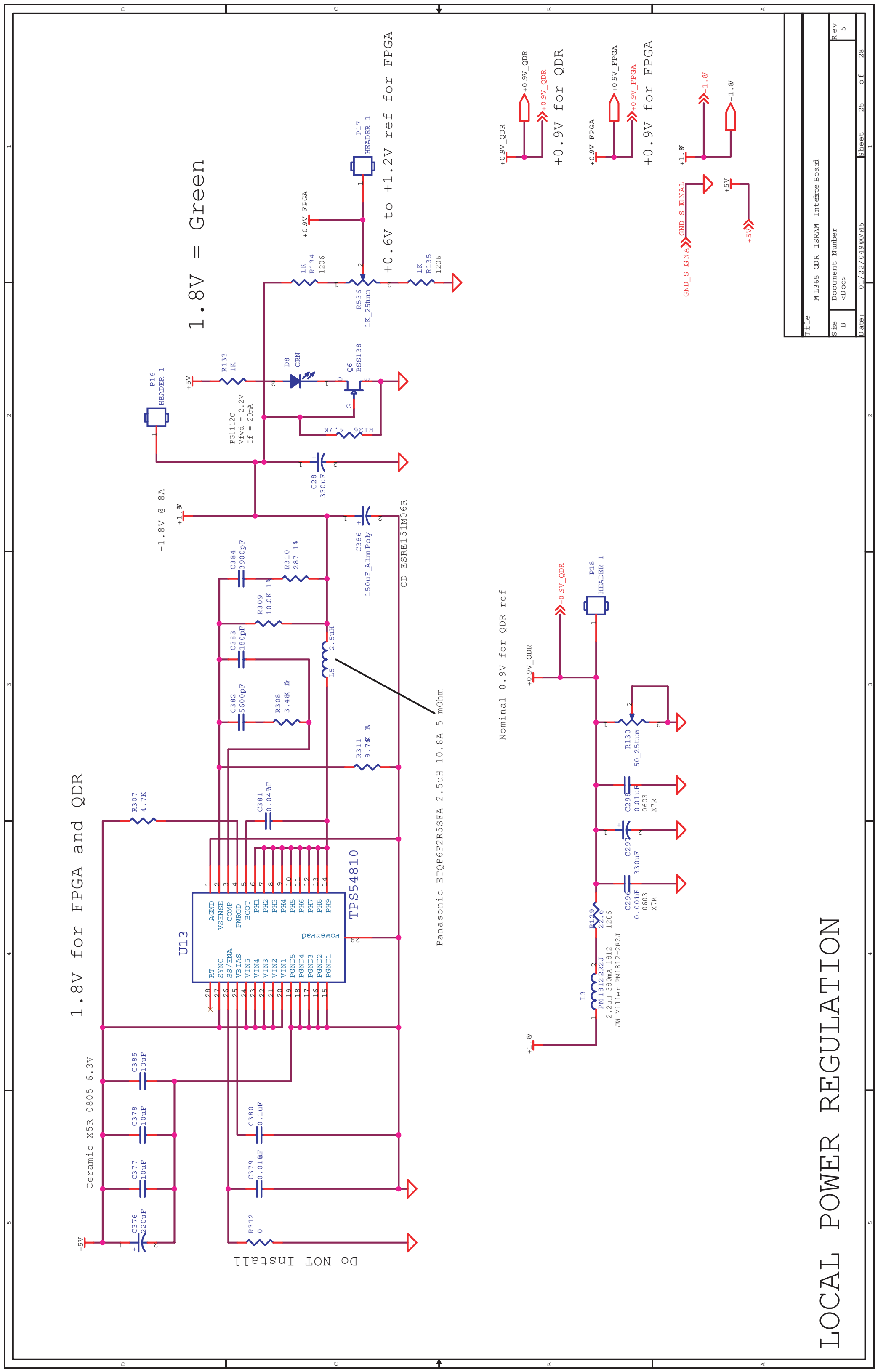

GND_SIGNAL
U6O
MGT NO CONNS
XC2VP20
U6N
BANK NO CONNS
XC2VP20
NO CONNECTS


This LCD requires two rows of 16 pins to support it physically
Place the 1X16 SIP headers 31mm apart per the LCD spec sheet
this divider should give approx. 0.1V at junction
+5V TTL
+2.5V LVCMOS25
2.3v to 3.6V supply
MC74LCX541DT
HEADER 16
LCD CONNECTOR
1x16 INLINE .025SQ. PINS
Seiko L167100J000
16 char x 2 line
LCD

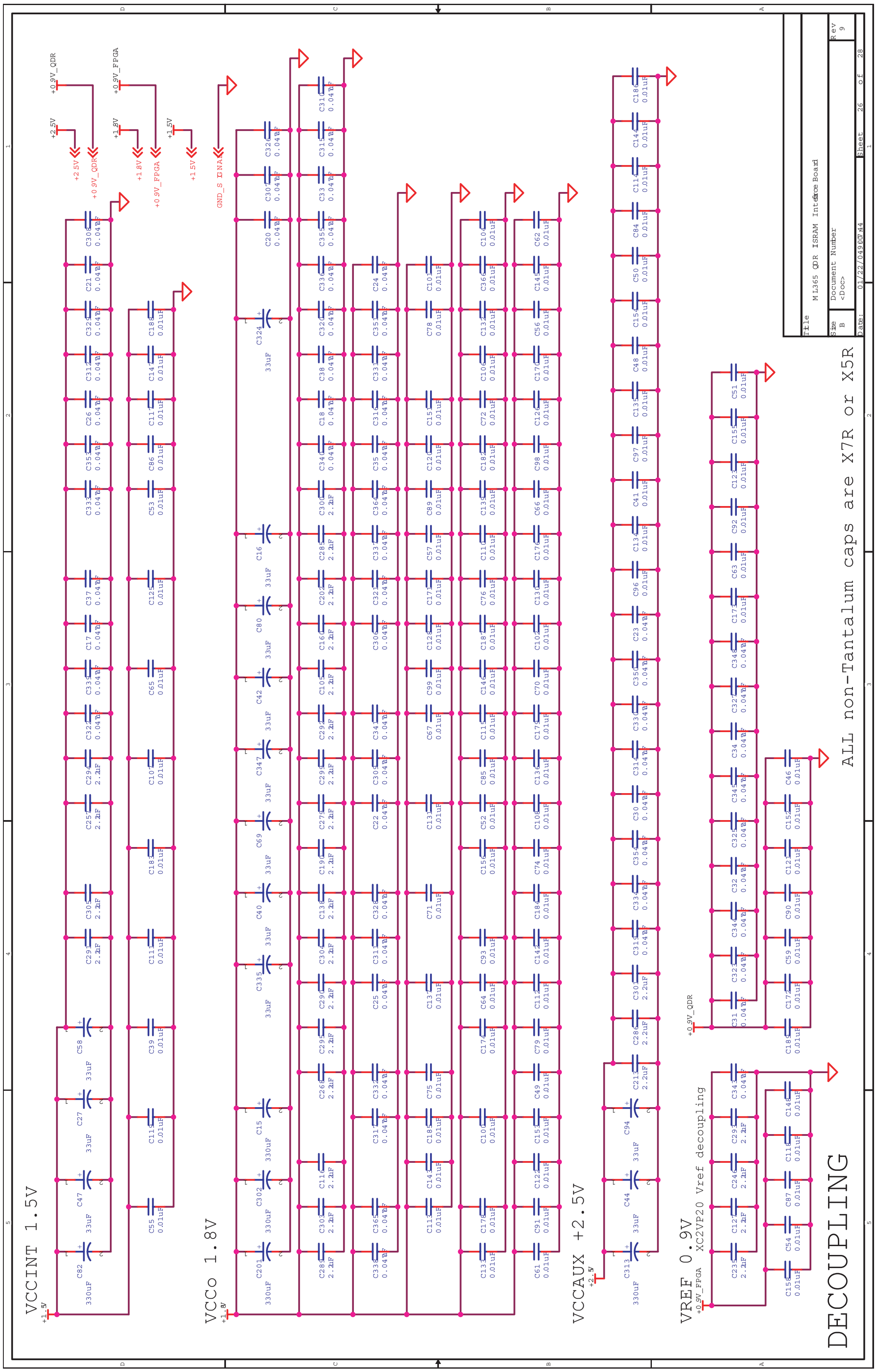

RS232 DRIVER
DB9 Female
CONN_DSUB_9-6
J5
check pin 2 and 3 for RX and TX
GND1/2 are mounting holes
U4
MAX3316ECUP
TSSOP20
RS232_T1IN
RS232_R1OUT
T1OUT
R1IN
TX
RX
+2.5V
GND_SIGNAL
ML365 QDR ISRAM Interface Board
Document Number
<Doc>

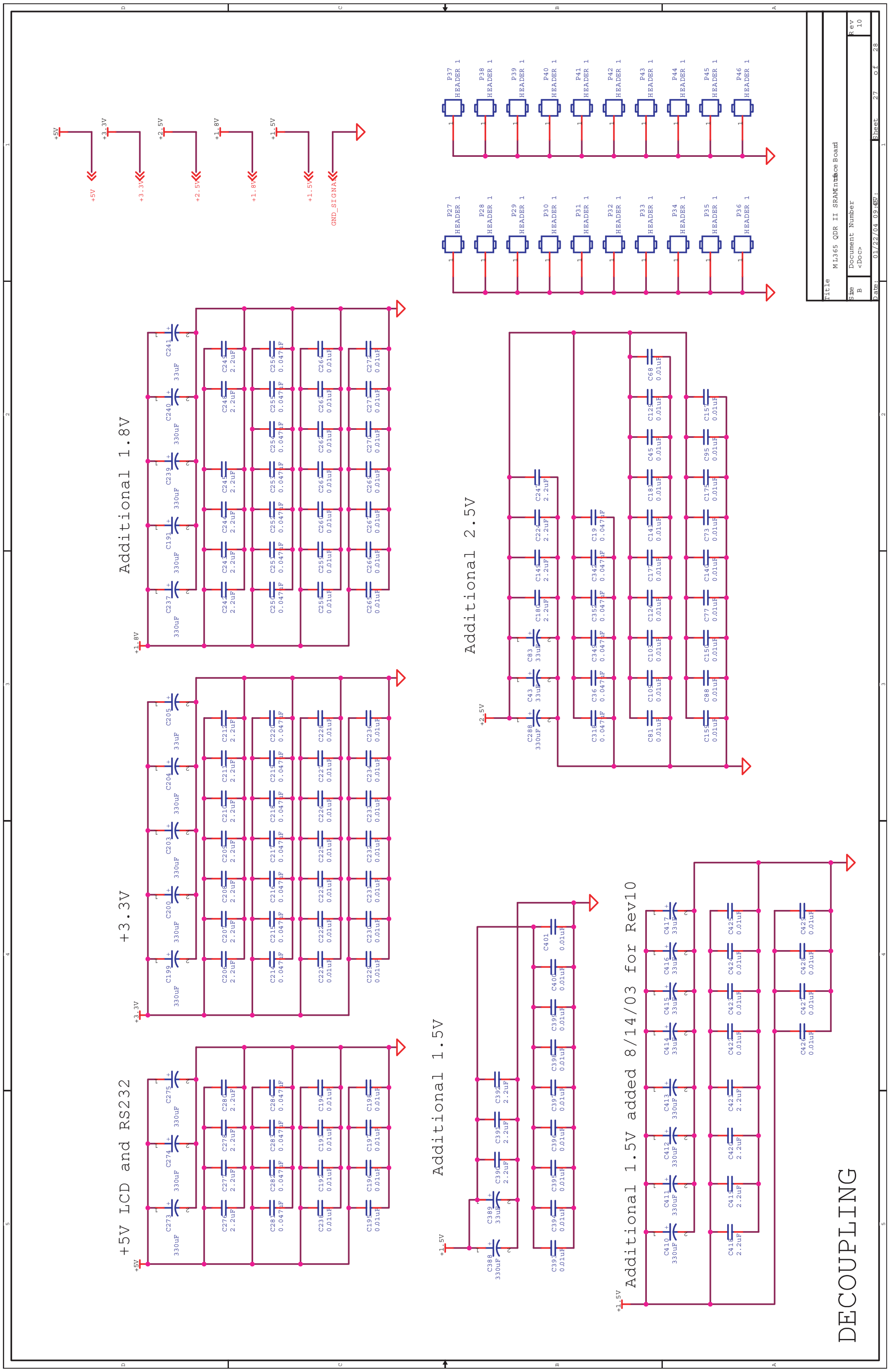


LOCAL POWER REGULATION
Make layout template and duplicate for each reg.
5V = Red
3.3V = Blue
2.5V = Green
1.5V = Yellow
1.5V VCCINT for FPGA
2.5V VCCAUX for FPGA
PT5501N
Fixed 3.3V vertical
PT5505N
PT5502N
Fixed 2.5V vertical
U10
U7
U9
5V input via barrel jack
Slide switch is for ON - OFF
change to blue?



LOCAL POWER REGULATION
1.8V for FPGA and QDR
1.8V = Green
+0.6V to +1.2V ref for FPGA
+0.9V for QDR
+0.9V for FPGA
Nominal 0.9V for QDR ref
TPS54810
U13
Panasonic ETQP6F2R5SFA 2.5uH 10.8A 5 mOhm
Ceramic X5R 0805 6.3V
Do NOT Install
+1.8V @ 8A


VCCINT 1.5V
VCCo 1.8V
VCCAUX +2.5V
VREF 0.9V
XC2VP20 Vref decoupling
DECOUPLING
ALL non-Tantalum caps are X7R or X5R



Additional 1.8V
+3.3V
+5V LCD and RS232
Additional 2.5V
Additional 1.5V
Additional 1.5V added 8/14/03 for Rev10
DECOUPLING
ML365 QDR II SRAM Interface Board

Rev#	Sheet#	Description
0	All	Initial Release
1		Change Bank2, Bank7 pinout per Olivier Despaux
2		Change Bank7 pinout R_n_int_A from L30 to P29 per Olivier Despaux
3		Change +3.3V on P3.2 to +2.5V (P3 is 2mm PC IV cable connector)
4		Add additional +1.5V decoupling caps, add 20 GND TP
5		Change QDR term pullup R's from 50 ohm to 100 ohm, add 100 ohm pulldown R's Change QDR CQ/CQ_n term R's to pullup/pulldown 100 ohm scheme Change QDR R_n_ext_* term R's to pullup/pulldown 100 ohm scheme Tied all unused FPGA Bank pins to GND Wired FPGA DONE signal to Bank3.AH8 Added 1K 25 turn trimpot to +0.9V_FPGA vref to give +0.6V to +1.2V adjustment Change TPS54610 1.8V@6A to TPS54810 1.8V @ 8A power
6		Updated component footprints only, no changes to schematic
7		Added P47 2x1 header wired to Bank4 for logic analyzer clock
8		Changed existing 51 ohm 0402 R's to 100 ohm: QDR1 R276-R281, QDR2 R282-R287, QDR3 R288-R293
9		Changed existing decoupling capacitors: From 1.5V To 2.5V: C318,C149,C224,C159,C88,C150,C77,C140,C73,C175,C95,C157 From 1.8V To 2.5V: C288,C43,C83,C180,C247,C342,C36,C352,C349,C19,C81,C109,C181,C103,C177,C45,C141,C68,C129,C124
10		Added additional +1.5V decoupling caps C410 - C429
11		Added additional 0.1uF filter caps C430-C435 to Bank0, 1, 2, 3, 6, 7 VRP pins Design formally renamed ML365, first board in Xilinx Memory Toolkit program under Olivier Despaux
12		Bank4, SW6 and SW7, change switch configuration from active low, to active high with pulldown R537 4.7K 0402 pull down, R538 4.7K 0402 pulldown added

Rev Notes

Title: ML365 QDR II SRAM Interface Board
Size: B | Document Number: <Doc> | Rev: 12
Date: 03/15/04 08:... | Sheet 28 of 28

Characterization Results

Long-Term Runs

The significant long-term runs are as follows:

- ML365 Serial 10 ran 215 MHz for 48 hours with no errors
- ML365 Serial 11 ran overnight at 240 MHz and 235 MHz with bit errors (one or more)
- ML635 Serial 11 ran 230 MHz for 144 hours with no errors

Corners Results Matrix

The measurements made on eleven boards are listed in Table 3-1. The slowest performance numbers are:

6C: 210 MHz   6C prod: 237 MHz

7C: 242 MHz   7C prod: 275 MHz

Table 3-1: **Corners Results Measurements**

Ambient Temp	V_{CC}	Bd 3	Bd 9	Bd 10	Bd 8	Bd9A	Bd 11	Bd 4	Bd 7	Bd 6	Bd B	Bd C
		-6 Slow					-6 Prod			-7 Prod	-7 Slow	
25 Degree C	Nom	218	219	223	217	223	247	260	271	284	248	254
	Nom -5%	216	218	219	215	219	245	257	267	271	246	253
	Nom +5%	219	220	224	218	224	248	263	266	285	249	256
70 Degrees C	Nom	213	219	216	212	215	241	257	263	280	243	251
	Nom -5%	212	216	214	210	214	237	254	262	275	242	250
	Nom +5%	214	220	217	213	215	243	258	263	282	245	252
0 Degrees C	Nom	228	230	231	226	229	266	278	273	292	264	268
	Nom -5%	224	229	230	226	228	265	278	272	290	263	268
	Nom +5%	230	231	232	228	230	267	279	291	302	266	272

Observations

Memory device V_{ref} levels are very important. They have been adjusted for each single test, and were set up at the optimal value for the memory interface under test. At optimal voltage (1.800V), it appears that 0.900V was, in almost all cases, the optimal setting; variations of 1.8V required significant adjustments of V_{ref} to obtain the best performance (+5% tests can require a +10% increase of V_{ref}).