Virtex-4 ML455 PCI/PCI-X Development Kit

User Guide

UG084 (v1.0) May 17, 2005

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/17/05	1.0	Initial Xilinx release.

Table of Contents

Chapter 4: Configuration

Appendix A: PCI Bus Clock Simulations

Chapter 1

Introduction

About the Virtex-4 ML455 PCI/PCI-X Development Kit

This kit provides a development platform for designing and verifying Virtex™-4 FPGA based PCI and PCI-X applications utilizing Xilinx PCI LogiCORE™ intellectual property (IP) cores in a 3.3V signaling environment. The ML455 is intended to plug-in to a 3.3V keyed system board. The ML455 board is not a Universal add-in card nor is it intended to plug into a 5V keyed system board. Figure 1-1 shows how to identify a 3.3V system board slot (left side) from a non-supported 5V-system board slot (right side).

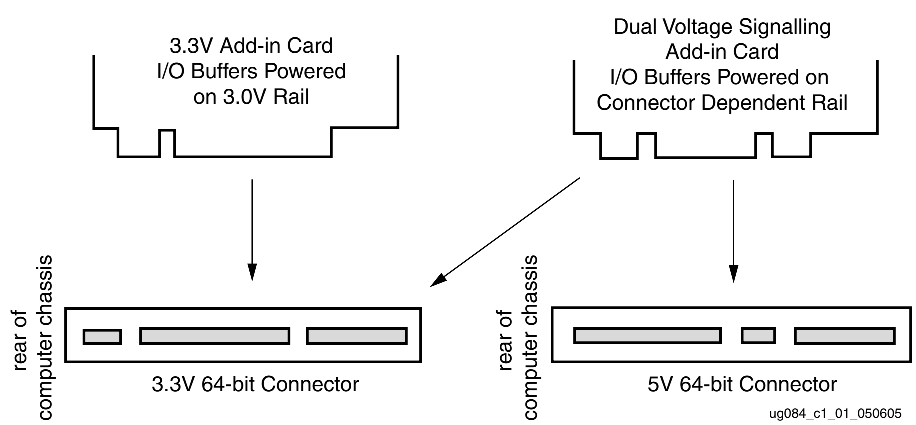


Figure 1-1: **Add-in Card Connectors**

The ML455 board is supported by Xilinx PCI and PCI-X LogiCORE versions 3.0 and 5.0, respectively. Table 1-1 lists the Xilinx PCI and PCI-X cores.

Table 1-1: **Xilinx PCI and PCI-X Cores**

Version	Bus Mode	Bus Width	Clock Frequency	Clock Type (FPGA Pin #)
v3.0	PCI	64 bits	66 MHz	Regional (D2)
v3.0	PCI	64 bits	33 MHz	Regional (D2)
v3.0	PCI	64 bits	33 MHz	Global (C13)
v5.0	PCI-X	64 bits	133 MHz	Global (C13)
v5.0	PCI-X	64 bits	100 MHz	Global (C13)
v5.0	PCI-X	64 bits	66 MHz	Global (C13)
v5.0	PCI	64 bits	33 MHz	Global (C13)

The Xilinx PCI and PCI-X interface cores are pre-implemented and fully tested modules for Xilinx FPGAs.

The v3.0 PCI 64-bit interface is compliant with the PCI Local Bus Specification, revision 3.0. The v5.0 PCI-X 64-bit interface is compliant with the PCI Local Bus Specification, revision 3.0, and the PCI-X Addendum, revision 2.0.

The PCI/PCI-X core pinout for each Xilinx Virtex-4 device and the relative placement of the internal logic are predefined. Critical paths are controlled by constraints to ensure predictable timing, significantly reducing the engineering time required to implement the PCI/PCI-X bus interface portion of a user design.

Resources can instead be focused on unique user application logic in the FPGA and on the system-level design. As a result, the Xilinx PCI and PCI-X interface products minimize product development time.

The following link provides more information about Xilinx LogiCORE products: www.xilinx.com/products/design_resources/conn_central/index.htm

The following link provides more information about PCI specific applications: www.xilinx.com/products/design_resources/conn_central/grouping/pci.htm

The following link provides more information about PCI-X specific applications: www.xilinx.com/products/design_resources/conn_central/grouping/pcix.htm

The ML455 board kit includes the following:

- Virtex-4 ML455 board (XC4VLX25-FF668 FPGA)
- Documentation and reference design CD
- Time-out evaluation licenses for the Xilinx PCI-X and PCI64 LogiCORE IP
- Evaluation CD for Jungo Software Technologies WinDriver device driver development kit
- Xilinx ChipScope™ Pro and Integrated Software Environment (ISE) Evaluation CDs

Optional items that also support development efforts include:

- Xilinx ISE software
- JTAG cable, Xilinx Parallel Cable IV, or Xilinx Platform Cable USB

For assistance with any of these items, contact your local Xilinx distributor or visit the Xilinx online store at www.xilinx.com.

The heart of the kit is the ML455 board. This manual provides comprehensive information on this board.

Virtex-4 ML455 Board

The ML455 board includes the following:

- XC4VLX25-FF668 - 11 speed grade FPGA
- 200-pin 2.5V SODIMM socket with 128 MB (16M x 64 bit) DDR SDRAM SODIMM
- Three on-board clock sources:
  - 200 MHz Epson 2.5V EG-2121CA LVPECL
  - 133 MHz Epson 2.5V EG-2121CA LVDS
  - 33 MHz LVCMOS
- One DB9-M RS232 port (serial cable not provided)
- Support for up to four FPGA design images in a Xilinx XCF32P-FSG48C Platform Flash configuration PROM
- Static or dynamic device reconfiguration support with the XC2C32 CoolRunner™ II CPLD
- 64-bit 3.3V system board keyed PCI or PCI-X connector
- Top mounted 64-bit 3.3V keyed PCI or PCI-X expansion socket (on top of board)
- User push-button switches, LEDs, and general-purpose I/O header
- Device configuration through on-board Platform Flash, Xilinx PC-IV JTAG cable, or Xilinx Platform Cable USB
- PCI clocking support for global and regional clocking applications
- On-board power regulators (3.0V PCI, 2.5V, 1.8V, 1.2V, 1.25V V_{TT})

Figure 1-2 shows the ML455 board.

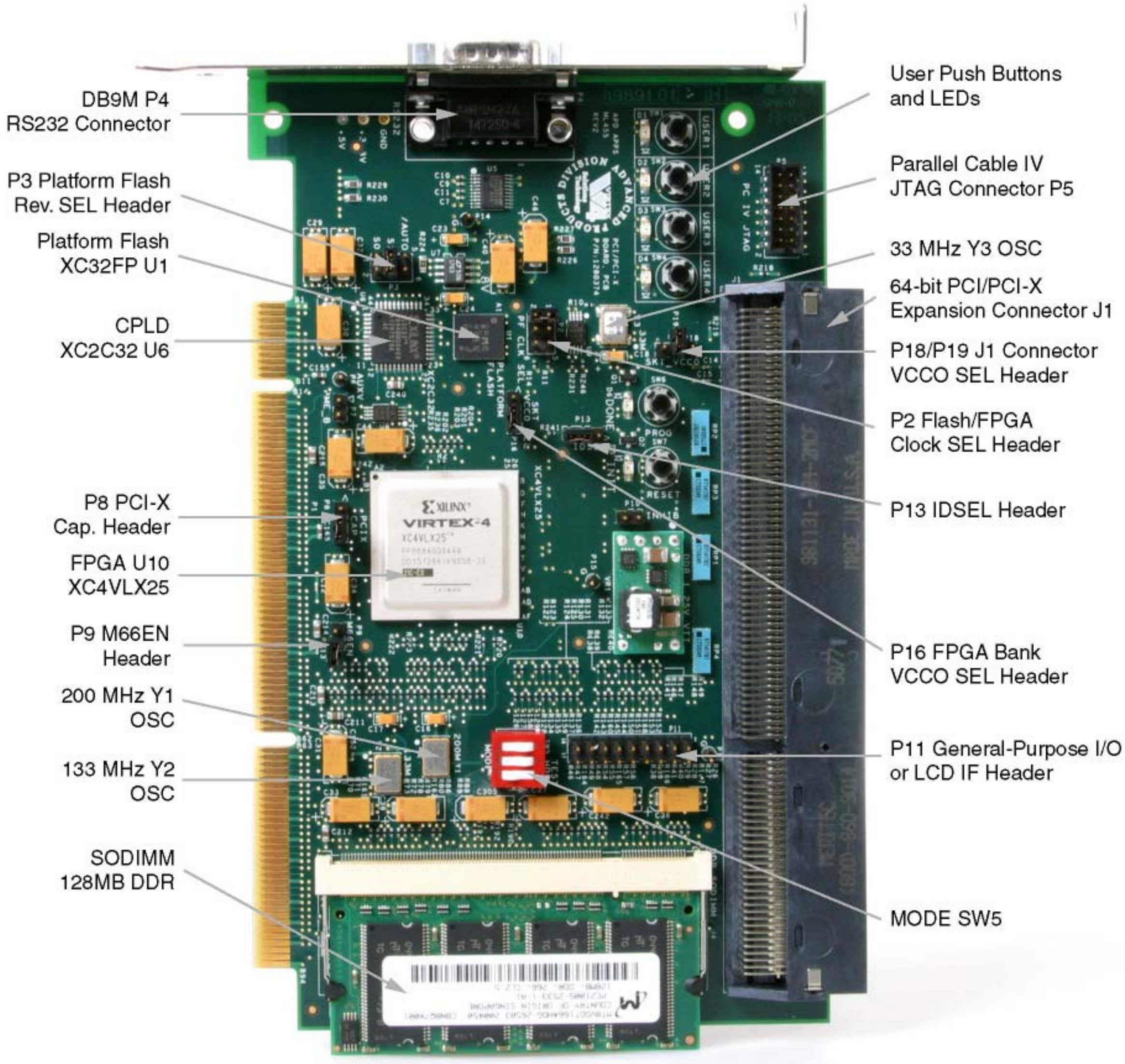


Figure 1-2: **Virtex-4 ML455 Board**

Chapter 2

Getting Started

This chapter describes the items needed to configure the Virtex-4 ML455 board. The ML455 board is tested prior to shipment and should work out of the box. The installer is recommended to inspect the board prior to use and confirm proper jumper and switch settings as directed in this chapter.

Documentation and Reference Design CD

The CD included in the Virtex-4 ML455 board kit contains the board design files for the ML455 board, including schematics, PCB layout, and bill of materials. Open the `ReadMe.txt` file on the CD to review the list of contents.

Initial Board Checks Before Applying Power

Perform these steps before plugging in the ML455 board:

1. Set up the Configuration Mode Switch SW5 (Master SelectMAP).

   [position 1, 2, 3, = open, open, closed = 110]

2. Jumper Block P2: shorting shunt on pins 1 - 2 (FPGA CCLK drives U1 CLKIN).
3. Jumper Block P3: shorting shunt on pins 3 - 4 (selects U1 flash image 01).

The ML455 board now can be plugged into a powered down PCI/PCI-X 3.3V (only) slot. See the `ReadMe.txt` file on the CD to view the instructions to run the default reference design loaded from the Platform Flash U1 image 3 location.

Chapter 3

Hardware Description

A high-level block diagram of the Virtex-4 ML455 board is shown in Figure 3-1, followed by a brief description of each board section.

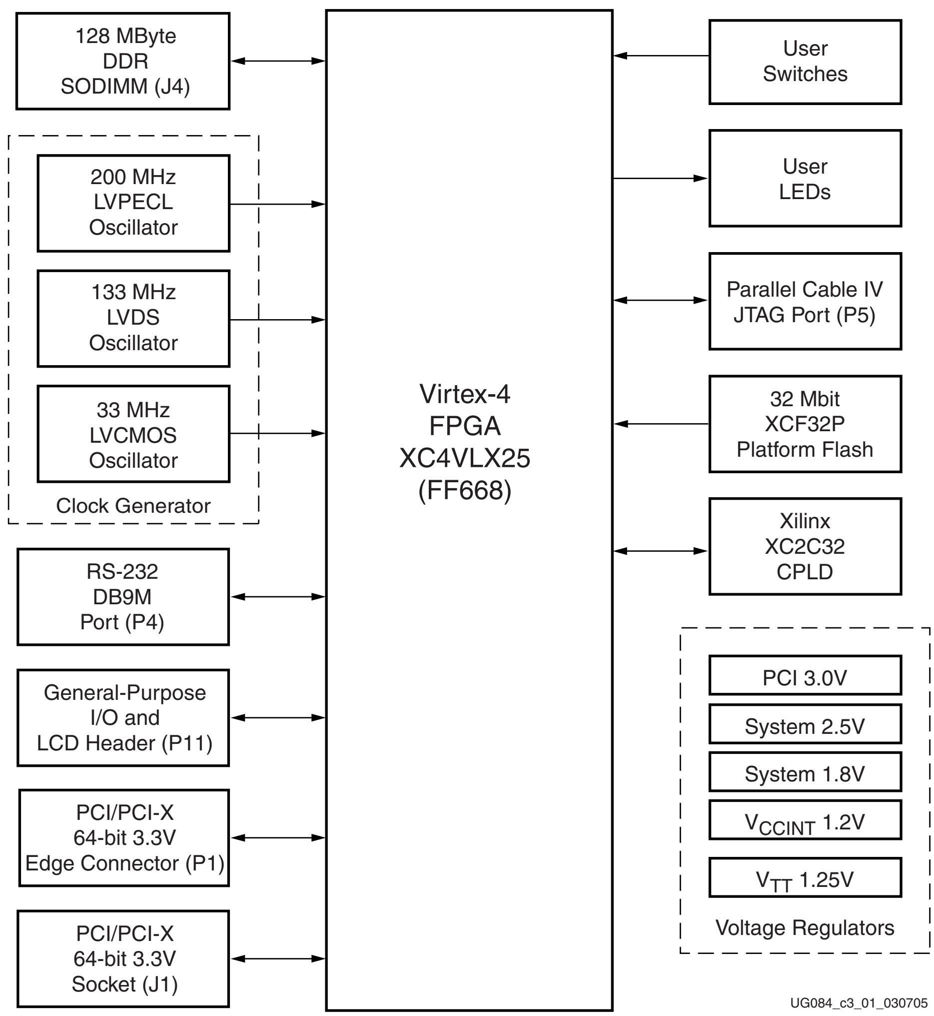


Figure 3-1: **ML455 Board Block Diagram**

The CD included in the kit contains ML455 board schematics and layout files.

Figure 3-2 shows a block diagram of the XC4VLX25FF668 banks, the number of I/Os per bank, the number of I/Os used on the board per bank, and the provided function(s).

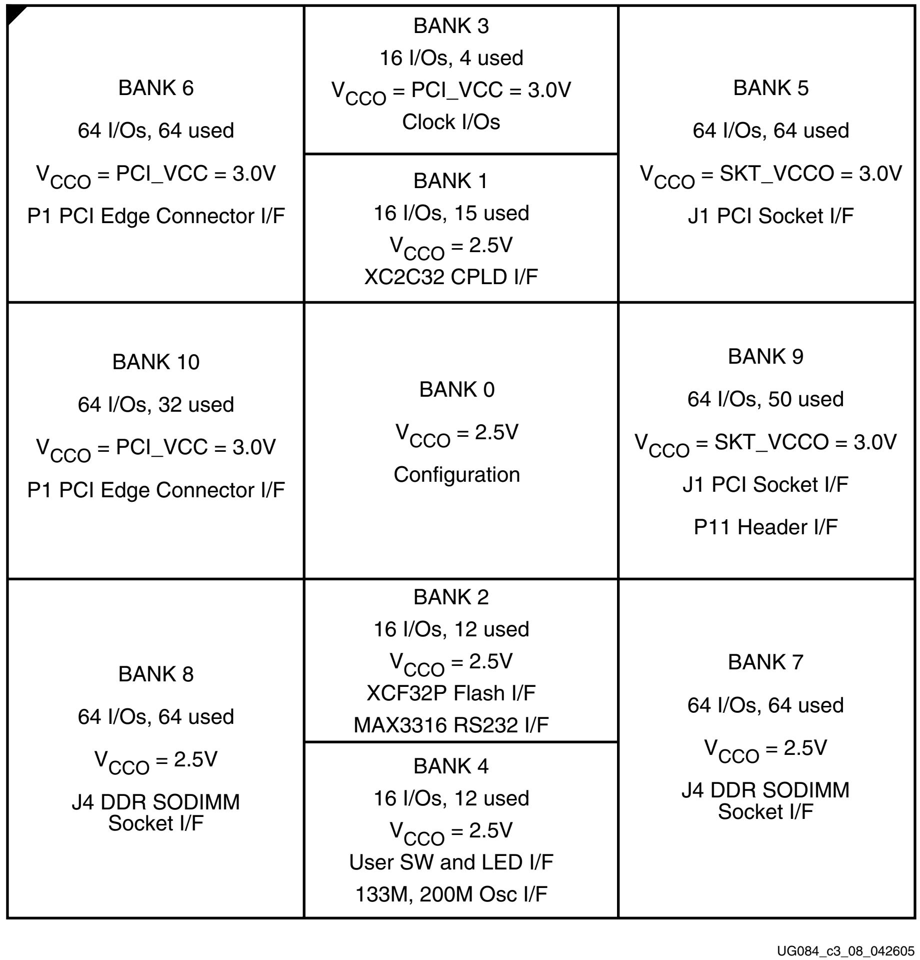


Figure 3-2: **Virtex-4 XC4VLX25FF668 Banking (Top View)**

Clock Generation

The clock generation section of the ML455 board provides three clock sources:

1. Epson EG-2121CA-200.0000M-PHPA 2.5V LVPECL (differential) oscillator
   - 200 MHz Virtex-4 FPGA IDELAY reference clock.
2. Epson EG-2121CA-133.0000M-LHPA 2.5V LVDS (differential) oscillator
   - 133 MHz clock for PCI-X designs and DDR SDRAM memory interface.
3. Epson SG-8002CA-33.0000M-PCC 3.3V LVCMOS (single-ended) oscillator
   - This oscillator is an optional configuration oscillator for Platform Flash (U1). This clock is buffered via U9.

Table 3-1 lists the destination pins of these clock sources.

Table 3-1: **ML455 Board Clock Sources**

Clock Designator	Output	Type	Frequency	Destination Pin
Y1	Differential	LVPECL	200 MHz	FPGA U10 Bank 4 AE14 (P) FPGA U10 Bank 4 AE13 (N)
Y2	Differential	LVDS	133 MHz	FPGA U10 Bank 4 AD12 (P) FPGA U10 Bank 4 AD11 (N)
Y3	Single-ended	LVCMOS	33 MHz	Clock Buffer U9 input pin 1 (P)
U9 pin 8	Single-ended	LVCMOS	33 MHz	FPGA U10 Bank 3 B15 (P)
P1 pin B15	Single-ended	PCI 3.3V	33 MHz to 133 MHz	FPGA U10 Bank 3 C13 (P) and FPGA U10 Bank 6 D2 (P)

The PCI specification calls for the PCI bus clock, sourced from the motherboard PCI slot, to have one load on the add-in cards. The Xilinx PCI and PCI-X IP cores, depending upon bus mode and frequency, require that the PCI bus clock enter the FPGA on a specific clock pin (refer to Table 1-1).

The ML455 board PCI bus clock is implemented as follows:

- The PCI bus clock (signal CLK_FROM_EDGE) enters the board on PCI edge connector P1 pin B16.
- The clock is then routed in a "Y" topology to two parallel 0 Ω resistors, R2 and R242.
- The output side of R2 (signal PCIBUSCLK1) is routed to FPGA pin C13 (the global clock pin of FPGA).
- The output side of R242 (signal PCIBUSCLK2) is routed to FPGA pin D2 (the regional clock pin of FPGA).
- The total length of each clock trace (including the length of the 0 Ω resistor) from pin P1.16 to its FPGA pin is 2.5 inches.

Refer to Appendix A, "PCI Bus Clock Simulations," for 133 MHz clock waveforms at the FPGA clock pins C13 and D2, with different R2 and R242 configurations.

If full electrical compliance is required, the designer has the option to remove one of the two 0 ohm resistors (R2 or R242). As shipped, the ML455 board has both resistors installed and works with all versions of the Xilinx PCI/PCI-X LogiCORE cores.

DDR SDRAM SODIMM Memory

The ML455 board contains a 200-pin, small-outline dual in-line memory module (SODIMM) connector (J4) that supports installation of DDR SDRAM SODIMM memory modules of 128 MB, 256 MB, 512 MB, or 1 GB. Xilinx provides a 128 MB memory SODIMM Micron Semiconductor part number MT8VDDT1664HDG-265B3, with the kit. Table 3-2 provides a description of the memory interface signal descriptions, SODIMM connector pin assignments, and associated FPGA pin assignments.

The ML455 board does not support a 72-bit DDR data interface required for parity or error correction codes (ECC).

Characteristics of the DDR SDRAM SODIMM (provided with the kit):

- Organization 16M x 64 bit
- Memory clock speed 7.5 ns/133 MHz
- CAS latency 2.5
- 2.5V I/O (Stub-Series Terminated Logic (SSTL2) compatible)

The data sheet for the DDR SDRAM Small Outline DIMM memory module kit can be obtained from Micron Semiconductor at www.micron.com/products/modules. Contact Micron for availability of other compatible products, including device capacity, clock speeds, and CAS latency options, in the 200-pin SODIMM form factor.

The ML455 board memory interface design includes on board 50 Ω termination resistors to V_{TT}, at both the FPGA and SODIMM ends of the interface, for the 64 bit bidirectional DQ data-bus and the 8 bit bidirectional DQS signals. The address and control signals have 50 Ω termination resistors to V_{TT} at the SODIMM end of the interface. The SODIMM provides a 120 Ω termination network for the differential clock inputs. The Xilinx Digitally Controlled Impedance (DCI) standard SSTL2_I_DCI can be utilized to terminate unidirectional address and control signals transmitted by the FPGA. External 50 Ω reference resistors are provided to VRN and VRP for the memory interface banks 7 and 8 of the XC4VLX25 FPGA. See the Virtex-4 *User Guide* for additional information on DCI.

Table 3-2: **SDRAM Memory Interface Signal Descriptions**

SODIMM J4 Pin #	Signal	XC4VLX25 U10 Pin #	SODIMM J4 Pin #	Signal	XC4VLX25 U10 Pin #
112	A0	AE21	89	CK2	AC25
111	A1	V6	91	CK2_B	AC26
110	A2	AE18	96	CKE0	AC18
109	A3	W1	95	CKE1	AB23
108	A4	AF18	12	DM0	Y19
107	A5	W2	26	DM1	AA18
106	A6	AF22	48	DM2	AB21
105	A7	AD23	62	DM3	Y17
102	A8	AF21	134	DM4	AF5
101	A9	AD22	148	DM5	AD4
115	A10	V5	170	DM6	Y10
100	A11	AB18	184	DM7	AE6

Table 3-2: **SDRAM Memory Interface Signal Descriptions *(Continued)***

SODIMM J4 Pin #	Signal	XC4VLX25 U10 Pin #	SODIMM J4 Pin #	Signal	XC4VLX25 U10 Pin #
99	A12	AA23	5	DQ0	V21
123	A13	W6	7	DQ1	V22
117	BA0	W7	13	DQ2	W26
116	BA1	AD21	17	DQ3	W21
35	CK0	AA24	6	DQ4	AF19
37	CK0_B	Y24	8	DQ5	AF20
160	CK1	AF7	14	DQ6	W19
158	CK1_B	AF8	18	DQ7	AF23
19	DQ8	W22	141	DQ40	Y4
23	DQ9	W23	145	DQ41	Y3
29	DQ10	V20	151	DQ42	Y5
31	DQ11	Y25	153	DQ43	AB1
20	DQ12	AE23	142	DQ44	Y9
24	DQ13	Y20	146	DQ45	AD5
30	DQ14	Y18	152	DQ46	AC6
32	DQ15	AF24	154	DQ47	AB6
41	DQ16	Y26	163	DQ48	AA1
43	DQ17	AB24	165	DQ49	AC4
49	DQ18	AB26	171	DQ50	AB3
53	DQ19	AA26	175	DQ51	AC5
42	DQ20	AE24	164	DQ52	AA8
44	DQ21	AC21	166	DQ53	Y8
50	DQ22	AD19	172	DQ54	AA10
54	DQ23	AC19	176	DQ55	AC7
55	DQ24	AD25	177	DQ56	AB5
59	DQ25	AD26	181	DQ57	AC2
65	DQ26	AC22	187	DQ58	AF3
67	DQ27	AB22	189	DQ59	AE3
56	DQ28	AA19	178	DQ60	AC9
60	DQ29	AA20	182	DQ61	AB9
66	DQ30	AA17	188	DQ62	AD6
68	DQ31	AB20	190	DQ63	AF9
127	DQ32	W5	11	DQS0	W25
129	DQ33	Y2	25	DQS1	W20
135	DQ34	AA4	47	DQS2	AB25

Table 3-2: **SDRAM Memory Interface Signal Descriptions *(Continued)***

SODIMM J4 Pin #	Signal	XC4VLX25 U10 Pin #	SODIMM J4 Pin #	Signal	XC4VLX25 U10 Pin #
139	DQ35	AA3	61	DQS3	Y22
128	DQ36	AC3	133	DQS4	Y1
130	DQ37	AF6	147	DQS5	Y6
136	DQ38	AA7	169	DQS6	AB4
140	DQ39	AA9	183	DQS7	AC1
118	RAS_B	AF4	196	SA1	AD8
120	CAS_B	AE4	198	SA2	AC8
121	S0_B	W4	195	SCL	AD1
122	S1_B	AD3	193	SDA	AD2
194	SA0	AE9	119	WE_B	V7

User LEDs

The ML455 board provides four user LEDs that can be turned ON by driving the LED signals Low. Table 3-3 lists the FPGA pin assignments.

Table 3-3: **User LED Pin Assignments**

LED Signal	Designation	FPGA Pin Number (FF668 Package)
USER_LED0	USER1 D1	AF10
USER_LED1	USER2 D2	AF11
USER_LED2	USER3 D3	AC17
USER_LED3	USER4 D4	AB17

Configuration INIT and DONE LEDs

The ML455 board provides INIT and DONE indicator LEDs, that are turned ON by the FPGA during the configuration process. The FPGA INIT pin (G15) drives the INIT LED (D5) buffer transistor (Q2). The FPGA DONE pin (H14) drives the DONE LED (D6) buffer transistor (Q1). Refer to schematic sheet 15. Table 3-4 lists the FPGA pin assignments.

Table 3-4: **Configuration INIT and DONE LED Pin Assignments**

LED	Designation	FPGA Pin Number (FF668 Package)
FPGA_INIT	D5 INIT	G15
FPGA_DONE	D6 DONE	H14

User Push-Button Switches

The ML455 board provides four user push-button switches. The switch outputs are pulled up to 2.5V using 4.7 KΩ resistors on the board. The push buttons generate a switch closure to GND when pressed. Switch contact debounce logic must be implemented inside the FPGA. Table 3-5 lists the FPGA pin assignments.

Table 3-5: **User Push-Button Switch Assignments**

Push-Button Switch Signal	Description	FPGA Pin Number (FF668 Package)
USER_SW0	USER1 SW1	AF12
USER_SW1	USER2 SW2	AE12
USER_SW2	USER3 SW3	AC10
USER_SW3	USER4 SW4	AB10

Push-Button Program Switch (SW6)

The ML455 board provides a push-button program switch for initiating reconfiguration of the Virtex-4 FPGA. A CPLD image is provided with the ML455 board to enable pressing and releasing the program push-button switch (SW6) to initiate a full FPGA device configuration cycle while the board is powered on. The CPLD design files and bit image are on the reference CD included in the kit. Pressing this switch causes the FPGA to clear its internal configuration memory and then load the currently selected image (via the P3 image select jumper block) from the Platform Flash (U1).

Push-Button Reset Switch (SW7)

The ML455 board provides a push-button switch SW7 for a user-assigned function. This switch, labelled RESET, is wired to the CPLD U6 pin 12 (general-purpose I/O pin). The switch output is connected by a 4.7 KΩ pull-up resistor to 2.5V. This push button generates a switch closure to GND when pressed. Switch contact debounce logic must be implemented inside the CPLD. There are multiple connections between the CPLD U6 and the FPGA U10 to transmit SW7 activity. Refer to schematic sheet 14.

RS232 Port

The ML455 board provides a DB9-M (P4) connector for the RS232 port. The board uses the Maxim MAX3316ECUP (U5) device to drive the RD, TD, RTS, and CTS signals. The MAX3316 RS232 interface device operates from a 2.5V supply. The interface between the MAX3316 and the FPGA is at LVCMOS_25 standard levels. Charge pump capacitors allow the MAX3316 connector (P4) RS232 interface signals a nominal ± 4V swing up to 460 kb/s data rate. The user must provide a UART core internal to the FPGA to enable serial communication.

Table 3-6 describes the RS232 interface pin assignments.

Table 3-6: **RS232 Interface Signal Names and Pin Assignments**

Signal Name	Description	DB9M (P4) Pin Number	MAX3316 (U5) Pin Number	Signal Level
RX (In)	Receive Data RD	2	16	Up to ±25V
TX (Out)	Transmit Data TD	3	17	±4V
RTS (Out)	Request to Send RTS	7	8	±4V
CTS (In)	Clear to Send CTS	8	9	Up to ±25V
GND	Signal Ground SG	5, 9	18	N/A

Table 3-7 describes the serial interface pin assignments.

Table 3-7: **Serial Interface Signal Names and Pin Assignments**

Signal Name	Description	MAX3316 Pin Number (U5)	Signal Level	Direction at MAX3316 (U5)	FPGA Pin Number XC4VLX25-FF668 (U10)
T1 (In)	Logic Level TX	14	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$	Output	AC12
R1 (Out)	Logic Level RX	15	$0.3 \times V_{CC}$ to $0.7 \times V_{CC}$	Input	AA14
R2 (Out)	Logic Level CTS	12	$0.3 \times V_{CC}$ to $0.7 \times V_{CC}$	Input	AB14
T2 (In)	Logic Level RTS	13	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$	Output	AC11

Notes:
1. MAX3316 (U5) $V_{CC} = 2.5V$.

Figure 3-3 is a high-level block diagram of the RS232 interface.

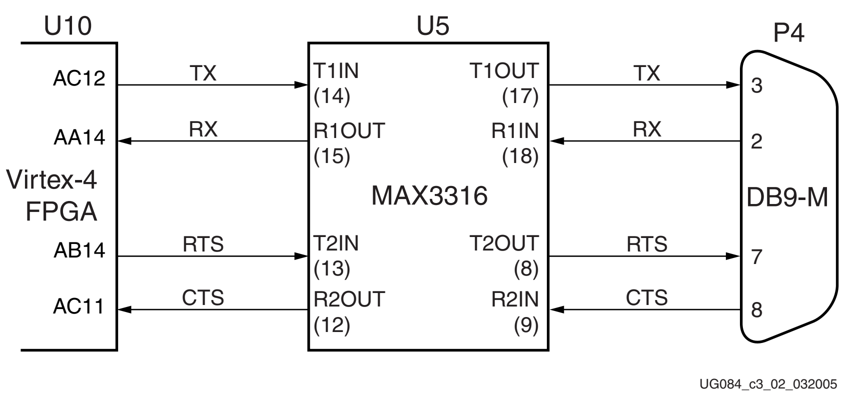


Figure 3-3: **RS232 Interface Block Diagram**

The RS232 DB9-F to DB9-F cable is not included in the kit. A NULL modem DB9-F to DB9-F serial cable is required for ML455 to PC serial communications.

General-Purpose I/O and LCD Header

P11 is a 2 x 9 male pin header providing two functions:

- General-purpose I/O header for logic analysis and so forth. Fifteen of the 16 test pins (TEST[16:1]) are wired directly to the U10 LX25 Bank 9 I/O pins. Signal TEST1 is wired to P11.3 using a 0 Ω resistor R243. This resistor is typically removed when P11 is used to support LCD operation (described below). There are no pull-up or pull-down resistors on these test signals. When this header is used in this (general-purpose) mode, P11 pins 1 and 2 normally are unused. R243 (0 Ω) is installed, and R244 and R245 are removed.
- Optional LCD support mode. The signals wired to P11 can optionally be assigned LCD interface functions. The 2 x 9 header is pinned out to match most standard LCD modules. P11 pins 1 and 2 can each be wired to either GND or V_{CC}. V_{CC} is selected from an array of available voltages via the placement of a 0 Ω resistor (one only) at locations R252 (5V) or R253 (3.3V) or R254 (SKT_VCCO). SKT_VCCO can be either 3.0V or 2.5V, selected at the 3-pin header P18. For the LCD mode, R243 is removed, and R244 and R245 are installed to provide the LCD contrast voltage required by most LCD modules. The values of R244 and R245 are calculated for a specific LCD display, since LCD displays have different LCD_DRIVE contrast voltage settings.

Figure 3-4 shows the P11 header with one possible, optional LCD signal assignment.

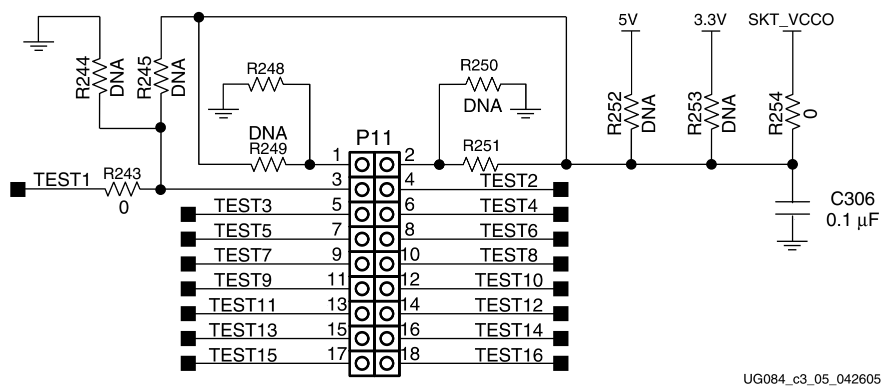


Figure 3-4: **P11 Header**

Table 3-8 lists the pinout of the P11 header for both General-Purpose and LCD modes.

Table 3-8: **General-Purpose Header P11**

Signal Name		P11 Pin #	FPGA Pin #
GP Mode	**LCD Mode**		
GND	VCC or GND	1	no connect
VCC	VCC or GND	2	no connect
test1	LCD_DRIVE	3	N21
test2	LCD_DATA7	4	N20
test3	LCD_DATA6	5	P24
test4	LCD_DATA5	6	P23
test5	LCD_DATA4	7	P20

Table 3-8: **General-Purpose Header P11 *(Continued)***

Signal Name		P11 Pin #	FPGA Pin #
GP Mode	LCD Mode		
test6	LCD_DATA3	8	P19
test7	LCD_DATA2	9	T24
test8	LCD_DATA1	10	T23
test9	LCD_DATA0	11	T26
test10	LCD_EN	12	U26
test11	LCD_RD_WR_B	13	U23
test12	LCD_REGSEL	14	V23
test13	LCD_RESET_B	15	T21
test14	LCD_CS_B	16	T20
test15	not used	17	V26
test16	not used	18	V25

Power Consumption

The PCI specification outlines the power consumption limitations for PCI add-in boards. The maximum allowable power consumption across all power rails (+5V, +3.3V, +12V, -12V) is 25W.

On the PCI connector two signals allow the power demand of a board to be specified.

The PRSNT[1:2]# signals are used by a system board to detect if an add-in card is physically present in the slot and the total power requirements of the add-in card. The signals are required for the add-in card but are optional for the system board. The ML455 board uses the EDGE_PRSNT1# and EDGE_PRSNT2# signals to request the maximum 25W power limit by grounding PRSNT1# and leaving PRSNT2# open. The SKT_PRSNT[1:2]# signals on the PCI-X expansion socket (J1) are routed to the FPGA for sensing.

A board plugged into the top-mounted PCI connector J1 should be configured to request no more than 15W.

Voltage Regulators

The ML455 board is powered from the PCI slot that it is plugged into, utilizing the +5V and the +3.3V power rails (see Table 3-11 for the specific power pins within the PCI edge connector pinout).

The ML455 board on-board power rails are 5.0V, 3.3V, 3.0V, 2.5V, 1.8V, 1.2V, and 1.25V. Table 3-9 lists the voltages.

Table 3-9: **Power Supplies**

Designation	Input	Output	I_{Max}	Device Type	Primary Use
None	5V	N/A	PCI	Edge Connector A5, A8, A61, A62, B5, B6, B61, B62	Voltage Regulator Input U3
					PCI 64-bit Socket J1
					LED Power D5, D6
					VR1 1.25V V_{TT} Regulator
None	3.3V	N/A	PCI	Edge Connector A10, A16, A21, A27, A33, A39, A45, A53, A59, A66, A75, AB4, B19, B25, B31, B36, B91, B93, B54, B59, B70, B79, B88	Voltage Regulator Input for U2, U4, and U7.
					LED Power D1, D2, D3, D4
					Y3 Osc V_{CC}
					PCI 64-bit Socket J1
U3	5V	3.0V	3A	LT1764A (adj.)	U10 LX25 Banks 3, 6, 10 V_{CCO}
					U8 Clk Buf V_{CC}
U2	3.3V	2.5V	3A	LT1764A (adj.)	U10 LX25 Banks 1, 2, 4, 7, 8 V_{CCO} and V_{CCAUX}
					J4 SODIMM Socket
					U5 MAX3316 V_{CC}
					U1 XC32FP V_{CCO}
					Y1,Y2 Oscillator V_{CC}
					P9 PC IV Cable Connector
U7	3.3V	1.8V	0.5A	LT1763CS8	U6 XC (CPLD) V_{CC}
					U1 XC32FP V_{CCINT}, V_{CCJ}
U4	3.3V	1.2V	3A	LT1764A (adj.)	U10 LX25 V_{CCINT}
VR1	5V	1.25V	6A	PTH0505Y-AH	J4 SODIMM Socket V_{REF}
					Memory Term. R Pullup V

Notes:

1. On-board voltage regulators are shown in the schematics provided on the kit CD, on schematic sheet 17.

Voltage Regulator Circuit Descriptions

This section describes the voltage regulators on the ML455 board.

LT1764A Voltage Regulators

Figure 3-5 shows the LT1764A 5-pin linear 3A capable voltage regulators (U2, U3, and U4), which have the same basic topology. The output adjust resistor is calculated from the formula given in the Linear Technology data sheet (part number LT1764AF) at www.linear-tech.com):

$V_{OUT} = 1.21V (1 + (R2/R1)) + (I_{ADJ})(R2)$

Where $I_{ADJ} = 3\ \mu A$ at $T_J = 25\ °C$ where T_J = junction temperature, R1 < 4.17 KΩ, and the output range is from 1.21V to 20V.

Choosing a 169 Ω, standard 1% resistor for R1, the formula can be re-arranged to:

$R2 = V_{OUT} - 1.21/.007162$

Using this formula with a V_{OUT} of 2.50V gives an R2 value of 180 Ω. The closest standard 1% resistor is 182 Ω, which, when plugged back into the original formula, gives $V_{OUT} = 2.513613V$ (0.5% difference).

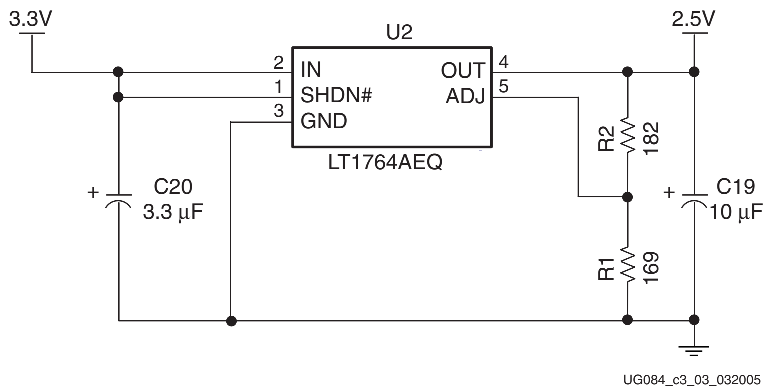


Figure 3-5: **LT1764A Voltage Regulator Circuit**

Table 3-10 summarizes the adjustment resistor values for the LT1764A regulators U2, U3, and U4.

Table 3-10: **LT1764 Resistor Calculations**

	V_{OUT}	R1	R2	V_{CALC}	Calc Diff	% Diff
U2 2.50V						
–5%	2.375	169	162	2.370367657	–0.051852937	–5.2%
Nom.	2.500	169	182	2.513622923	0.005449169	+0.5%
+5%	2.625	169	200	2.642552663	0.057021065	+5.7%
U3 3.0V						
–5%	2.850	169	226	2.828784509	–0.05707183	–5.7%
Nom.	3.000	169	255	3.036504645	0.012168215	+1.2%
+5%	3.150	169	274	3.172597148	0.057532383	+5.7%
U4 1.2V						
–5%	1.140	N/A	N/A			
Nom.	1.200	none	none	1.21	0.008333333	+0.8%
+5%	1.260	N/A	N/A			

Notes:

1. The LT1764A minimum voltage out is 1.21V, achieved with no adjust resistor network. Adj pin 5 is wired to V_{OUT} pin 4. Because the minimum V_{OUT} = 1.21V, this regulator cannot be adjusted ± 5%.

LT1763CS88 Voltage Regulator

Figure 3-6 shows the LT1763CS8 SOIC8 linear 0.5A capable voltage regulator (U7). The output adjust resistor is calculated from the formula given in the Linear Technology data sheet (part number LT1763A) at www.linear-tech.com):

$$V_{OUT} = 1.22V\,(1 + (R2/R1) + (I_{ADJ})R2)$$

Where I_{ADJ} = 30 nA at T_J = 25 °C, R1 < 250KΩ, and the output range is from 1.22V to 20V.

Choosing a 78.7 Ω, standard 1% resistor for R1, The formula can be re-arranged to:

$$R2 = V_{OUT} - 1.22/.01550194$$

Using this formula with a V_{OUT} of 1.80V gives an R2 value of 37.41 Ω. A close standard 1% resistor is 38.3 Ω, which, when plugged back into the original formula, gives V_{OUT} = 1.8137244V (0.762% difference).

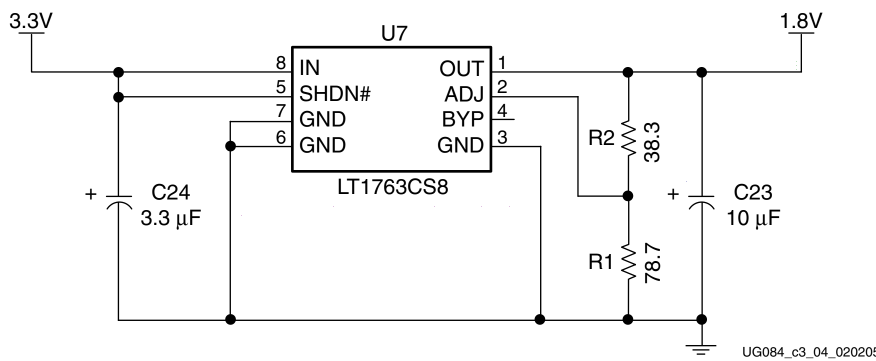


Figure 3-6: **LT1763CS8 Voltage Regulator**

PCI 3.0V Interface Voltage Regulator

Figure 3-7 shows the LT1764AEQ (U3) voltage regulator, set at 3.0V. This regulator sources V_{CCO} to U10 LX25 Banks 6 and 10, the PCI edge connector interface banks. The following Xilinx application notes provide PCI interface designs using Xilinx devices:

- XAPP646: "Connecting Virtex-II Devices to a 3.3V/5V PCI Bus"
- XAPP653: "3.3V PCI Design Guidelines"
- XAPP659: "Using 3.3V I/O Guidelines in a Virtex-II Pro Design"

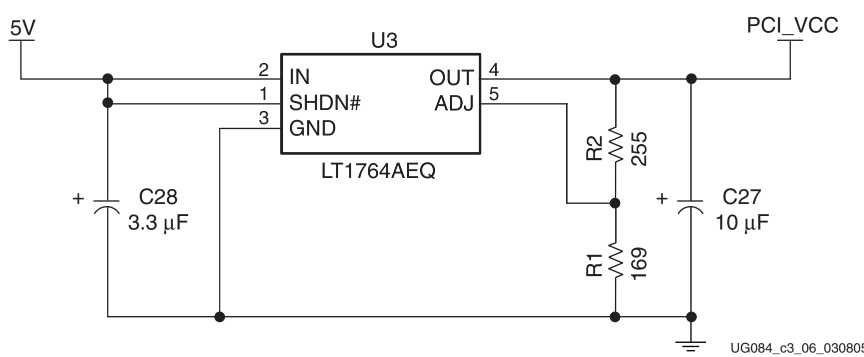


Figure 3-7: **LT1764AEQ (PCI 3.0V) Voltage Regulator**

DDR Memory Bus Termination Module

The ML455 board has an onboard 2.5V 200-pin DDR SODIMM socket. The SODIMM provided with the ML455 is the Micron 128 MB MT8VDDT1664HDG-265B3, organized as 16M x 64. The data sheet for this SODIMM is located at http://www.micron.com.

The linear voltage regulator U2 provides the 2.5V required by the SODIMM. The memory interface also requires a termination resistor network, typically driven by memory $V_{DD}/2$. The 1.25V V_{TT} termination supply VR1 is a TI PTH0505Y-AH switching source/sink reference module capable of handling 6A (see Figure 3-8). A resistor divider network (two 1 KΩ 1% resistors in series) is applied to the U2 2.5V output to create the 1.25V reference module input voltage. The module output closely tracks the input.

The data sheet for the TI module is located at http://focus.ti.com/docs/prod/folders/print/pth05050y.html.

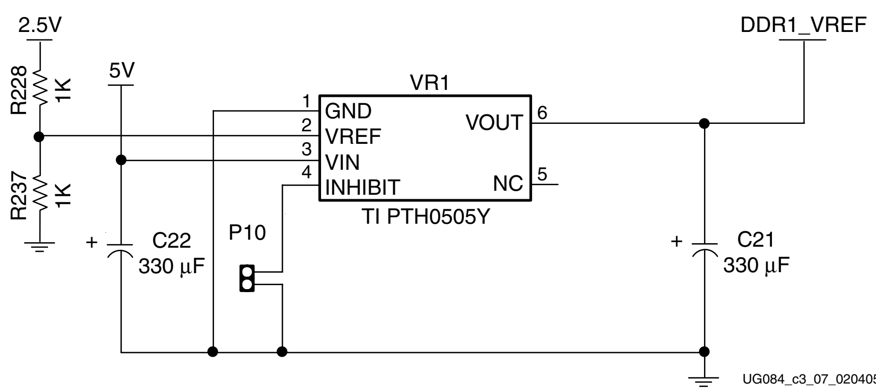


Figure 3-8: **PTH0505Y-A V_{TT} Termination Supply**

64-bit PCI Edge Connector

Table 3-11 shows the edge connector pin assignment (the component side of the PCB is side A, and the non-component side or the back of the PCB is side B).

Table 3-11: **P1 PCI Edge Connector Pinout**

P1 A Side	Signal	P1 B Side	Signal
32-Bit Connector			
A1	unused	B1	VCC_MINUS12
A2	VCC12	B2	unused
A3	unused	B3	GND
A4	EDGE_JTAG	B4	EDGE_JTAG
A5	VCC5	B5	VCC5
A6	EDGE_INTA_B	B6	VCC5
A7	EDGE_INTC_B	B7	EDGE_INTB_B
A8	VCC5	B8	EDGE_INTD_B

Table 3-11: **P1 PCI Edge Connector Pinout *(Continued)***

P1 A Side	Signal	P1 B Side	Signal
A9	unused	B9	GND
A10	VCC3V3	B10	unused
A11	unused	B11	unused
	3.3V KEY		3.3V KEY
	3.3V KEY		3.3V KEY
A14	2N375	B14	unused
A15	EDGE_RST_B	B15	GND
A16	VCC3V3	B16	CLK_FROM_EDGE
A17	EDGE_GNT_B	B17	GND
A18	GND	B18	EDGE_REQ_B
A19	EDGE_PME_B	B19	VCC3V3
A20	EDGE_AD30	B20	EDGE_AD31
A21	VCC3V3	B21	EDGE_AD29
A22	EDGE_AD28	B22	GND
A23	EDGE_AD26	B23	EDGE_AD27
A24	GND	B24	EDGE_AD25
A25	EDGE_AD24	B25	VCC3V3
A26	EDGE_IDSEL	B26	EDGE_CBE3
A27	VCC3V3	B27	EDGE_AD23
A28	EDGE_AD22	B28	GND
A29	EDGE_AD20	B29	EDGE_AD21
A30	GND	B30	EDGE_AD19
A31	EDGE_AD18	B31	VCC3V3
A32	EDGE_AD16	B32	EDGE_AD17
A33	VCC3V3	B33	EDGE_CBE2
A34	EDGE_FRAME_B	B34	GND
A35	GND	B35	EDGE_IRDY_B
A36	EDGE_TRDY_B	B36	VCC3V3
A37	GND	B37	EDGE_DEVSEL_B
A38	EDGE_STOP_B	B38	EDGE_PCIXCAP
A39	VCC3V3	B39	unused
A40	unused	B40	EDGE_PERR_B

Table 3-11: **P1 PCI Edge Connector Pinout *(Continued)***

P1 A Side	Signal	P1 B Side	Signal
A41	unused	B41	VCC3V3
A42	GND	B42	EDGE_SERR_B
A43	EDGE_PAR	B43	VCC3V3
A44	EDGE_AD15	B44	EDGE_CBE1
A45	VCC3V3	B45	EDGE_AD14
A46	EDGE_AD13	B46	GND
A47	EDGE_AD11	B47	EDGE_AD12
A48	GND	B48	EDGE_AD10
A49	EDGE_AD9	B49	EDGE_M66EN
A50	GND	B50	GND
A51	GND	B51	GND
A52	EDGE_CBE0	B52	EDGE_AD8
A53	VCC3V3	B53	EDGE_AD7
A54	EDGE_AD6	B54	VCC3V3
A55	EDGE_AD4	B55	EDGE_AD5
A56	GND	B56	EDGE_AD3
A57	EDGE_AD2	B57	GND
A58	EDGE_AD0	B58	EDGE_AD1
A59	VCC3V3	B59	VCC3V3
A60	EDGE_REQ64_B	B60	EDGE_ACK64_B
A61	VCC5	B61	VCC5
A62	VCC5	B62	VCC5
64-Bit Connector			
A63	GND	B63	unused
A64	EDGE_CBE7	B64	GND
A65	EDGE_CBE5	B65	EDGE_CBE6
A66	VCC3V3	B66	EDGE_CBE4
A67	EDGE_PAR64	B67	GND
A68	EDGE_AD62	B68	EDGE_AD63
A69	GND	B69	EDGE_AD61
A70	EDGE_AD60	B70	VCC3V3
A71	EDGE_AD58	B71	EDGE_AD59

Table 3-11: **P1 PCI Edge Connector Pinout *(Continued)***

P1 A Side	Signal	P1 B Side	Signal
A72	GND	B72	EDGE_AD57
A73	EDGE_AD56	B73	GND
A74	EDGE_AD54	B74	EDGE_AD55
A75	VCC3V3	B75	EDGE_AD53
A76	EDGE_AD52	B76	GND
A77	EDGE_AD50	B77	EDGE_AD51
A78	GND	B78	EDGE_AD49
A79	EDGE_AD48	B79	VCC3V3
A80	EDGE_AD46	B80	EDGE_AD47
A81	GND	B81	EDGE_AD45
A82	EDGE_AD44	B82	GND
A83	EDGE_AD42	B83	EDGE_AD43
A84	VCC3V3	B84	EDGE_AD41
A85	EDGE_AD40	B85	GND
A86	EDGE_AD38	B86	EDGE_AD39
A87	GND	B87	EDGE_AD37
A88	EDGE_AD36	B88	VCC3V3
A89	EDGE_AD34	B89	EDGE_AD35
A90	GND	B90	EDGE_AD33
A91	EDGE_AD32	B91	GND
A92	unused	B92	unused
A93	GND	B93	unused
A94	unused	B94	GND

The two PCI buses on the board schematics have signal names of the form EDGE_<signal name> (denoting the card edge connector signals) and SKT_<signal name> (denoting the signals wired to the top mounted PCI socket). The signal names listed in the A Side and B Side columns of Table 3-11 and Table 3-12 are standard PCI signal names.

The ML455 board supports both PCI and PCI-X applications. The edge connector interfaces with the system board connector. Xilinx has both PCI and PCI-X LogiCORE intellectual property cores available to facilitate getting started with application specific design.

ML455 Board Implementation

IDSEL

The three-pin P13 IDSEL header for PCI socket J1 is wired as follows:

- P13.1 - The FPGA_SPARE signal is wired to the spare FPGA I/O pin U10.R23.
- P13.2 - SKT_IDSEL is wired to J1.A26 (the standard PCI socket IDSEL pin).
- P13.3 - A 2 KΩ series resistor is wired to SKT_AD17, pin J1.B32.

M66EN - 66MHz Enable

P1.B49 is wired to two-pin header pin P9.1. With the P9 jumper shunt removed, M66EN has a 0.01 µF capacitor to GND. Placing the jumper shunt across pins 1 and 2 of P9 shorts M66EN to GND.

- M66EN = GND indicates 0 to 33 MHz operation.
- M66EN = open indicates 33 MHz to 66 MHz operation. (M66EN is pulled up on the system board.)

PME# - Power Management Event

P1.A19 is wired to a two-pin header pin P7.1. PME# is pulled up on the system board. P7.2 is wired to U10 LX25 Bank 6 pin A7, allowing the FPGA to drive or sense the PME# signal when a jumper shunt is placed across pins 1 and 2 of P7. The PCI/PCI-X LogiCore User Guide can be consulted for more information on proper use of PME#.

PCIXCAP - PCI-X Capability

P1.B38 is wired to 3-pin header P8 (center pin).

- P8.1 is wired to GND through a 10KΩ pulldown resistor.
- P8.2 is wired to P1.B38 and a 0.01µF capacitor to GND.
- P8.3 is wired to GND.
- A jumper shunt across P8 pins 1 and 2 indicates that the card is PCI-X 66 capable.
- No jumper shunt across P8 indicates that the card is PCI-X 133 capable.
- A jumper shunt across P8 pins 2 and 3 indicates that the card is not PCI-X capable (i.e., is PCI, not PCI-X).

64-bit PCI Socket (Top of the ML455 Board)

Table 3-12 shows the top PCI connector pin assignment.

Table 3-12: **J1 PCI Socket Pinout**

J1 A Side	Signal	J1 B Side	Signal
32-Bit Socket			
A1	SKT_TRST_B	B1	VCC_MINUS12
A2	VCC12	B2	SKT_TCK
A3	SKT_TMS	B3	GND
A4	SKT_TDI	B4	unused
A5	VCC5	B5	VCC5
A6	SKT_INTA_I_B	B6	VCC5
A7	SKT_INTC_I_B	B7	SKT_INTB_I_B
A8	VCC5	B8	SKT_INTD_I_B
A9	unused	B9	SKT_PRSNT1_B
A10	VCC3V3	B10	unused
A11	unused	B11	SKT_PRSNT2_B
	3.3V KEY		3.3V KEY
	3.3V KEY		3.3V KEY
A14	VCC3V3	B14	unused
A15	SKT_RST_O_B	B15	GND
A16	VCC3V3	B16	CLK_TO_SOCKET
A17	SKT_GNT_I_B	B17	GND
A18	GND	B18	SKT_REQ_O_B
A19	SKT_PME_O_B	B19	VCC3V3
A20	SKT_AD30	B20	SKT_AD31
A21	VCC3V3	B21	SKT_AD29
A22	SKT_AD28	B22	GND
A23	SKT_AD26	B23	SKT_AD27
A24	GND	B24	SKT_AD25
A25	SKT_AD24	B25	VCC3V3
A26	SKT_IDSEL	B26	SKT_CBE3_B
A27	VCC3V3	B27	SKT_AD23
A28	SKT_AD22	B28	GND

Table 3-12: **J1 PCI Socket Pinout *(Continued)***

J1 A Side	Signal	J1 B Side	Signal
A29	SKT_AD20	B29	SKT_AD21
A30	GND	B30	SKT_AD19
A31	SKT_AD18	B31	VCC3V3
A32	SKT_AD16	B32	SKT_AD17
A33	VCC3V3	B33	SKT_CBE2_B
A34	SKT_FRAME_B	B34	GND
A35	GND	B35	SKT_IRDY_B
A36	SKT_TRDY_B	B36	VCC3V3
A37	GND	B37	SKT_DEVSEL_B
A38	SKT_STOP_B	B38	SKT_PCIXCAP
A39	VCC3V3	B39	unused
A40	SKT_SMBCLK	B40	SKT_PERR_B
A41	SKT_SMBDAT	B41	VCC3V3
A42	GND	B42	SKT_SERR_B
A43	SKT_PAR	B43	VCC3V3
A44	SKT_AD15	B44	SKT_CBE1_B
A45	VCC3V3	B45	SKT_AD14
A46	SKT_AD13	B46	GND
A47	SKT_AD11	B47	SKT_AD12
A48	GND	B48	SKT_AD10
A49	SKT_AD9	B49	SKT_M66EN
A50	GND	B50	GND
A51	GND	B51	GND
A52	SKT_CBE0_B	B52	SKT_AD8
A53	VCC3V3	B53	SKT_AD7
A54	SKT_AD6	B54	VCC3V3
A55	SKT_AD4	B55	SKT_AD5
A56	GND	B56	SKT_AD3
A57	SKT_AD2	B57	GND
A58	SKT_AD0	B58	SKT_AD1
A59	VCC3V3	B59	VCC3V3
A60	SKT_REQ64_B	B60	SKT_ACK64_B

Table 3-12: **J1 PCI Socket Pinout *(Continued)***

J1 A Side	Signal	J1 B Side	Signal
A61	VCC5	B61	VCC5
A62	VCC5	B62	VCC5
64-Bit Socket			
A63	GND	B63	unused
A64	SKT_CBE7_B	B64	GND
A65	SKT_CBE5_B	B65	SKT_CBE6_B
A66	VCC3V3	B66	SKT_CBE4_B
A67	SKT_PAR64	B67	GND
A68	SKT_AD62	B68	SKT_AD63
A69	GND	B69	SKT_AD61
A70	SKT_AD60	B70	VCC3V3
A71	SKT_AD58	B71	SKT_AD59
A72	GND	B72	SKT_AD57
A73	SKT_AD56	B73	GND
A74	SKT_AD54	B74	SKT_AD55
A75	VCC3V3	B75	SKT_AD53
A76	SKT_AD52	B76	GND
A77	SKT_AD50	B77	SKT_AD51
A78	GND	B78	SKT_AD49
A79	SKT_AD48	B79	VCC3V3
A80	SKT_AD46	B80	SKT_AD47
A81	GND	B81	SKT_AD45
A82	SKT_AD44	B82	GND
A83	SKT_AD42	B83	SKT_AD43
A84	VCC3V3	B84	SKT_AD41
A85	SKT_AD40	B85	GND
A86	SKT_AD38	B86	SKT_AD39
A87	GND	B87	SKT_AD37
A88	SKT_AD36	B88	VCC3V3
A89	SKT_AD34	B89	SKT_AD35
A90	GND	B90	SKT_AD33
A91	SKT_AD32	B91	GND

Table 3-12: **J1 PCI Socket Pinout *(Continued)***

J1 A Side	Signal	J1 B Side	Signal
A92	unused	B92	unused
A93	GND	B93	unused
A94	unused	B94	GND

The PCI bus clock for the top mounted socket J1 is created by the FPGA, at pin U10.B17. This signal SOURCE_SOCKET_CLK is routed to U8 pin 1. U8 is a four-channel PCI clock buffer device.

Channel OUT1 of U8, on pin 5, is wired to PCI bus clock J1.B16.

There are also two feedback clock traces wired from U8 back to FPGA U10, U8.3 (OUT0), signal FEEDBACK_SOCKET_CLK_GLOBAL is routed to U10.A17, and U8.8 (OUT3), signal FEEDBACK_SOCKET_CLK_REGIONAL is routed to U10.D25.

The three clock traces driven from U8 are length matched to enable the FPGA to sense the clock timing at the J1 PCI socket.

XC2C32 CoolRunner-II CPLD U6

Figure 4-5, page 38 and Table 4-4, page 40 summarize the CPLD connections to:

- U1: XCF32PFSG48C Platform Flash configuration device
- U10: XC4VLX25 FPGA Bank 1
- U10: XC4VLX25 FPGA Bank 0 Configuration I/F
- P3: Configuration Image select header
- SW6 (PROG), SW7: General purpose push-button switches

All XC2C32 I/O are 2.5V, and the XC2C32 V_{CCINT} is 1.8V. Chapter 4, "Configuration," includes more details concerning the ML455 board configuration.

XCF32PFS48C Platform Flash U1

Figure 4-5, page 38 and Table 4-5, page 41 summarize the Platform Flash connections to the XC4VLX25 FPGA U10 and the XC2C32 CPLD U6.

The XCF32PFS48C V_{CCO} is 2.5V.

The Platform Flash holds up to four configuration images for the XC4VLX25 FPGA. As shown in Figure 4-5, the configuration image is selected by applying shorting blocks to header P3.

In concert with the XC2C32 CPLD, the XCF32PFS48C supports static and dynamic reconfiguration of the FPGA. Chapter 4, "Configuration," provides more details concerning the ML455 board configuration.

Reference Documents

Xilinx Documents

- DS090: CoolRunner-II CPLD Family
  http://www.xilinx.com/bvdocs/publications/ds090.pdf
- DS112: Virtex-4 Family Overview
  http://www.xilinx.com/bvdocs/publications/ds112.pdf
- DS123: Platform Flash In-System Programmable Configuration PROMS
  http://www.xilinx.com/bvdocs/publications/ds123.pdf
- DS302: Virtex-4 Data Sheet: DC and Switching Characteristics
  http://www.xilinx.com/bvdocs/publications/ds302.pdf
- UG070: Virtex-4 User Guide
  http://www.xilinx.com/bvdocs/userguides/ug070.pdf
- UG071: Virtex-4 Configuration Guide
  http://www.xilinx.com/bvdocs/userguides/ug071.pdf

PCI Special Interest Group (PCISIG)

PCI and PCI-X specifications are available from the PCI Special Interest Group (PCISIG). Contact the PCI Special Interest Group office to obtain the latest revision of these specifications. Questions regarding the PCI Local Bus Specification or the PCI-X Addendum or membership in the PCI Special Interest Group can be forwarded through:

PCI Special Interest Group (PCI-SIG)
5440 SW Westgate Dr., #217
Portland, OR 97221

Phone: 800-433-5177 (inside the U.S.), 503-291-2569 (outside the U.S.)
Fax: 503-297-1090
e-mail: administration@pcisig.com

Website: http://www.pcisig.com

- PCI Local Bus Specification, Revision 3.0
- PCI-X Addendum to the PCI Local Bus Specification

Chapter 4

Configuration

The Virtex-4 ML455 board includes several options to configure the XC4VLX25 Virtex-4 FPGA, XC2C32 CoolRunner-II CPLD, and the XCF32PF Platform Flash. The basic configuration modes for the Virtex-4 family are:

- JTAG mode via Parallel Cable IV or equivalent
- Master SelectMap mode via CPLD/Platform Flash
- Slave SelectMap mode via CPLD/Platform Flash

The CPLD and Platform Flash may only be configured via JTAG. The Platform Flash contains up to four unique bitstreams for programming the FPGA. The unique combination of the FPGA connected to the Platform Flash through the CPLD allows for static and dynamic bitstream selection of the FPGA via Slave and Master SelectMAP modes.

This chapter provides a description of the FPGA configuration circuitry and methods used on the ML455 Development Board.

Configuration Modes

Table 4-1 shows the Virtex-4 configuration modes along with the correct settings for the Configuration Mode switch (SW5). Figure 4-1 shows the Configuration Mode switch.

Table 4-1: **Configuration Modes**

Mode	JTAG P5	Mode SW5[1]		
		1 (M0)	2 (M1)	3 (M2)
Master SelectMAP	N/A	1	1	0
Slave SelectMAP	N/A	0	1	1
JTAG	Yes	1	0	1

Notes:

1. 0 = switch position is Closed. 1 = switch position is Open.

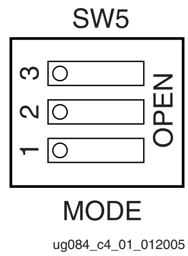


Figure 4-1: **Configuration Mode Switch**

JTAG Chain

Figure 4-2 shows the JTAG chain on the ML455 board. The chain can be driven by the following sources:

- Xilinx Parallel Cable IV
- Other JTAG cables

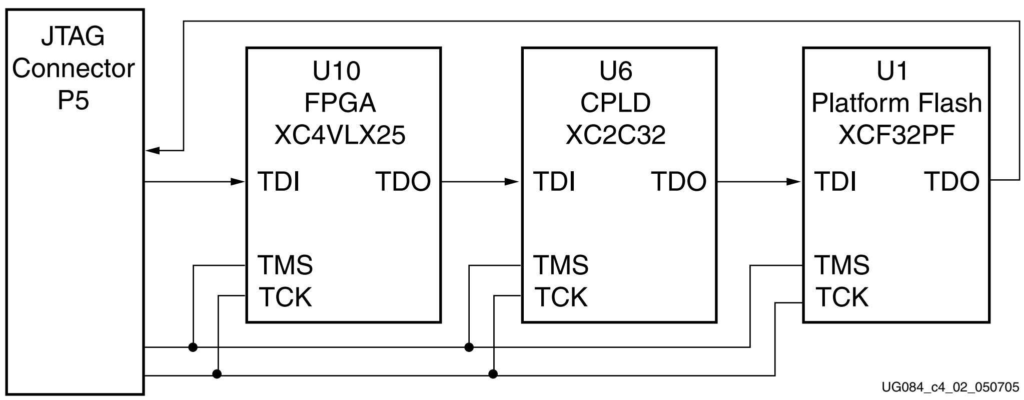


Figure 4-2: **JTAG Chain**

JTAG Port

The Virtex-4 ML455 board provides a JTAG connector (P5) to configure the Virtex-4 FPGA and program JTAG devices located in the JTAG chain. Figure 4-3 shows the pin assignments for the JTAG connector. The JTAG cable connects to P5 as shown in Figure 4-4.

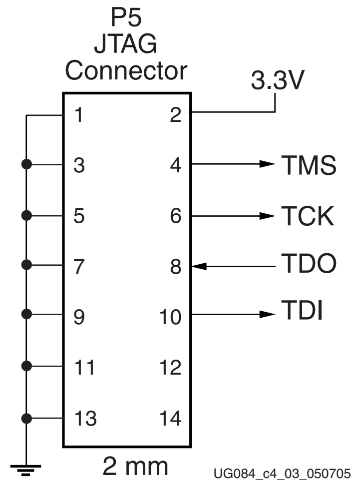


Figure 4-3: **JTAG Cable Hook-up**

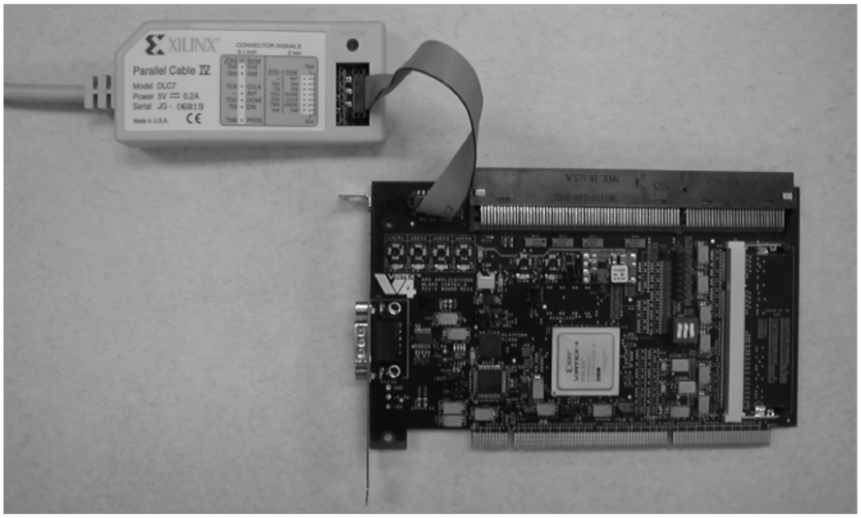


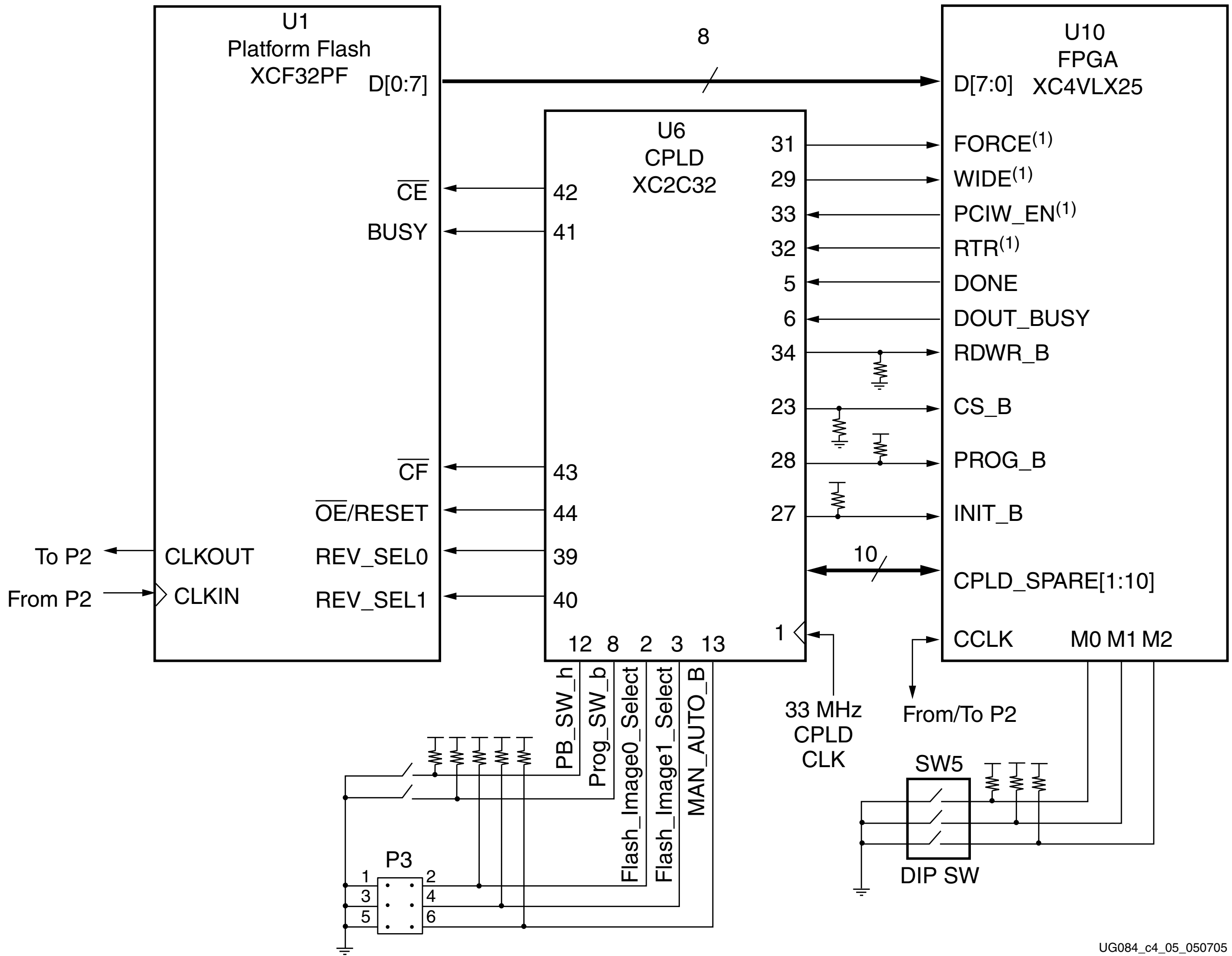
Figure 4-4: **Photo of ML455 Board and PC IV Pod Flat Cable Connection to P5**

Table 4-2: **P5 JTAG Header Signal Descriptions and Pin Assignments**

Signal Name	Description	P5 Pin Number	FPGA Pin Number	CPLD Pin Number	Flash Pin Number
JTAG_TMS	JTAG TMS to FPGA/CPLD/ FLASH	4	Y11	10	E2
JTAG_TCK	JTAG TCK to FPGA/CPLD/ FLASH	6	W12	11	H3
JTAG_TDO	JTAG TDO from FLASH	8	N/A	N/A	E6
JTAG_TDI	JTAG TDI to FPGA TDI	10	Y12	N/A	N/A

SelectMAP Interface

The SelectMAP interface is connected to the Platform Flash indirectly through the CPLD. For the SelectMAP interface to operate correctly, the CPLD needs to be programmed (via JTAG) such that the correct connections are made between the FPGA and the Flash. Figure 4-5 is a general schematic for the Flash/CPLD/FPGA SelectMAP Interface. Table 4-3 through Table 4-5 list the pinouts for the FPGA, CPLD, and Platform Flash, respectively.



Notes:

1. FORCE, WIDE, PCIW_EN, and RTR are FPGA general-purpose I/Os.

Figure 4-5: **Schematic of Flash/CPLD/FPGA SelectMAP Interface**

Table 4-3: **Pin Listing for FPGA Configuration Pins**

Pin Number	Net Name	Direction	Pin Type	Description
G14	FPGA_CCLK	I/O	CCLK	Configuration Clock Input or Output
H12	FPGA_RDWR_B	I	RDWR_B	Active-Low Read Write
G11	FPGA_CS_B	I	CS_B	Active-Low Chip Select
W15	MODE0	I	M0	Mode Select 0
Y15	MODE1	I	M1	Mode Select 1
W15	MODE2	I	M2	Mode Select 2
H15	PROG_B	I	PROGRAM_B	Active-Low asynchronous full-chip reset
G15	INIT_B	I	INIT_B	Active-Low Delay Configuration Pin
H14	FPGA_DONE	O	DONE	Active-High signal indicating configuration is complete
Y14	FPGA_BUSY_B	O	DOUT_BUSY	Active-Low Busy signal
AD13	FLASH_D0	I	IO_L8N_D0_LC	SelectMAP data bit 0 connected to Flash
AC13	FLASH_D1	I	IO_L8P_D1_LC	SelectMAP data bit 1 connected to Flash
AC15	FLASH_D2	I	IO_L7N_D2_LC	SelectMAP data bit 2 connected to Flash
AC16	FLASH_D3	I	IO_L7P_D3_LC	SelectMAP data bit 3 connected to Flash
AA11	FLASH_D4	I	IO_L6N_D4_LC	SelectMAP data bit 4 connected to Flash
AA12	FLASH_D5	I	IO_L6P_D5_LC	SelectMAP data bit 5 connected to Flash
AD14	FLASH_D6	I	IO_L5N_D6_LC	SelectMAP data bit 6 connected to Flash
AC14	FLASH_D7	I	IO_L5P_D7_LC	SelectMAP data bit 7 connected to Flash
F13	FORCE(1, 2)	I	IO_L1N_D30_LC	Input connected from Pin 31 of CPLD
F12	WIDE(1, 2)	I	IO_L2P_D29_LC	Input connected from Pin 29 of CPLD
F11	PCIW_EN(1, 2)	O	IO_L2N_D28_LC	Output connected to Pin 33 of CPLD
F16	RTR(1, 2)	O	IO_L3P_D27_LC	Output connected to Pin 32 of CPLD
D14	CPLD_SPARE1(2)	I/O	IO_L4P_D25_LC	Spare I/O connected to CPLD pin 14
D13	CPLD_SPARE2(2)	I/O	IO_L4N_D24_VREF_LC	Spare I/O connected to CPLD pin 16
D15	CPLD_SPARE3(2)	I/O	IO_L5P_D23_LC	Spare I/O connected to CPLD pin 18
E14	CPLD_SPARE4(2)	I/O	IO_L5N_D22_LC	Spare I/O connected to CPLD pin 19
C11	CPLD_SPARE5(2)	I/O	IO_L6P_D21_LC	Spare I/O connected to CPLD pin 20
D11	CPLD_SPARE6(2)	I/O	IO_L6N_D20_LC	Spare I/O connected to CPLD pin 21
D16	CPLD_SPARE7(2)	I/O	IO_L7P_D19_LC	Spare I/O connected to CPLD pin 22
C16	CPLD_SPARE8(2)	I/O	IO_L7N_D18_LC	Spare I/O connected to CPLD pin 36
E13	CPLD_SPARE9(2)	I/O	IO_L8P_D17_LC	Spare I/O connected to CPLD pin 37
D12	CPLD_SPARE10(2)	I/O	IO_L8N_D16_LC	Spare I/O connected to CPLD pin 38

Notes:

1. The Net Names and Directions for pins F13, F12, F11, and F16 were chosen to support a specific PCI/PCI-X design as described below in "CPLD Programming Examples." The user can use these pins as spare, bidirectional pins.
2. Use LVCMOS_25 I/O standard for general-purpose I/O connected to the CPLD.

Table 4-4: **Pin Listing for CPLD**

Pin Number	Net Name	Direction	Pin Type	Description
1	CPLD_CLK_33MHZ	I	IO/GC1	33 MHz Global Clock Input
41	BUSY_TO_FLASH_B	O	IO23	Output connected to BUSY pin of Flash
30	EDGE_RST_I_B(1)	I	IO/GS-R	Input connected from Pin A15 of Edge PCI
42	FLASH_CE_B	O	IO24	Output connected to /CE pin of Flash
43	FLASH_CF_B	O	IO/GC2	Output connected to /CF pin of Flash
2	FLASH_IMAGE0_SELECT	I	IO1	Revision Select Pin 0 from Header P3
3	FLASH_IMAGE1_SELECT	I	IO2	Revision Select Pin 1 from Header P3
44	FLASH_OE_RESET_B	O	IO/GC3	Output connected to OE_/RESET pin of Flash
39	FLASH_REV_SEL0	O	IO21	Output connected to REV_SEL0 pin of Flash
40	FLASH_REV_SEL1	O	IO22	Output connected to REV_SEL1 pin of Flash
31	FORCE(1)	O	IO/GOE1	Output connected to Pin F13 of FPGA
6	FPGA_BUSY_B	I	IO4	DOUT Busy pin from FPGA
23	FPGA_CS_B	I	IO14	Chip Select from FPGA
5	FPGA_DONE	I	IO3	DONE pin from FPGA
34	FPGA_RDWR_B	O	IO/GOE4	Output connected to RDWR_B pin of FPGA
27	INIT_B	O	IO15	Output connected to INIT_B pin of FPGA
11	JTAG_TCK	I	TCK	JTAG TCK
10	JTAG_TMS	I	TMS	JTAG TMS
9	FPGA_TDO	I	TDI	JTAG TDI from FPGA
24	CPLD_TDO	O	TDO	JTAG TDO to Flash
13	MAN_AUTO_B	I	IO7	Manual/Auto Select pin from Header P3
12	PB_SW_B	I	IO6	Input from Push Button SW7
33	PCIW_EN(1)	I	IO/GOE3	Input connected from Pin F11 of FPGA
28	PROG_B	O	IO16	Output connected to PROG_B pin of FPGA
8	PROG_SW_B	I	IO5	Input from Push Button SW6
32	RTR(1)	I	IO/GOE2	Input connected from Pin F16 of FPGA
29	WIDE(1)	O	IO17	Output connected to Pin F12 of FPGA
14	CPLD_SPARE1	I/O	IO8	Spare I/O connected to FPGA pin D14
38	CPLD_SPARE10	I/O	IO20	Spare I/O connected to FPGA pin D12
16	CPLD_SPARE2	I/O	IO9	Spare I/O connected to FPGA pin D13
18	CPLD_SPARE3	I	I	Spare Input connected to FPGA pin D15
19	CPLD_SPARE4	I/O	IO10	Spare I/O connected to FPGA pin E14
20	CPLD_SPARE5	I/O	IO11	Spare I/O connected to FPGA pin C11

Table 4-4: **Pin Listing for CPLD *(Continued)***

Pin Number	Net Name	Direction	Pin Type	Description
21	CPLD_SPARE6	I/O	IO12	Spare I/O connected to FPGA pin D11
22	CPLD_SPARE7	I/O	IO13	Spare I/O connected to FPGA pin D16
36	CPLD_SPARE8	I/O	IO18	Spare I/O connected to FPGA pin C16
37	CPLD_SPARE9	I/O	IO19	Spare I/O connected to FPGA pin E13
4	GND	I	GND1	Ground
17	GND	I	GND2	Ground
25	GND	I	GND3	Ground
15	VCC1V8	I	VCC	1.8V Power
7	VCC2V5	I	VCCIO1	2.5V I/O Power
26	VCC2V5	I	VCCIO2	2.5V I/O Power
35	VCC2V5	I	VAUX	2.5V Auxiliary Power

Notes:

1. The Net Names and Directions for pins 29 through 33 were chosen to support a specific PCI/PCI-X design as described in "CPLD Programming Examples." The user can use these pins as spare, bidirectional pins.
2. All CPLD I/O are 2.5V LVCMOS.

Table 4-5: **Pin Listing for Flash**

Pin Number	Net Name	Direction	Pin Type	Description
C1	BUSY_TO_FLASH_B	I	BUSY	Active-Low Busy signal connected from CPLD Pin 41
G1	CPLD_TDO	I	TDI	JTAG TDI connected from CPLD JTAG TDO
B4	FLASH_CE_B	I	$\overline{\text{CE}}$	Active-Low Chip Enable connected from CPLD Pin 42
D1	FLASH_CF_B	I	$\overline{\text{CF}}$	Active-Low Configuration Pulse input connected to CPLD Pin 43
B3	FLASH_CLKIN	I	CLK	Clock Input connected from Pin 1 of Header P2
C2	FLASH_CLKOUT	O	CLKOUT	Clock Output connected to Pin 5 of Header P2
H6	FLASH_D0	O	D0	SelectMAP data bit 0 connected to FPGA
H5	FLASH_D1	O	D1	SelectMAP data bit 1 connected to FPGA
E5	FLASH_D2	O	D2	SelectMAP data bit 2 connected to FPGA
D5	FLASH_D3	O	D3	SelectMAP data bit 3 connected to FPGA
C5	FLASH_D4	O	D4	SelectMAP data bit 4 connected to FPGA
B5	FLASH_D5	O	D5	SelectMAP data bit 5 connected to FPGA
A5	FLASH_D6	O	D6	SelectMAP data bit 6 connected to FPGA
A6	FLASH_D7	O	D7	SelectMAP data bit 7 connected to FPGA

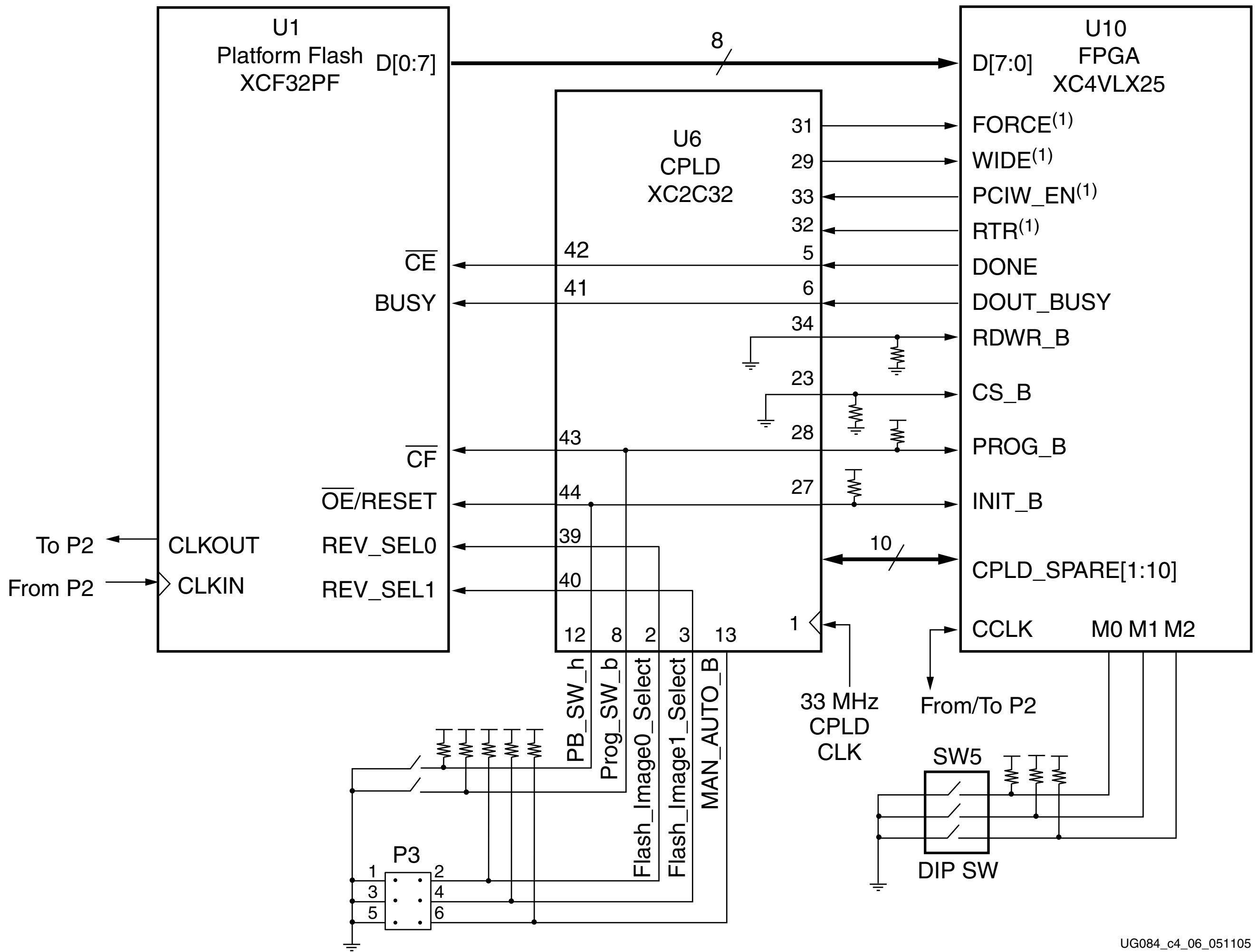
Table 4-5: **Pin Listing for Flash *(Continued)***

Pin Number	Net Name	Direction	Pin Type	Description
H4	FLASH_EN_EXT_SEL_B	I	$\overline{\text{EN\_EXT\_SEL}}$	Enable External Selection input – tied Low
A3	FLASH_OE_RESET_B	I/O	$\overline{\text{OE}}$/RESET	Output Enable / Active-Low Reset
G3	FLASH_REV_SEL0	I	REV_SEL0	Revision Select 0 input connected to CPLD Pin 39
G4	FLASH_REV_SEL1	I	REV_SEL1	Revision Select 1 input connected to CPLD Pin 40
H3	JTAG_TCK	I	TCK	JTAG TCK
E6	JTAG_TDO	O	TDO	JTAG TDO connected to Header P5
E2	JTAG_TMS	I	TMS	JTAG TMS
A1	GND	I	GND1	Ground
A2	GND	I	GND2	Ground
B6	GND	I	GND3	Ground
F1	GND	I	GND4	Ground
F5	GND	I	GND5	Ground
F6	GND	I	GND6	Ground
H1	GND	I	GND7	Ground
B1	VCC1V8	I	VCCINT1	1.8V Power
E1	VCC1V8	I	VCCINT2	1.8V Power
G6	VCC1V8	I	VCCINT3	1.8V Power
H2	VCC1V8	I	VCCJ	1.8V Power
D6	VCC2V5	I	VCCO3	2.5V I/O Power
B2	VCC2V5	I	VCCO1	2.5V I/O Power
C6	VCC2V5	I	VCCO2	2.5V I/O Power
G5	VCC2V5	I	VCCO4	2.5V I/O Power
A4	Unused	I	DNC1	Do Not Connect
C3	Unused	I	DNC2	Do Not Connect
C4	Unused	I	DNC3	Do Not Connect
D2	Unused	O	$\overline{\text{CEO}}$	Do Not Connect
D3	Unused	I	DNC4	Do Not Connect
D4	Unused	I	DNC5	Do Not Connect
E3	Unused	I	DNC6	Do Not Connect
E4	Unused	I	DNC7	Do Not Connect
F2	Unused	I	DNC8	Do Not Connect
F3	Unused	I	DNC9	Do Not Connect
F4	Unused	I	DNC10	Do Not Connect
G2	Unused	I	DNC11	Do Not Connect

CPLD Programming Examples

Static Configuration

Figure 4-6 shows one possibility of connecting the FPGA to the Flash. This example allows the FPGA to be statically selected and programmed with up to four bitstreams located in the Flash. The selection of the bitstream is based on the configuration of the Flash Image Select header P3. Table 4-6 shows the jumper settings for header P3.



Notes:

1. FORCE, WIDE, PCIW_EN, and RTR are FPGA general-purpose I/Os.

Figure 4-6: **CPLD Configuration for Static Configuration**

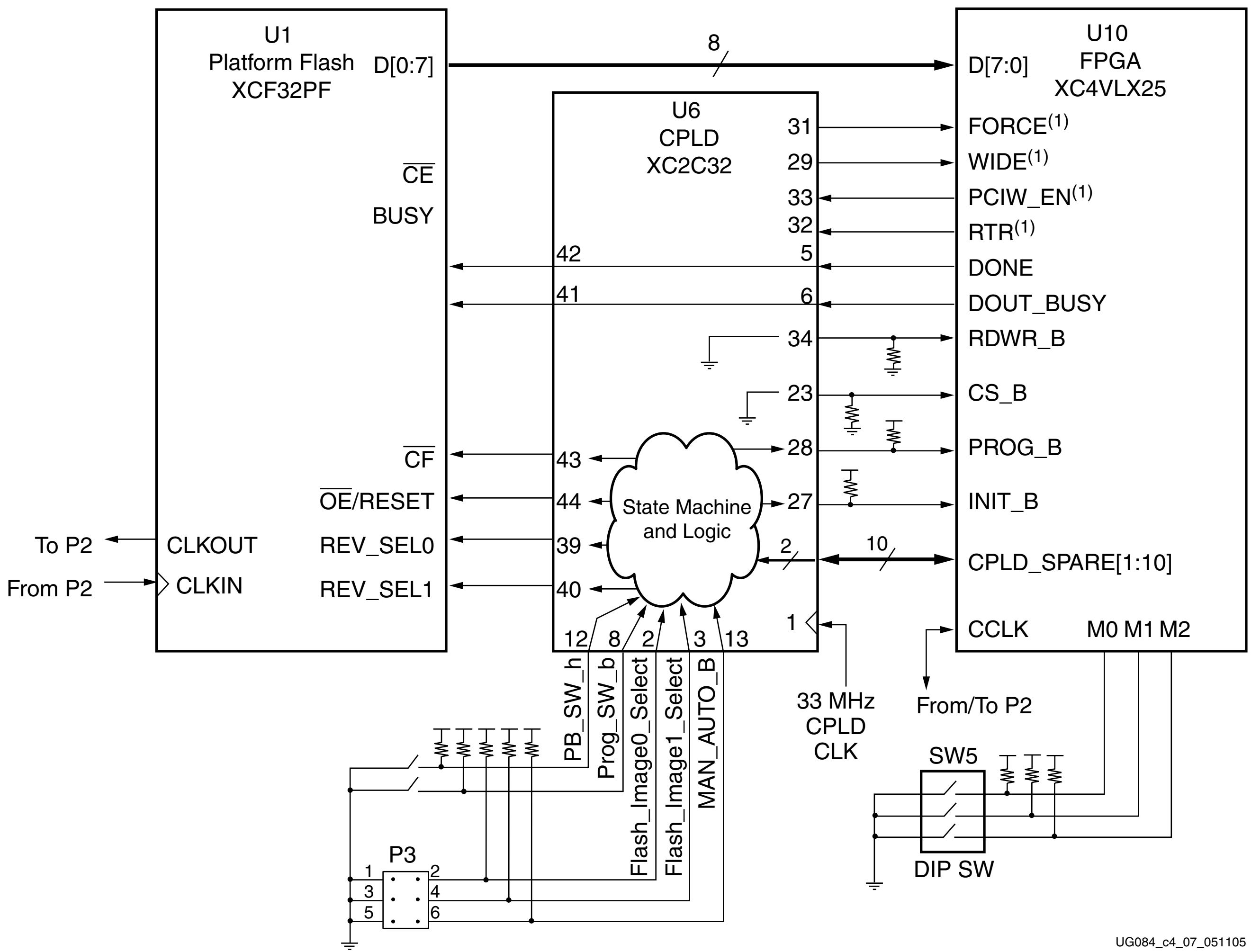
Table 4-6: **Bitstream Selection Setting for Header P3**

Bitstream Revision	Jumper Settings for P3
0	1-2 and 3-4
1	3-4
2	1-2
3	None

Generic Dynamic Reconfiguration

It is possible to dynamically reconfigure the entire FPGA after power-up. With this method, the CPLD loads a predetermined, default bitstream from the Platform Flash upon power-up. After initial configuration, the FPGA can signal to the CPLD that it wants to be reconfigured with a different bitstream, using the CPLD_SPARE[1:10] pins. The FPGA simply specifies the bitstream revision along with a signal to indicate when to start the configuration process. Logic within the CPLD then controls the configuration pins to the FPGA and Platform Flash to complete the configuration cycle. This logic can be as simple as driving the REV_SEL pins to the Flash and the PROG_B pin on the FPGA to begin configuration. The MAN_AUTO_B input to the CPLD can be incorporated into the design to override the dynamic reconfiguration and allow only static configuration as described in XAPP693: *A CPLD-Based Configuration and Revision Manager from Xilinx Platform Flash PROMs and FPGAs*. This application note provides details on using a CPLD and Platform Flash to dynamically reconfigure an FPGA. Figure 4-7 illustrates this method.

The *PCI-X LogiCORE Getting Started Guide* can be consulted for information on using the FORCE, WIDE, PCIW_EN, and RTR signals to support dynamic reconfiguration.



Notes:

1. FORCE, WIDE, PCIW_EN, and RTR are FPGA general-purpose I/Os.

Figure 4-7: **CPLD Configuration for Dynamic Reconfiguration**

SelectMAP Clock Selection

There are two clock modes for Slave SelectMAP and one clock mode for Master SelectMAP. These modes are selected using jumpers with Header P2. The default jumper setting upon shipment is Master SelectMAP.

Table 4-7 shows the Virtex-4 configuration modes along with the correct settings for the Mode Switch SW5.

Table 4-7: **SelectMAP Clock Modes**

Mode	Function	Header P2 Jumper Settings
Master SelectMAP (default)	FPGA CCLK drives Flash CLKIN	1-2
Slave SelectMAP	33 MHz oscillator drives FPGA CCLK and Flash CLKIN	1-2 3-4
Slave SelectMAP	33 MHz oscillator drives Flash CLKIN. Flash CLKOUT drives FPGA CCLK	1-3 5-6

Figure 4-8 shows the clock structure for SelectMAP mode along with Header (P2).

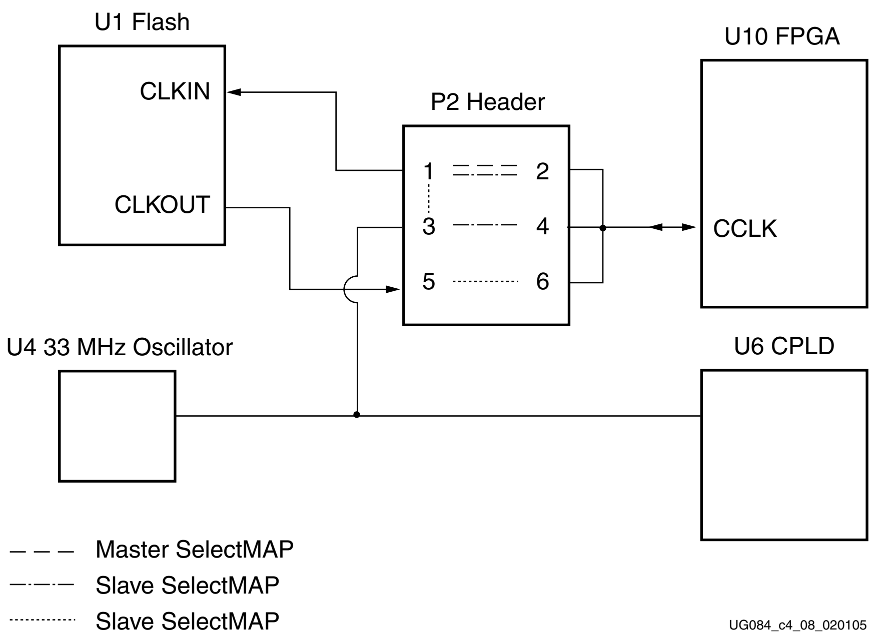


Figure 4-8: **SelectMAP Clock Circuitry**

Platform Flash Image Generation and Programming

This section provides general guidelines on how to create a PROM image file with four different revisions (bitstreams) using the Configuration File Wizard in the iMPACT FPGA programming tool. Online documentation from the Configuration File Wizard and iMPACT is available through the **Help -> Help Topics** menu selection in iMPACT. Chapter 16 of the Xilinx *Development System Reference Guide* provides details on how to create a PROM image file using PROMGen.

Setup

Follow these steps to prepare the PROM files:

1. Open iMPACT: **Start->Programs->Xilinx ISE 6->Accessories ->iMPACT.**
2. Under **Operation Mode Selection**, select **`Prepare Config…Files`**, then click **`Next`**.
3. Under **Prepare Configuration Files**, select **`PROM File`**, then click **`Next`**.
4. Under **Prepare PROM Files**, shown in Figure 4-9, select the following:
   - Select the **`Xilinx PROM with Design Revisioning Enabled`** radio button.
   - Under **PROM File Format**, select the **`MCS`** radio button.
   - In the PROM File Name box, enter a filename of your choice.
   - In the Location box, browse to or enter the directory where your bitstreams are located.
   - Click **`Next`**.

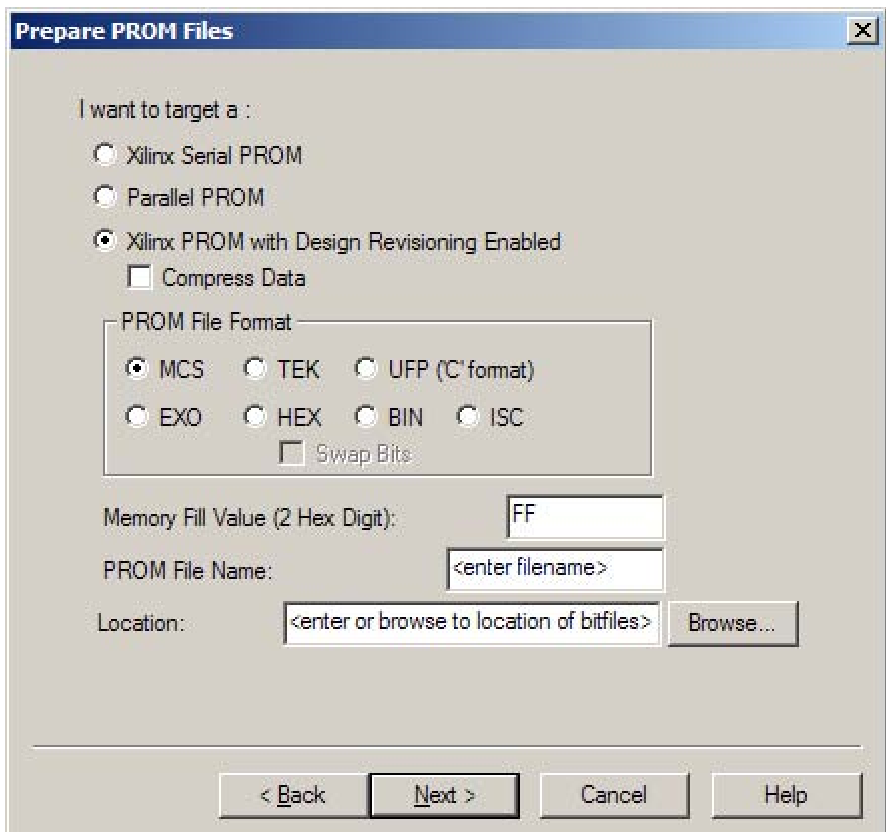


Figure 4-9: **Prepare PROM Files**

Specifying the Xilinx PROM Device

Follow these steps to specify the PROM device:

1. Under **Specify Xilinx PROM Device**, shown in Figure 4-10, select the following:
   - From the Select a PROM drop-down boxes, choose **`xcfp`** and **`xcf32p`**, then click **`Add`**.
   - From the Number of Revisions drop-down box, choose 4.
   - Click **Next**.

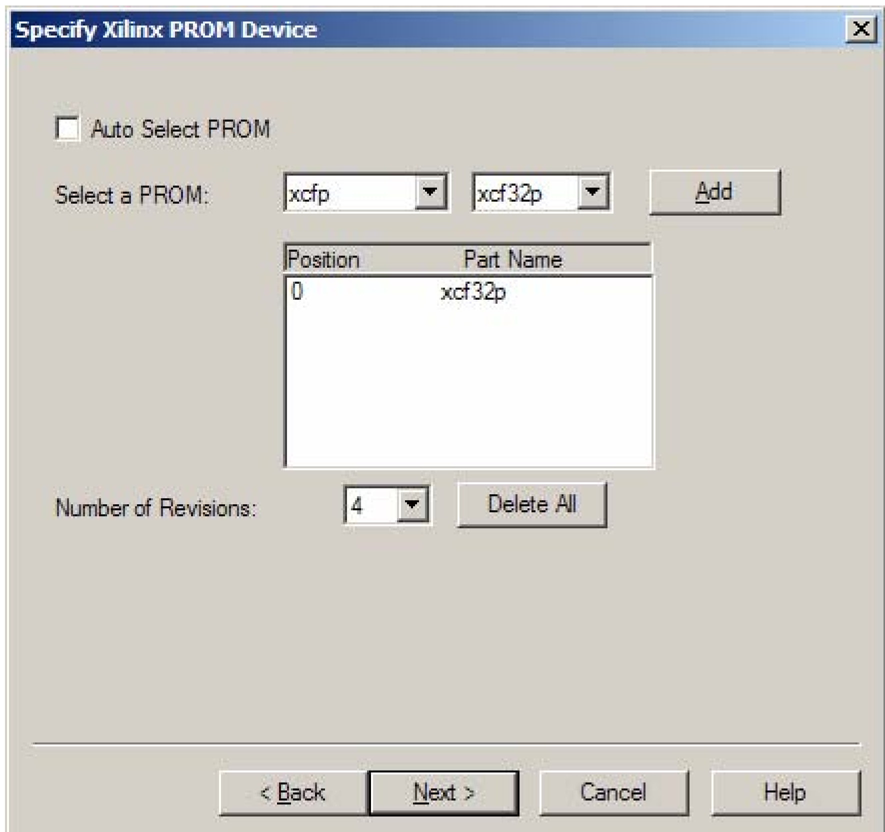


Figure 4-10: **Specify Xilinx PROM Device**

2. Under **File Generation Summary**, click **`Next`**
3. Under **Add Device File**, click **`Add File`**, browse for the bitfile you want for Configuration Address 0, and click **`Open`**.
4. Under **Add Device →Would you like to add…to Revision:0?**, click **`No`**.
5. Browse for the bitfile you want for Configuration Address 1, and click **`Open`**.
6. Under **Add Device →Would you like to add…to Revision:1?**, click **`No`**.
7. Browse for the bitfile you want for Configuration Address 2, and click **`Open`**.
8. Under **Add Device →Would you like to add…to Revision:2?**, click **`No`**.
9. Browse for the bitfile you want for Configuration Address 3 and click **`Open`**.
10. Under **Add Device →Would you like to add…to Revision:3?**, click **`No`**.
11. Under **Add Device →Click Finish to start generating file**, click **`Finish`**.

12. Under **PROM File Generation →Do you want to generate…now?**, click **`Yes`**.
13. Under **Xilinx iMPACT →Do you want to compress file?**, click **`No`**.
14. After a pause, **PROM File Generation Succeeded** is displayed.

A PROM image file is now created and is ready for programming into the ML455 board. A fully populated PROM file (.mcs) with all 4 revisions must always be generated even if all of the Configuration Address (0,1,2, or 3) in the Platform Flash are not programmed. The unused revisions can be populated with dummy bitstreams.

Programming the PROM

To program the PROM, follow these steps:

1. Select **Mode →Configuration Mode**.
2. Scan the JTAG chain by clicking the scan chain icon: 
3. The **Boundary Scan… Summary** indicates four devices are found. Click **`OK`**.
4. Under Assign New Configuration File, click **`Cancel All`**.
5. Double-click on the third device, **`xcf32p`**.
6. Under Assign New Configuration File, browse to your directory. Select the `.mcs` file by clicking it, then click **`Open`**.
7. Right-click the xcf32p icon and select **`Program`**.
8. Under the Advanced PROM Programming Options menu, shown in Figure 4-11, select the following:
   - In the Design Revision column, check the **`Rev`** boxes for the revisions to be programmed.
   - In the Erase column, check the ER boxes for those revisions to be programmed.
   - Select the **`Slave`** radio button under Operating Mode.
   - In the I/O Configuration drop-down box, select **`Parallel Mode`**.
   - This formats the PROM file for Master SelectMAP mode.
   - Click **`OK`** to program the Platform Flash with the PROM file via Boundary-Scan.

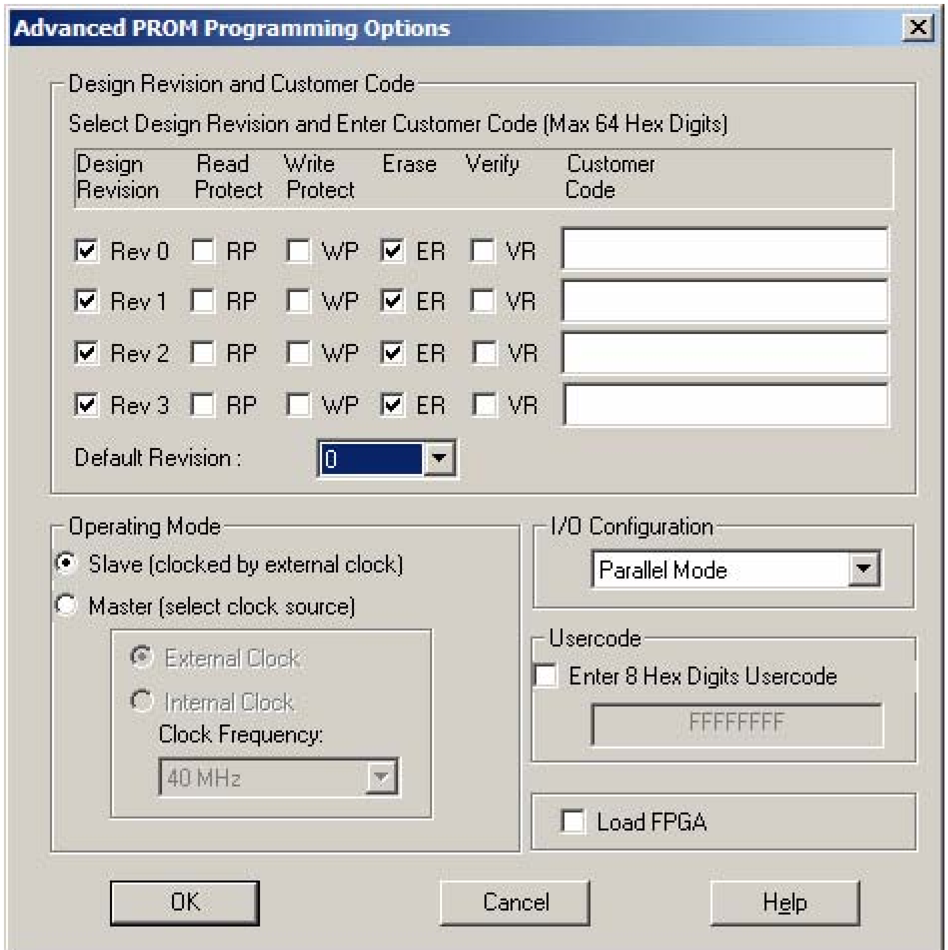


Figure 4-11: **Programming the PROM**

Appendix A

PCI Bus Clock Simulations

This appendix shows six simulations of the PCI clock waveforms on the Virtex-4 ML455 board. In the simulations, the split termination on the ML455 board is 100/100 ohms. The waveforms are measured at the U10 pin on the Virtex-4 FPGA on the ML455 board. The operation is at 133 MHz. The mother board is the Xilinx ML310, which has a 13-inch clock trace with series and parallel resistors. For this simulation, the series R was set to 0 ohms, and the parallel termination to GND was set to open.

Note: Designers should consult their mother board manuals and set the simulation parameters for the simulation source clock to account for the mother board's clock net characteristics.

The differences between the six simulations are based on the top and bottom jumpers:

- Figure A-1, Bottom Jumper in Place (R242 only)
- Figure A-2, Top Jumper in Place (R2 only)
- Figure A-3, Both Jumpers in Place (R2 and R242)
- Figure A-4, Top Jumper is a Transmission Line (Hard Routed through the Net)
- Figure A-5, Bottom Jumper is a Transmission Line (Hard Routed through the Net)
- Figure A-6, Top and Bottom Jumpers are Transmission Lines (Hard Routed through Nets)

In Figure A-1, the Magenta waveform (with the highest peaks) is the clock source on the mother board, and the Green waveform shows U10.D2 on the ML455 board.

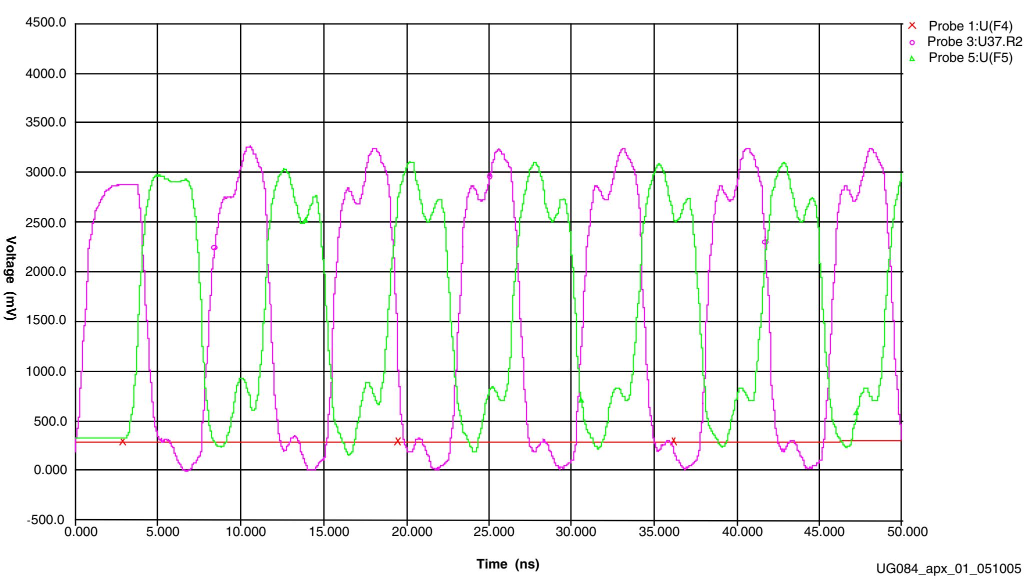


Figure A-1: **Bottom Jumper in Place (R242 only)**

In Figure A-2, the waveform shows destination pin U10.C13.

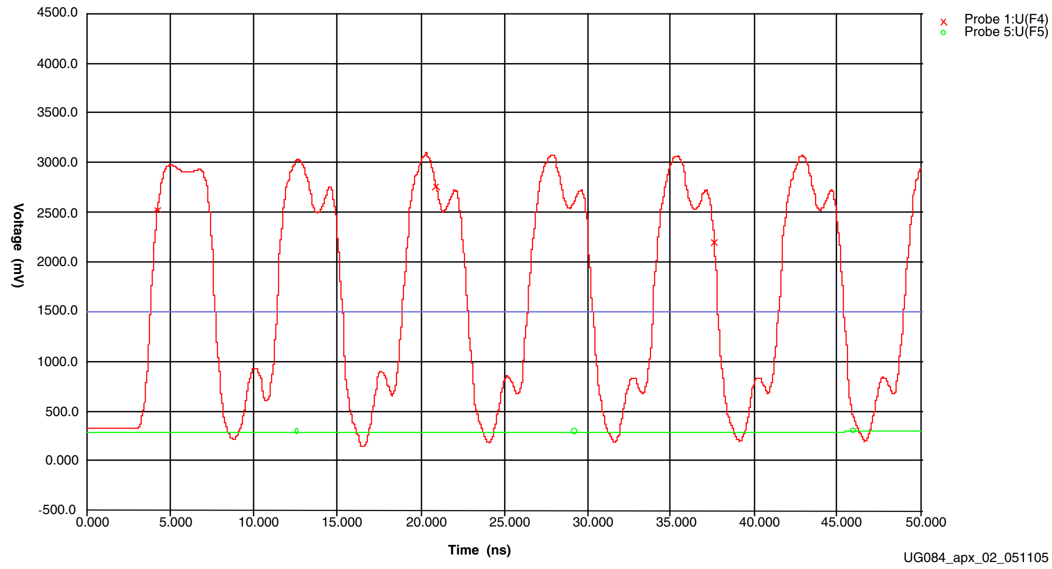


Figure A-2: **Top Jumper in Place (R2 only)**

In Figure A-3, the waveform shows either destination pin U10.C13 or U10.D2.

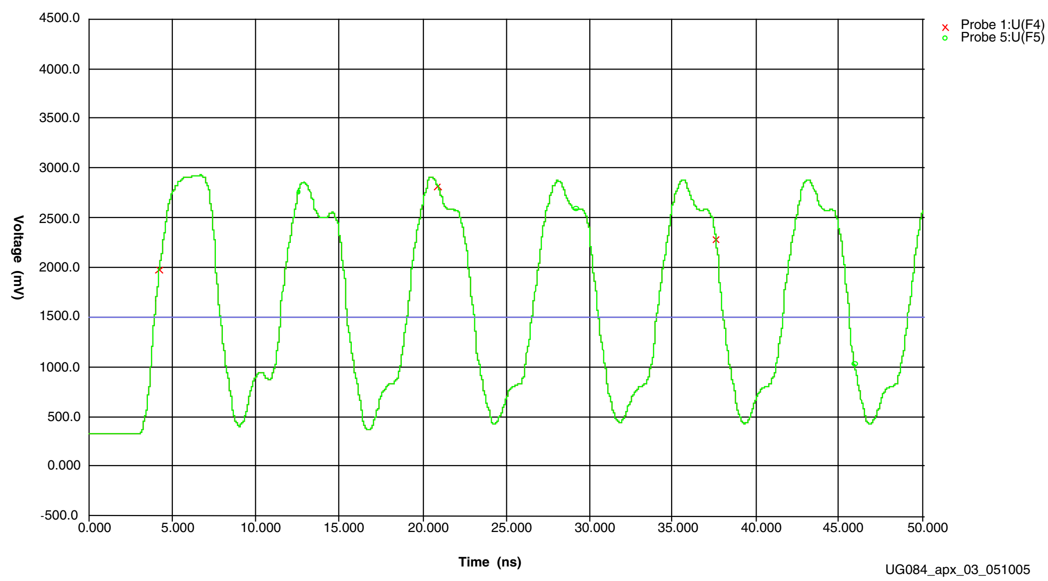


Figure A-3: **Both Jumpers in Place (R2 and R242)**

In Figure A-4, the waveform shows destination pin U10.C13.

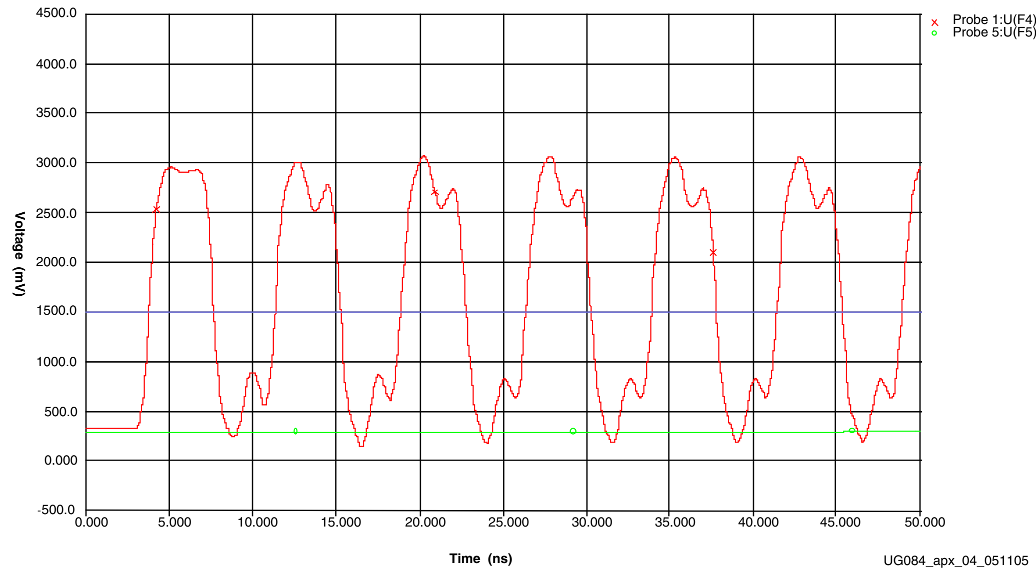


Figure A-4: **Top Jumper is a Transmission Line (Hard Routed through the Net)**

In Figure A-5, the waveform shows destination pin U10.D2.

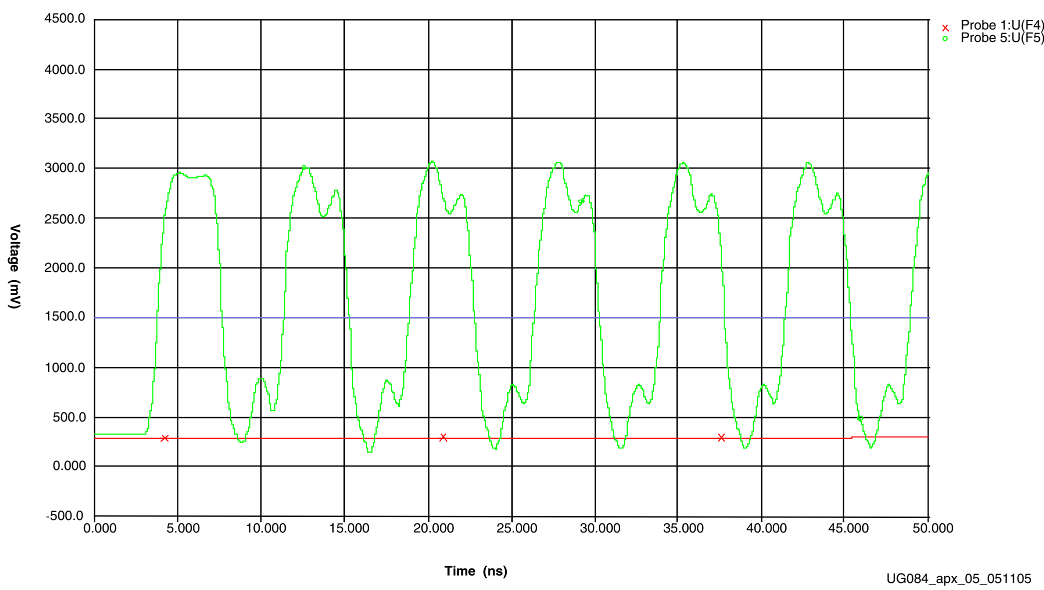


Figure A-5: **Bottom Jumper is a Transmission Line (Hard Routed through the Net)**

In Figure A-6, the waveform shows either destination pin U10.C13 or U10.D2.

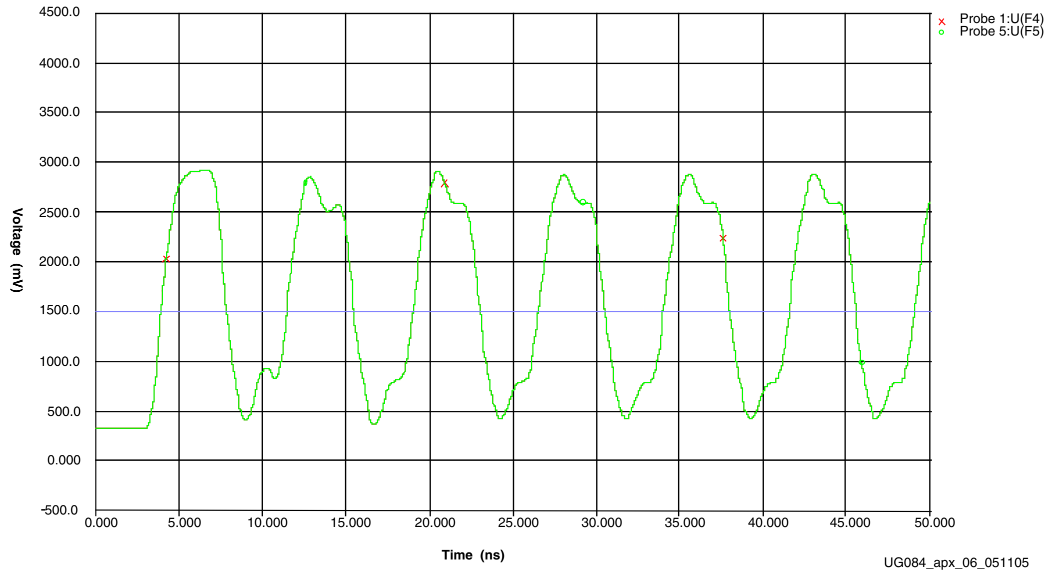


Figure A-6: **Top and Bottom Jumpers are Transmission Lines (Hard Routed through Nets)**