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SHEET 0 OF 12

SDRAM Daughter Card User Guide

For ML32x Development Platforms

UG127 (v1.0.1) P/N 0402278 October 12, 2004

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SDRAM Daughter Card User Guide
UG127 (v1.0.1) P/N 0402278 October 12, 2004

The following table shows the revision history for this document..

	Version	Revision
04/06/04	1.0	Initial Xilinx release.
10/12/04	1.0.1	Template update.

Table of Contents

About This Guide

This guide documents the SDRAM daughter card for use with Xilinx ML32x Development Platforms.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

SDRAM Daughter Card

Overview

The SDRAM daughter card provides 64 MB of memory to Xilinx ML32x Development Platforms by using two Infineon 256 Mb (16Mb x 16) Mobile-RAM modules, HYB25L256160AC-7.5. The SDRAM daughter card is fully tested and operates at up to 100 MHz. Figure 1 shows the SDRAM daughter card connected to a Xilinx ML320 board. It can only be connected to the BERT headers, J53 and J54, of the ML32x boards.

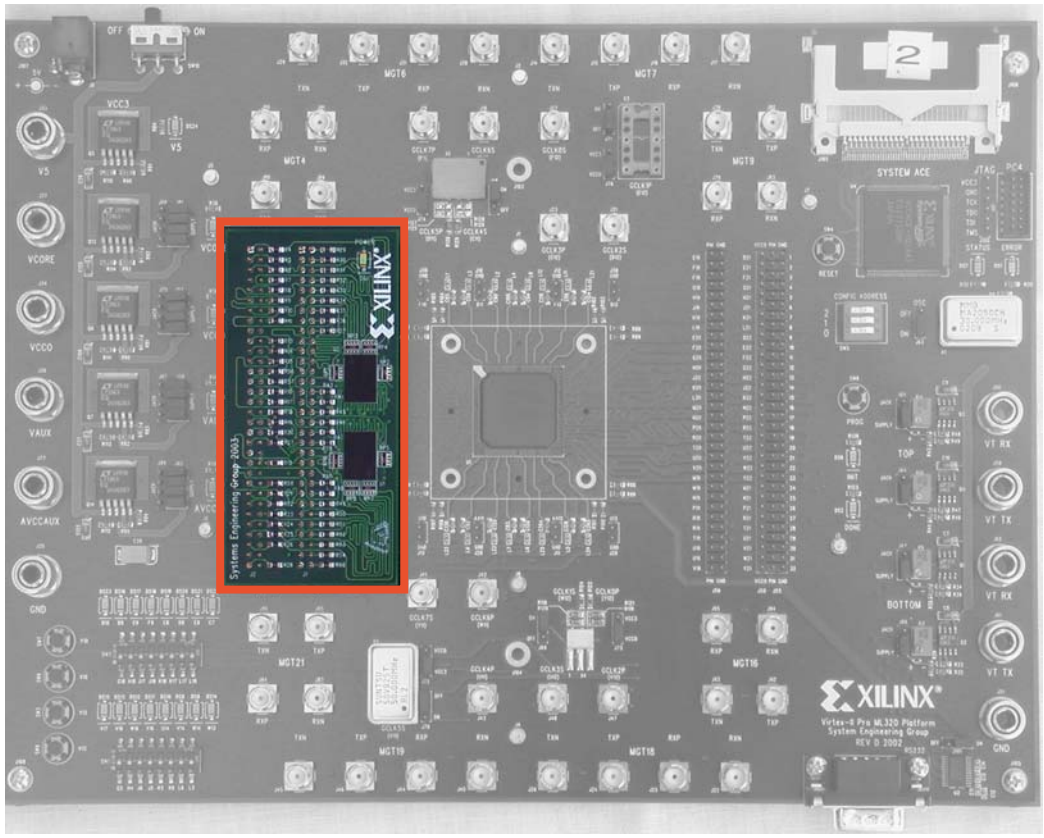

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Figure 1: **SDRAM Daughter Card Connected to an ML320 Board**

SDRAM Connections

Table 1, Table 2, page 11, and Table 3, page 12 list the header definitions of the SDRAM signals and the connections between the SDRAM daughter card and the ML320, ML321, and ML323 Development Platforms.

Table 1: **Headers for the SDRAM Signals**

J1 Header	SDRAM Signal
1	DQ3
2	DQ6
3	DQ4
4	DQ2
5	DQ15
6	DQ14
7	DQ10
8	DQ8
9	UDQM1/SDQM1
10	A12
11	A8
12	A5
13	A4
14	CKE
15	$\overline{CAS}$
16	A0
17	A1
18	BA1
19	$\overline{RAS}$
20	LDQM1/SDQM0
21	
22	
23	
24	LDQM2/SDQM2
25	DQ23
26	DQ21
27	DQ17
28	DQ16
29	DQ29
30	DQ27
31	DQ25
32	DQ28

J2 Header	SDRAM Signal
1	DQ5
2	DQ7
3	DQ1
4	DQ0
5	DQ13
6	DQ11
7	DQ12
8	DQ9
9	
10	A11
11	A7
12	A6
13	A9
14	BA0
15	A3
16	A2
17	A10
18	$\overline{CS}$
19	$\overline{WE}$
20	DQ24
21	
22	CLK
23	
24	UDQM2/SDQM3
25	DQ22
26	DQ19
27	DQ20
28	DQ18
29	DQ31
30	DQ30
31	
32	DQ26

Table 2: **Connection between SDRAM J2 Header and ML32x J53 BERT Header**

J53 BERT Header	SDRAM Signal	ML320	ML321	ML323
1	DQ5	D2	A2	N2
2	DQ7	E2	C2	P2
3	DQ1	F2	D2	R2
4	DQ0	G2	E2	T2
5	DQ13	H2	H2	U2
6	DQ11	J2	B1	V2
7	DQ12	K2	C1	E1
8	DQ9	L2	D1	F4
9		D1	E1	L5
10	A11	E1	F1	H1
11	A7	F1	G1	K1
12	A6	G1	H1	L1
13	A9	H1	J1	M1
14	BA0	J1	K1	N1
15	A3	K1	L1	P1
16	A2	N1	M1	R1
17	A10	P1	R1	Y1
18	$\overline{CS}$	R1	T1	AA1
19	$\overline{WE}$	T1	U1	AB1
20	DQ24	U1	V1	AC1
21		V1	W1	AD1
22	CLK	W1	Y1	AE1
23		Y1	AA1	AG1
24	UDQM2/SDQM3	M2	AC1	AE4
25	DQ22	N2	AD1	AH5
26	DQ19	P2	AE1	AK3
27	DQ20	R2	T2	AL1
28	DQ18	T2	V2	W22
29	DQ31	U2	W2	Y22
30	DQ30	V2	AC2	AA2
31		W2	AD2	AB2
32	DQ26	Y2	AF2	AC2

Table 3: **Connection between SDRAM J1 Header and ML32x J54 BERT Header**

J54 BERT Header	SDRAM Signals	ML320	ML321	ML323
1	DQ3	E4	E4	K5
2	DQ6	F4	G4	L3
3	DQ4	F5	H4	M3
4	DQ2	G4	J4	N3
5	DQ15	H5	E3	P3
6	DQ14	J4	G3	R3
7	DQ10	K4	H3	T3
8	DQ8	L4	J3	U3
9	UDQM1/SDQM1	E3	K3	E2
10	A12	F3	L3	F5
11	A8	G3	M3	L6
12	A5	H3	N3	H2
13	A4	J3	J2	J2
14	CKE	K3	L2	K2
15	$\overline{CAS}$	L3	M2	L2
16	A0	M3	N2	M2
17	A1	N3	P2	AE2
18	BA1	P3	R2	AF2
19	$\overline{RAS}$	R3	P3	AG2
20	LDQM1/SDQM0	T3	R3	AE5
21		U3	T3	AH6
22		V3	U3	AK4
23		M4	V3	AL2
24	LDQM2/SDQM2	M5	W3	V3
25	DQ23	N4	Y3	W3
26	DQ21	P4	AB3	Y3
27	DQ17	R5	AC3	AA3
28	DQ16	R4	V4	AB3
29	DQ29	T4	W4	AC3
30	DQ27	T5	Y4	AD3
31	DQ25	U4	AB4	AF3
32	DQ28	V4	AD4	AF4