FMC XM107 Loopback Card User Guide

UG539 (v1.0) March 30, 2010

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/30/10	1.0	Initial Xilinx release.

Table of Contents

About This Guide

This document describes the FPGA Mezzanine Card (FMC) XM107 loopback card, referred to as the *XM107* in this guide. Xilinx® supported evaluation (carrier) boards are referred to simply as *boards* in this guide.

Guide Contents

This manual contains the following chapter:

- Chapter 1, "XM107."

Additional Documentation

Prior to using the XM107, users should be familiar with Xilinx resources. See the following locations for additional documentation on Xilinx tools and solutions:

- ISE® Design Suite: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Intellectual Property: www.xilinx.com/ipcenter

Information about the latest *VITA 57 FMC Specification* is located at:

- www.vita.com/fmc.html

The XM107 can be used with Xilinx FMC high pin count (HPC) boards and, with limited functionality, FMC low pin count (LPC) boards. Board documentation, schematics and PCB design files are available at www.xilinx.com/fmc.

Additional Support Resources

To find additional documentation, see the Xilinx website at:

www.xilinx.com/support/documentation/index.htm

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

www.xilinx.com/support/mysupport.htm

Chapter 1

XM107

Overview

This document describes the FPGA Mezzanine Card (FMC) XM107 loopback card, referred to as the *XM107* in this guide. A "Quick Start" section and "XM107 Board Technical Description" are combined within this document.

Quick Start

System Requirements

Hardware

Table 1-1 details the board that is validated to support the XM107. The ML605 board provides one FMC high pin count (HPC) (J64) and one FMC low pin count (LPC) (J63) connector interface. The XM107 connector must be installed on the HPC J64 connector of the ML605 board to have full functionality, as shown in Figure 1-1, page 9.

Table 1-1: **FMC Supported Boards**

Xilinx Platform	Part Number	FMC HPC Connector	FMC LPC Connector
Virtex-6 FPGA ML605 Evaluation Kit	EK-V6-ML605-G	J64	J63

Notes:

While every effort has been made to comply with the *FPGA Mezzanine Card Specification*, Xilinx cannot claim nor assume full compliance with the FMC/VITA-57-1 specification. Consequently, Xilinx cannot claim nor support the usage of the XM107 on any other FMC (VITA-57.1) board.

The XM107 can work on LPC FMC interfaces, but with limited functionality. Xilinx boards containing LPC connectors are supported as follows:

- ML605 J63 - LA[00:33], CLK[0:1]_M2C_P/N, GBTCLK0_M2C_P/N
- SP605 J2 - LA[00:33], CLK[0:1]_M2C_P/N, GBTCLK0_M2C_P/N
- SP601 J1 - LA[00:33], CLK[0:1]_M2C_P/N, GBTCLK0_M2C_P/N

Software

Example designs that use this hardware are not provided.

Package Contents

The following items are included in the XM107 shipment:

- XM107 card
- Four (4) mounting screws
- Two (2) standoffs
- Welcome letter

Necessary Equipment

- Small Phillips screwdriver to secure the XM107 to the board
- PC with Internet access to download documentation, board files, and schematics

System Setup

Complete the following steps to install the XM107 to a Xilinx board. For additional information on Xilinx boards, refer to the particular board's user guide. See "Additional Documentation," page 5.

1. Turn off the ML605 board DC power switch and disconnect its input power source.
2. Remove the XM107 from the electrostatic device (ESD) bag.
3. Using a small Phillips screwdriver, remove the two screws from the bottom side of the two standoffs on the XM107.
4. Install the XM107 to the ML605 FMC HPC connector J64. The XM107 hangs off the edge of the ML605 board as shown in Figure 1-1, page 9.
5. Turn the ML605 and attached XM107 board over such that the ML605 FPGA is facing the table. Install two screws from the bottom side of ML605 board FMC HPC mounting holes into the two standoffs attached to the XM107. Hand tighten the two mounting screws to the bottom of the board.
6. Turn the ML605 and attached XM107 boards over such that the Xilinx FPGA is visible.
7. Connect the input power source to the ML605 board. Turn the ML605 board power input switch to ON.

The system is now ready for use.

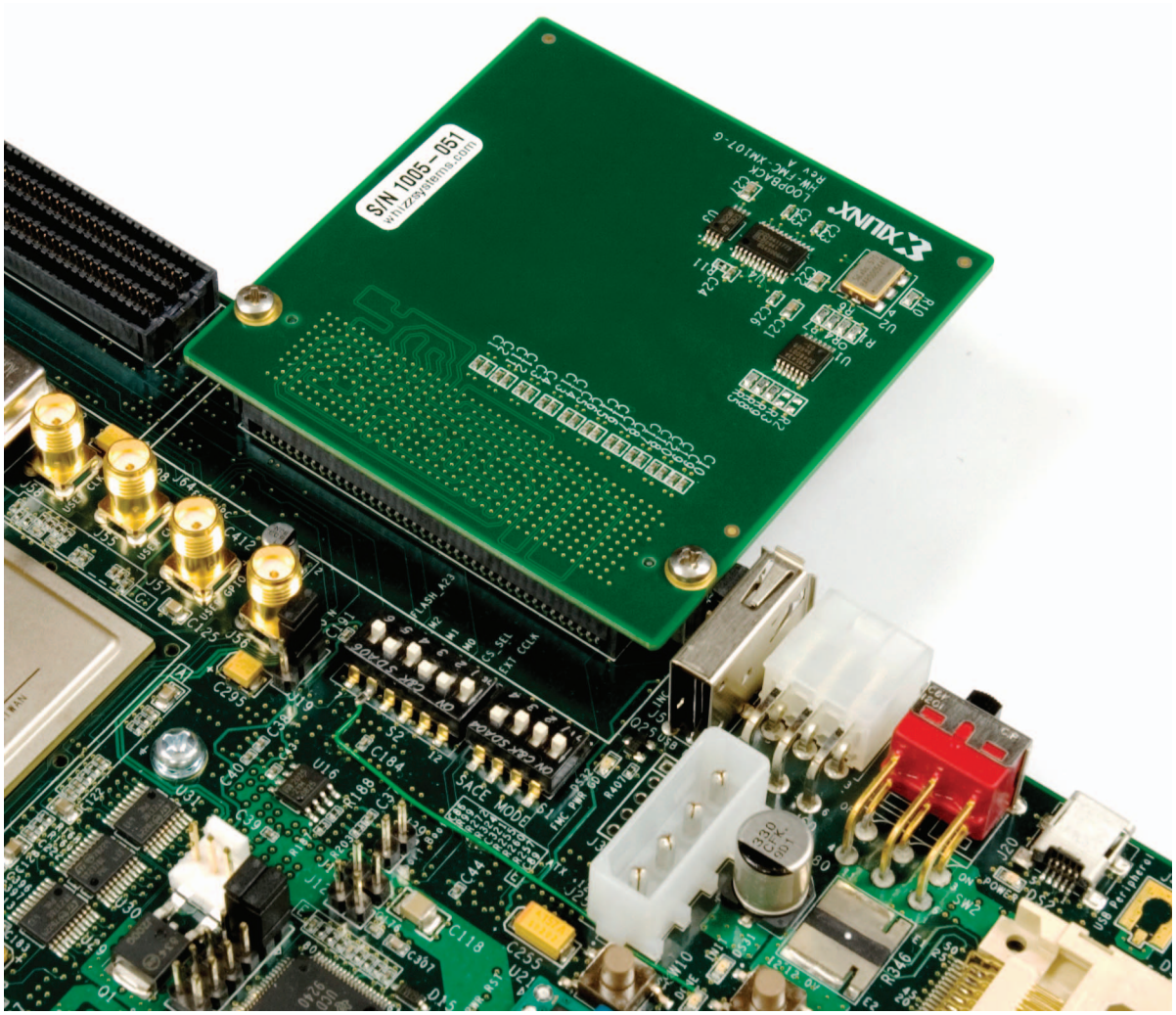

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Figure 1-1: **Installation of XM107 to ML605 Board FMC HPC Connector**

Technical Support

Xilinx offers technical support for this product *only* when used in conjunction with boards listed in Table 1-1. For assistance with the XM107 and other Xilinx boards, contact Xilinx for technical support at www.xilinx.com/support.

XM107 Board Technical Description

Figure 1-2 shows a block diagram of the XM107.

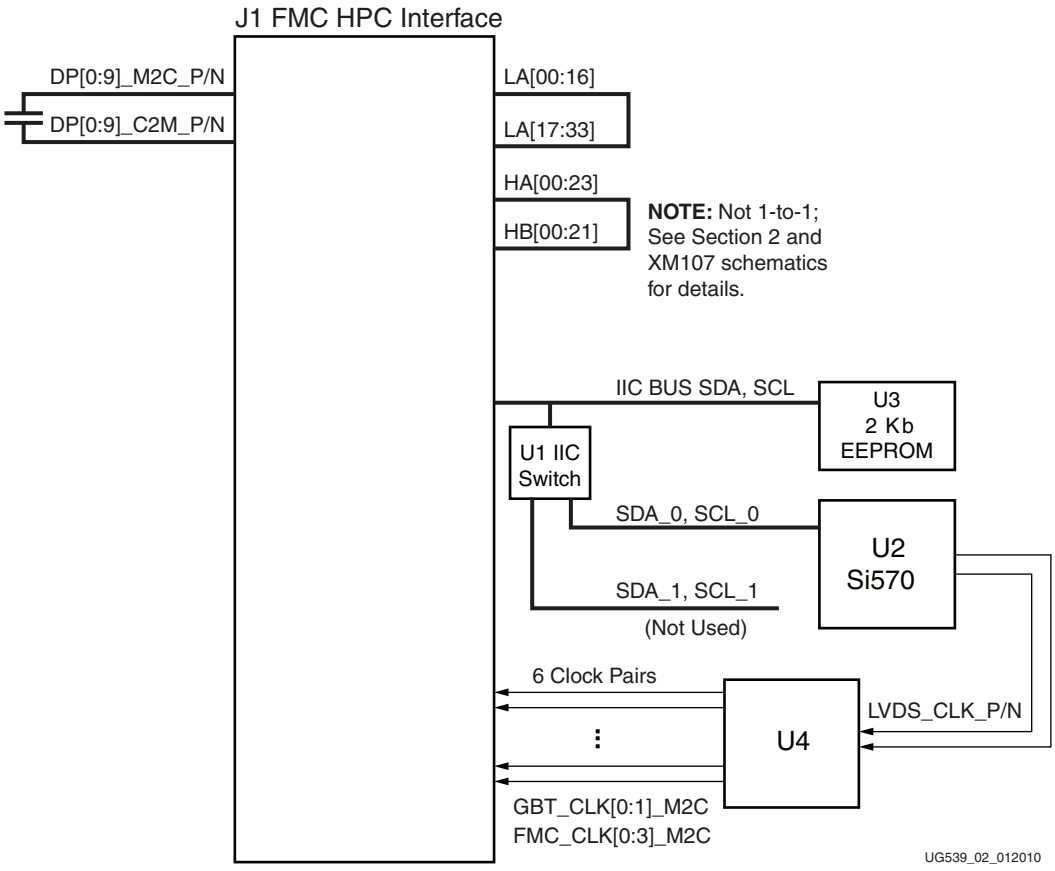

Figure 1-2: **XM107 Block Diagram**

The XM107 provides hard-wired loopback of a subset of the FMC HPC signal set, as discussed in "2. FMC HPC Connector Onboard Loopback."

The FMC HPC signals are looped as length-matched, differential pair signals.

The XM107 also provides a Silicon Laboratories Si570 IIC bus-programmable 10–810MHz clock source (U2) which drives an IDT ICS854S006A 1-to-6 clock buffer (U4). U4 then sources six clock pairs back to the FMC HPC J1 connector.

The FMC HPC connector IIC bus hosts two IIC devices, a 2-Kb M24C02 IIC EEPROM (U3) and an NXP PCA9543 IIC bus switch (U1). The M24C02 is directly connected to the IIC bus.

The Si570 U2 IIC bus programmable clock source is accessible via the PCA9543 IIC bus switch port 0. Details of this connectivity are discussed in "3. PCA9543 IIC Bus Switch U1" and "4. Silicon Labs Si570 Clock Source U2."

Detailed Description

The numbered features in Figure 1-3 correlate to the features and notes listed in Table 1-2, page 11. For full functionality, the XM107 must be installed on a board FMC connector supporting high pin count interfaces.

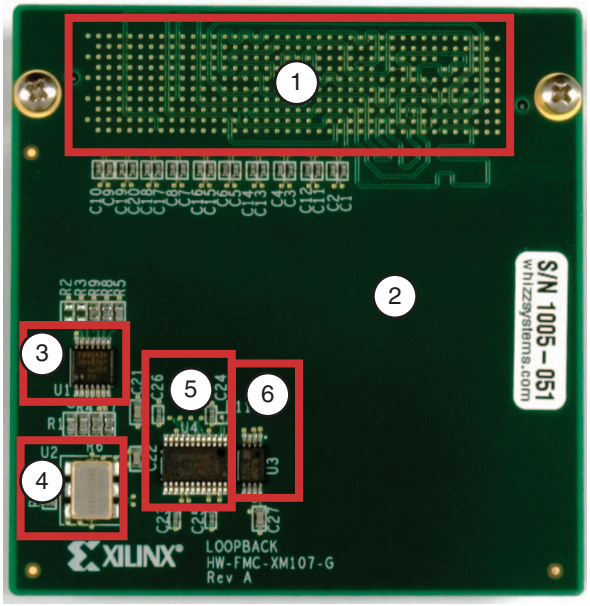

Figure 1-3: **XM107 Features**

Table 1-2: **XM107 Features**

Number	Feature	Notes	Schematic Page
1	VITA 57.1 FMC HPC Connector J1	J1: 80 signal pairs comprised of LA[00:33], HA[00:23] and HB[00:21]. 6 clock pairs and the IIC bus SDA,SCL. The connector is mounted on the bottom side of the card.	3 – 6
2	FMC HPC Connector J1 Onboard Loopback	J1: Connector pins LA[00:33], HA[00:23], HB[00:21] are looped with length matched signal traces. See detailed description in "2. FMC HPC Connector Onboard Loopback" for details.	3 – 5
3	PCA9543 IIC Bus Switch (U1)	U1: IIC bus switch is connected to the main FMC HPC IIC bus SDA and SCL signals. This component can switch its input IIC bus to one of two backside IIC bus connectons. Si570 clock chip U2 resides on backside IIC bus 0, bus 1 is not used.	7
4	Silicon Labs Si570 Programmable XO/VCXO (U2)	U2: Silicon Labs Si570 IIC serial bus programmable clock source device with frequency range 10MHz - 810MHz. U2 LVDS ouput drives 1-to-6 clock buffer U4.	7
5	ICS854S006A 1-to-6 Clock Buffer (U4)	U4: The ICS854S006A 1-to-6 clock buffer drives 6 clock pairs to the J1 FMC HPC connector: GBTCLK[1:0]_M2C_P/N and CLK[3:0]_M2C_P/N.	7
6	M24C02 2Kb IIC EEPROM (U3)	U3: IIC compatible electrically erasable programmable memory (EEPROM) with 2 Kb (256 bytes) of non-volatile storage.	7

1. VITA 57.1 FMC HPC Connector J1

This connector interfaces to the board containing the Xilinx FPGA and mating FMC connector. The XM107 uses Samtec FMC HPC connector part number ASP-134488-01.

See Xilinx board user guides and schematics for a description of features provided by HPC interfaces contained on the board, including power supply specifications, FPGA banking connectivity, and FPGA pin assignments.

- For ML605 LPC and HPC interfaces, see UG534 *ML605 Hardware User Guide*

See the *VITA57.1 Specification* at www.vita.com/fmc.html for additional information on FMC.

2. FMC HPC Connector Onboard Loopback

The XM107 board implements length-matched signal pair traces that are looped on the FMC HPC connector pins. The following trace sets are provided:

- Ten sets of differential pair nets DP[0:9]_M2C_P/N are looped one-to-one to DP[0:9]_C2M_P/N. These loops are *not* direct-connect, but are capacitively coupled with a 0.1uF cap in each net.
- Thirty-four sets of differential pair nets LA[00:16]_P/N are looped one-to-one to LA[17:33]_P/N (Table 1-3). These loops are direct-connect.
- Twenty-two sets of differential pair nets HA[00:21]_P/N are looped to HB[00:21]_P/N. These loops are direct-connect but are *not* one-to-one. See Table 1-4, page 13 for the HA-to-HB connectivity.
- One differential pair HA[22]_P/N is looped to HA[23]_P/N. This loop is direct-connect.

Table 1-3: **J1 FMC HPC LA Loopback Connections**

FMC Pin Name	FMC Pin Number	<=Loops to =>	FMC Pin Number	FMC Pin Name
LA00_CC_P	G6		D20	LA17_CC_P
LA00_CC_N	G7		D21	LA17_CC_N
LA01_CC_P	D8		C22	LA18_CC_P
LA01_CC_N	D9		C23	LA18_CC_N
LA02_P	H7		H22	LA19_P
LA02_N	H8		H23	LA19_N
LA03_P	G9		G21	LA20_P
LA03_N	G10		G22	LA20_N
LA04_P	H10		H25	LA21_P
LA04_N	H11		H26	LA21_N
LA05_P	D11		G24	LA22_P
LA05_N	D12		G25	LA22_N
LA06_P	C10		D23	LA23_P
LA06_N	C11		D24	LA23_N
LA07_P	H13		H28	LA24_P

Table 1-3: **J1 FMC HPC LA Loopback Connections *(Cont'd)***

FMC Pin Name	FMC Pin Number	<=Loops to =>	FMC Pin Number	FMC Pin Name
LA07_N	H14		H29	LA24_N
LA08_P	G12		G27	LA25_P
LA08_N	G13		G28	LA25_N
LA09_P	D14		D26	LA26_P
LA09_N	D15		D27	LA26_N
LA10_P	C14		C26	LA27_P
LA10_N	C15		C27	LA27_N
LA11_P	H16		H31	LA28_P
LA11_N	H17		H32	LA28_N
LA12_P	G15		G30	LA29_P
LA12_N	G16		G31	LA29_N
LA13_P	D17		H34	LA30_P
LA13_N	D18		H35	LA30_N
LA14_P	C18		G33	LA31_P
LA14_N	C19		G34	LA31_N
LA15_P	H19		H37	LA32_P
LA15_N	H20		H38	LA32_N
LA16_P	G18		G36	LA33_P
LA16_N	G19		G37	LA33_N

Table 1-4: **J1 FMC HPC HA-to-HB Loopback Connections**

FMC Pin Name	FMC Pin Number	<=Loops to =>	FMC Pin Number	FMC Pin Name
HA00_CC_P	F4		K25	HB00_CC_P
HA00_CC_N	F5		K26	HB00_CC_N
HA01_CC_P	E2		K28	HB06_CC_P
HA01_CC_N	E3		K29	HB06_CC_N
HA02_P	K7		J24	HB01_P
HA02_N	K8		J25	HB01_N
HA03_P	J6		F22	HB02_P
HA03_N	J7		F23	HB02_N
HA04_P	F7		E21	HB03_P
HA04_N	F8		E22	HB03_N
HA05_P	E6		F25	HB04_P
HA05_N	E7		F26	HB04_N
HA06_P	K10		E24	HB05_P

Table 1-4: **J1 FMC HPC HA-to-HB Loopback Connections *(Cont'd)***

FMC Pin Name	FMC Pin Number	<=Loops to =>	FMC Pin Number	FMC Pin Name
HA06_N	K11		E25	HB05_N
HA07_P	J9		J27	HB07_P
HA07_N	J10		J28	HB07_N
HA08_P	F10		F28	HB08_P
HA08_N	F11		F29	HB08_N
HA09_P	E9		E27	HB09_P
HA09_N	E10		E28	HB09_N
HA10_P	K13		K31	HB10_P
HA10_N	K14		K32	HB10_N
HA11_P	J12		J30	HB11_P
HA11_N	J13		J31	HB11_N
HA12_P	F13		F31	HB12_P
HA12_N	F14		F32	HB12_N
HA13_P	E12		E30	HB13_P
HA13_N	E13		E31	HB13_N
HA14_P	J15		K34	HB14_P
HA14_N	J16		K35	HB14_N
HA15_P	F16		J33	HB15_P
HA15_N	F17		J34	HB15_N
HA16_P	E15		F34	HB16_P
HA16_N	E16		F35	HB16_N
HA17_CC_P	K16		K37	HB17_CC_P
HA17_CC_N	K17		K38	HB17_CC_N
HA18_P	J18		J36	HB18_P
HA18_N	J19		J37	HB18_N
HA19_P	F19		E33	HB19_P
HA19_N	F20		E34	HB19_N
HA20_P	E18		F37(1)	HB20_P
HA20_N	E19		F38(1)	HB20_N
HA21_P	K19		E36(1)	HB21_P
HA21_N	K20		E37(1)	HB21_N
HA22_P	J21		K22	HA23_P
HA22_N	J22		K23	HA23_N

Notes:

1. The ML605 board FMC HPC connector J64 does not support these signals.

3. PCA9543 IIC Bus Switch U1

The XM107 IIC bus hosts two components, U3 M24C02 2 Kb EEPROM and U1 IIC bus switch (Figure 1-4).

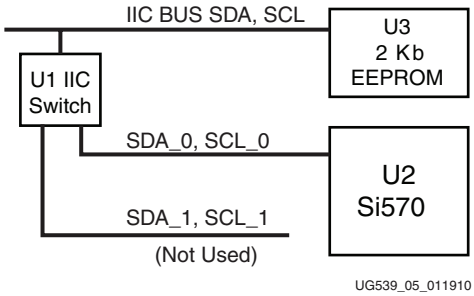

Figure 1-4: **XM107 IIC Bus Topology**

Table 1-5 shows the addresses for the IIC components.

Table 1-5: **IIC Address Table**

Component	Address
M24C02 (U3)	1010_0_GA0_GA1_RW
PCA9543 (U1)	1110_0_GA0_GA1_RW
SI570 (U2)	1011_1_0_1_RW

The IIC bus switch provides bidirectional bus isolation and isolates the fixed addresses of the Si570 device from the main IIC bus of the board. The upstream side of the switch connects to the FMC HPC connector. Downstream switch port 0 interfaces to the Silicon Laboratories Si570 clock integrated circuit U2. The downstream switch port 1 is not used.

The PCA9543 is a bidirectional translating switch, controlled by the upstream board side IIC bus. The PCA9543 must be initialized prior to attempting to communicate with the Si570 clock circuit on the downstream IIC bus 0.

The PCA9543 component data sheet contains detailed application information and is available online at www.nxp.com.

The IIC address of this component is controlled by a combination of the board interface and chip-enable connections to the component inputs on the XM107. Signals GA0 and GA1 from the board are connected to the two address inputs A1 and A0 of the PCA9543 component.

Xilinx boards provide GA0 and GA1 signal strapping to 3.3V and GND signals creating different A0 and A1 address decodes on the PCA9543.

The IIC memory addressing protocol requires a bus master to initiate communication to a peripheral device using a start condition followed by a device select code. The device select code consists of a 4-bit Device Type Identifier and a 3-bit Address (A2, A1 and A0). A2 is internally grounded inside the PCA9543. Bit 0 is used to indicate read/write. The Device Type Identifier for the PCA9543 is 1110 binary. Table 1-6, page 16 defines the generic PCA9543 Device Select Code as well as specific Device Code Select address when the XM107 is connected to a Xilinx board as defined in Table 1-1, page 7.

Table 1-6: **PCA9543 IIC Switch Device Select Code**

Bit 7:4 Device Type Identifier	Bit 3	Bit 2	Bit 1	Bit 0 LSB	Description
1110	0	GA0	GA1	Read/$\overline{\text{Write}}$	Connected to mezzanine FMC HPC interface

The PCA9543 has a Control register which must be initialized by the IIC bus master to enable the channel 0 downstream IIC port. Channel 0 must be enabled prior to attempting to communicate with the downstream programmable clock device on the XM107.

After the IIC bus master enables PCA9543 channel 0 downstream IIC bus, the bus master can communicate directly with the Si570 component without further interaction with the Control register. The Control register can be read by the IIC bus master. Table 1-7 defines the PCA9543 Control register.

Table 1-7: **PCA9543 Control Register**

Bit 7:4	Bit 3:2	Bit 1	Bit 0
XXXX	XX	Channel 1 Enable	Channel 0 Enable(1)

Notes:

1. Channel 0 must be set to a logic 1 state by IIC bus master prior to attempting to communicate with the Si570 U2.

The downstream IIC device connected to the PCA9543 is at IIC address 0x5D:

- Si570 U2 IIC address is at 0x5D, PCA9543 control register bits CR[1:0] = 01

The U1 PCA9543 IIC bus switch to J1 FMC HPC connections are shown in Table 1-8.

Table 1-8: **IIC Bus Switch to J1 FMC HPC Connections**

U1 PCA9543 IIC Bus Switch		J1 FMC Connector
Net Name	**Pin Number**	**Pin Number**
SDA	U1.13	C31
SCL	U1.12	C30

4. Silicon Labs Si570 Clock Source U2

The Silicon Labs Si570 serial IIC bus programmable clock source provides a low-jitter clock with a user-programmable output frequency from 10 to 810 MHz.

U2 Si570 is located at IIC address 0x5D and is accessed through the U1 PCA9543 IIC bus switch as described in "3. PCA9543 IIC Bus Switch U1."

The U2 Si570 component is factory programmed with parameters in Table 1-9.

Table 1-9: **Characteristics of Si570 Component**

Si570 Characteristic	XM107
Output Format	LVDS
Output Enable Polarity	High
Temperature Stability	50 ppm
Frequency Range	10–810 MHz
Six-Digit Startup Frequency	156.250 MHz
Power Supply	3.3V
IIC Address	x5D

For additional information on this component, including reprogramming the clock frequency through the IIC serial bus interface, consult the manufacturer's data sheet at: www.silabs.com.

The U2 Si570 output clock drives the input of the U4 ICS84S008A 1-to-6 clock buffer described in "5. ICS854S006A Clock Buffer Connections U4."

5. ICS854S006A Clock Buffer Connections U4

The U2 Si570 output clock drives the input of the U4 ICS854S006A 1-to-6 clock buffer.

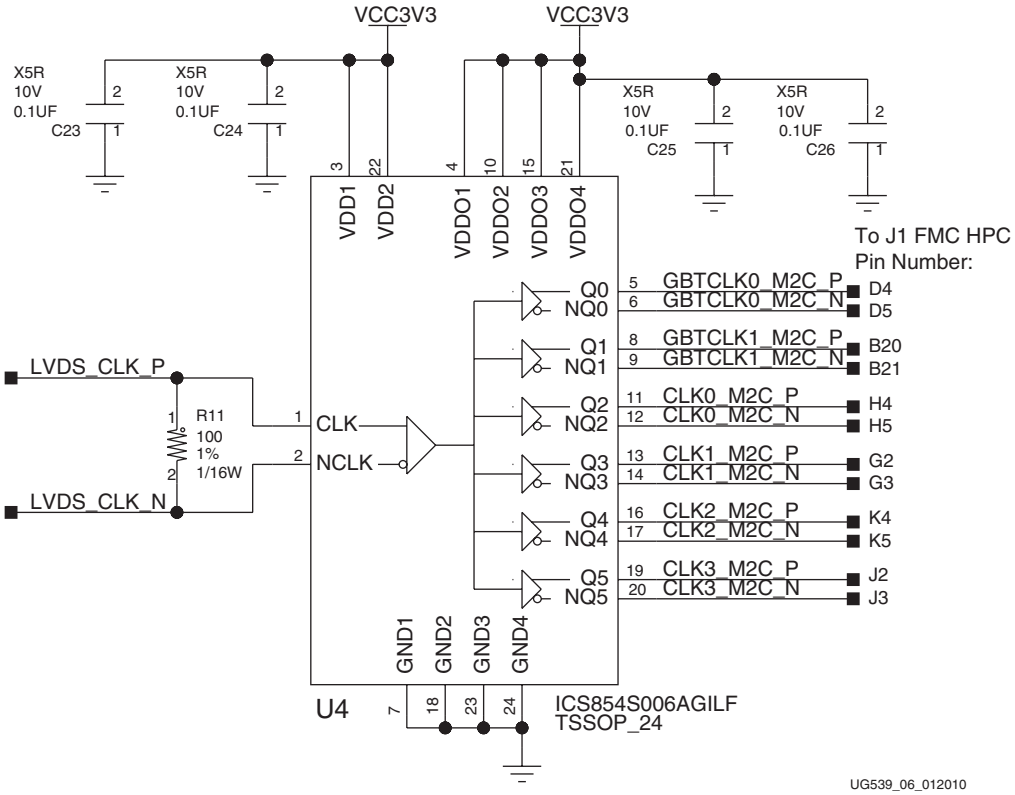

Figure 1-5: **XM107 U4 ICS854S006A Clock Buffer**

Table 1-10 shows the U4 output connections to the J1 FMC HPC connector.

Table 1-10: **U4 ICS854S006A Clock Buffer to J1 FMC HPC Connections**

U4 ICS854S006A		J1 FMC Connector
Net Name	**Pin Number**	**Pin Number**
GBTCLK0_M2C_P	5	D4
GBTCLK0_M2C_N	6	D5
GBTCLK1_M2C_P	8	B20
GBTCLK1_M2C_N	9	B21
CLK0_M2C_P	11	H4
CLK0_M2C_N	12	H5
CLK1_M2C_P	13	G2
CLK1_M2C_N	14	G3
CLK2_M2C_P	16	K4
CLK2_M2C_N	17	K5

Table 1-10: **U4 ICS854S006A Clock Buffer to J1 FMC HPC Connections *(Cont'd)***

U4 ICS854S006A		J1 FMC Connector
Net Name	**Pin Number**	**Pin Number**
CLK3_M2C_P	19	J2
CLK3_M2C_N	20	J3

The ICS854S006A component data sheet is available online at www.idt.com.

6. M24C02 2 Kb IIC EEPROM U3

An STMicroelectronics M24C02 2 Kb serial IIC bus EEPROM (U3) component provides a small amount of non-volatile memory storage on the XM107. The IIC interface is connected directly to the board IIC interface as shown in Figure 1-2, page 10.

The IIC address of this component is controlled by a combination of the board's interface and chip-enable connections to the component inputs on the XM107. Signals GA0 and GA1 from the board are connected to the chip-enable inputs of the M24C02 component enables E0 and E1. Xilinx boards provide GA0 and GA1 signal strapping to 3.3V and GND signals, creating different E0 and E1 chip-enable decodes on the E1 and E0 inputs of the EEPROM.

The IIC memory addressing protocol requires a bus master to initiate communication to a peripheral device using a start condition followed by a device select code. The device select code consists of a 4-bit Device Type Identifier and a 3-bit Chip Enable Address (E2, E1 and E0). Bit 0 is used to indicate read/write. The Device Type Identifier for the EEPROM is 1010 binary. Table 1-11 defines the generic EEPROM Device Select Code as well as specific Device Code Select addresses of the EEPROM when the XM107 is connected to a Xilinx board defined in Table 1-1, page 7.

Table 1-11: **EEPROM IIC Device Select Code**

Bit 7:4 Device Type Identifier	Bit 3	Bit 2	Bit 1	Bit 0 LSB	Description
1010	0	GA0	GA1	Read/$\overline{\text{Write}}$	Connected to mezzanine FMC HPC interface

The M24C02 component data sheet is available online at www.st.com.