ML623 IBERT Getting Started Guide (ISE 11.5)

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/22/10	1.0	Initial Xilinx release.
01/28/11	1.0.1	Revised cover title. Was: “ML623 IBERT Getting Started Guide.” Is: “ML623 IBERT Getting Started Guide (ISE 11.5).”

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Chapter 1

ML623 IBERT Getting Started Guide

Overview

This document provides a procedure for setting up the ML623 Virtex®-6 FPGA GTX Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration. The designs that are required to run the IBERT demonstration are stored in the CompactFlash memory card that is provided with the ML623 board. The demonstration shows the capabilities of the Virtex-6 XC6VLX240T FPGA GTX transceivers.

The IBERT demonstration operates one GTX Quad at a time. This procedure describes the steps to test a single Quad, Q112. The remaining four Quads are tested following the same series of steps. The procedure consists of:

1. Extracting the IBERT Demonstration Files.
2. Setting Up the ML623 Board.
3. Connecting the GTX Transceivers and Reference Clocks.
4. Configuring the FPGA.
5. Setting Up the ChipScope Pro Analyzer Tool.
6. Running the IBERT Demonstration.
7. Repeating the IBERT Demonstration for the Remaining GTX Quads.

The ML623 board is described in detail in UG724, *ML623 Virtex-6 FPGA GTX Transceiver Characterization Board User Guide*.

Requirements

The equipment and software required to run the demonstration are:

- ML623 Virtex-6 FPGA GTX Transceiver Characterization Board including:
  - CompactFlash memory card containing the IBERT demonstration designs
  - GTX transceiver power supply module (installed on ML623 board)
  - SuperClock-2 module (installed on ML623 board)
  - 12 SMA to SMA Cables
- One of these download cables:
  - Platform Cable USB-II (DLC10)
  - Parallel IV Cable (PC4)
- Host PC with USB ports and a PCMCIA interface
- CompactFlash PCMCIA adapter card

- Xilinx® ChipScope™ Pro analyzer software, version 11.4 or higher. Software is available at: http://www.xilinx.com/chipscopepro

Caution! The ML623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Procedure

Extracting the IBERT Demonstration Files

The ChipScope Pro Analyzer CPJ project files for the IBERT demonstration are located on the CompactFlash memory card that is provided with the ML623 board. The project files are used to load pre-saved MGT/IBERT and clock module control settings for the demonstration. These files must be copied from the CompactFlash memory card to a working directory on the host PC. To copy the project files:

1. Connect the CompactFlash memory card to the host computer.

   Note: The CompactFlash memory card can be plugged into the host PC PCMCIA interface using a PCMCIA adapter card.

2. Use Windows Explorer to locate `ml623.zip` on the Compact Flash memory card. The ZIP file content is similar to the files shown in Figure 1-1.

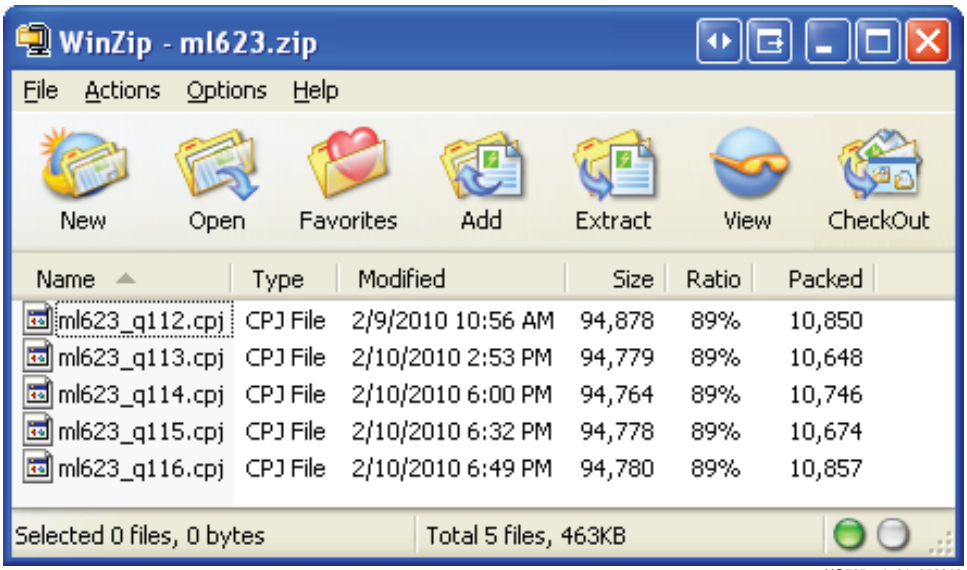

Figure 1-1: **ChipScope Software Project Files Included in the ml623.zip File**

3. Unzip the files to a working directory on the host PC.

Setting Up the ML623 Board

Caution! The ML623 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

To set up the ML623 board:

1. Install the GTX transceiver power module:
   a. Plug the module into connectors J34 and J179.
   b. Remove DCPS ENABLE jumpers at J184 and J185 located on the ML623 board.
2. Verify the four SYSACE JTAG ENABLE jumpers are installed at locations J22, J23, J195, and J196 on the ML623 board.
3. Place a jumper across pins 1–2 of the JTAG FMC BYPASS header at J162.
4. Enable the 200 MHz LVDS system clock by placing two jumpers (P, N) across pins 1–3 and pins 2–4 of J188.
5. Verify there is a 30 MHz oscillator in the SYSTEM ACE CLK oscillator socket at location X1 on the ML623 board.
6. Enable the System ACE™ controller clock by placing the jumper on J4 to the ON position.
7. Insert the CompactFlash memory card into the CF card connector (U24) located on the underside of the ML623 board.
8. Install the SuperClock-2 module:
   a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the CLOCK MODULE interface of the ML623 board.
   b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the ML623 board.
   c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18.

Connecting the GTX Transceivers and Reference Clocks

All GTX transceiver pins are connected to differential SMA connector pairs. The GTX transceivers are grouped into five sets of four (referred to as Quads) which share two differential reference clock pin pairs. Figure 1-2 shows the SMA locations for the GTX transceiver Quads (Q112 through Q116) and their associated reference clocks (112 Clocks through 116 Clocks).

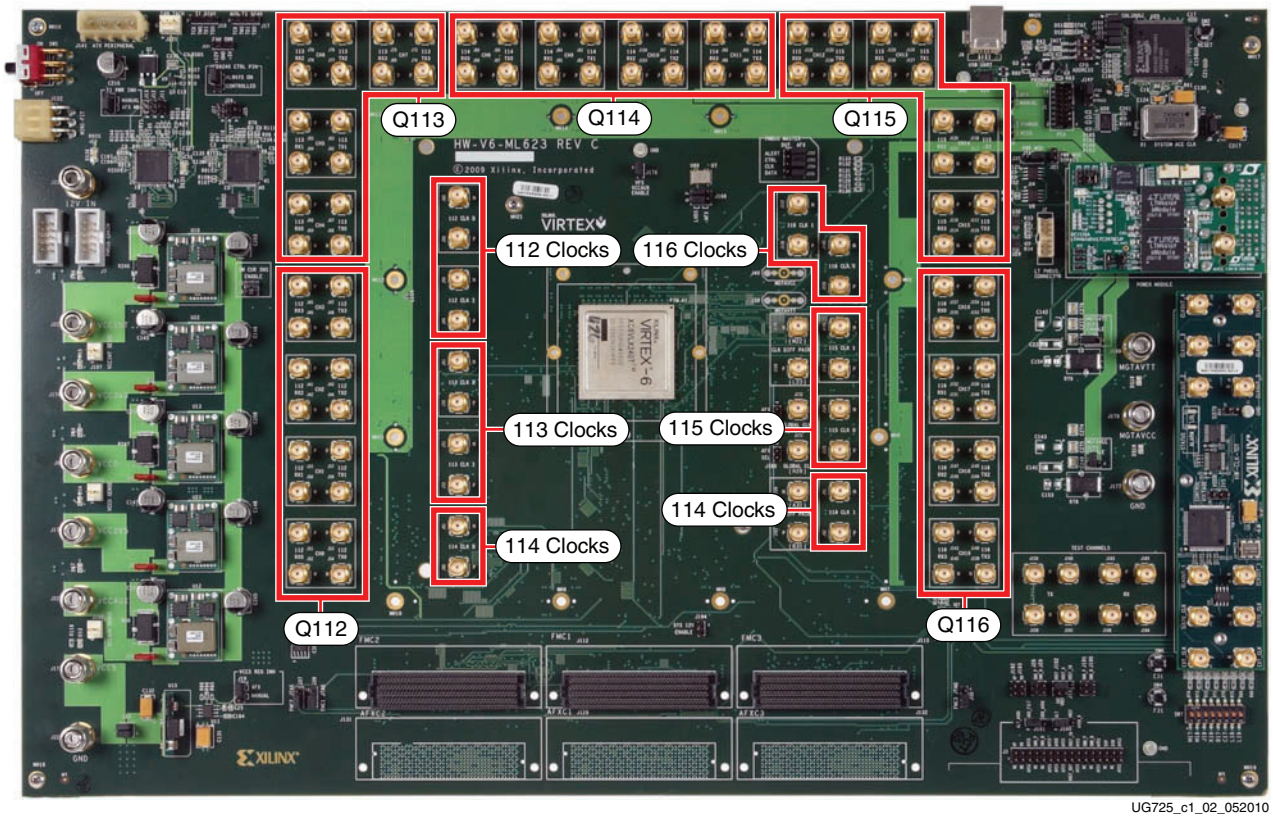

Figure 1-2: **GTX Transceiver and Reference Clock SMA Locations**

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

The SuperClock-2 module clocks the GTX transceivers in the IBERT demonstration. Figure 1-3 shows the location of the differential clock SMA connector pairs on the SuperClock-2 module which connect to the GTX transceiver reference clocks on the ML623 board. For the IBERT demonstration, the frequencies of both output clocks from the SuperClock-2 module are the same.

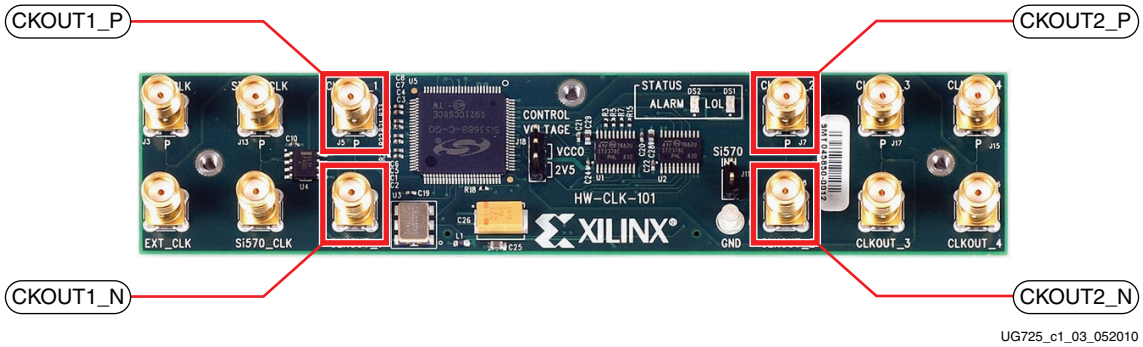

Figure 1-3: **SuperClock-2 Module Output Clock SMA Locations**

Note: The image in Figure 1-3 is for reference only and might not reflect the current revision of the board.

GTX Transceiver Clock Connections

Refer to Table 1-1 and use four SMA cables to connect the output clock SMAs from the SuperClock-2 module to the reference clock SMAs of GTX Quad Q112 on the ML623 board. In other words, for each row in Table 1-1, connect the source SMA with its corresponding destination SMA. For example, connect CKOUT1_P (J5) to 112_REFCLK0_P (J59).

Table 1-1: **Q112 Reference Clock Connections**

Source		Destination	
SuperClock-2 Module		ML623 Board	
Net Name	SMA Connector	Net Name	SMA Connector
CKOUT1_P	J5	112_REFCLK0_P	J59
CKOUT1_N	J6	112_REFCLK0_N	J60
CKOUT2_P	J7	112_REFCLK1_P	J49
CKOUT2_N	J8	112_REFCLK1_N	J50

See Appendix A for a complete listing of reference clock SMA connections for the remaining GTX Quads.

GTX TX/RX Connections

Refer to Table 1-2 and use eight SMA cables to connect the transmitter SMAs to the receiver SMAs in GTX Quad Q112. In other words, for each row in Table 1-2, connect the transmitter SMA with its corresponding receiver SMA.

For example, connect 112_TX0_P (J53) to 112_RX0_P (J51) on the ML623 board.

Table 1-2: **Q112 TX/RX Connections**

Transmitter		Receiver	
Net Name	SMA Connector	Net Name	SMA Connector
112_TX0_P	J53	112_RX0_P	J51
112_TX0_N	J54	112_RX0_N	J52
112_TX1_P	J57	112_RX1_P	J55
112_TX1_N	J58	112_RX1_N	J56
112_TX2_P	J43	112_RX2_P	J41
112_TX2_N	J44	112_RX2_N	J42
112_TX3_P	J47	112_RX3_P	J45
112_TX3_N	J48	112_RX3_N	J46

See Appendix A for a complete listing of TX/RX SMA connections for the remaining GTX Quads.

The final SMA cable connections for Q112 are shown in Figure 1-4.

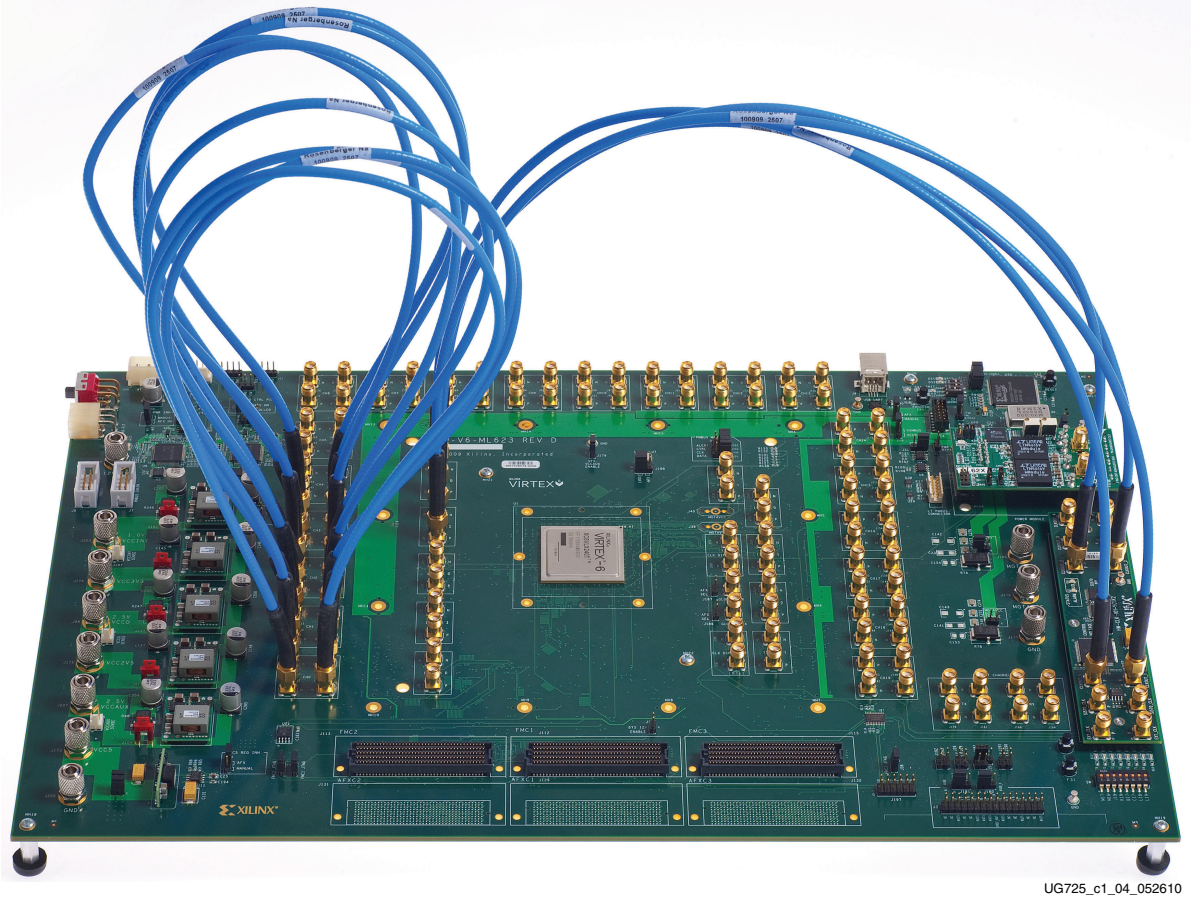

Figure 1-4: **SMA Cable Connections for Q112 Transceivers and Clocks**

Configuring the FPGA

1. Plug the 12V output from the power supply into connector J122.
2. Connect the ML623 board to the Host PC. Either of these cables may be used for this connection:
   - Platform Cable USB-II (DLC10)
   - Parallel IV Cable (PC4)

   Connect one end of the cable to the host PC. Connect the other end to the download cable connector (J1) on the ML623 board.
3. Set the System Ace Controller Configuration Address switch, SW3. The setting on this 3-bit DIP switch (shown in Figure 1-5) determines which bitstream stored in the CompactFlash card configures the FPGA. There are five IBERT demonstration designs on the CompactFlash card, one for each of the five GTX Quads available on the ML623 board. Note that Figure 1-5 shows an example setting of ADR[2:0] = `100`. For Q112, the configuration address is `000`.

   Table 1-3 lists the SW3 DIP switch settings for each of five Quads available on the ML623 board.

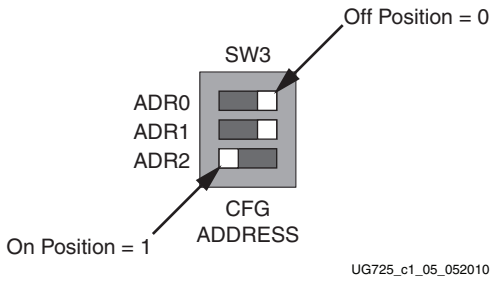

Figure 1-5: **Configuration Address DIP Switch (SW3)**

Table 1-3: **DIP Switch SW3 Configuration Addresses**

Demonstration Design	ADR2	ADR1	ADR0
Q112	0	0	0
Q113	0	0	1
Q114	0	1	0
Q115	0	1	1
Q116	1	0	0

4. Apply power to the board by placing SW1 in the ON position. After a few seconds, the FPGA is configured and the Done LED (DS6) lights.

Setting Up the ChipScope Pro Analyzer Tool

1. Open the ChipScope Pro Analyzer tool and select **File** → **Open Project**.
2. When the Open Project window appears, navigate to the location on the host PC where the `.cpj` project files were extracted, select `ml623_q112.cpj` and click **Open** (Figure 1-6).

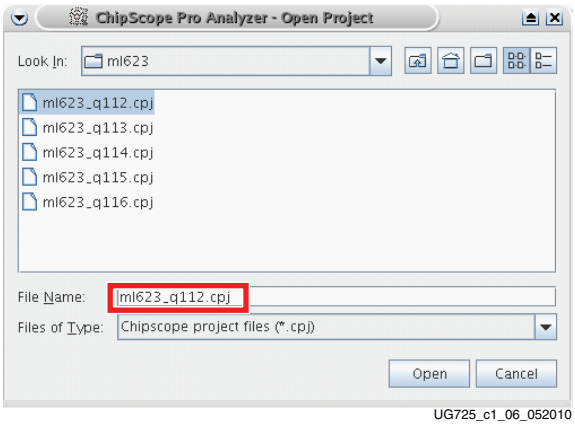

Figure 1-6: **Open Project Window**

Note: The `.cpj` file loads pre-saved project settings for the demonstration including MGT/IBERT and clock module control parameters. For more information regarding MGT/IBERT settings, refer to UG029, *ChipScope Pro Software and Cores User Guide*.

3. When the new project window opens, click the **Open Cable** button (Figure 1-7).

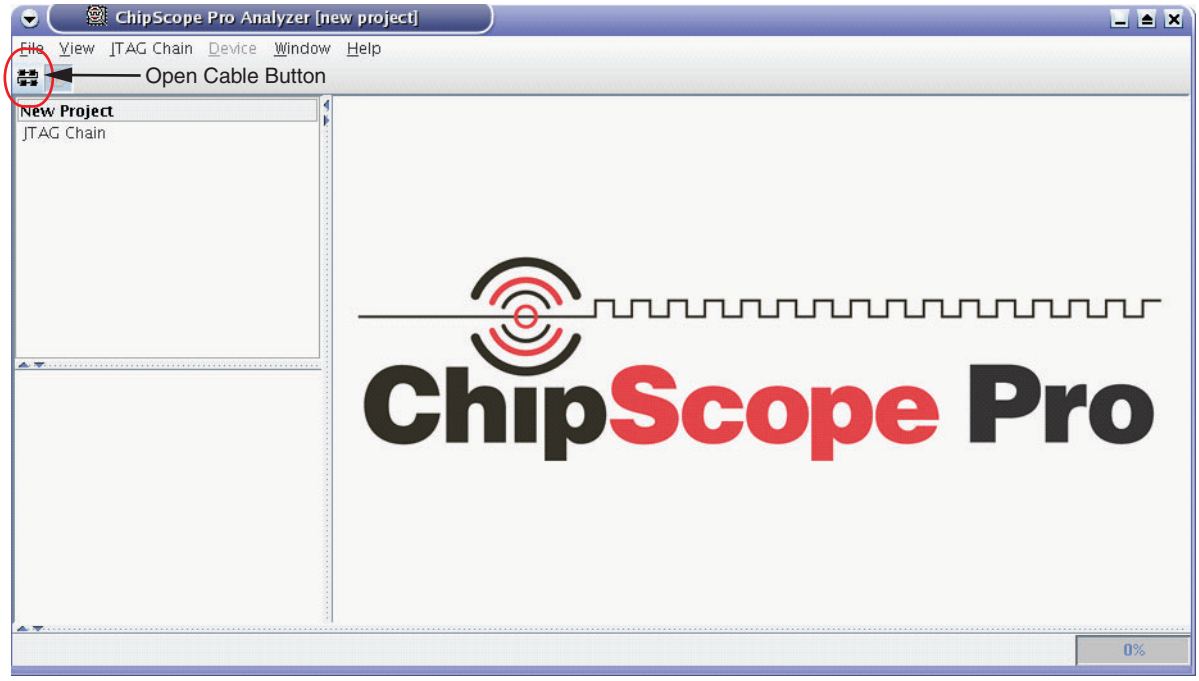

Figure 1-7: **Open Cable Button**

4. When the dialog box opens asking to set up the core with settings from the current project, click **Yes** (Figure 1-8).

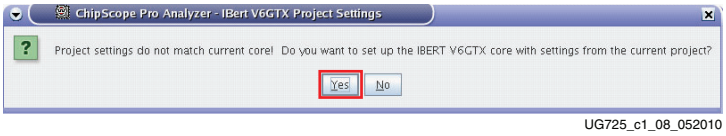

Figure 1-8: **Core Settings Dialog Box**

5. When the project panel opens, verify the JTAG chain shows the devices listed in Figure 1-9.

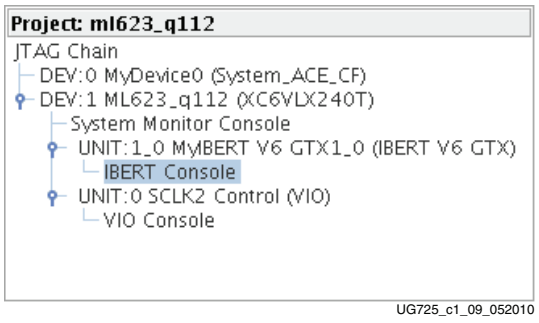

Figure 1-9: **Project Panel**

Starting the Clock Module

The IBERT demonstration design uses a ChipScope VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components: An always-on Si570 crystal oscillator and an Si5368 jitter-attenuating clock multiplier. The IBERT demonstration uses the output from the Si5368 device to clock the GTX transceivers.

1. In the project panel, double-click **VIO Console** (Figure 1-10).

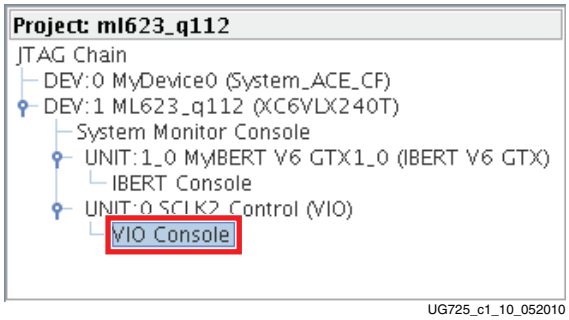

Figure 1-10: **VIO Console Selection**

2. Having selected the VIO Console, click the **Si5368 Start** button (Figure 1-11). A transition arrow flashes ON/OFF to the right of **Si5368 Done** when the command is complete.

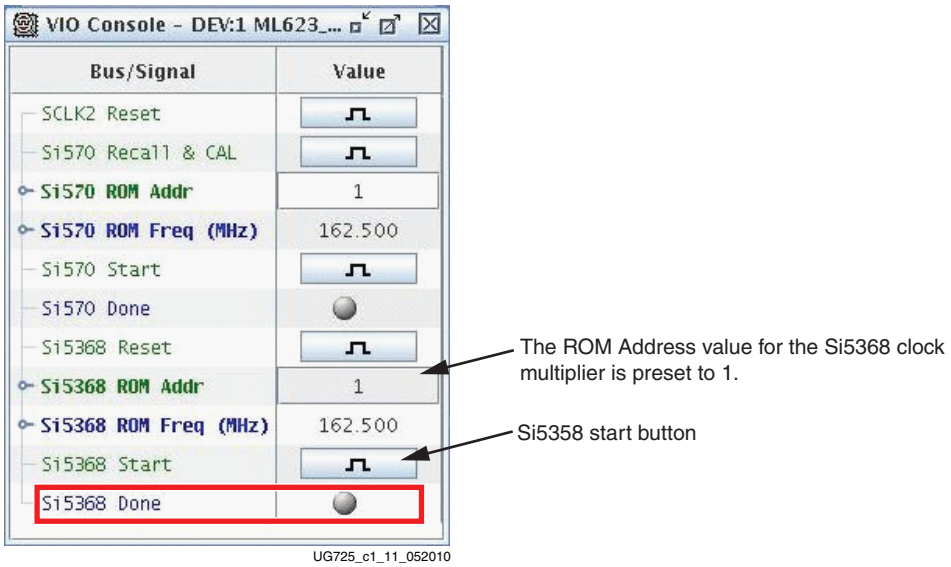

Figure 1-11: **VIO Console**

Note: The ROM address value for the Si5368 is preset to `1` to produce an output frequency of 162.5 MHz. Typing in a different address changes the frequency of the GTX transceiver reference clocks. A complete list of frequency options and their associated ROM addresses is provided in Table 1-4, page 18.

3. In the project panel, double-click **IBERT Console** (Figure 1-12).

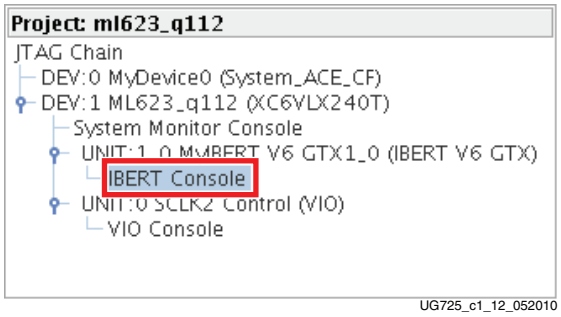

Figure 1-12: **IBERT Console Selection**

4. At the top of the ChipScope Pro Analyzer window, click the **Reset All** button (Figure 1-13).

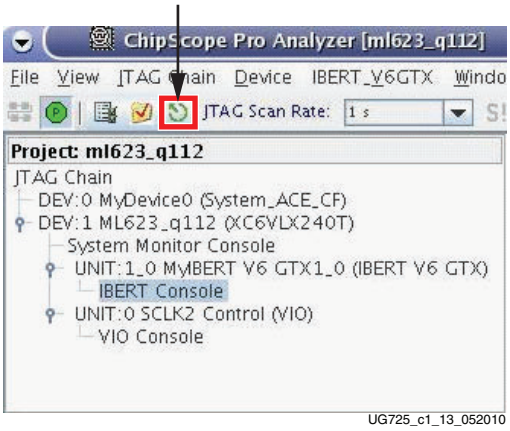

Figure 1-13: **Reset All Button**

5. When the confirmation dialog box opens, click **Yes** (Figure 1-14).

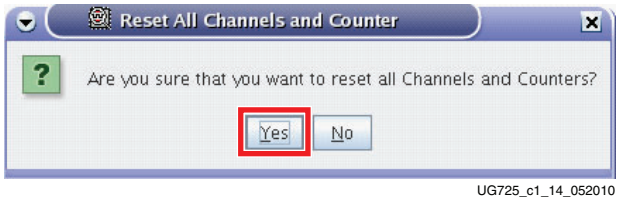

Figure 1-14: **Reset Confirmation Dialog Box**

Running the IBERT Demonstration

After completing step 5 in Starting the Clock Module, the IBERT demonstration is configured and running as indicated by the **MGT/IBERT Settings** tab within the IBERT Console.

Viewing GTX Transceiver Operation

1. Note the line rate is 6.5 Gb/s for all four GTX transceivers (MGT Link Status in Figure 1-15).

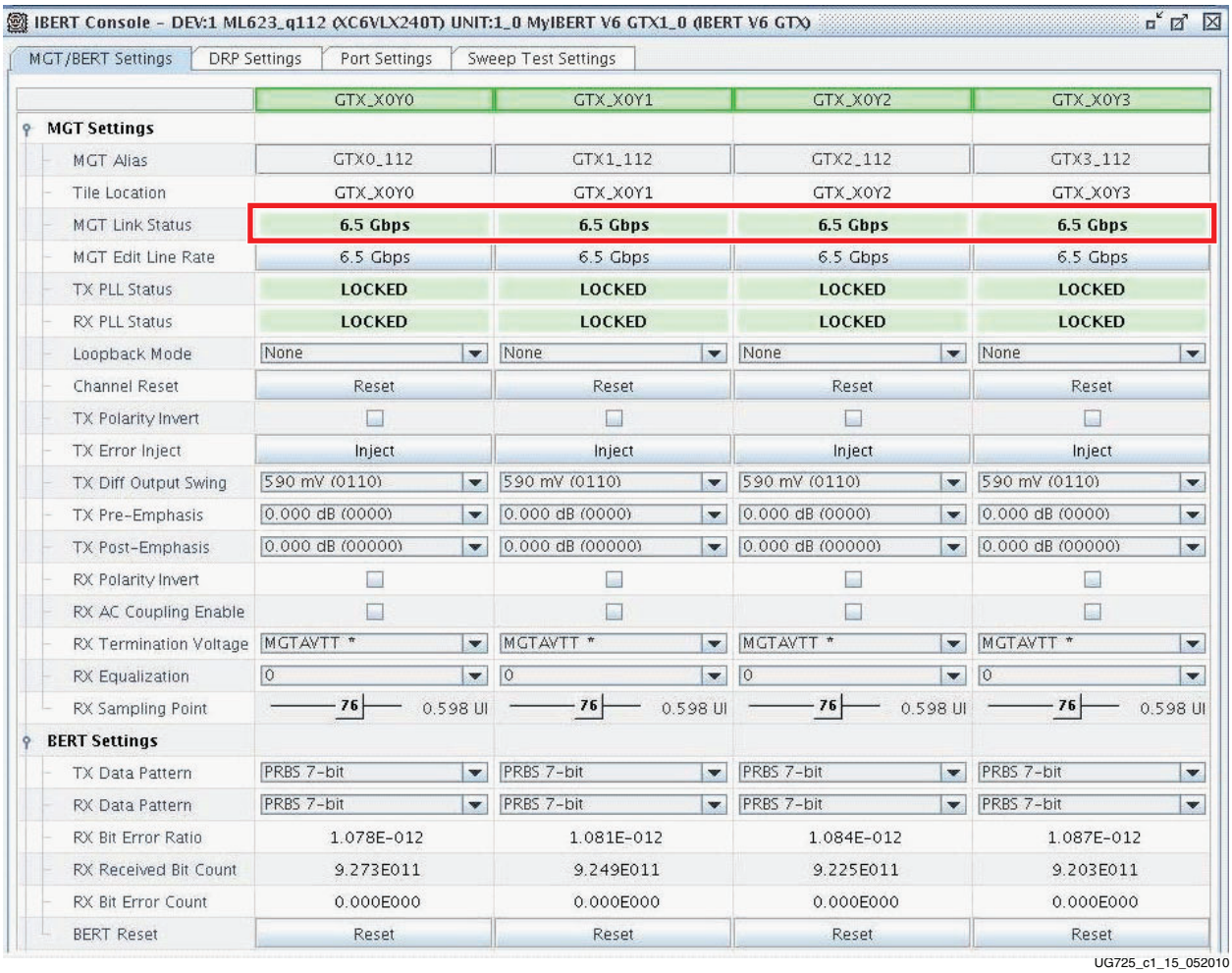

Figure 1-15: **GTX Transceiver Link Status**

2. Note the GTX transmitter differential output swing is preset to 590 mV (`0110`) as shown in Figure 1-16.

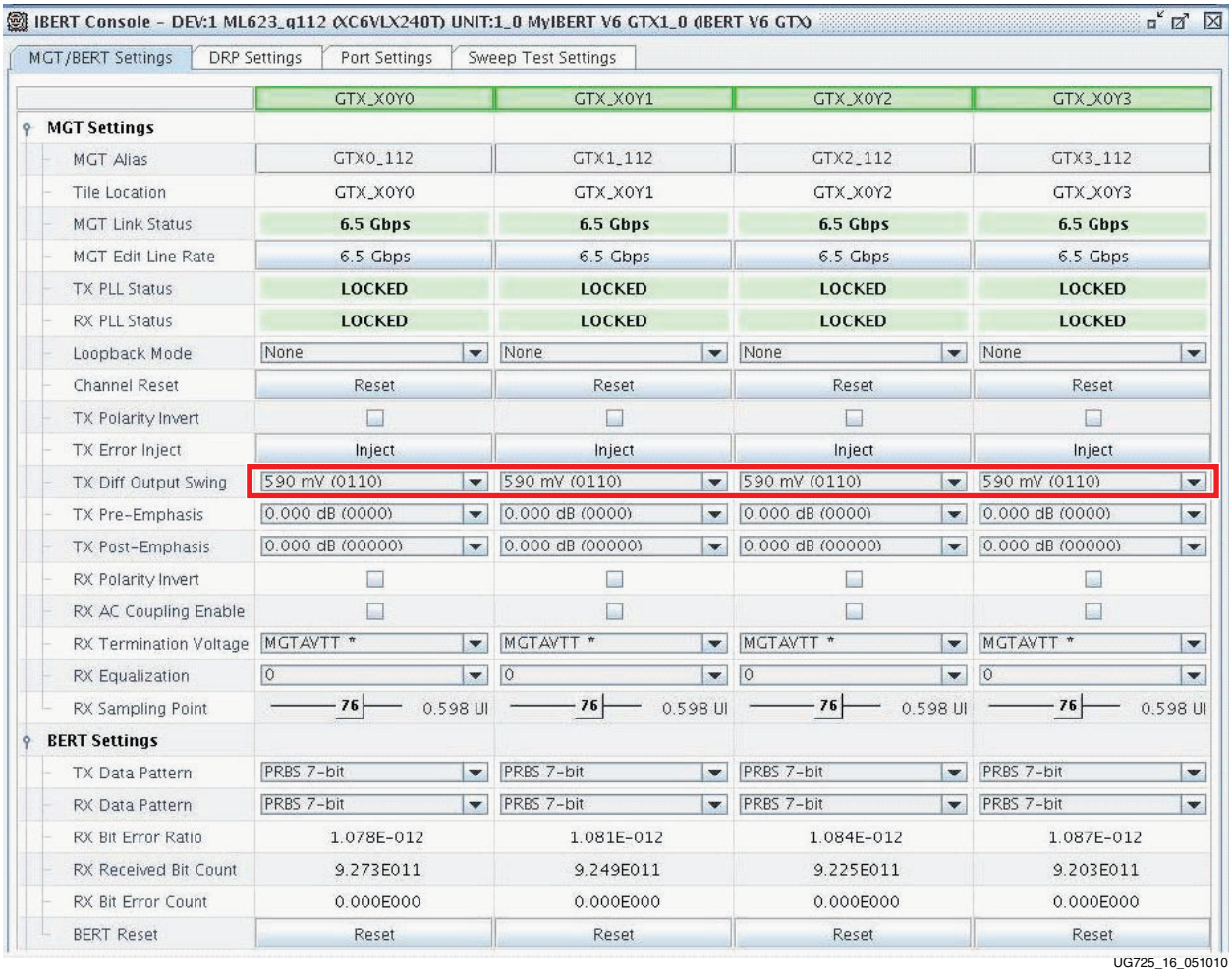

Figure 1-16: **GTX Transceiver TX Differential Output Swing**

3. Note that there are no bit errors as indicated by the RX Bit Error Count as shown in Figure 1-17.

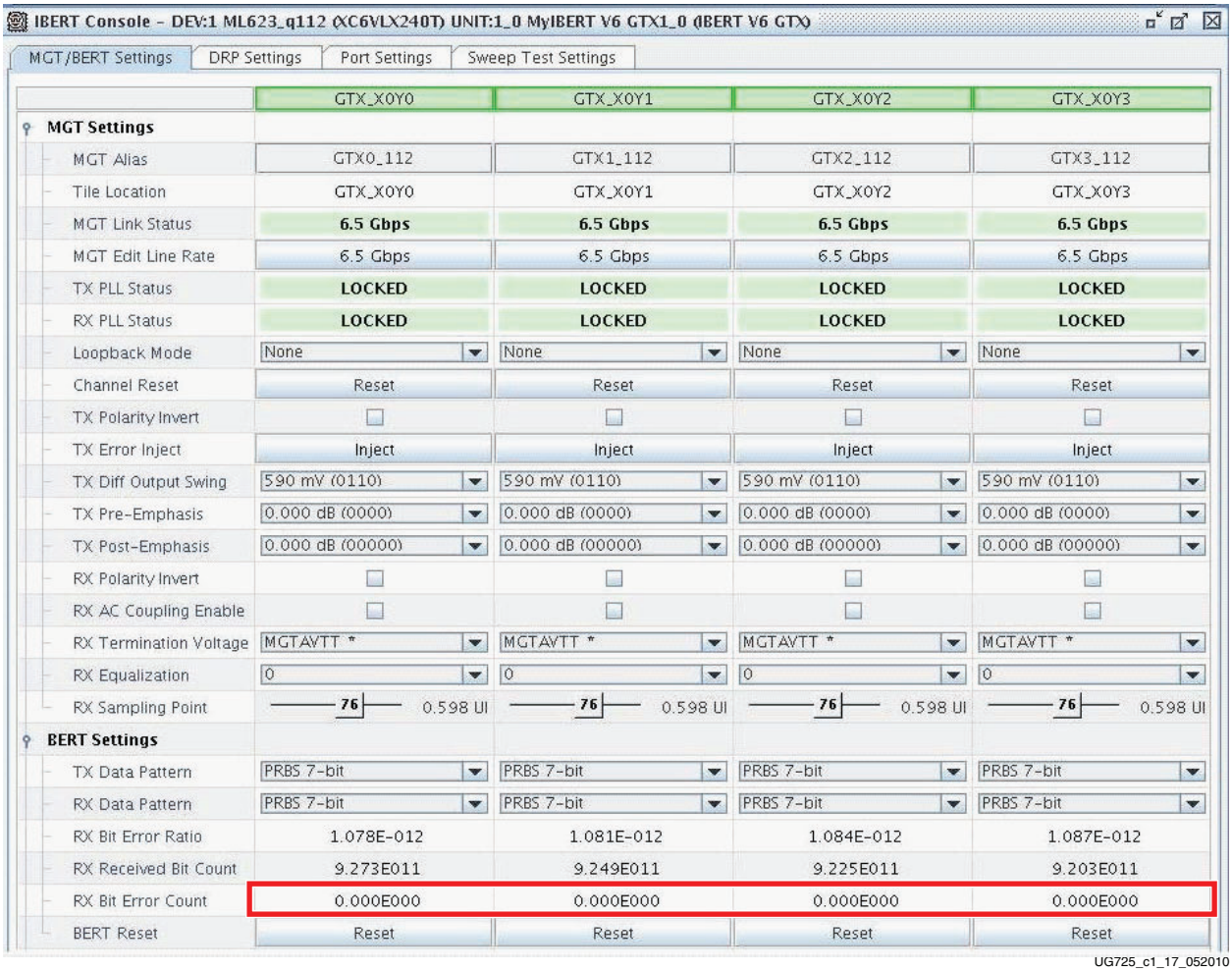

Figure 1-17: **RX Bit Error Count**

Stopping the IBERT Demonstration

To stop the IBERT demonstration:

1. Close the ChipScope Pro Analyzer tool.

   Note: Do not save changes to the project.

2. Remove power to the ML623 board by placing SW1 in the OFF position.
3. Remove the SMA cables from the ML623 board.

Repeating the IBERT Demonstration for the Remaining GTX Quads

Start at Connecting the GTX Transceivers and Reference Clocks, page 7 and repeat the procedure for the remaining GTX Quads. Appendix A lists the connections for Q113, Q114, Q115, and Q116.

Frequency Table

Table 1-4 lists the addresses of the output frequencies of the Si570 and Si5360 programmable clock sources.

Table 1-4: **Si570 and Si5368 Frequency Table**

Address	Protocol	Frequency	Address	Protocol	Frequency	Address	Protocol	Frequency
0	Aurora	81.250	30	OC-48	77.760	60	Generic	533.333
1	Aurora	162.500	31	OC-48	155.520	61	Generic	644.000
2	Aurora	325.000	32	OC-48	311.040	62	Generic	666.667
3	Aurora	650.000	33	OC-48	622.080	63	Generic	205.000
4	CPRI	61.440	34	OTU-1	166.629	64	Generic	210.000
5	CPRI	122.880	35	OTU-1	333.257	65	Generic	215.000
6	CPRI	245.760	36	OTU-1	666.514	66	Generic	220.000
7	CPRI	491.520	37	PCIe	100.000	67	Generic	225.000
8	Display Port	67.500	38	PCIe	125.000	68	Generic	230.000
9	Display Port	81.000	39	PCIe	250.000	69	Generic	235.000
10	Display Port	135.000	40	SATA	75.000	70	Generic	240.000
11	Display Port	162.000	41	SATA	150.000	71	Generic	245.000
12	Fibre channel	106.250	42	SATA	300.000	72	Generic	250.000
13	Fibre channel	212.500	43	SATA	600.000	73	Generic	255.000
14	Fibre channel	425.000	44	SDI	74.250	74	Generic	260.000
15	Gigabit Ethernet	62.500	45	SDI	148.500	75	Generic	265.000
16	Gigabit Ethernet	125.000	46	SDI	297.000	76	Generic	270.000
17	Gigabit Ethernet	250.000	47	SDI	594.000	77	Generic	275.000
18	Gigabit Ethernet	500.000	48	SMPTE435M	167.063	78	Generic	280.000
19	GPON	187.500	49	SMPTE435M	334.125	79	Generic	285.000
20	Interlaken	132.813	50	SMPTE435M	668.250	80	Generic	290.000
21	Interlaken	195.313	51	XAUI	78.125	81	Generic	295.000
22	Interlaken	265.625	52	XAUI	156.250	82	Generic	300.000
23	Interlaken	390.625	53	XAUI	312.500	83	Generic	305.000
24	Interlaken	531.250	54	XAUI	625.000	84	Generic	310.000
25	OBSAI	76.800	55	Generic	66.667	85	Generic	315.000
26	OBSAI	153.600	56	Generic	133.333	86	Generic	320.000
27	OBSAI	307.200	57	Generic	166.667	87	Generic	325.000
28	OBSAI	614.400	58	Generic	266.667	88	Generic	330.000
29	OC-48	19.440	59	Generic	333.333	89	Generic	335.000

Table 1-4: **Si570 and Si5368 Frequency Table *(Cont'd)***

Address	Protocol	Frequency	Address	Protocol	Frequency	Address	Protocol	Frequency
90	Generic	340.000	103	Generic	405.000	116	Generic	470.000
91	Generic	345.000	104	Generic	410.000	117	Generic	475.000
92	Generic	350.000	105	Generic	415.000	118	Generic	480.000
93	Generic	355.000	106	Generic	420.000	119	Generic	485.000
94	Generic	360.000	107	Generic	425.000	120	Generic	490.000
95	Generic	365.000	108	Generic	430.000	121	Generic	495.000
96	Generic	370.000	109	Generic	435.000	122	Generic	500.000
97	Generic	375.000	110	Generic	440.000	123	Generic	505.000
98	Generic	380.000	111	Generic	445.000	124	Generic	510.000
99	Generic	385.000	112	Generic	450.000	125	Generic	515.000
100	Generic	390.000	113	Generic	455.000	126	Generic	520.000
101	Generic	395.000	114	Generic	460.000	127	Generic	525.000
102	Generic	400.000	115	Generic	465.000			

References

UG029, *ChipScope Pro Software and Cores User Guide*

UG724, *ML623 Virtex-6 FPGA GTX Transceiver Characterization Board User Guide*.

HW-CLK-101-SCLK2 SuperClock-2 Module User Guide

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Appendix A

SMA Connections for Quads Q113-Q116

Connecting the GTX Transceivers and Reference Clocks, page 7 describes how to connect the GTX transceivers and reference clocks to run the IBERT demonstration for Quad Q112. To run the IBERT demonstration for Quad Q113, Q114, Q115, or Q116, follow the procedure from the start of the aforementioned section substituting the connections for the Quad of interest as provided by the tables listed in Q113, Q114, Q115, or Q116.

Q113

Use the connections in Table A-1 and Table A-2 to run the IBERT demonstration with `ml623_q113.cpj`.

Table A-1: **Q113 Reference Clock Connections**

Source		Destination	
SuperClock-2 Module		ML623 Board	
Net Name	SMA Connector	Net Name	SMA Connector
CKOUT1_P	J5	113_REFCLK0_P	J70
CKOUT1_N	J6	113_REFCLK0_N	J61
CKOUT2_P	J7	113_REFCLK1_P	J72
CKOUT2_N	J8	113_REFCLK1_N	J71

Table A-2: **Q113 TX/RX Connections**

Transmitter		Receiver	
Net Name	SMA Connector	Net Name	SMA Connector
113_TX0_P	J67	113_RX0_P	J68
113_TX0_N	J66	113_RX0_N	J69
113_TX1_P	J63	113_RX1_P	J65
113_TX1_N	J62	113_RX1_N	J64
113_TX2_P	J77	113_RX2_P	J79
113_TX2_N	J76	113_RX2_N	J78
113_TX3_P	J74	113_RX3_P	J80
113_TX3_N	J73	113_RX3_N	J75

Q114

Use the connections in Table A-3 and Table A-4 to run the IBERT demonstration with `ml623_q114.cpj`.

Table A-3: **Q114 Reference Clock Connections**

Source		Destination	
SuperClock-2 Module		ML623 Board	
Net Name	SMA Connector	Net Name	SMA Connector
CKOUT1_P	J5	114_REFCLK0_P	J90
CKOUT1_N	J6	114_REFCLK0_N	J81
CKOUT2_P	J7	114_REFCLK1_P	J92
CKOUT2_N	J8	114_REFCLK1_N	J91

Table A-4: **Q114 TX/RX Connections**

Transmitter		Receiver	
Net Name	SMA Connector	Net Name	SMA Connector
114_TX0_P	J87	114_RX0_P	J88
114_TX0_N	J86	114_RX0_N	J89
114_TX1_P	J83	114_RX1_P	J85
114_TX1_N	J82	114_RX1_N	J84
114_TX2_P	J99	114_RX2_P	J103
114_TX2_N	J97	114_RX2_N	J100
114_TX3_P	J94	114_RX3_P	J96
114_TX3_N	J93	114_RX3_N	J95

Q115

Use the connections in Table A-5 and Table A-6 to run the IBERT demonstration with `ml623_q115.cpj`.

Table A-5: **Q115 Reference Clock Connections**

Source		Destination	
SuperClock-2 Module		ML623 Board	
Net Name	SMA Connector	Net Name	SMA Connector
CKOUT1_P	J5	115_REFCLK0_P	J125
CKOUT1_N	J6	115_REFCLK0_N	J124
CKOUT2_P	J7	115_REFCLK1_P	J123
CKOUT2_N	J8	115_REFCLK1_N	J106

Table A-6: **Q115 TX/RX Connections**

Transmitter		Receiver	
Net Name	SMA Connector	Net Name	SMA Connector
115_TX0_P	J134	115_RX0_P	J136
115_TX0_N	J133	115_RX0_N	J135
115_TX1_P	J127	115_RX1_P	J130
115_TX1_N	J126	115_RX1_N	J128
115_TX2_P	J118	115_RX2_P	J120
115_TX2_N	J117	115_RX2_N	J121
115_TX3_P	J111	115_RX3_P	J116
115_TX3_N	J110	115_RX3_N	J114

Q116

Use the connections in Table A-7 and Table A-8 to run the IBERT demonstration with `ml623_q116.cpj`.

Table A-7: **Q116 Reference Clock Connections**

Source		Destination	
SuperClock-2 Module		ML623 Board	
Net Name	SMA Connector	Net Name	SMA Connector
CKOUT1_P	J5	116_REFCLK0_P	J156
CKOUT1_N	J6	116_REFCLK0_N	J148
CKOUT2_P	J7	116_REFCLK1_P	J138
CKOUT2_N	J8	116_REFCLK1_N	J137

Table A-8: **Q116 TX/RX Connections**

Transmitter		Receiver	
Net Name	SMA Connector	Net Name	SMA Connector
116_TX0_P	J154	116_RX0_P	J157
116_TX0_N	J153	116_RX0_N	J155
116_TX1_P	J150	116_RX1_P	J152
116_TX1_N	J149	116_RX1_N	J151
116_TX2_P	J145	116_RX2_P	J147
116_TX2_N	J144	116_RX2_N	J146
116_TX3_P	J140	116_RX3_P	J143
116_TX3_N	J139	116_RX3_N	J142