

Virtex-7 FPGA VC7203 Characterization Kit IBERT

Getting Started Guide

Vivado Design Suite 2013.3

UG847 (v4.0) November 6, 2013



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Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|------------|---------|--|
| 11/07/2012 | 1.0 | Initial Xilinx release. |
| 01/23/2013 | 2.0 | Updated for ISE® Design Suite 14.4 and Vivado® Design Suite 2012.4. |
| 07/10/2013 | 3.0 | Updated for Vivado Design Suite 2013.2. Updated Extracting the Project Files, page 7 , Launching the Vivado Design Suite Software, page 14 , Starting the SuperClock-2 Module, page 16 , and Creating the GTX IBERT Core, page 25 for the latest procedures. |
| 11/06/2013 | 4.0 | Updated for Vivado® Design Suite 2013.3. Device number was corrected from XC7V485T to XC7VX485T. Updated most figures in Chapter 1, VC7203 IBERT Getting Started Guide . The ZIP project file name changed to <code>rd0272-vc7203-ibert-2013-3.zip</code> . In Figure 1-11, Diligent JTAG cable changed to <i>Xilinx TCF agent</i> . Figure 1-30 was renamed <i>Design Sources File Hierarchy</i> . Figure 1-31, Synthesize Out-Of-Context Module was deleted. Updated Appendix A, Additional Resources links. |

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Chapter 1

VC7203 IBERT Getting Started Guide

Overview

This document provides a procedure for setting up the VC7203 Virtex®-7 FPGA GTX Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration using the Vivado® Design Suite. The designs that are required to run the IBERT demonstration are stored in a Secure Digital (SD) memory card that is provided with the VC7203 board. The demonstration shows the capabilities of the Virtex-7 XC7VX485T FPGA GTX transceiver.

The VC7203 board is described in detail in *VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide* (UG957).

The IBERT demonstrations operate one GTX Quad at a time. The procedure consists of:

1. [Setting Up the VC7203 Board, page 6](#)
2. [Extracting the Project Files, page 7](#)
3. [Connecting the GTX Transceivers and Reference Clocks, page 8](#)
4. [Configuring the FPGA, page 13](#)
5. [Launching the Vivado Design Suite Software, page 14](#)
6. [Starting the SuperClock-2 Module, page 16](#)
7. [Viewing GTX Transceiver Operation, page 23](#)
8. [Closing the IBERT Demonstration, page 23](#)

Requirements

The hardware and software required to run the GTX IBERT demonstrations are:

- VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board including:
 - One SD card containing the IBERT demonstration designs
 - One Samtec BullsEye cable
 - Eight SMA female-to-female (F-F) adapters
 - Six 50Ω SMA terminators
 - GTX transceiver power supply module (installed on board)
 - SuperClock-2 module, Rev 1.0 (installed on board)
 - 12V DC power adapter
 - USB cable, standard-A plug to Micro-B plug
- Host PC with:
 - SD card reader
 - USB ports
- Xilinx Vivado Design Suite software, version 2013.3

The hardware and software required to rebuild the IBERT demonstration designs are:

- Xilinx Vivado Design Suite version 2013.3
- PC with a version of the Windows operating system supported by Xilinx Vivado Design Suite

Setting Up the VC7203 Board

This section describes how to set up the VC7203 board.

Caution! The VC7203 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

When the VC7203 board ships from the factory, it is configured for the GTX IBERT demonstrations described in this document. If the board has been re-configured it must be returned to the default set-up before running the IBERT demonstrations.

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in *VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide* (UG957).
2. Install the GTX transceiver power module by plugging it into connectors J66 and J97.
3. Install the SuperClock-2 module:
 - a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the VC7203 board.
 - b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the VC7203 board.
 - c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.
 - d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.

Extracting the Project Files

The Vivado project files required to run the IBERT demonstrations are located in `rdf0272-vc7203-ibert-2013-3.zip` on the SD card provided with the VC7203 board. This collection is also available online at the [Virtex-7 FPGA VC7203 Characterization Kit documentation website](#).

The ZIP collection also contains two Tcl scripts: `add_scm2.tcl` and `setup_scm2_156_25.tcl`, and seven Vivado probe files: `vc7203_q113.ltx`, `vc7203_q114.ltx`, `vc7203_q115.ltx`, `vc7203_q116.ltx`, `vc7203_q117.ltx`, `vc7203_q118.ltx`, and `vc7203_q119.ltx`. The Tcl scripts are used to help merge the IBERT and SuperClock-2 source code (described in [Creating the GTX IBERT Core, page 25](#)) and to set up the SuperClock-2 module to run at 156.25 MHz (described in [Launching the Vivado Design Suite Software, page 14](#)). The debug probes are used by Vivado design tools to properly load the SuperClock-2 VIO core.

To copy the files from the Secure Digital memory card:

1. Connect the Secure Digital memory card to the host computer.
2. Locate the file `rdf0272-vc7203-ibert-2013-3.zip` on the Secure Digital memory card.
3. Unzip the files to a working directory on the host computer.

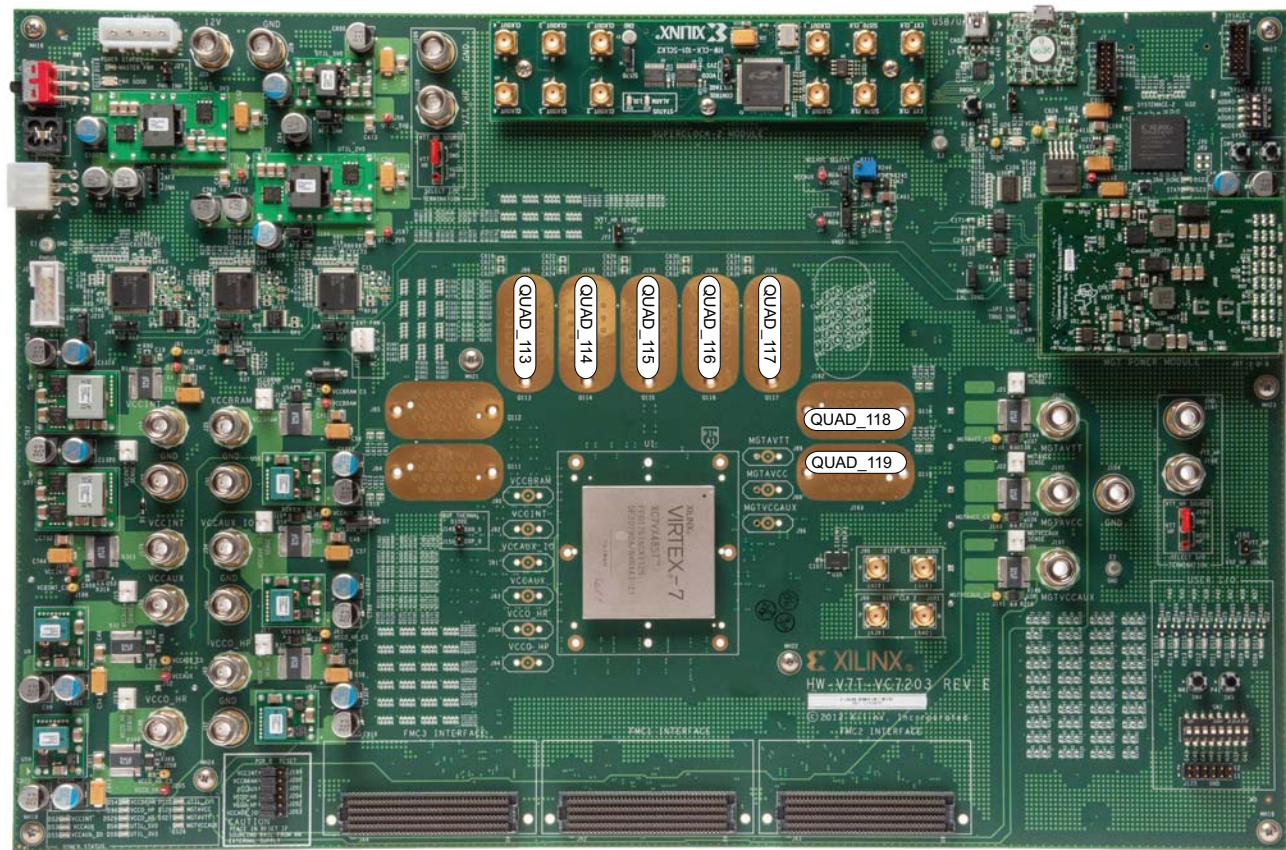
Running the GTX IBERT Demonstration

The GTX IBERT demonstration operates one GTX Quad at a time. This section describes how to test GTX Quad 115. The remaining GTX Quads are tested following a similar series of steps.

Connecting the GTX Transceivers and Reference Clocks

Figure 1-1 shows the locations for GTX transceiver Quads 113, 114, 115, 116, 117, 118, and 119 on the VC7203 board.

Note: Figure 1-1 is for reference only and might not reflect the current revision of the board.



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Figure 1-1: GTX Quad Locations

All GTX transceiver pins and reference clock pins are routed from the FPGA to a connector pad which interfaces with Samtec BullsEye connectors. **Figure 1-2 A** shows the connector pad. **Figure 1-2 B** shows the connector pinout.

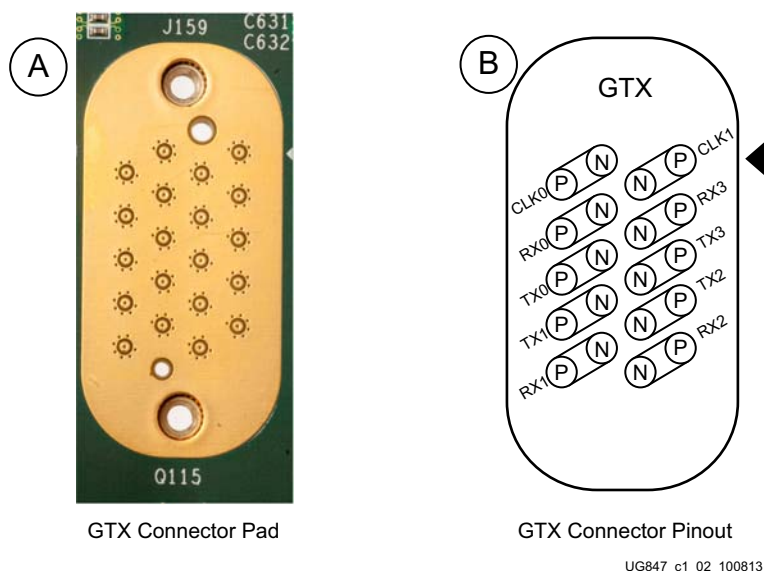


Figure 1-2: A – GTX Connector Pad. B – GTX Connector Pinout

The SuperClock-2 module provides LVDS clock outputs for the GTX transceiver reference clocks in the IBERT demonstrations. **Figure 1-3** shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

Note: The image in **Figure 1-3** is for reference only and might not reflect the current revision of the board.

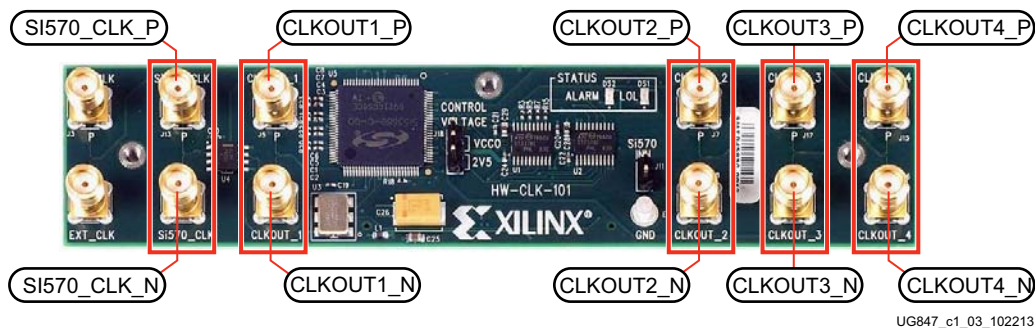


Figure 1-3: SuperClock-2 Module Output Clock SMA Locations

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

Note: The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For the GTX IBERT demonstration, the output clock frequencies are preset to 156.25 MHz. For more information regarding the SuperClock-2 module, see *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770).

Attach the GTX Quad Connector

Before connecting the BullsEye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if it is not already inserted (see [Figure 1-4](#)).

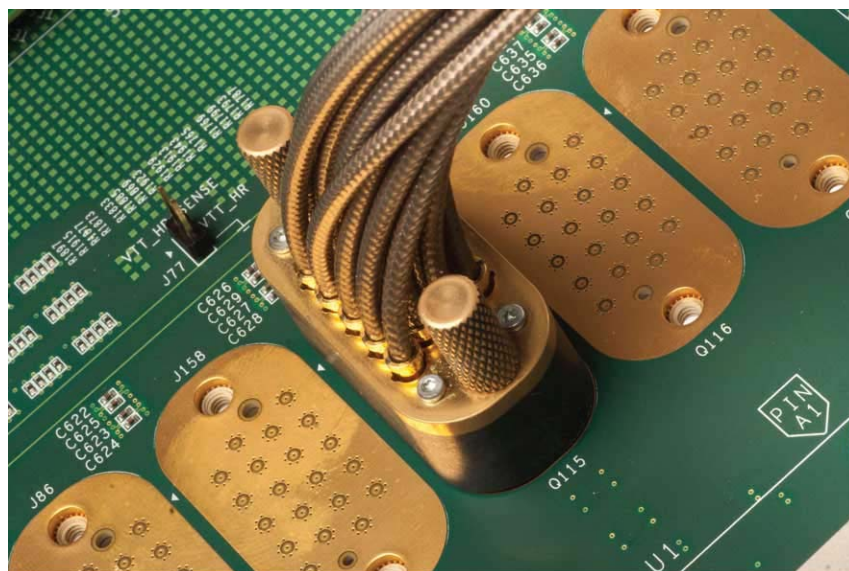
Note: [Figure 1-4](#) is for reference only and might not reflect the current version of the connector.



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Figure 1-4: BullsEye Connector with Elastomer Seal

Attach the Samtec BullsEye connector to GTX Quad 115 ([Figure 1-5](#)), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.



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Figure 1-5: BullsEye Connector Attached to Quad 115

GTX Transceiver Clock Connections

See [Figure 1-2, page 9](#) to identify the P and N coax cables that are connected to the CLK1 reference clock inputs. Connect these cables to the SuperClock-2 module as follows:

- CLK1_P coax cable → SMA connector J5 (CLKOUT1_P) on the SuperClock-2 module
- CLK1_N coax cable → SMA connector J6 (CLKOUT1_N) on the SuperClock-2 module

Note: Any one of the five differential outputs from the SuperClock-2 module can be used to source the GTX reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.

GTX TX/RX Loopback Connections

See [Figure 1-2, page 9](#) to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2 and RX3) and the four transmitters (TX0, TX1, TX2 and TX3). Use eight SMA female-to-female (F-F) adapters ([Figure 1-6](#)), to connect the transmit and receive cables as shown in [Figure 1-7](#) and detailed here:

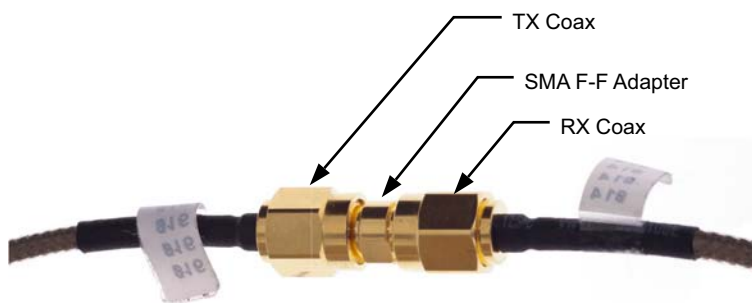
- TX0_P → SMA F-F Adapter → RX0_P
- TX0_N → SMA F-F Adapter → RX0_N
- TX1_P → SMA F-F Adapter → RX1_P
- TX1_N → SMA F-F Adapter → RX1_N
- TX2_P → SMA F-F Adapter → RX2_P
- TX2_N → SMA F-F Adapter → RX2_N
- TX3_P → SMA F-F Adapter → RX3_P
- TX3_N → SMA F-F Adapter → RX3_N

Note: To ensure good connectivity, it is recommended that the adapters be secured with a wrench; however, do not over tighten the SMAs.



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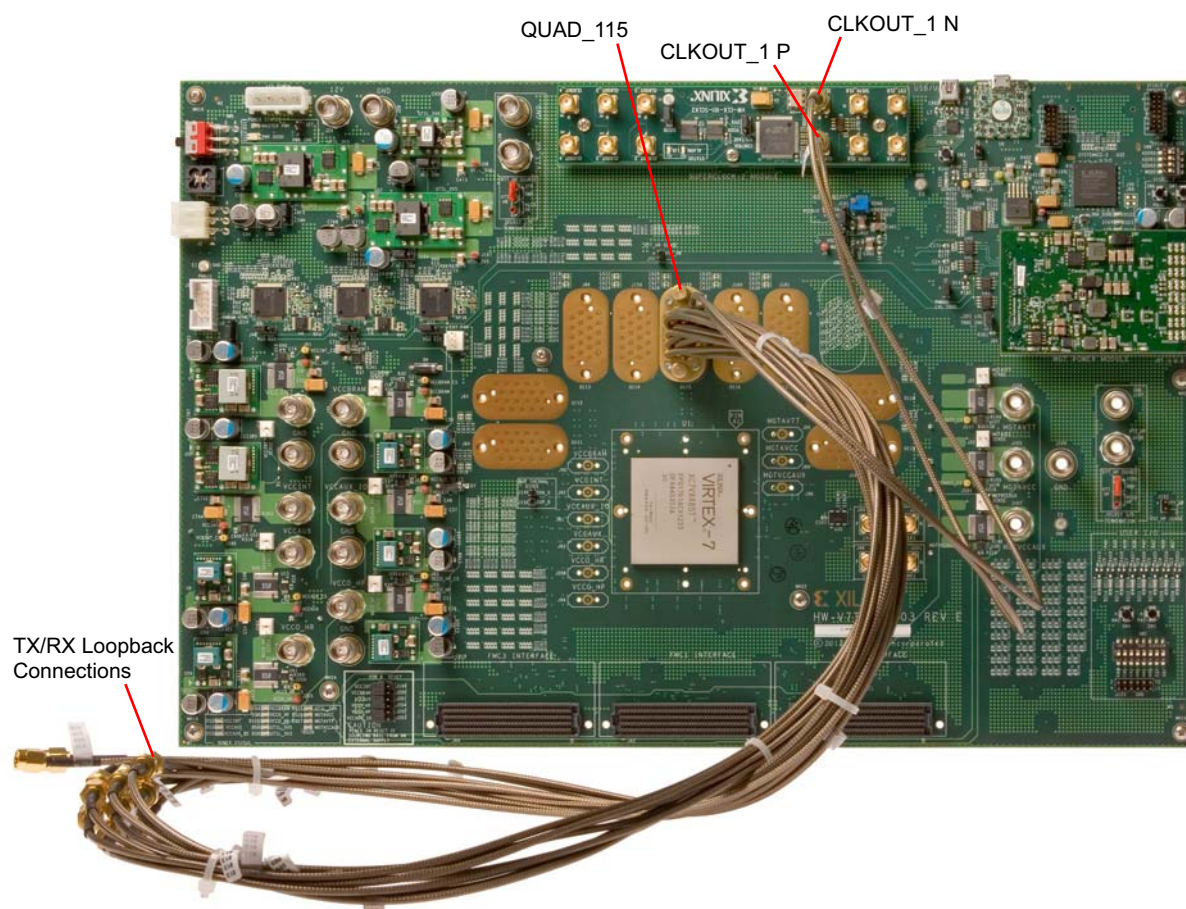
Figure 1-6: SMA F-F Adapter



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Figure 1-7: TX-To-RX Loopback Connection Example

Figure 1-8 shows the VC7203 board with the cable connections required for the Quad 115 GTX IBERT demonstration.



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Figure 1-8: Cable Connections for Quad 115 GTX IBERT Demonstration

Configuring the FPGA

This section describes how to configure the FPGA using the SD card included with the board. The FPGA can also be configured through the Vivado Design Suite software using the .bit files and .ltx probe files which are available online (as collection rdf0272-vc7203-ibert-2013-3.zip) at the [Virtex-7 FPGA VC7203 Characterization Kit documentation website](#).

To configure from the SD card:

1. Insert the SD card provided with the VC7203 board into the SD card reader slot located on the bottom-side (upper-right corner) of the VC7203 board.
2. Plug the 12V output from the power adapter into connector J2 on the VC7203 board.
3. Connect the host computer to the VC7203 board using a standard-A plug to Micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the Micro-B plug connects to U8, the Digilent USB JTAG configuration port on the VC7203 board.
4. Select the GTX IBERT demonstration with the System ACE™ SD controller SYSACE-2 CFG switch, SW8. The setting on this 4-bit DIP switch ([Figure 1-9](#)) selects the file used to configure the FPGA. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. For the Quad 115 GTX IBERT demonstration, set ADR2 = ON, ADR1 = OFF, and ADR0 = ON. The MODE bit (switch position 4) is not used and can be set either ON or OFF.
5. Place the main power switch SW1 to the ON position.



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Figure 1-9: Configuration Address DIP Switch (SW8)

There is one IBERT demonstration design for each GTX Quad on the VC7203 board, for a total of seven IBERT designs. An additional design is provided to demonstrate the USB/UART interface (details of this demonstration are described in the README file on the SD card). All eight designs are organized and stored on the SD card as shown in [Table 1-1](#).

Table 1-1: SD Card Contents and Configuration Addresses

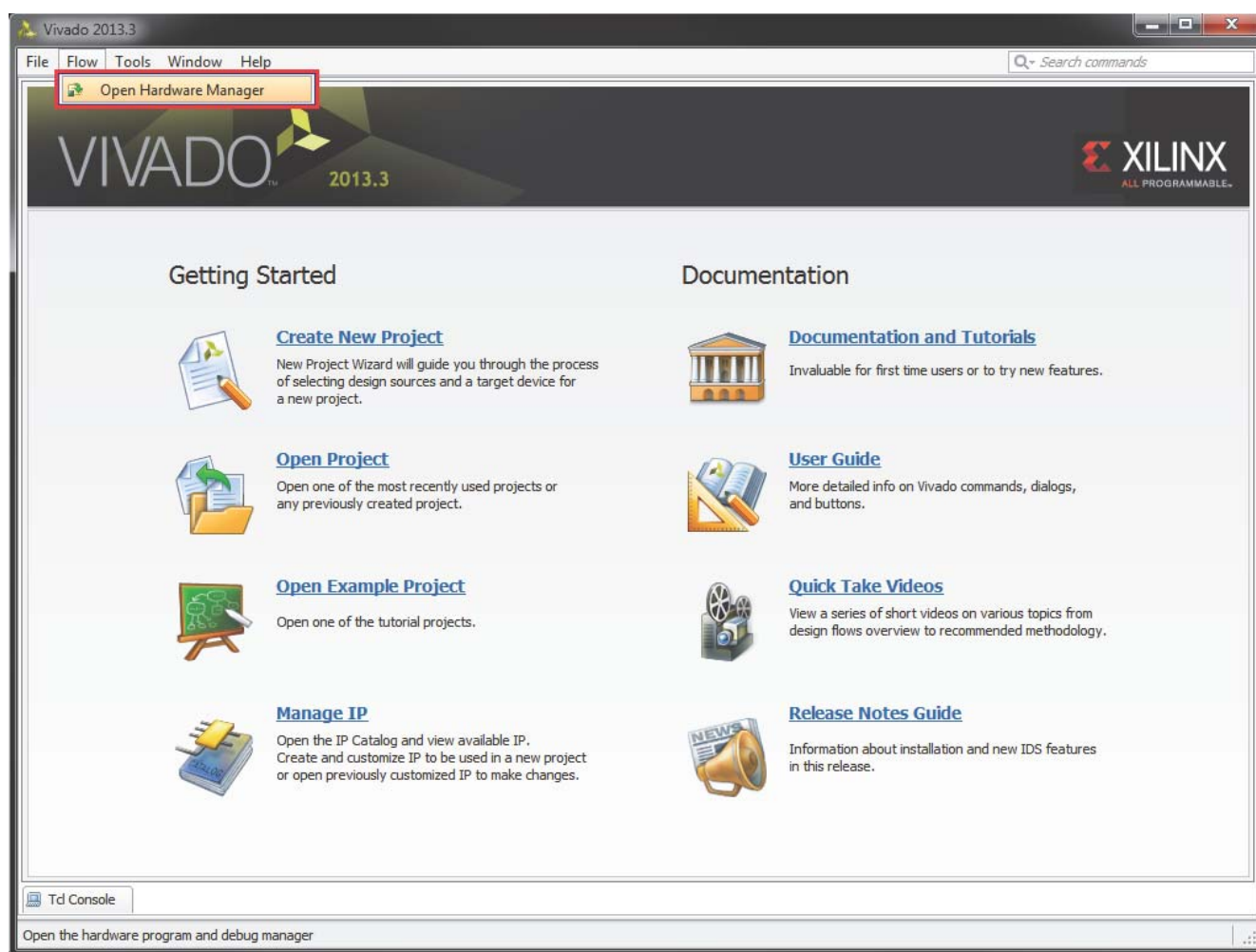
| Demonstration Design | ADR2 | ADR1 | ADR0 |
|----------------------|------|------|------|
| GTX Quad 113 | ON | ON | ON |
| GTX Quad 114 | ON | ON | OFF |
| GTX Quad 115 | ON | OFF | ON |
| GTX Quad 116 | ON | OFF | OFF |
| GTX Quad 117 | OFF | ON | ON |
| GTX Quad 118 | OFF | ON | OFF |

Table 1-1: SD Card Contents and Configuration Addresses (Cont'd)

| Demonstration Design | ADR2 | ADR1 | ADR0 |
|----------------------|------|------|------|
| GTX Quad 119 | OFF | OFF | ON |
| USB/UART | OFF | OFF | OFF |

Launching the Vivado Design Suite Software

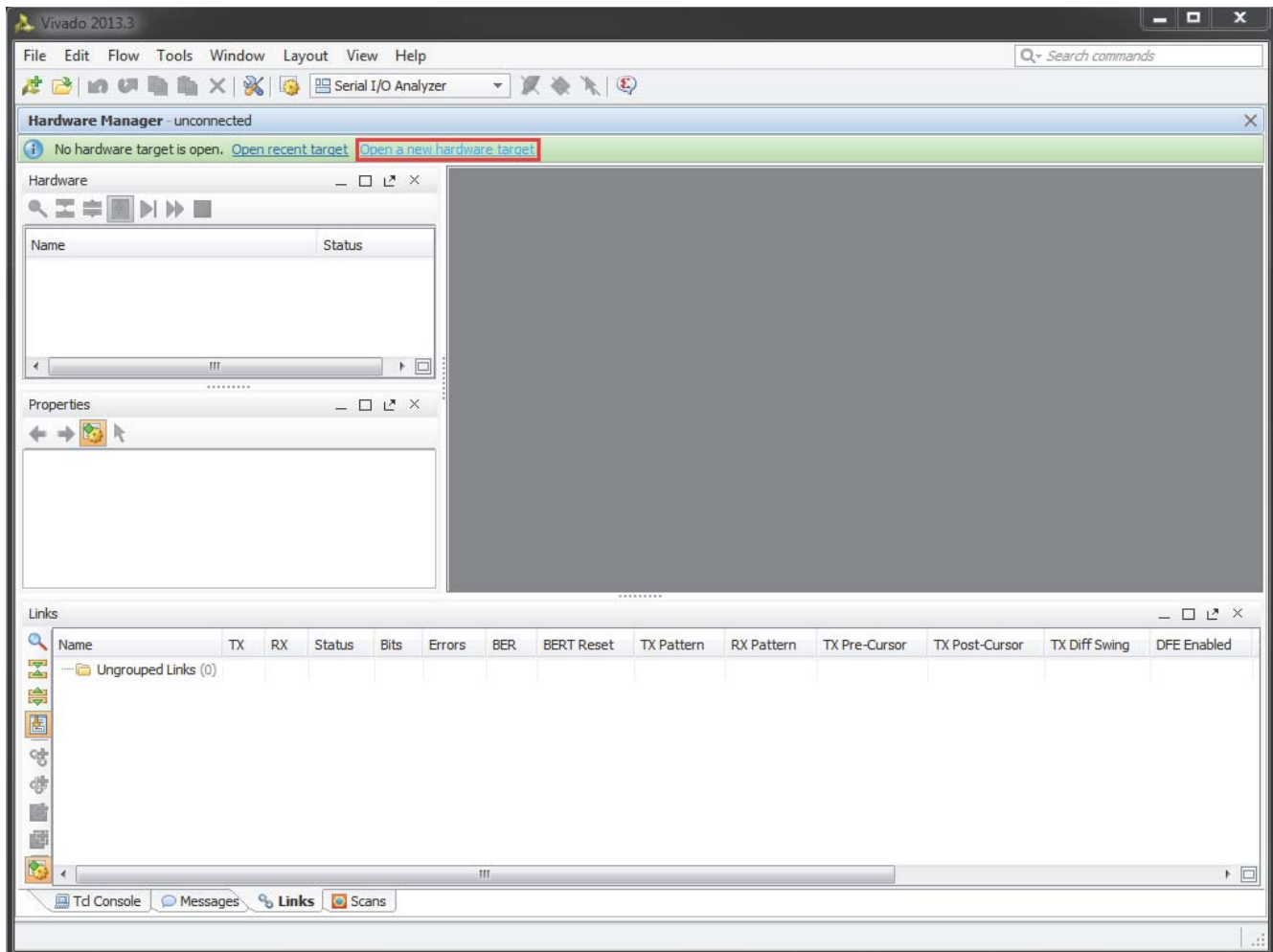
1. Start Vivado Design Suite on the host computer and click **Flow > Open Hardware Manager** (highlighted in Figure 1-10).



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Figure 1-10: Vivado Design Suite, Open Hardware Manager

2. In the Hardware Manager window, click **Open a new hardware target** (highlighted in Figure 1-11).

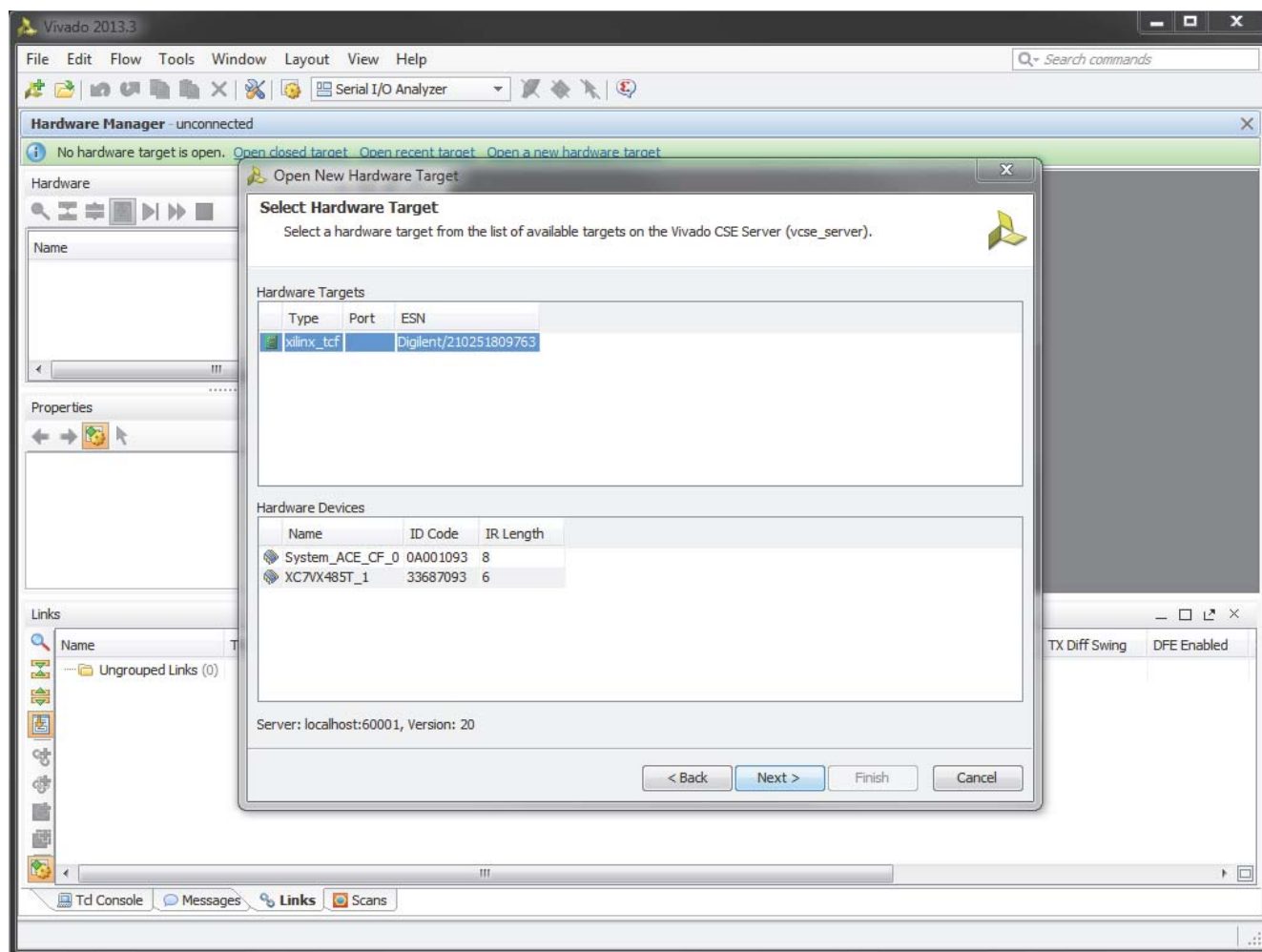


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Figure 1-11: Open a New Hardware Target

3. An Open Hardware Target wizard pops up. Click **Next** on the first window.
4. In the Vivado CSE Server Name window, make sure **localhost:60001** is entered for the Server name. Click **Next** and it opens the server to connect to the Xilinx TCF agent.

5. In the Select Hardware Target window, the **xilinx_tcf** cable appears under Type. The JTAG chain contents of the selected cable appears under the Hardware Devices window (Figure 1-12). Select **xilinx_tcf** and click **Next**.



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Figure 1-12: Select Hardware Target

6. In the Set Hardware Target Properties window, leave the defaults and click **Next**. In the Open Hardware Target Summary window, click **Finish**. The wizard closes and the Vivado tool opens the hardware target.

Starting the SuperClock-2 Module

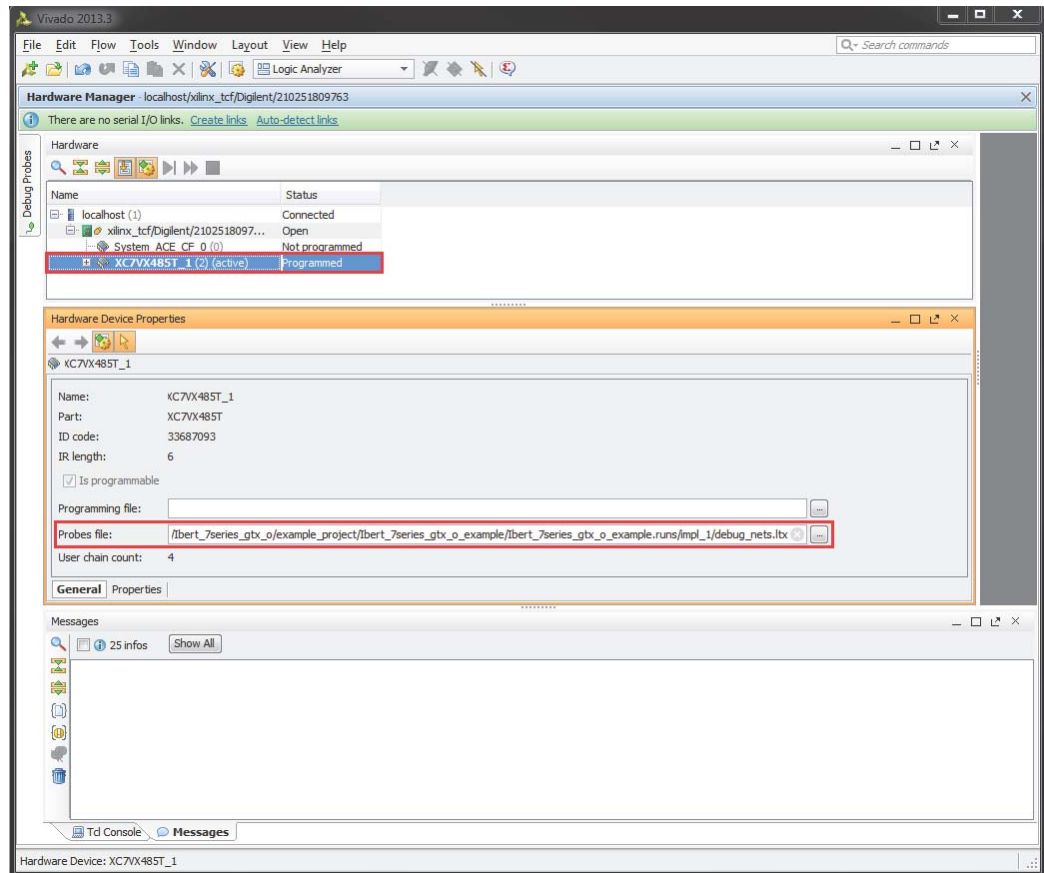
The IBERT demonstration designs use an integrated VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components:

- 1) An always-on Si570 crystal oscillator and,
- 2) an Si5368 jitter-attenuating clock multiplier.

Outputs from either device can be used to drive the transceiver reference clocks.

To start the SuperClock-2 module:

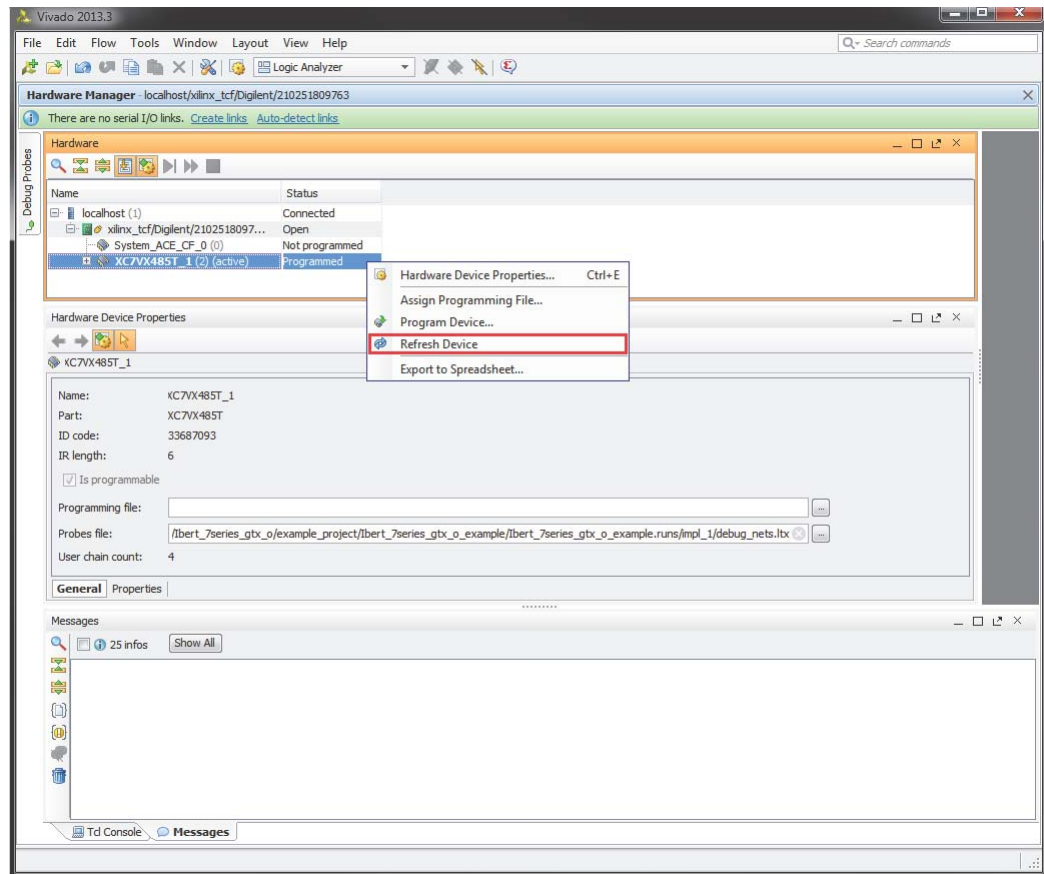
1. The Hardware window shows the System ACE and the XC7VX485T device and reports that it is programmed. Select **XC7VX485T_1**. In the Hardware Device Properties window, enter the file path to the Probes file associated with the Q115 IBERT design (vc7203_q115.1tx) (Figure 1-13).



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Figure 1-13: Adding the Probes File

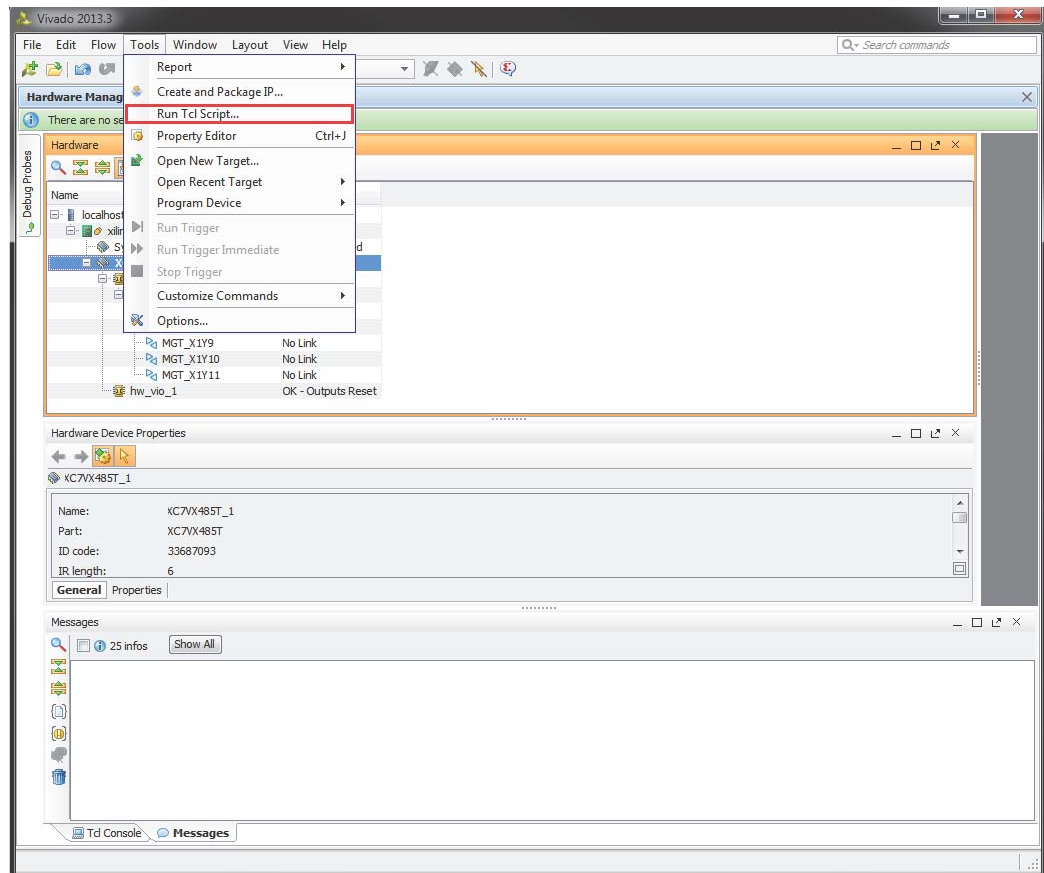
2. In the Hardware window, right-click **XC7VX485T_1** and select **Refresh Device** (Figure 1-14).



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Figure 1-14: Refresh Device

- The Vivado tool now shows the SuperClock-2 VIO core and the IBERT core. To configure the SuperClock-2 module, select **Tools > Run Tcl Script** (Figure 1-15). In the following Run Script window, navigate to the `setup_scm2_156_25.tcl` script in the extracted files and click **OK**.



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Figure 1-15: Run Tcl Script...

- To view the SuperClock 2 settings in the VIO core, select the following signals:
u_scm2/u_vio_sclk2_control/si570_start
u_scm2/u_vio_sclk2_control/si570_addr[6:0]
u_scm2/u_vio_sclk2_control/si5368_start
u_scm2/u_vio_sclk2_control/si5368_addr[6:0]

Drag these signals from the Debug Probes window to the VIO Probes window (Figure 1-16).

Note: The ROM address values for the Si5368 and Si570 devices (that is, si5368_addr[6:0] and si570_addr[6:0]) are preset to 60 to produce an output frequency of 156.250 MHz. Entering a different ROM address changes the reference clock(s) frequency. The complete list of pre-programmed SuperClock-2 frequencies and their associated ROM addresses is provided in Table 1-2, page 24.

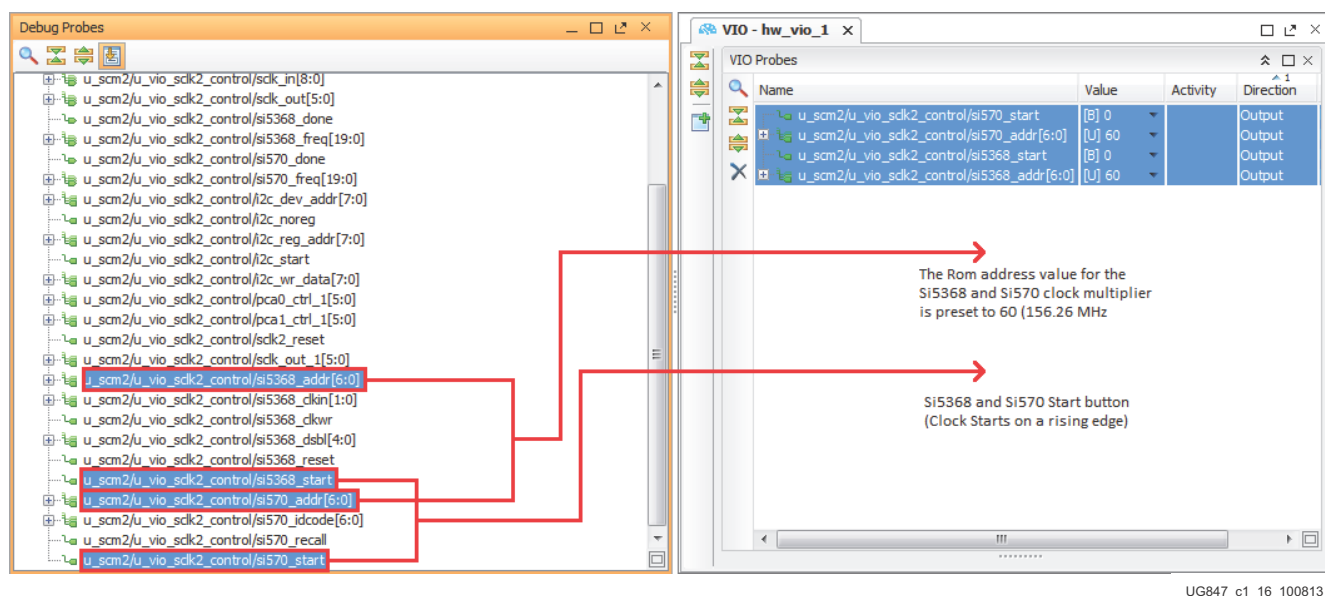
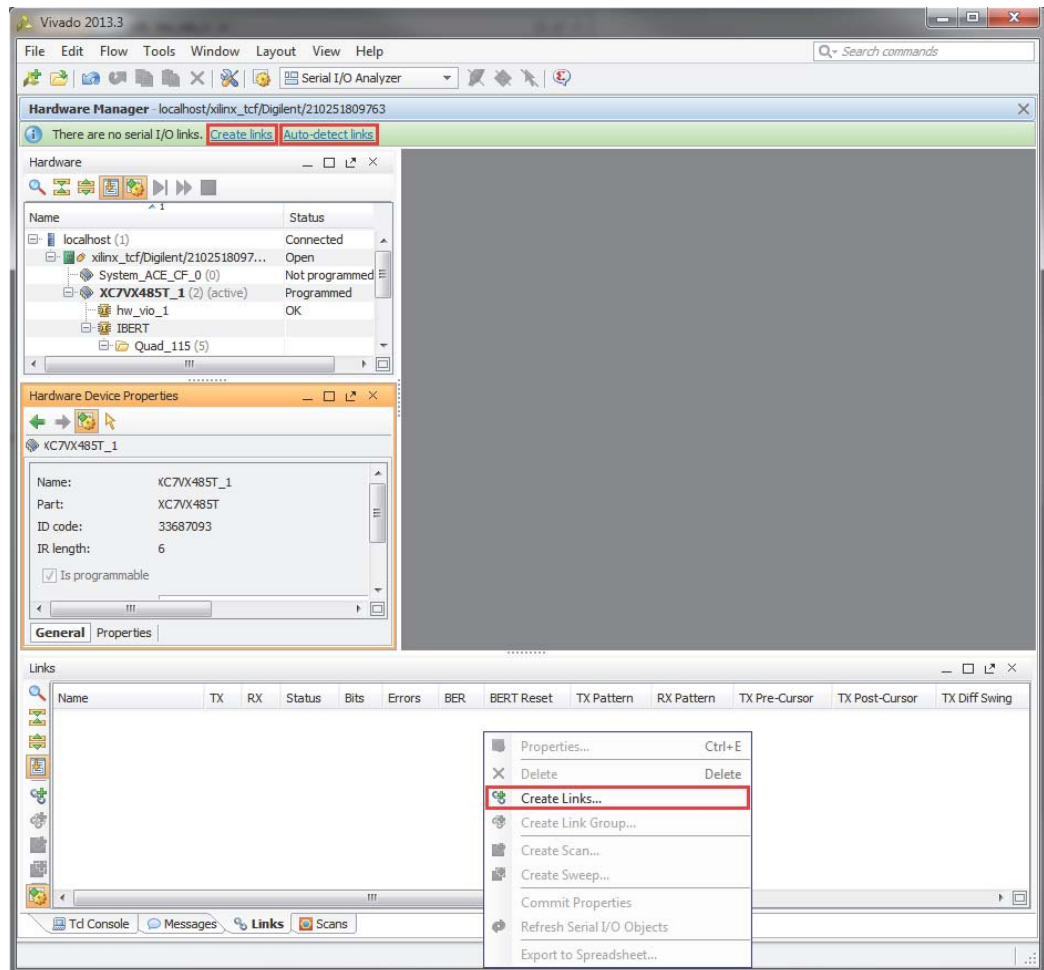


Figure 1-16: SuperClock-2 Module VIO Core

- To view the GTX transceiver operation, click Layout > Serial I/O Analyzer. In the Links window, right-click and select **Create Links...** or press the **Create Links** button. The **Auto-detect links** button can also be used to have the tools automatically scan for any links that are connected and currently linked (Figure 1-17).

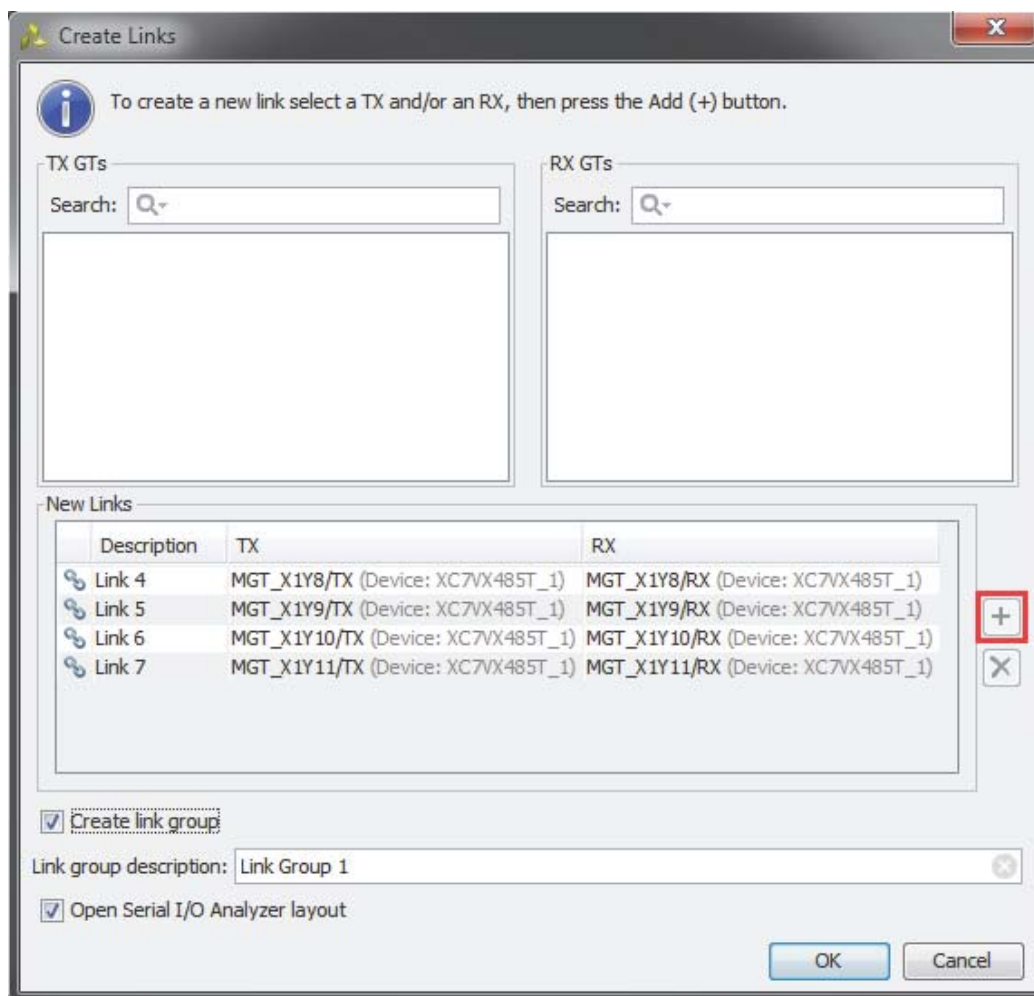


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Figure 1-17: Serial I/O Analyzer - Create Links...

- If **Create Links** was selected, a pop up window displays. In this window you can link any TX to RX GT transceivers. To create links, select the **TX GT** and **RX GT** from the two lists, then press the **Add (+)** button. For this project, connect the following links:
MGT_X1Y8/TX to MGT_X1Y8/RX
MGT_X1Y9/TX to MGT_X1Y9/RX
MGT_X1Y10/TX to MGT_X1Y10/RX
MGT_X1Y11/TX to MGT_X1Y11/RX

This is shown in [Figure 1-18](#).



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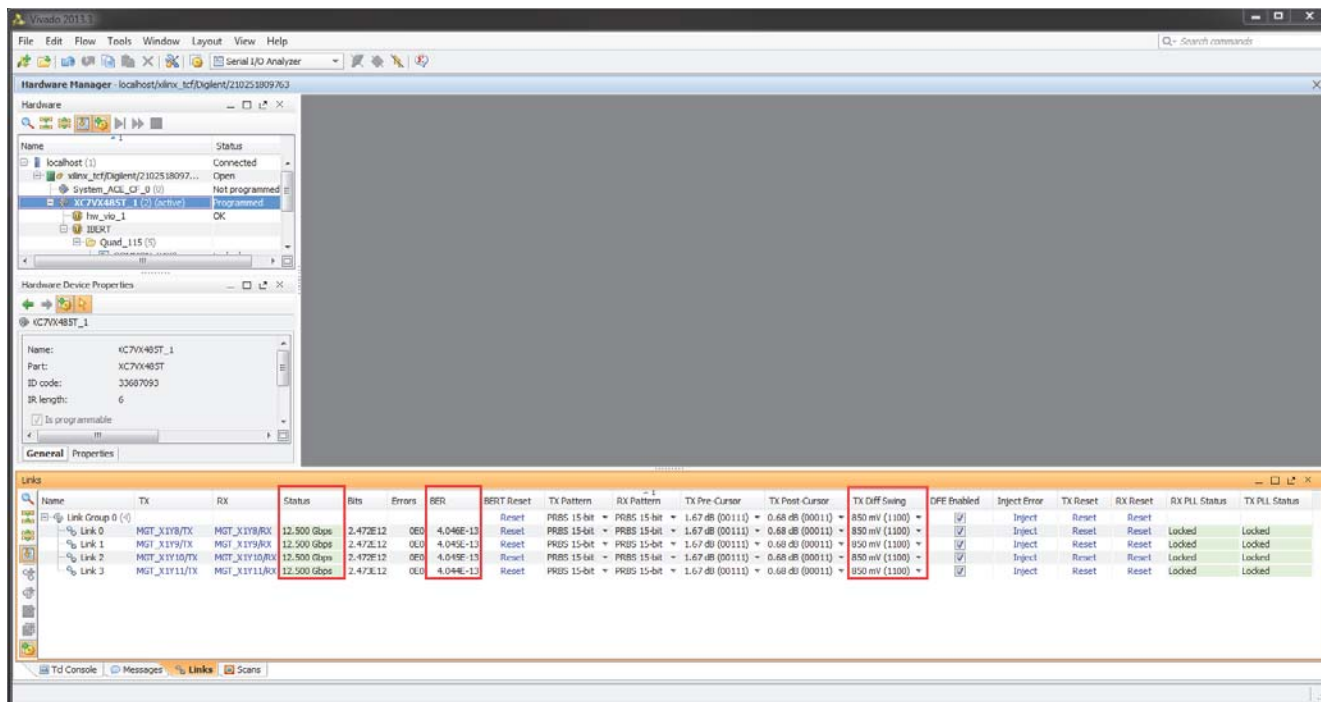
Figure 1-18: Create Links Window

Viewing GTX Transceiver Operation

After completing [step 6](#) in [Starting the SuperClock-2 Module](#), the IBERT demonstration is configured and running. The status and test settings are displayed on the Links tab in the Links window shown in [Figure 1-19](#).

Note the line rate, TX differential output swing, and error count:

- The line rate for all four GTX transceivers is 12.5 Gb/s (see **Status** in [Figure 1-19](#)).
- The GTX transmitter differential output swing is preset to 850 mV.
- Verify that there are no bit errors.



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Figure 1-19: Serial I/O Analyzer Links

Additional information on the Vivado Design Suite software and IBERT core can be found in *Vivado Design Suite User Guide: Programming and Debugging* (UG908) and *LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers Product Guide for Vivado Design Suite* (PG132).

Closing the IBERT Demonstration

To stop the IBERT demonstration:

1. Close the Vivado Design Suite application by selecting **File > Exit**.
2. Place the main power switch SW1 in the off position.

SuperClock-2 Frequency Table

Table 1-2 lists the addresses for the frequencies that are programmed into the SuperClock-2 read-only-memory (ROM).

Table 1-2: Si570 and Si5368 Frequency Table

| Address | Protocol | Frequency (MHz) | Address | Protocol | Frequency (MHz) | Address | Protocol | Frequency (MHz) |
|---------|-----------------|-----------------|---------|-----------|-----------------|---------|----------|-----------------|
| 0 | 100GE/40GE/10GE | 161.130 | 30 | OBSAI | 307.200 | 60 | XAUI | 156.250 |
| 1 | Aurora | 81.250 | 31 | OBSAI | 614.400 | 61 | XAUI | 312.500 |
| 2 | Aurora | 162.500 | 32 | OC-48 | 19.440 | 62 | XAUI | 625.000 |
| 3 | Aurora | 325.000 | 33 | OC-48 | 77.760 | 63 | Generic | 66.667 |
| 4 | Aurora | 650.000 | 34 | OC-48 | 155.520 | 64 | Generic | 133.333 |
| 5 | CE111 | 173.370 | 35 | OC-48 | 311.040 | 65 | Generic | 166.667 |
| 6 | CPRI | 61.440 | 36 | OC-48 | 622.080 | 66 | Generic | 266.667 |
| 7 | CPRI | 122.880 | 37 | OTU-1 | 166.629 | 67 | Generic | 333.333 |
| 8 | CPRI | 153.630 | 38 | OTU-1 | 333.257 | 68 | Generic | 533.333 |
| 9 | CPRI | 245.760 | 39 | OTU-1 | 666.514 | 69 | Generic | 644.000 |
| 10 | CPRI | 491.520 | 40 | OTU-1 | 666.750 | 70 | Generic | 666.667 |
| 11 | Display Port | 67.500 | 41 | OTU-2 | 167.330 | 71 | Generic | 205.000 |
| 12 | Display Port | 81.000 | 42 | OTU-2 | 669.310 | 72 | Generic | 210.000 |
| 13 | Display Port | 135.000 | 43 | OTU-3 | 168.050 | 73 | Generic | 215.000 |
| 14 | Display Port | 162.000 | 44 | OTU-4 | 174.690 | 74 | Generic | 220.000 |
| 15 | Fibrechannel | 106.250 | 45 | PCIe | 100.000 | 75 | Generic | 225.000 |
| 16 | Fibrechannel | 212.500 | 46 | PCIe | 125.000 | 76 | Generic | 230.000 |
| 17 | Fibrechannel | 425.000 | 47 | PCIe | 250.000 | 77 | Generic | 235.000 |
| 18 | GigE | 62.500 | 48 | SATA | 75.000 | 78 | Generic | 240.000 |
| 19 | GigE | 125.000 | 49 | SATA | 150.000 | 79 | Generic | 245.000 |
| 20 | GigE | 250.000 | 50 | SATA | 300.000 | 80 | Generic | 250.000 |
| 21 | GigE | 500.000 | 51 | SATA | 600.000 | 81 | Generic | 255.000 |
| 22 | GPON | 187.500 | 52 | SDI | 74.250 | 82 | Generic | 260.000 |
| 23 | Interlaken | 132.813 | 53 | SDI | 148.500 | 83 | Generic | 265.000 |
| 24 | Interlaken | 195.313 | 54 | SDI | 297.000 | 84 | Generic | 270.000 |
| 25 | Interlaken | 265.625 | 55 | SDI | 594.000 | 85 | Generic | 275.000 |
| 26 | Interlaken | 390.625 | 56 | SMPTE435M | 167.063 | 86 | Generic | 280.000 |
| 27 | Interlaken | 531.250 | 57 | SMPTE435M | 334.125 | 87 | Generic | 285.000 |
| 28 | OBSAI | 76.800 | 58 | SMPTE435M | 668.250 | 88 | Generic | 290.000 |
| 29 | OBSAI | 153.600 | 59 | XAUI | 78.125 | 89 | Generic | 295.000 |
| 90 | Generic | 300.000 | 103 | Generic | 365.000 | 116 | Generic | 430.000 |
| 91 | Generic | 305.000 | 104 | Generic | 370.000 | 117 | Generic | 435.000 |

Table 1-2: Si570 and Si5368 Frequency Table (Cont'd)

| Address | Protocol | Frequency (MHz) | Address | Protocol | Frequency (MHz) | Address | Protocol | Frequency (MHz) |
|---------|----------|-----------------|---------|----------|-----------------|---------|----------|-----------------|
| 92 | Generic | 310.000 | 105 | Generic | 375.000 | 118 | Generic | 440.000 |
| 93 | Generic | 315.000 | 106 | Generic | 380.000 | 119 | Generic | 445.000 |
| 94 | Generic | 320.000 | 107 | Generic | 385.000 | 120 | Generic | 450.000 |
| 95 | Generic | 325.000 | 108 | Generic | 390.000 | 121 | Generic | 455.000 |
| 96 | Generic | 330.000 | 109 | Generic | 395.000 | 122 | Generic | 460.000 |
| 97 | Generic | 335.000 | 110 | Generic | 400.000 | 123 | Generic | 465.000 |
| 98 | Generic | 340.000 | 111 | Generic | 405.000 | 124 | Generic | 470.000 |
| 99 | Generic | 345.000 | 112 | Generic | 410.000 | 125 | Generic | 475.000 |
| 100 | Generic | 350.000 | 113 | Generic | 415.000 | 126 | Generic | 480.000 |
| 101 | Generic | 355.000 | 114 | Generic | 420.000 | 127 | Generic | 485.000 |
| 102 | Generic | 360.000 | 115 | Generic | 425.000 | | | |

Creating the GTX IBERT Core

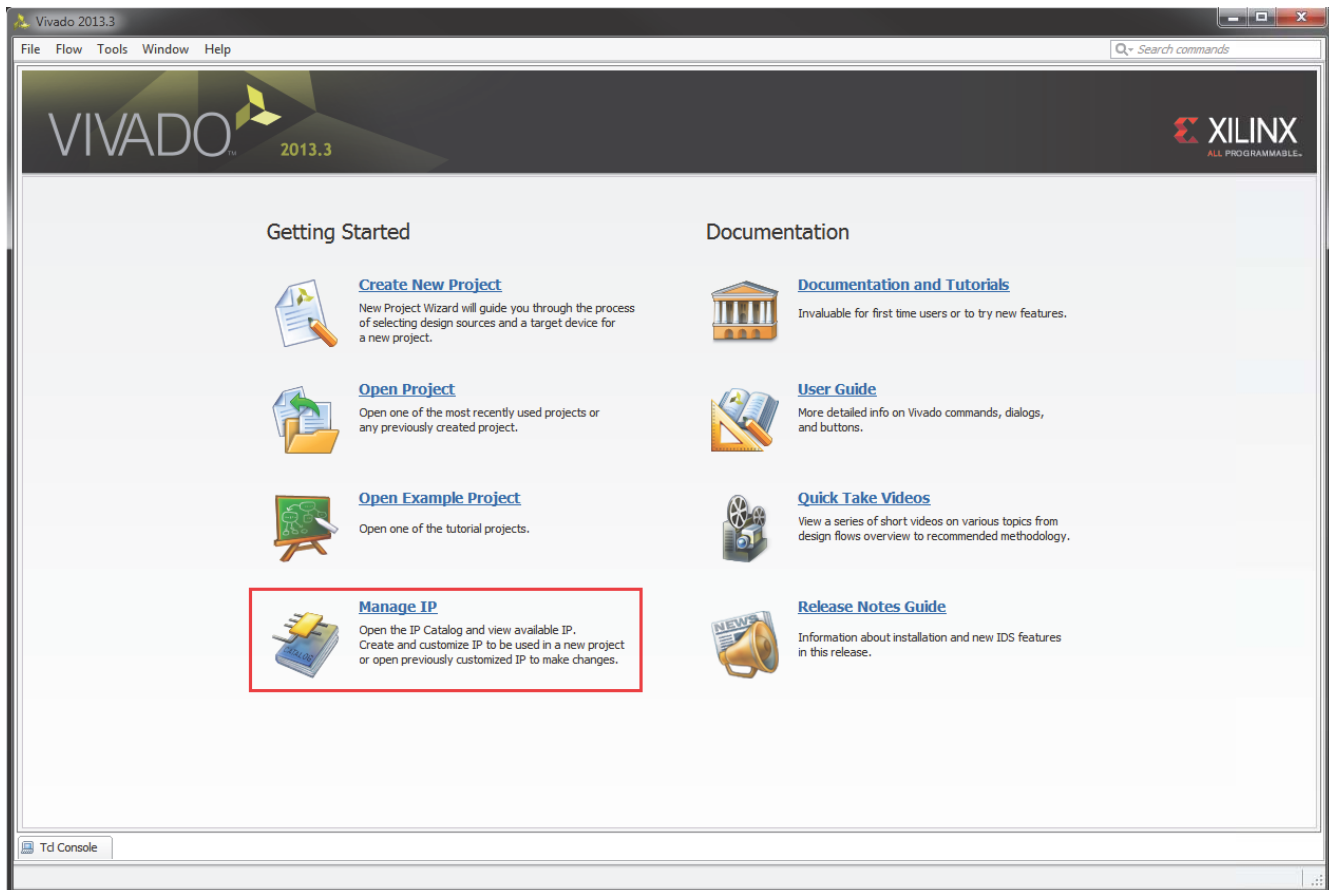
Vivado Design Suite version 2013.3 is required to rebuild the designs shown here.

This section provides a procedure to create a single Quad GTX IBERT core with integrated SuperClock-2 controller. The procedure assumes Quad 113 and 12.5 Gb/s line rate, but cores for any of the GTX Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, refer to *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

1. Start the Vivado Design Suite.

2. In the Vivado design tools window, click the **Manage IP** icon (highlighted in [Figure 1-20](#)), then select **Open IP Catalog**.

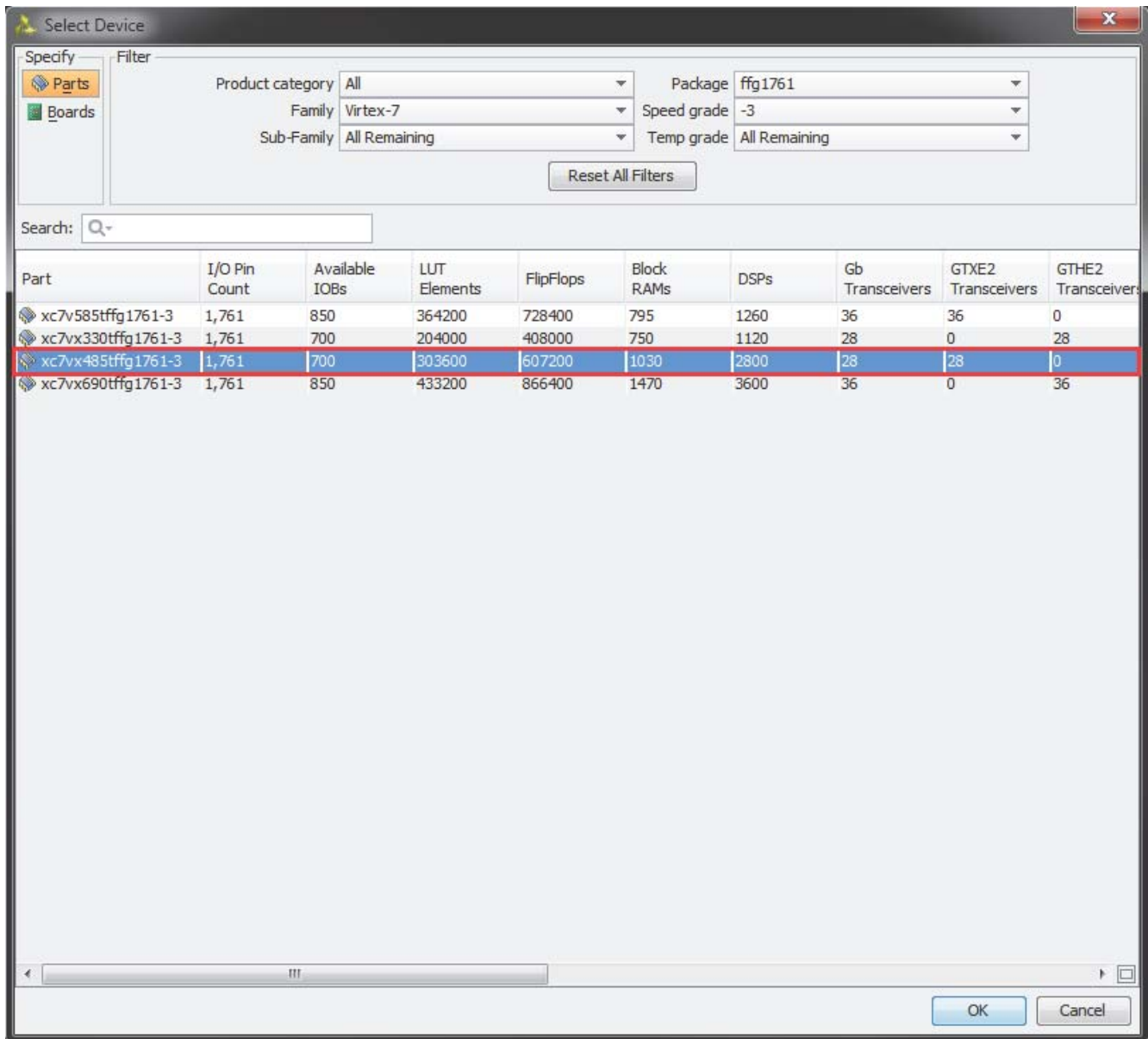


UG847_c1_20_100813

Figure 1-20: Initial Window, Vivado Design Suite

3. When the Create a New Customized IP Location dialog window opens (not shown), click **Next**.

- In the Manage IP Settings window, select a part by clicking the (...) button next to the Part field. A Select Device window pops up. Use the drop-down menu items to narrow the choices. Select the **xc7vx485tffg1761-3** device (Figure 1-21). Click **OK**.

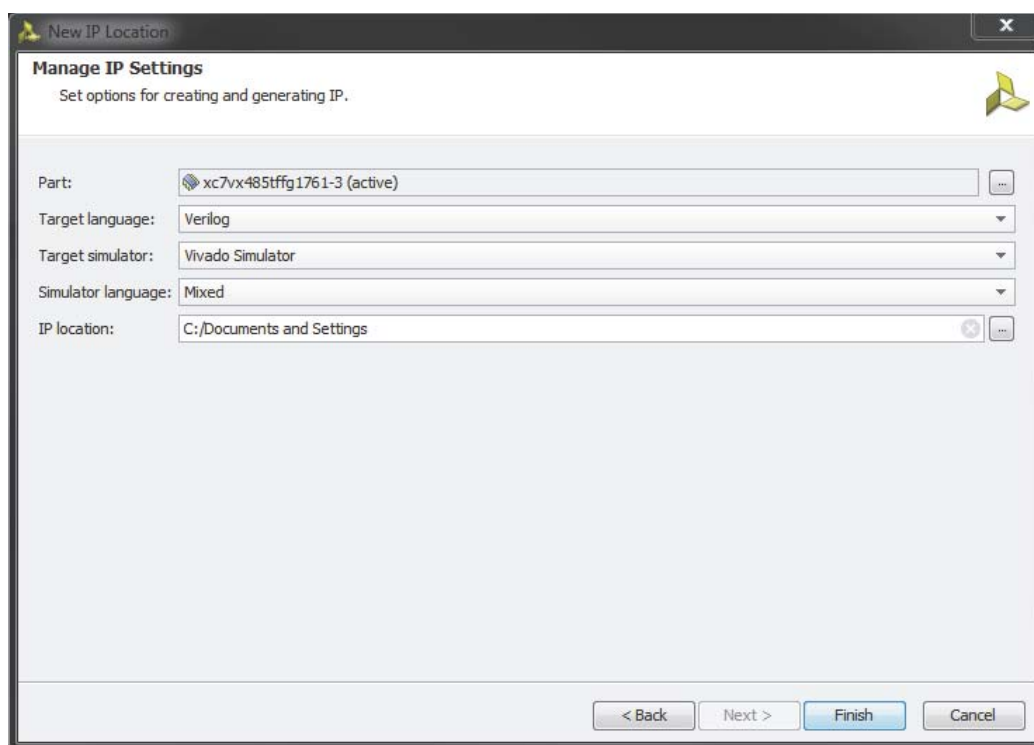


UG847_c1_21_100813

Figure 1-21: Select Device

- Back on the Manage IP Settings window, select **Verilog** for Target language, **Vivado Simulator** for Target simulator, **Mixed** for Simulator language, and a directory to save

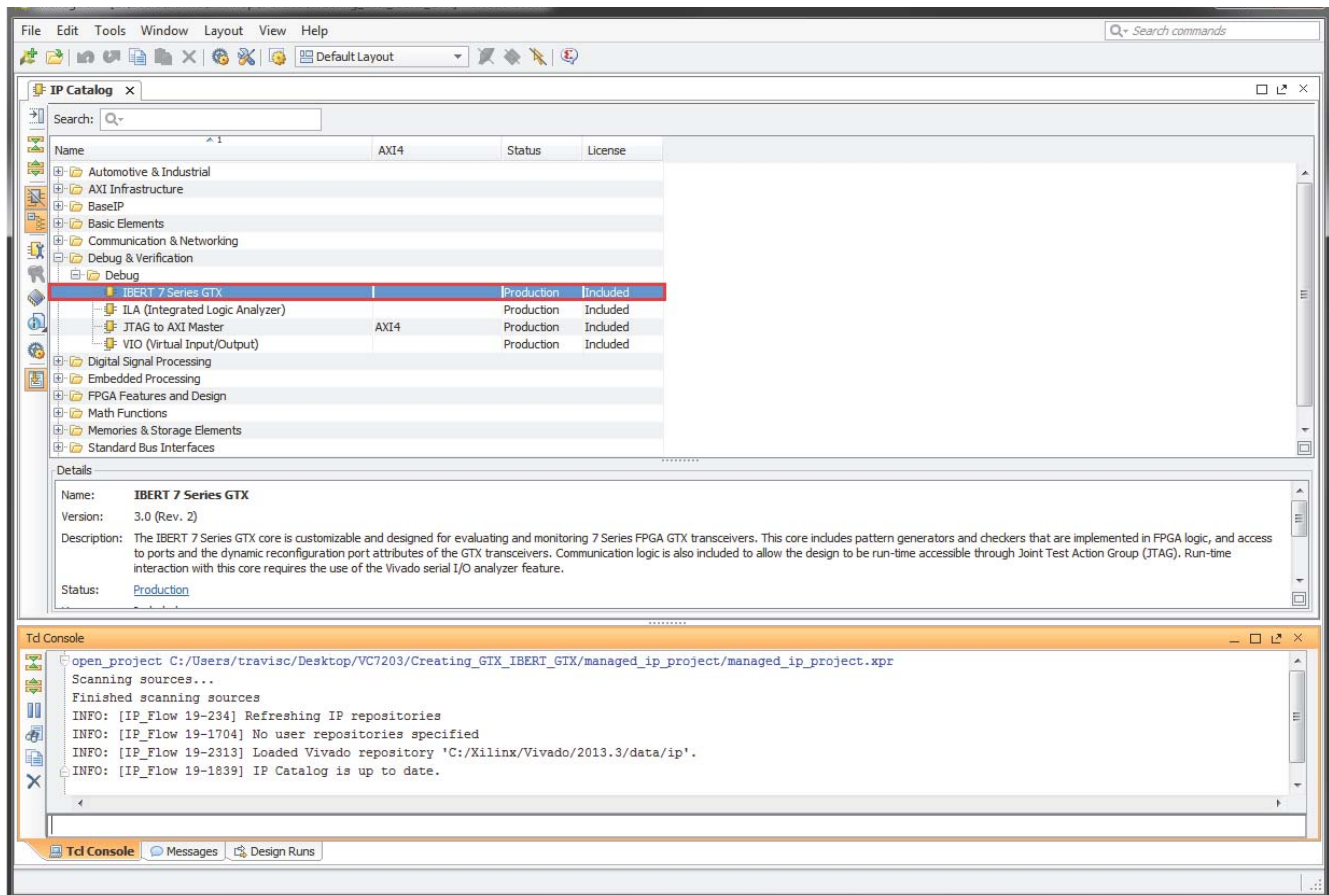
the customized IP (Figure 1-22). Click **Finish**.



UG847_c1_22_100813

Figure 1-22: Manage IP Settings

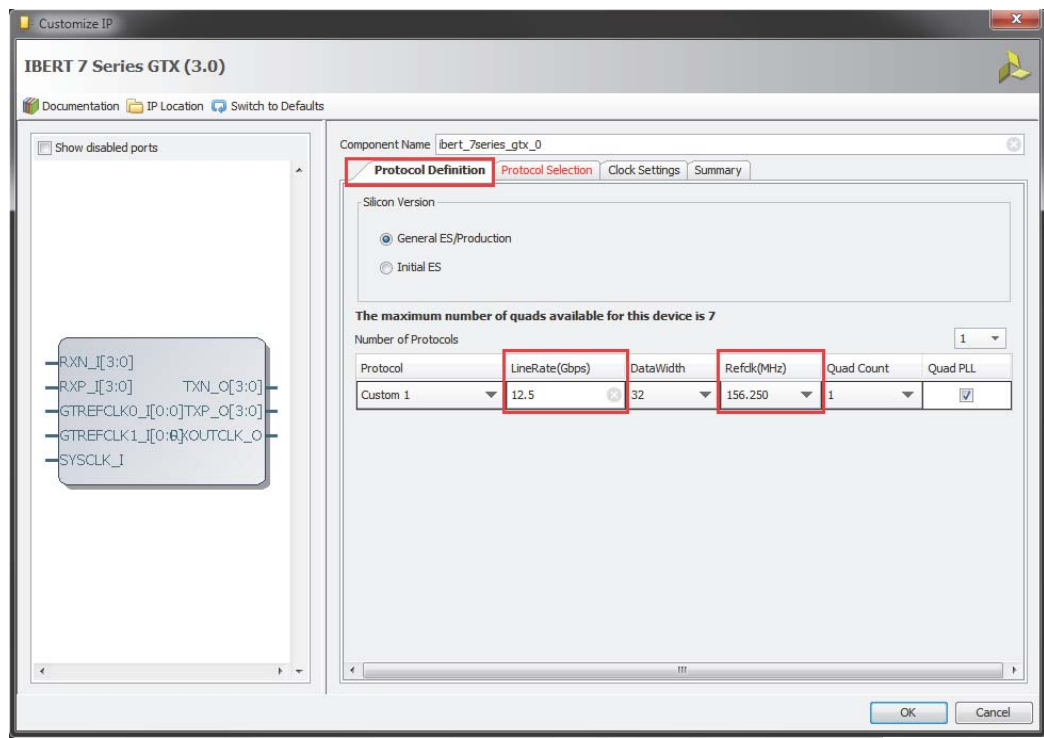
6. In the Vivado IP Catalog window, open the **Debug & Verification** folder, then open the **Debug** folder, and double-click **IBERT 7 Series GTX** (Figure 1-23).



UG847_c1_23_100813

Figure 1-23: IP Catalog

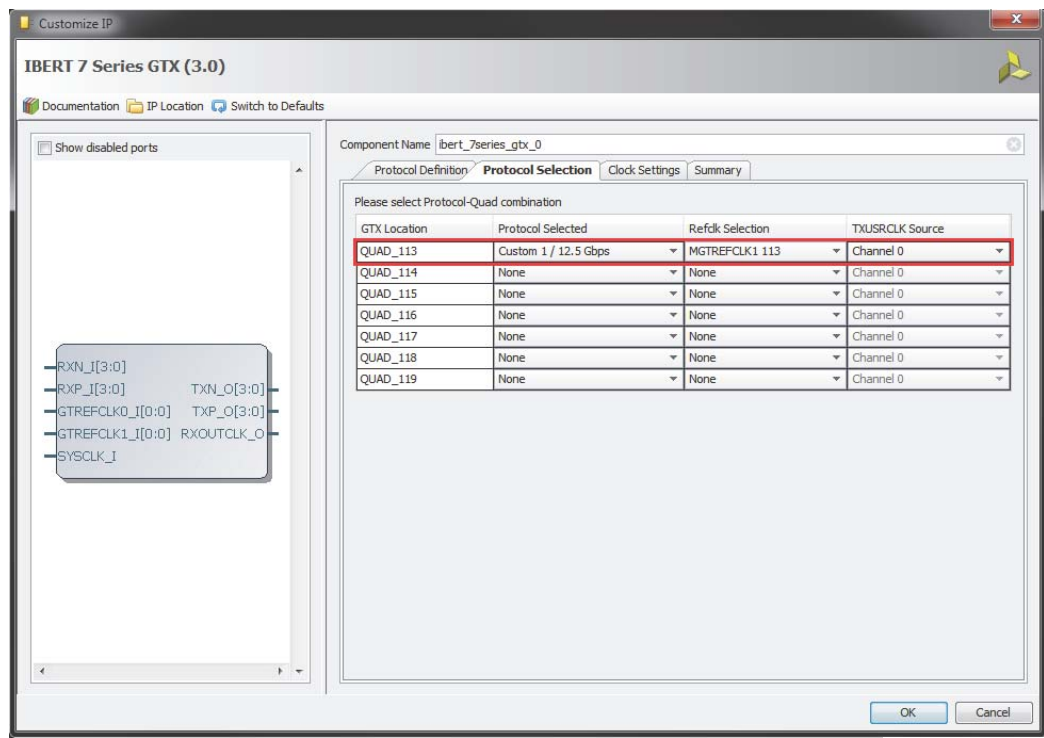
7. A Customize IP window opens. In the Protocol Definition tab, change **LineRate (Gbps)** to **12.5**, then use the drop-down to change the **Refclk (MHz)** to **156.250**. Do not change the other defaults (Figure 1-24).



UG847_c1_24_100813

Figure 1-24: Customize IP - Protocol Definition

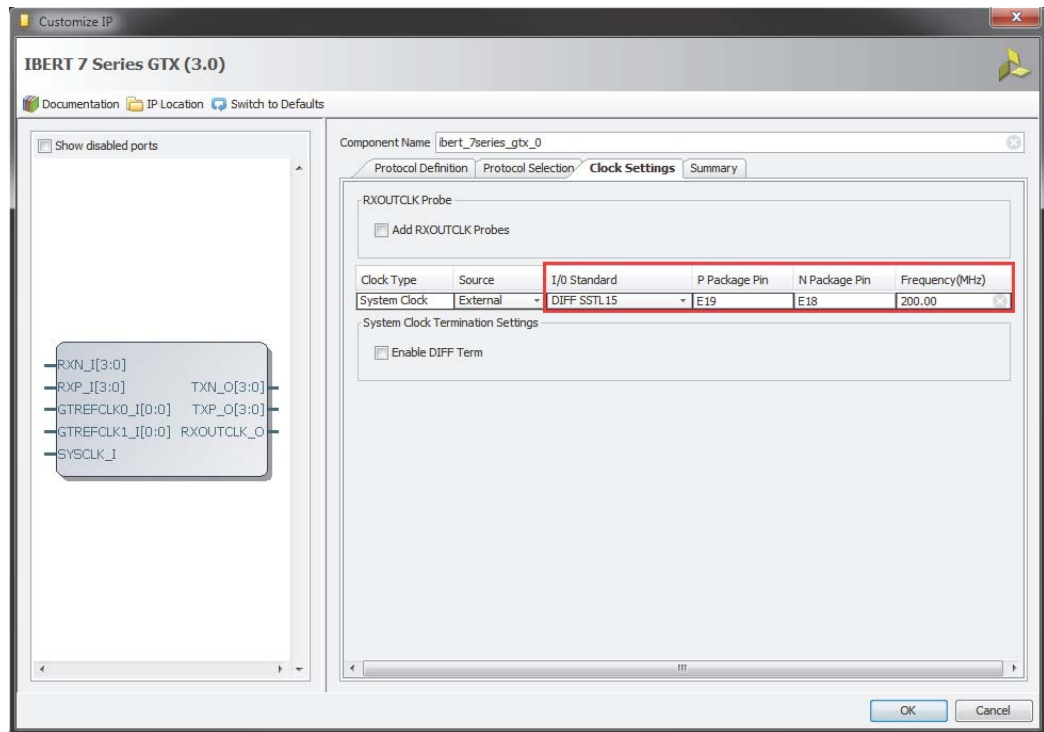
8. In the Protocol Selection tab, select **Custom 1 / 12.5 Gbps** in the drop-down menu under Protocol Selected next to **QUAD_113**, and select **MGTREFCLK1 113** in the Refclk Selection drop-down menu (Figure 1-25).



UG847_c1_25_100813

Figure 1-25: Customize IP - Protocol Selection

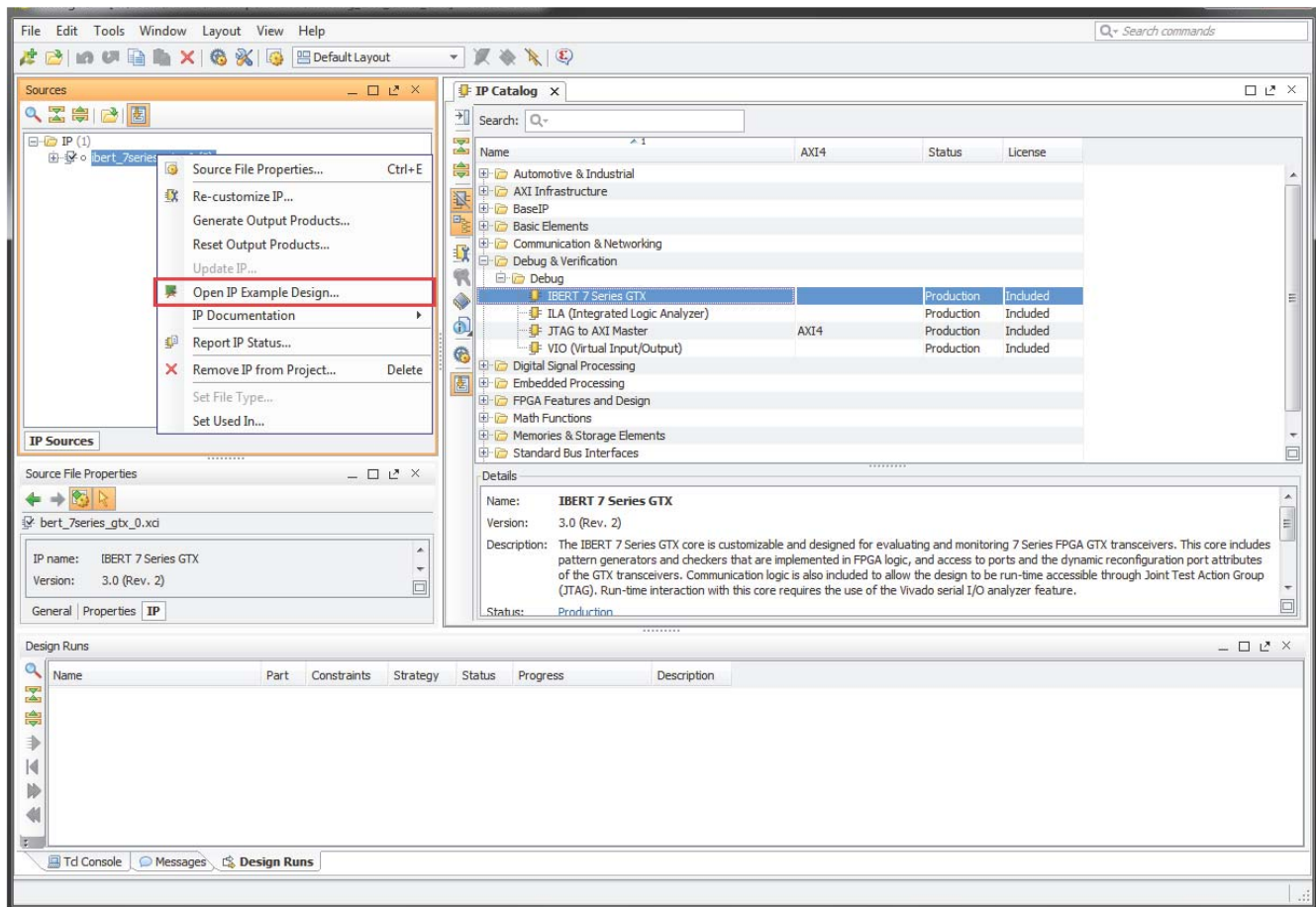
9. In the Clock Settings tab, select **DIFF SSTL15** for the I/O Standard, enter **E19** for P Package Pin and **E18** for N Package Pin (the FPGA pins that the system clock connects to), and make sure the Frequency is set to **200.00** (Figure 1-26). Press **OK**. A Generate Output Products window opens. Leave the defaults unchanged, and press **Generate**.



UG847_c1_26_100813

Figure 1-26: Customize IP - Clock Settings

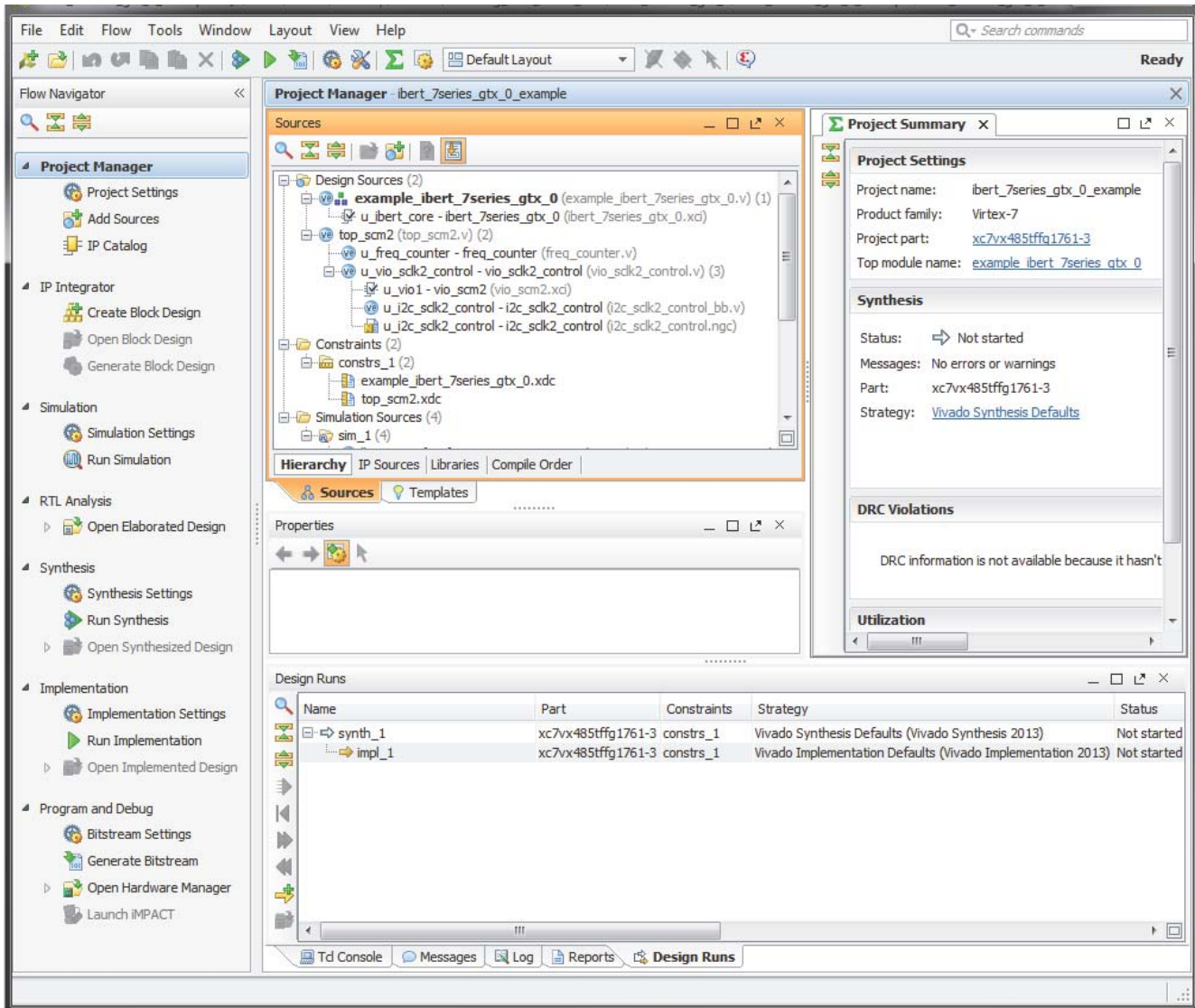
10. Back to Manage IP, in the Sources window, right-click the **IBERT IP** and select **Open IP Example Design** (Figure 1-27). Specify a location to save the design, press **OK**, and the design opens in a new Vivado design tools window.



UG847_c1_27_100813

Figure 1-27: Open IP Example Design

11. In the new window, select **Tools > Run Tcl Script**. In the Run Script window, navigate to `add_scm2.tcl` in the extracted files and press **OK**. The SuperClock-2 Module Design Sources and Constraints are automatically added to the example design (Figure 1-28).



UG847_c1_28_100813

Figure 1-28: Sources after Running `add_scm2.tcl`

12. The SuperClock-2 source code now needs to be added to the example ibert wrapper. Double-click **example_ibert_7series_gtx_0** in the Design Sources to open the verilog code. Add the top level ports from **top_scm2.v** to the module declaration and instantiate the **top_scm2** module in the example ibert wrapper (Figure 1-29). Click **File > Save File**.

```

example_ibert_7series_gtx_0.v
example_ibert_7series_gtx_0_example.srscs/sources_1/imports/example_design/example_ibert

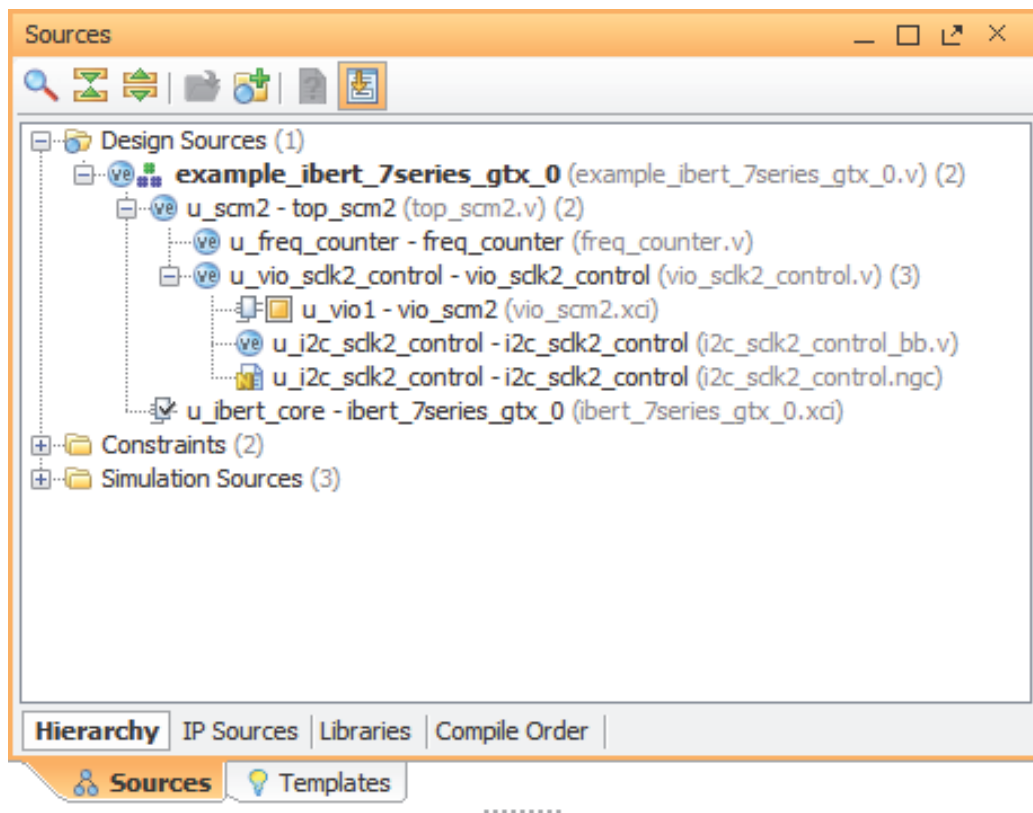
18
19 `define C_NUM_QUADS 1
20 `define C_REFCLKS_USED 1
21 module example_ibert_7series_gtx_0
22 (
23 // GT top level ports
24 output [(4*C_NUM_QUADS)-1:0] TXN_0,
25 output [(4*C_NUM_QUADS)-1:0] TXP_0,
26 input [(4*C_NUM_QUADS)-1:0] RXN_I,
27 input [(4*C_NUM_QUADS)-1:0] RXP_I,
28 input SYSCLKP_I,
29 input SYSCLKN_I,
30 input [C_REFCLKS_USED-1:0] GTREFCLKOP_I,
31 input [C_REFCLKS_USED-1:0] GTREFCLKON_I,
32 input [C_REFCLKS_USED-1:0] GTREFCLKIP_I,
33 input [C_REFCLKS_USED-1:0] GTREFCLKIN_I,
34 // SuperClock-2 Module top level ports
35 input [2:0] usrc1k_p,
36 input [2:0] usrc1k_n,
37 inout i2c_sda,
38 inout i2c_scl,
39 output [5:0] sclk_out,
40 input [8:0] sclk_in,
41 output [1:0] sclk_c1k_p,
42 output [1:0] sclk_c1k_n
43);
44
45 //
46 // Ibert refclk internal signals
47 //
48 wire [C_NUM_QUADS-1:0] gtrefclk0_i;
49 wire [C_NUM_QUADS-1:0] gtrefclk1_i;
50 wire [C_REFCLKS_USED-1:0] refclk0_i;
51 wire [C_REFCLKS_USED-1:0] refclk1_i;
52 wire sysclk_i;
53
54 //
55 // SuperClock-2 Module instantiations
56 //
57 top_scm2 u_scm2
58 (
59 .sysclk_i(sysclk_i),
60 .usrc1k_p(usrc1k_p),
61 .usrc1k_n(usrc1k_n),
62 .i2c_sda(i2c_sda),
63 .i2c_scl(i2c_scl),
64 .sclk_out(sclk_out),
65 .sclk_in(sclk_in),
66 .sclk_c1k_p(sclk_c1k_p),
67 .sclk_c1k_n(sclk_c1k_n)
68 );
69
70 //
71 // Refclk IBUFDS instantiations
72 //
73
74 IBUFDS_GTE2 u_buf_q9_c1k0

```

UG847_c1_29_102213

Figure 1-29: SuperClock-2 in the Example IBERT Wrapper

13. In the Sources window, Design Sources should now reflect that the SuperClock-2 module is part of the example IBERT design (Figure 1-30).

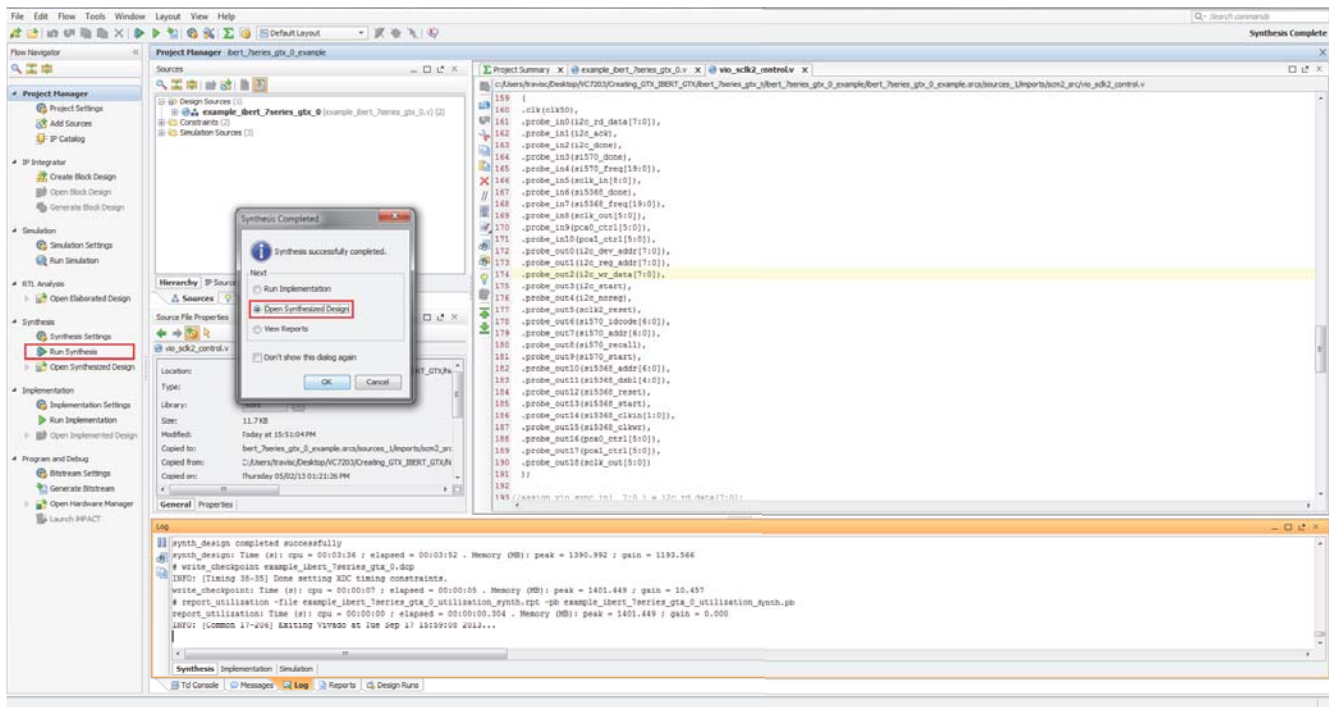


UG847_c1_30_100813

Figure 1-30: Design Sources File Hierarchy

14. Click **Run Synthesis** in the Flow Navigator, which synthesizes the design.

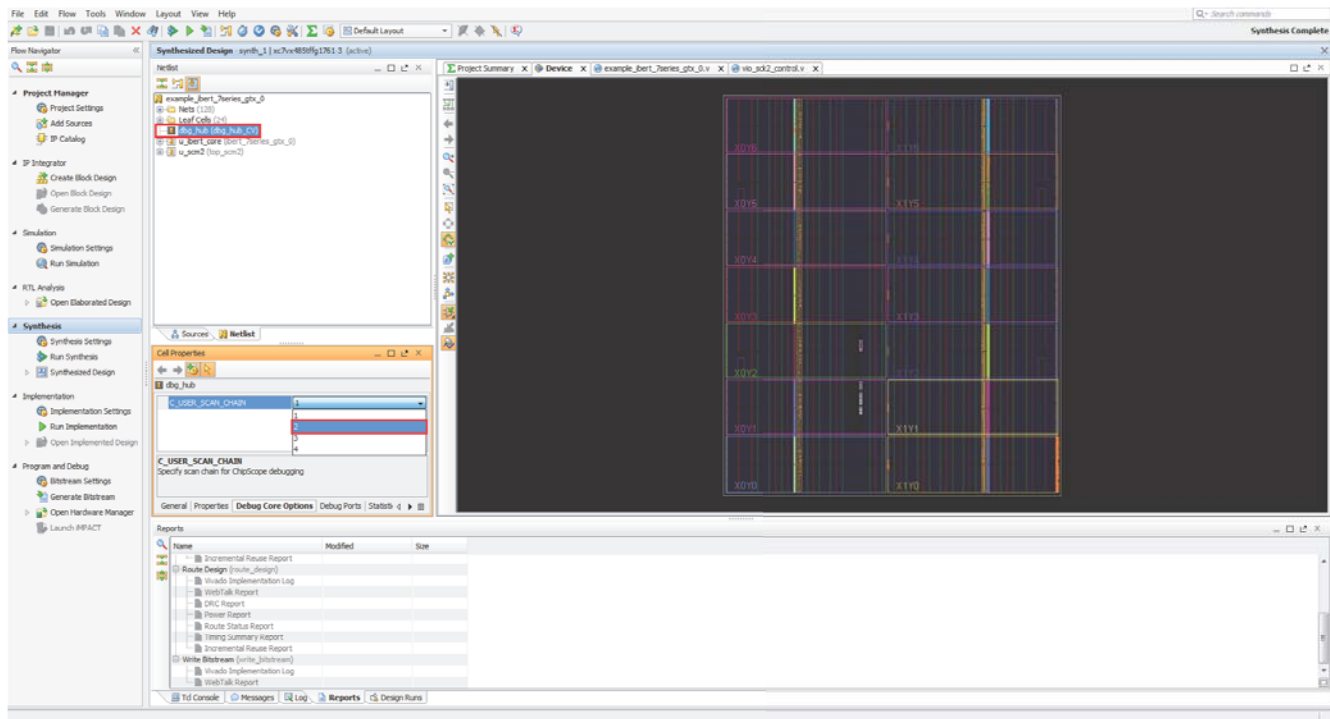
15. When synthesis is done, a Synthesis Complete window pops up. Select **Open Synthesized Design** and click **OK** (Figure 1-31).



UG847_c1_31_110213

Figure 1-31: Synthesis Completed

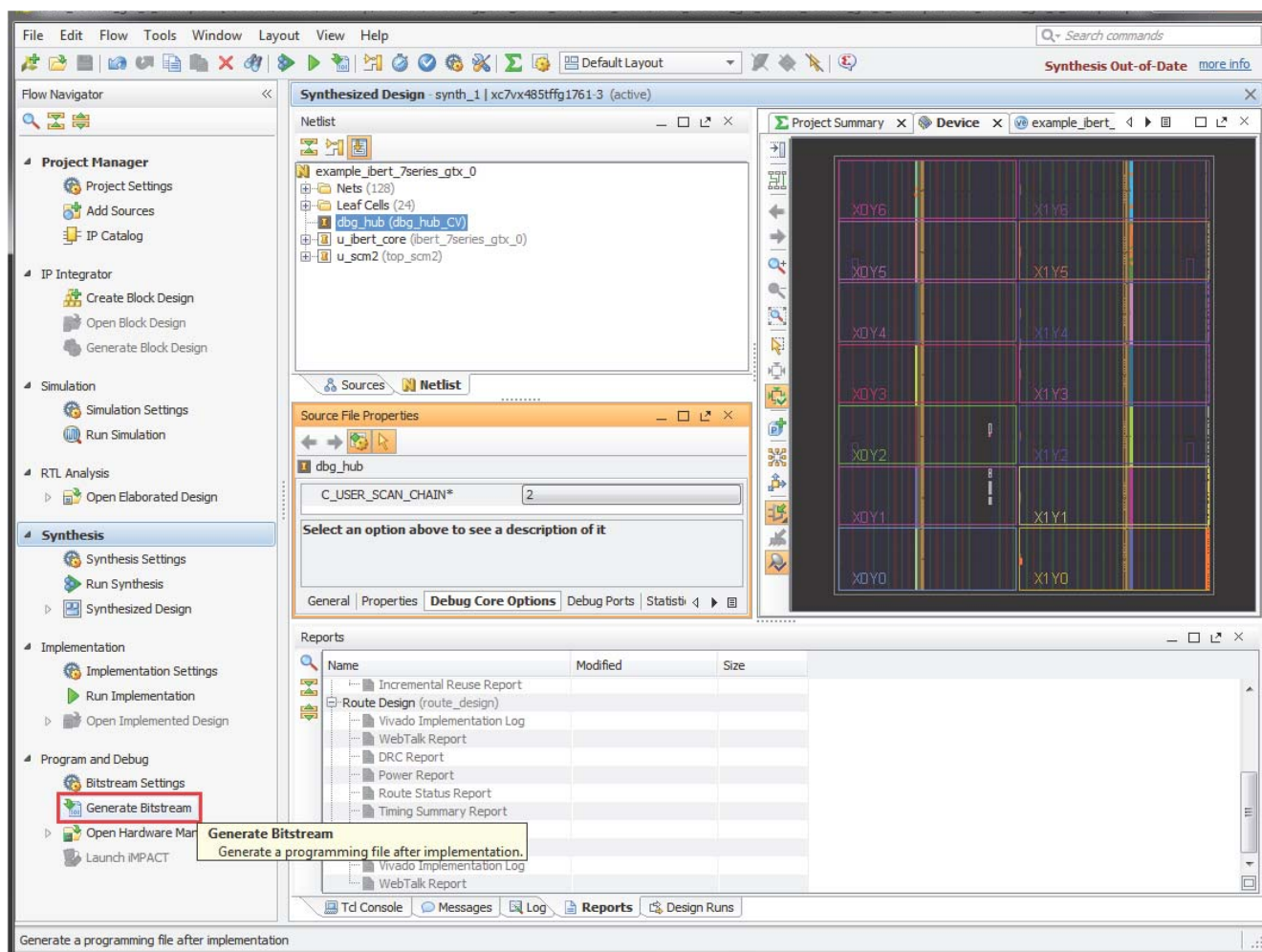
16. When the Synthesized Design opens, select **dbg_hub** in the Netlist window, then select the **Debug Core Options** tab in the Cell Properties window and change **C_USER_SCAN_CHAIN*** to 2 (Figure 1-32). Click **File > Save Constraints**.



UG847_c1_32_110213

Figure 1-32: Debug Core Options for dbg_hub

17. In the Flow Navigator under Program and Debug, click **Generate Bitstream** (Figure 1-33). A window pops up asking if it is ok to launch implementation. Click **Yes**.



UG847_c1_33_110213

Figure 1-33: Generate Bitstream

18. When implementation completes, navigate to the project directory and locate the resultant bitstream here:
`\ibert_7series_gtx_0\example_project\ibert_7series_gtx_0_example\ibert_7series_gtx_0_example.runs\impl_1\.`

Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the [Xilinx Support website](#).

For continual updates, add the Answer Record to your [myAlerts](#).

For definitions and terms, see the [Xilinx Glossary](#).

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the VC7203 kit and its documentation is available on these websites.

[Virtex-7 FPGA VC7203 Characterization Kit](#)

[Virtex-7 FPGA VC7203 Characterization Kit documentation](#)

[Virtex-7 FPGA VC7203 Characterization Master Answer Record \(AR 52383\)](#)

These Xilinx documents and sites provide supplemental material useful with this guide:

1. [UG957](#), VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide
2. [UG770](#), HW-CLK-101-SCLK2 SuperClock-2 Module User Guide
3. [UG908](#), Vivado Design Suite User Guide: Programming and Debugging
4. [PG132](#), LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers Product Guide for Vivado Design Suite

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