SP601 Built-In Self Test Flash Application

December 2009

XTP041

Overview

- Xilinx SP601 Board
- Software Requirements
- SP601 Setup
- SP601 BIST (Built-In Self Test)
- Compile SP601 BIST Design
- Program SP601 BPI
- References

Note: This presentation applies to the SP601

SP601 BIST Design Description

- **Description**
  - The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.
- **Reference Design IP**
  - EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_iic, xps_mch_emc, xps_spi, util_io_mux, util_bus_split, xps_ethernetlite
    - Embedded System Tools Reference Guide (UG111)
    - http://www.xilinx.com/ise/embedded/edk_ip.htm
- **Reference Design Source**
  - rdf0045.zip

Note: Presentation applies to the SP601

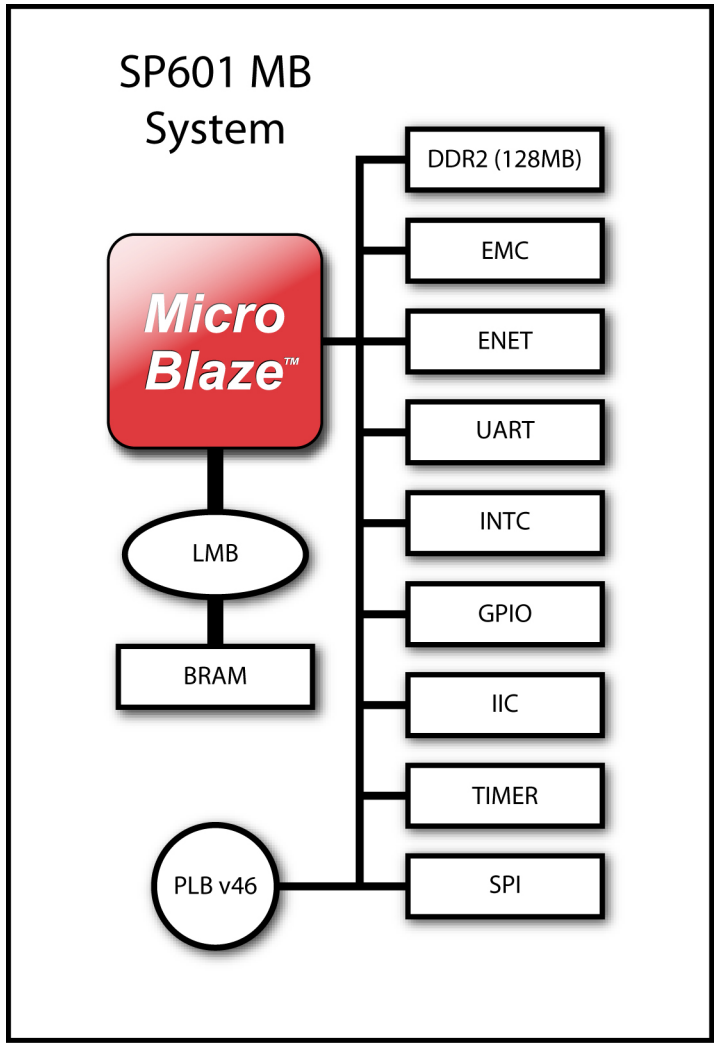
Embedded Processor Design

- **The provided embedded reference design is supported "as is"**
  - Please refer to the click through license agreement
- **Embedded reference design has been verified on the SP601 Evaluation Kit**
  - Design consists of Early Access IP
  - Design may change in subsequent releases
- **The reference design will allow users to:**
  - Re-build and verify functionality on the SP601 evaluation kit

Note: Presentation applies to the SP601

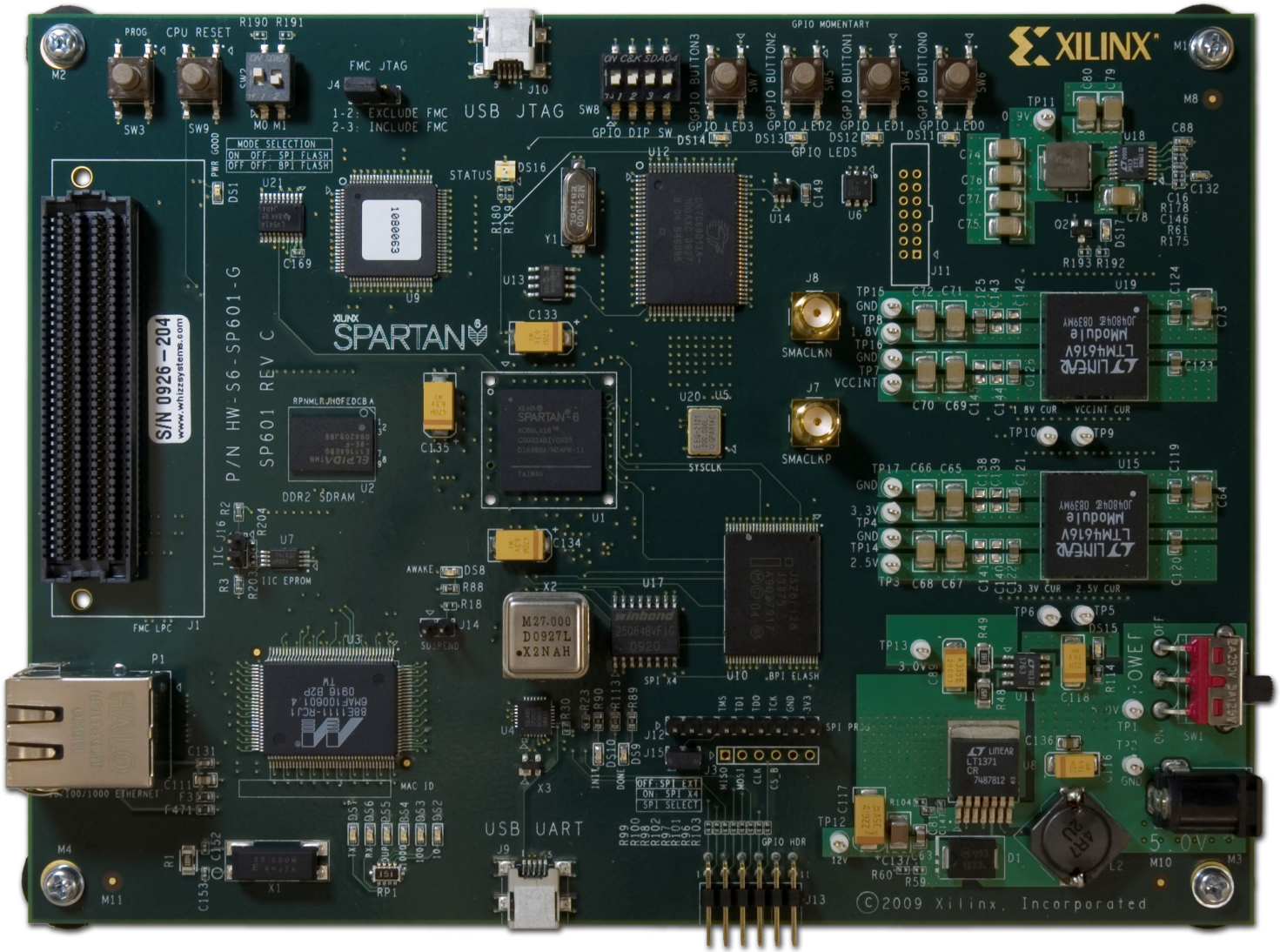
SP601 MicroBlaze Hardware

- **The SP601 MicroBlaze Design Hardware includes:**
  - DDR2 Interface (128 MB)
  - BRAM
  - External Memory Controller (EMC)
    - Flash Memory
  - Networking
  - UART
  - Interrupt Controller
  - GPIO (IIC, LEDs and LCD)
  - PLB Arbiter
  - SPI



Note: Presentation applies to the SP601

Xilinx SP601 Board

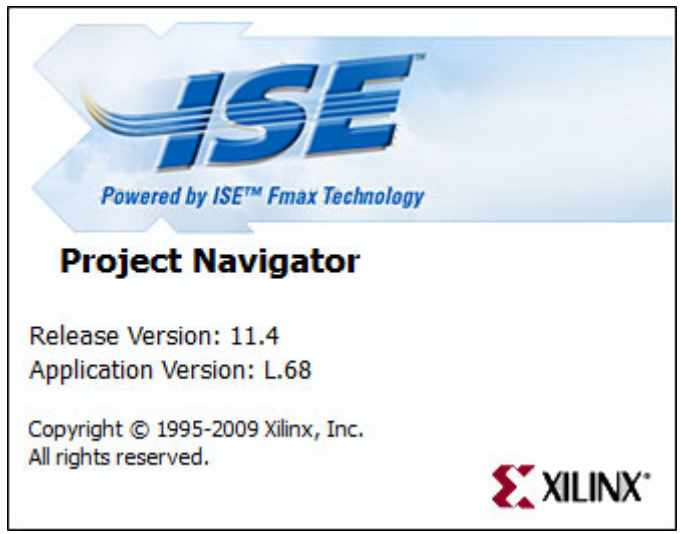


Note: Presentation applies to the SP601

XILINX

ISE Software Requirement

- **Xilinx ISE 11.4 software**
  - Install the Webpack for the Spartan-6 LX16 devices
  - Run XilinxUpdate and download the Webpack devices



Note: Presentation applies to the SP601

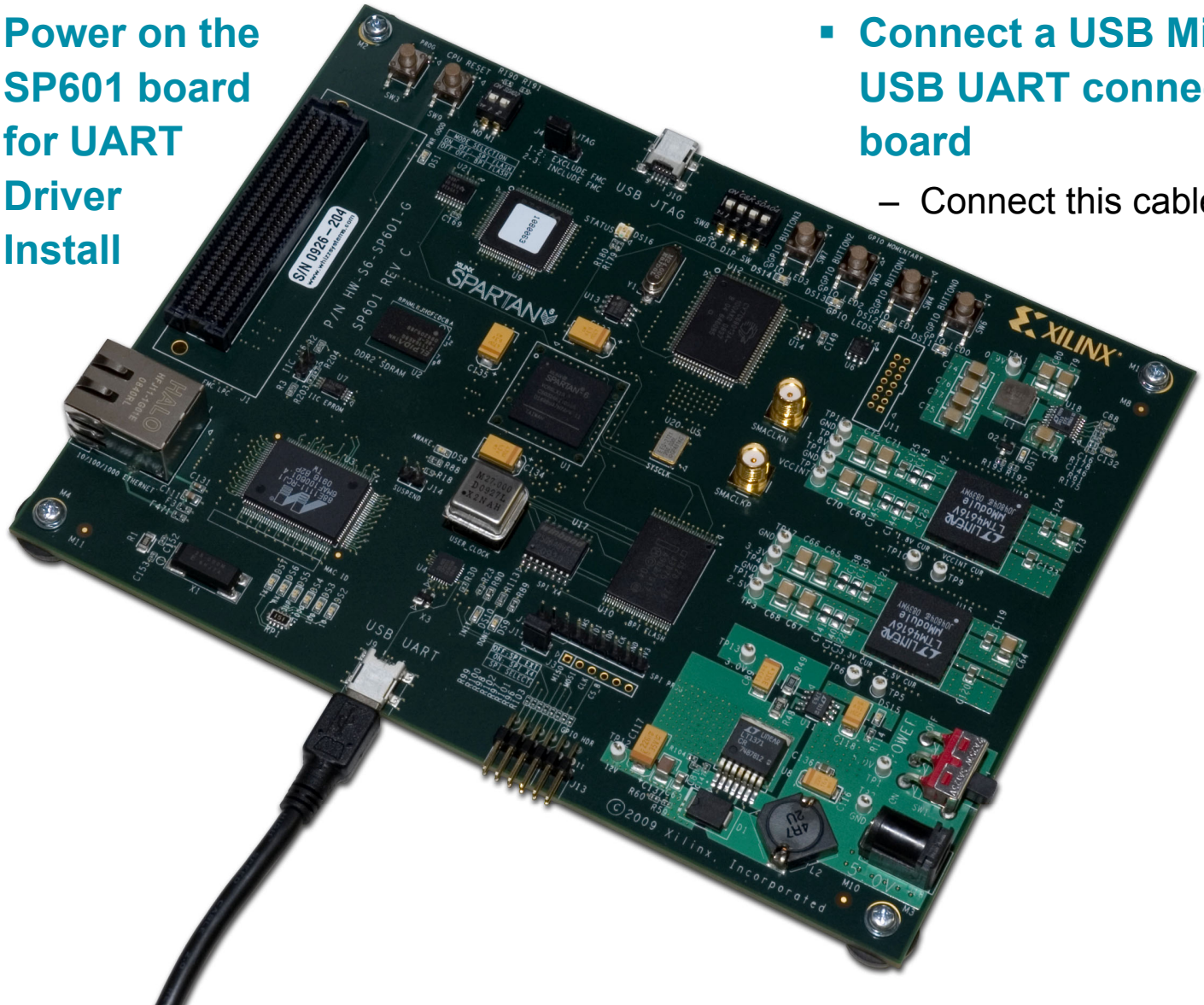
EDK Software Requirement

- Xilinx EDK 11.4 software

Note: Presentation applies to the SP601

SP601 Setup

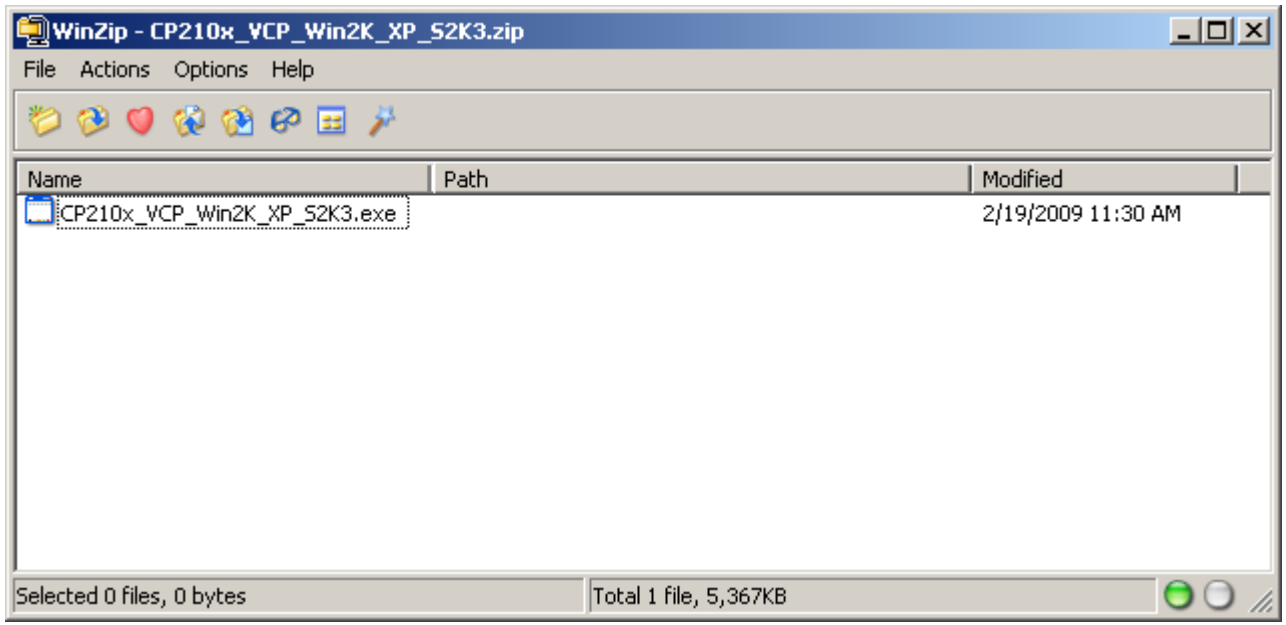
- **Power on the SP601 board for UART Driver Install**



- **Connect a USB Mini-B Cable to the USB UART connector on the SP601 board**
  - Connect this cable to your PC

SP601 Setup

- **Install USB UART Drivers**
  - https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip

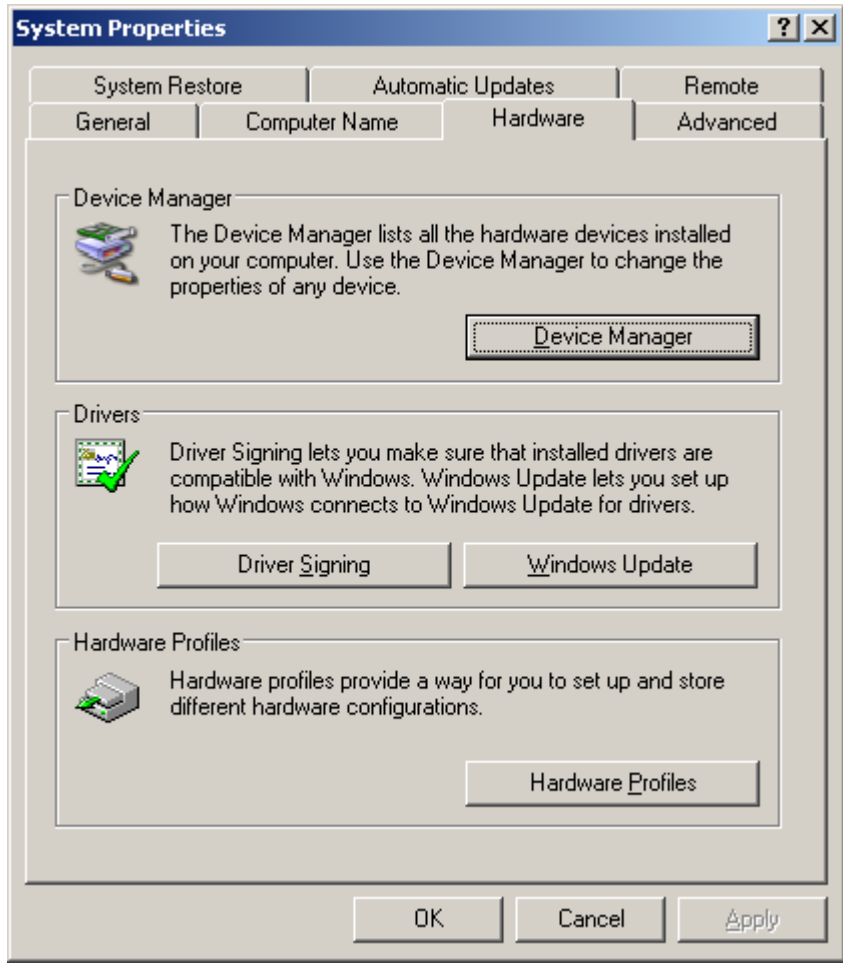


Note: Presentation applies to the SP601

XILINX®

SP601 Setup

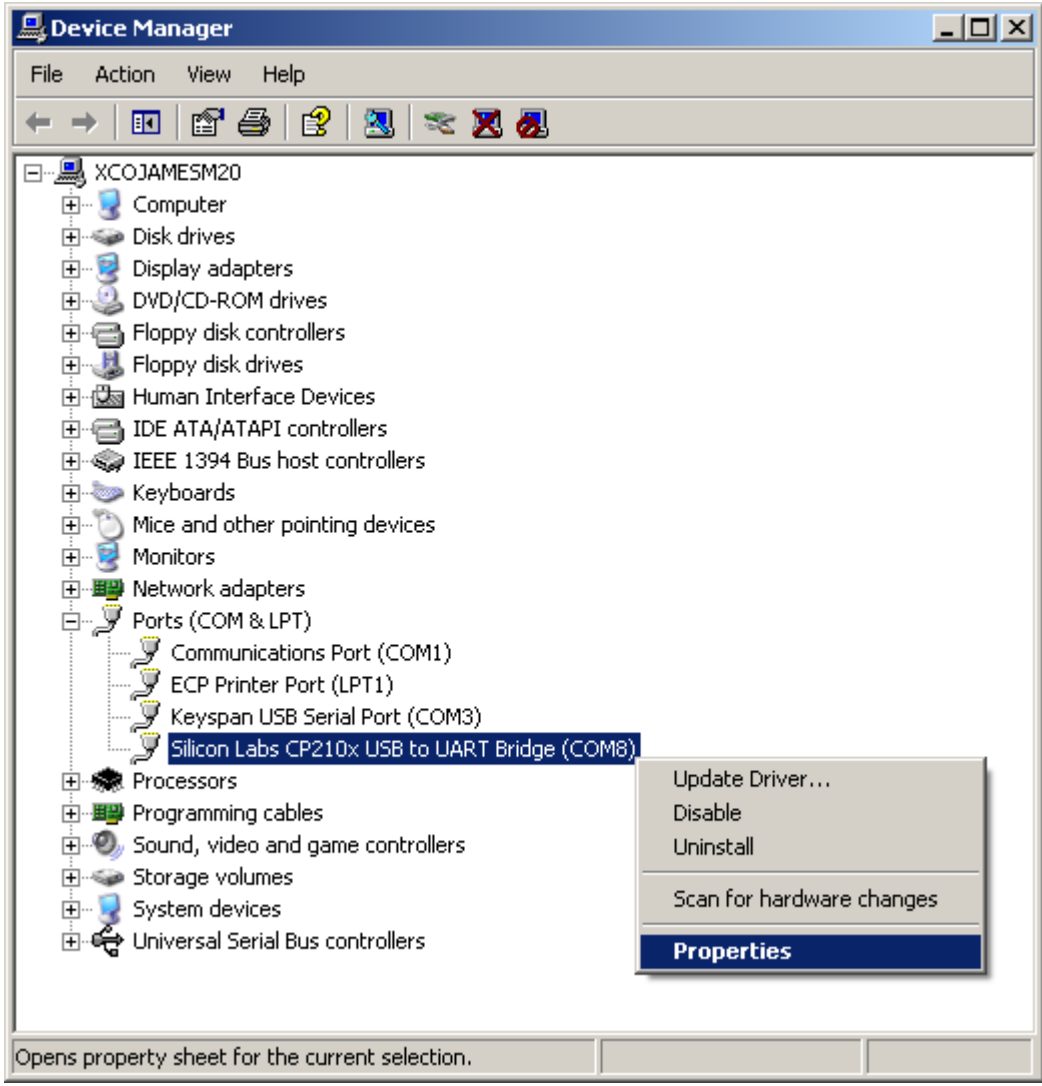
- **Right-click on My Computer and select Properties**
  - Select the Hardware tab
  - Click on Device Manager



Note: Presentation applies to the SP601

SP601 Setup

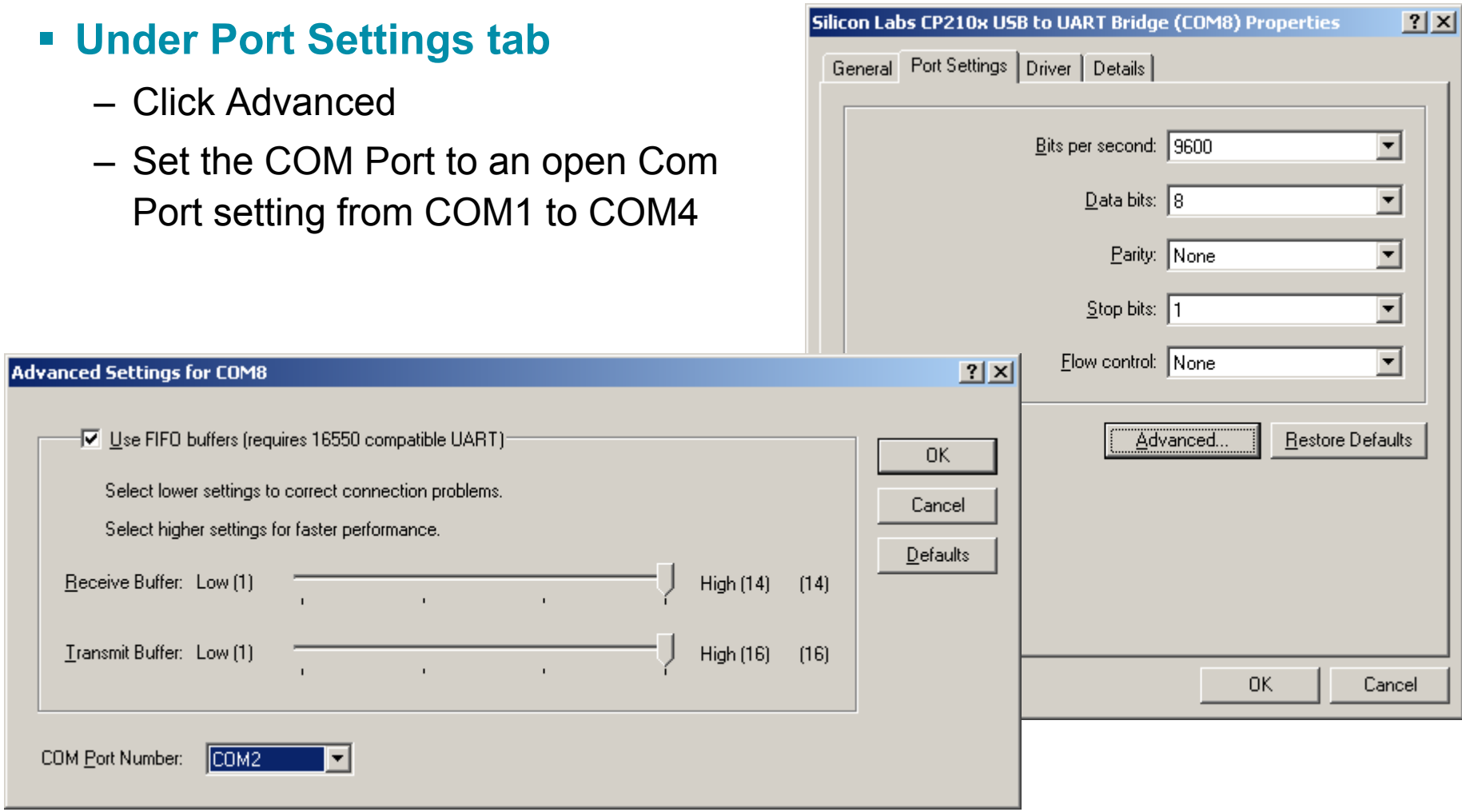
- **Expand the Ports Hardware**
  - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select Properties



Note: Presentation applies to the SP601

SP601 Setup

- **Under Port Settings tab**
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4

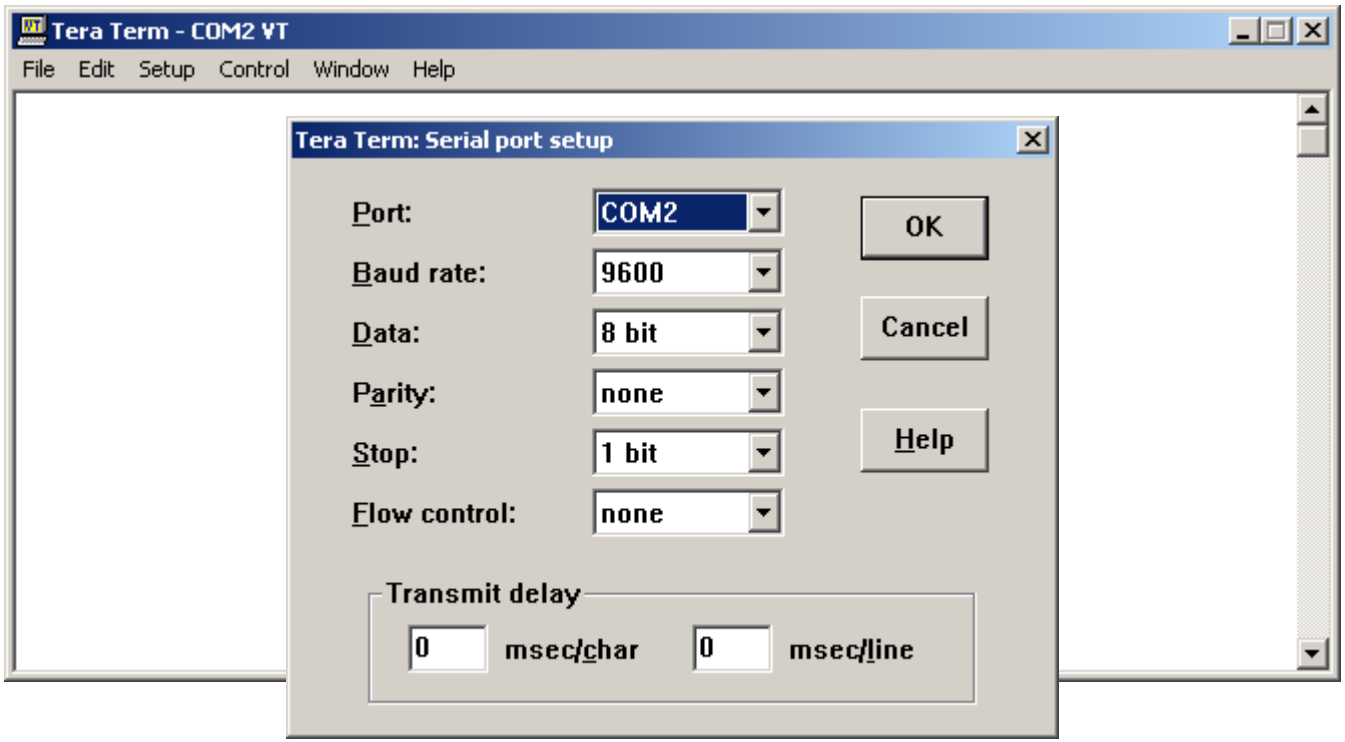


Note: Presentation applies to the SP601

XILINX

SP601 Setup

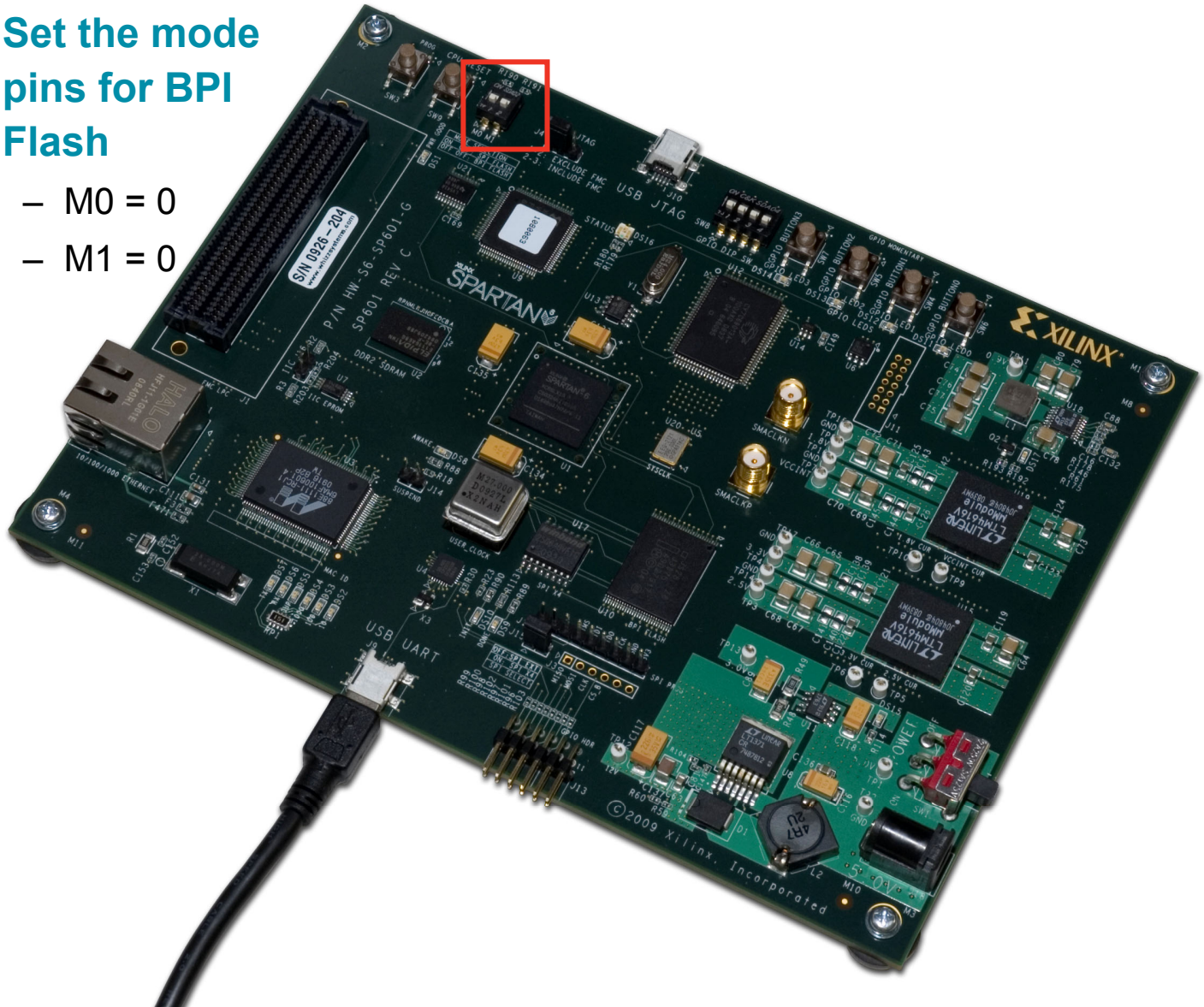
- **Board Power must be on before starting Tera Term**
- **Start the Terminal Program**
  - Select your USB Com Port
  - Set the baud to 9600



Note: Tera Term may need to be restarted if board power is cycled

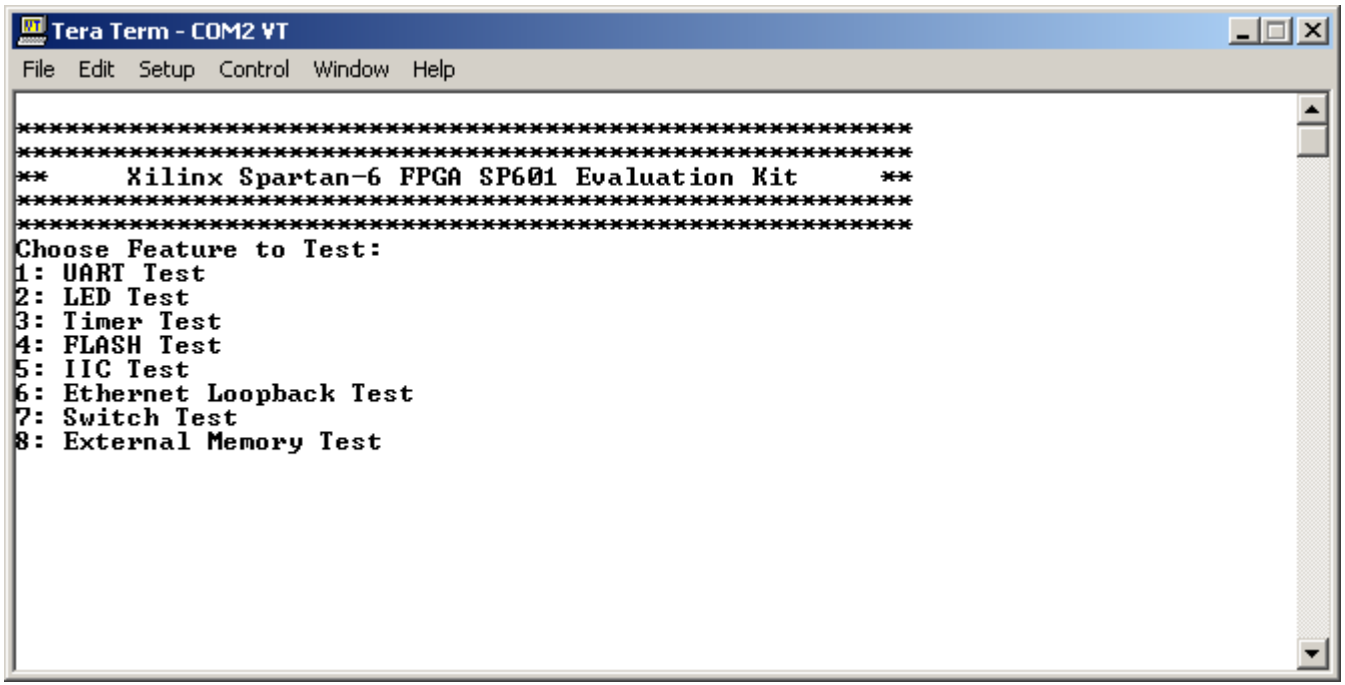
SP601 Setup

- **Set the mode pins for BPI Flash**
  - M0 = 0
  - M1 = 0



SP601 BIST

- **Press PROG and view initial BIST screen**
  - Type "**1**" to start the UART Test

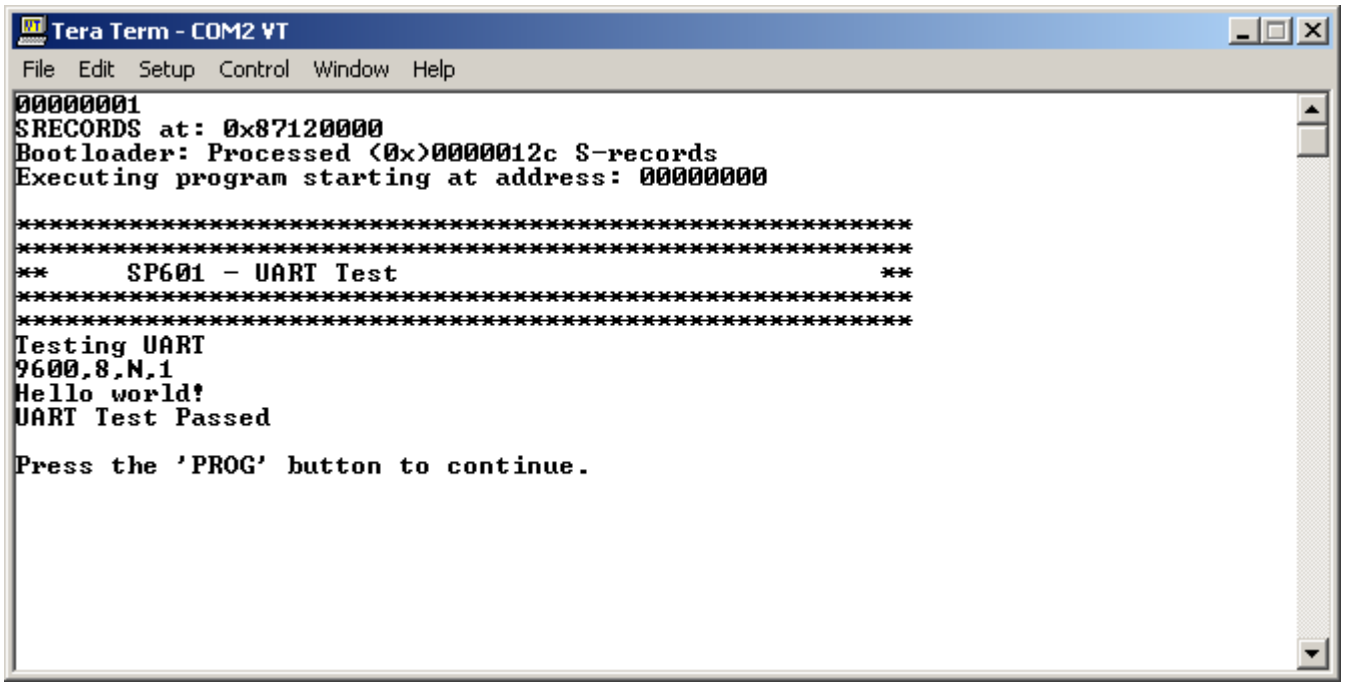


Note: Presentation applies to the SP601

XILINX®

SP601 BIST

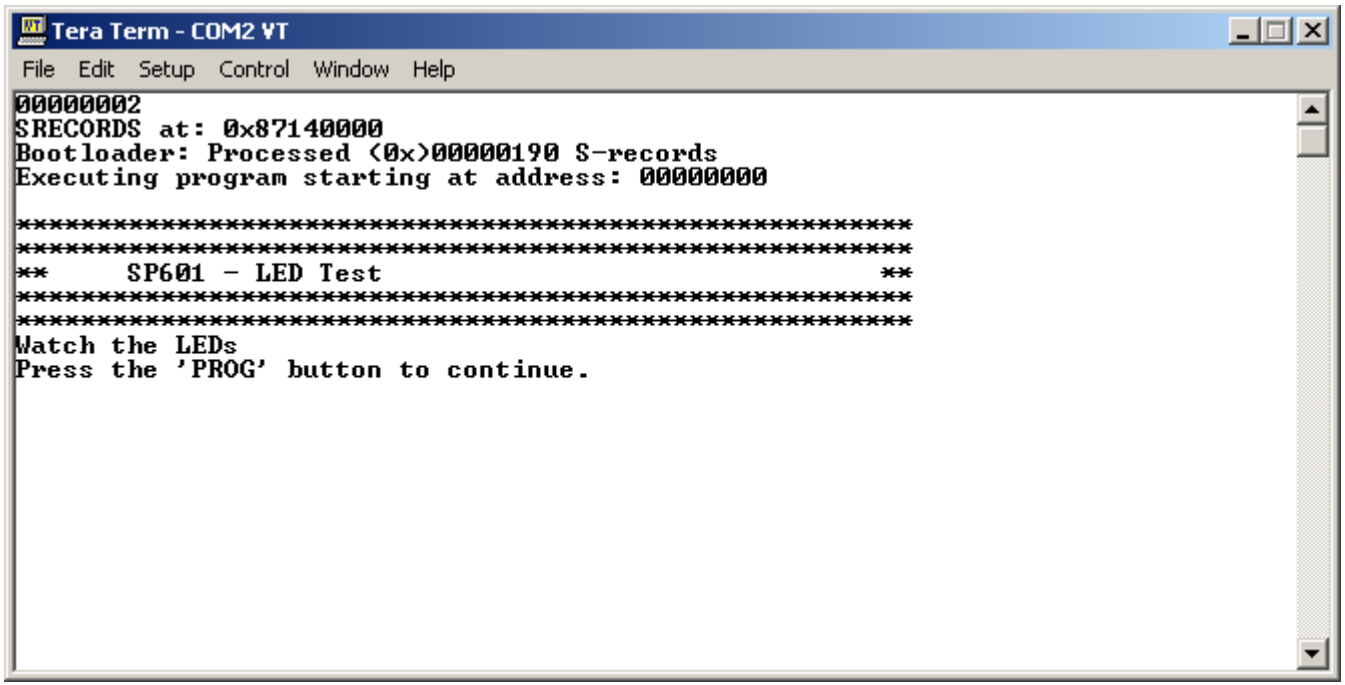
- **UART Test completed**
  - Press **PROG** and type **2** to begin LED Test



Note: Presentation applies to the SP601

SP601 BIST

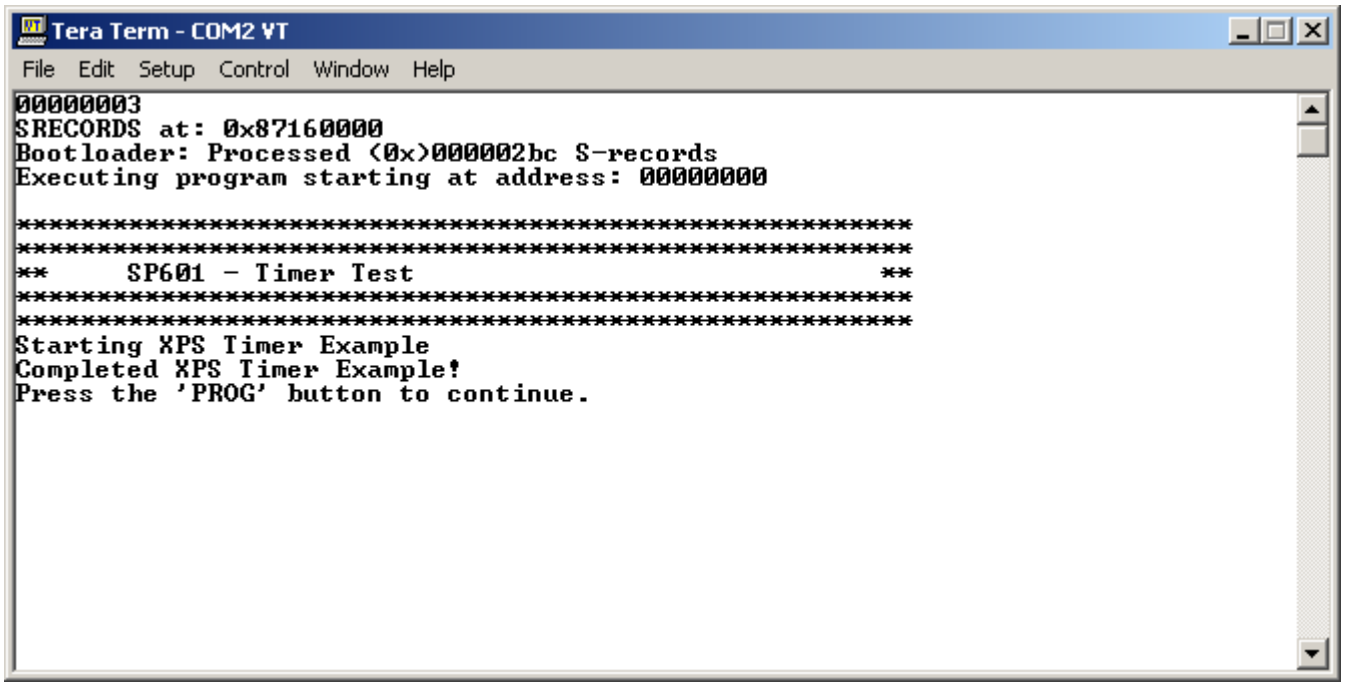
- **LED Test completed**
  - Press **PROG** and type **3** to begin Timer Test



Note: Presentation applies to the SP601

SP601 BIST

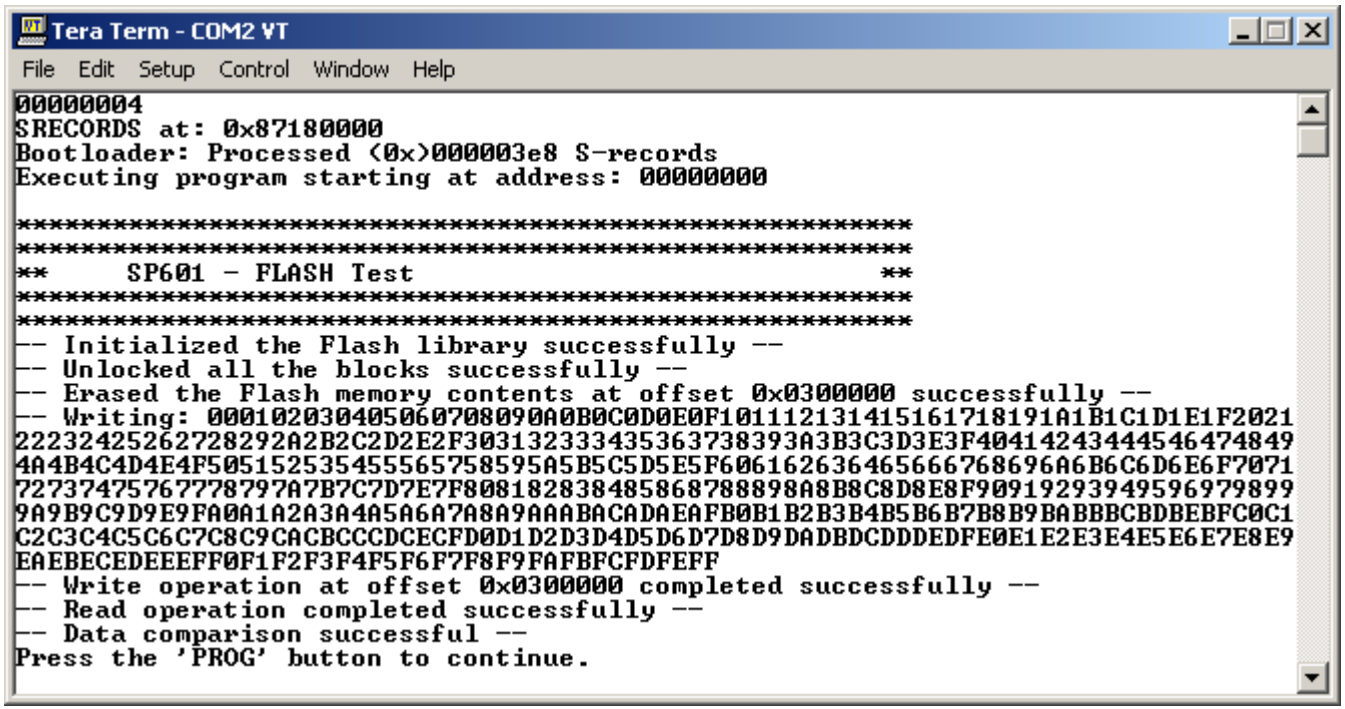
- **Timer Test completed**
  - Press **PROG** and type **4** to begin Flash test



Note: Do not press PROG until this test completes

SP601 BIST

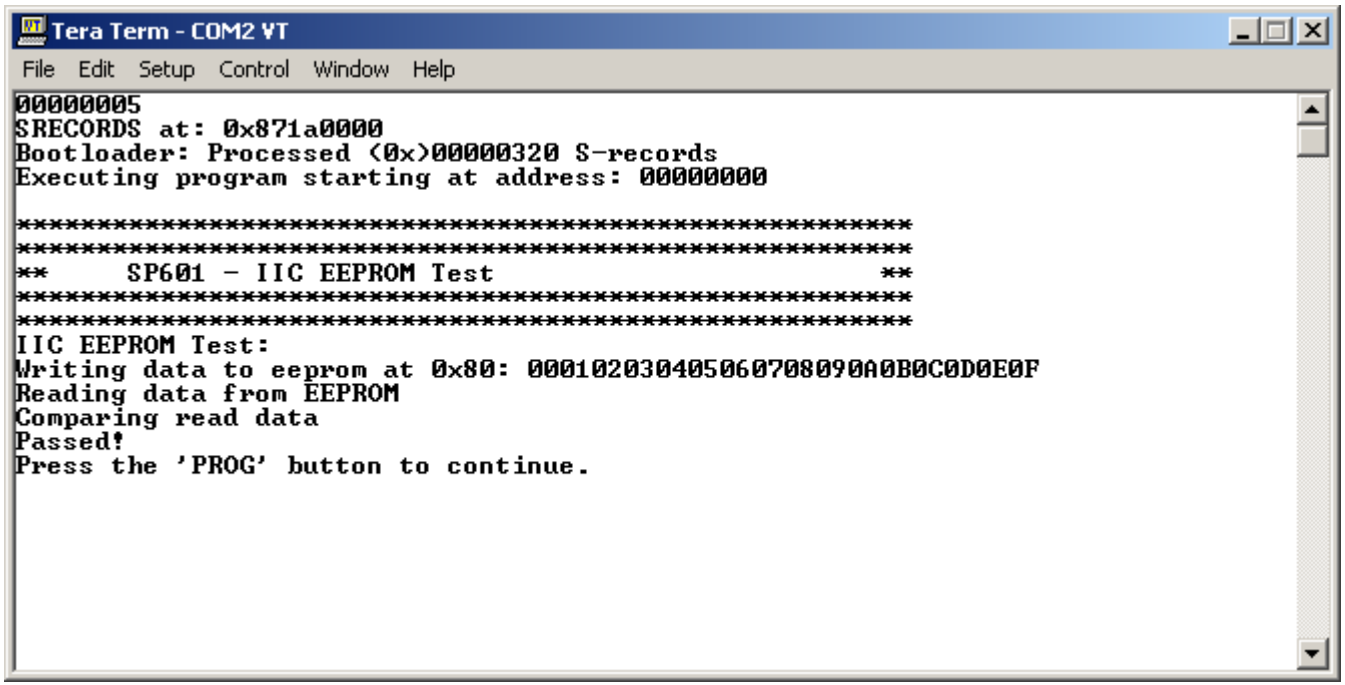
- **Flash Test completed**
  - Press **PROG** and type **5** to begin IIC EEPROM Test



Note: Presentation applies to the SP601

SP601 BIST

- **IIC EEPROM Test completed**
  - Press **PROG** and type **6** to begin Ethernetlite Test

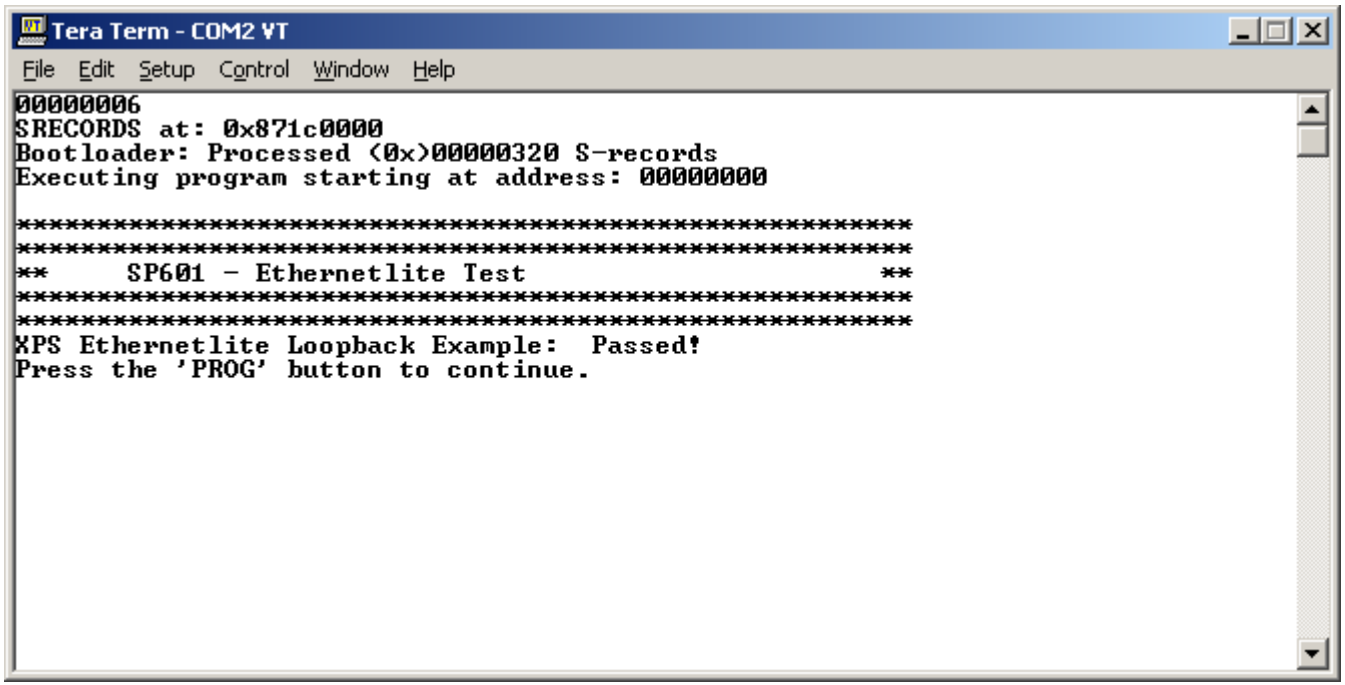


Note: Presentation applies to the SP601

XILINX®

SP601 BIST

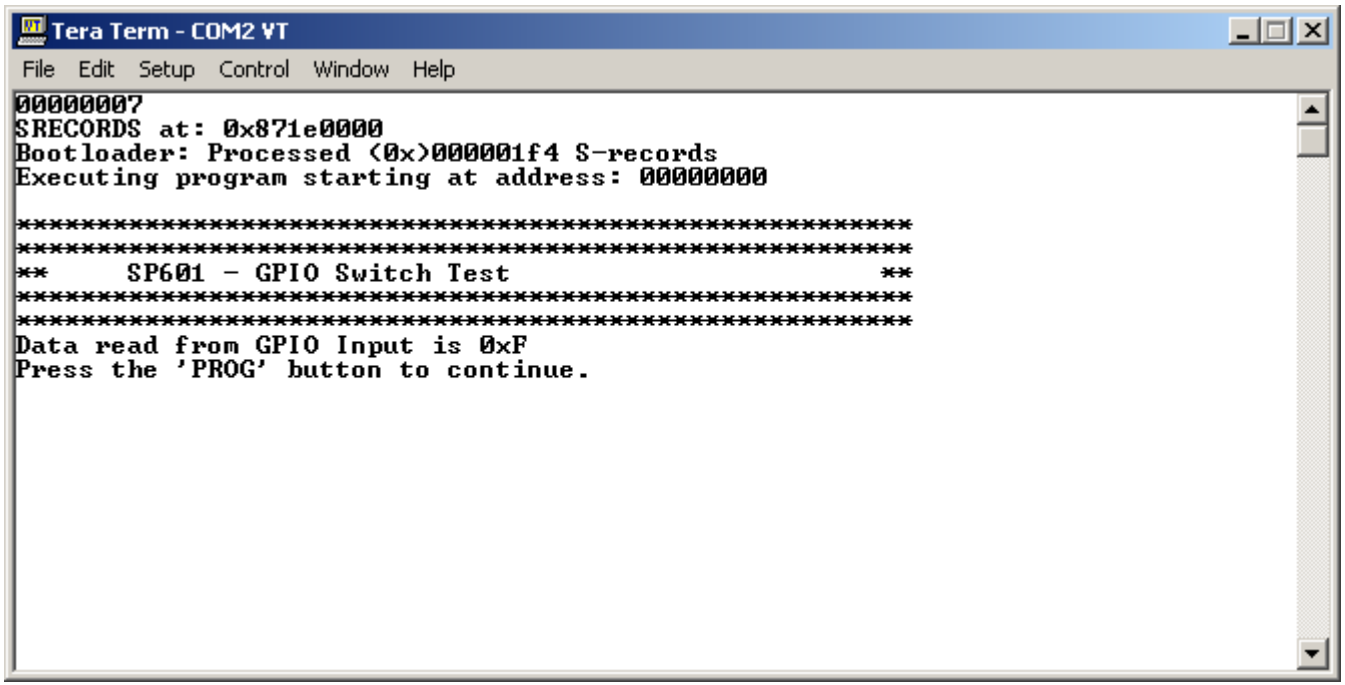
- **Ethernetlite Test completed**
  - Press **PROG** and type **7** to begin GPIO Switch Test



Note: Presentation applies to the SP601

SP601 BIST

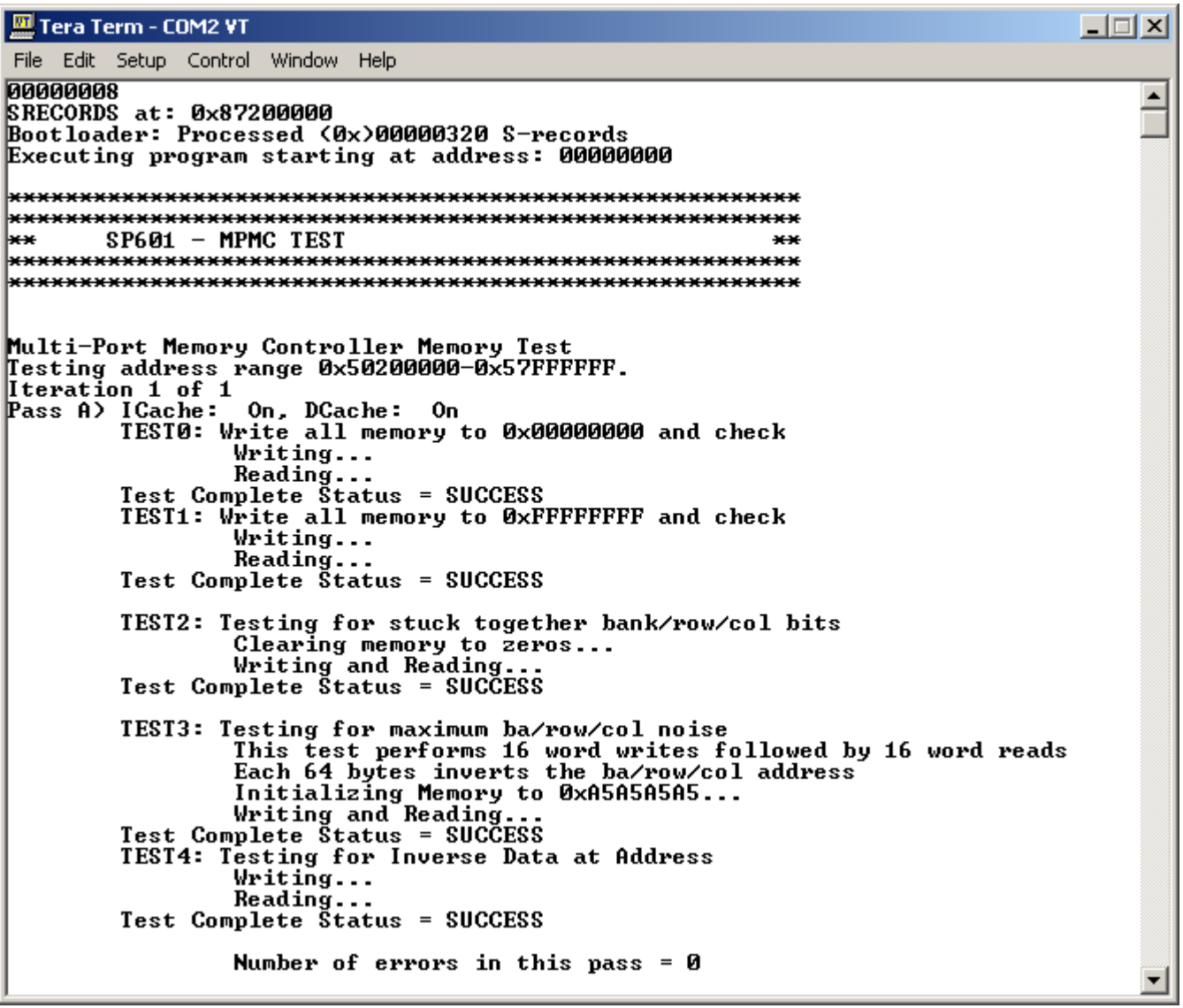
- **GPIO Switch Test completed**
  - Press **PROG** and type **8** to begin External Memory Test



Note: Presentation applies to the SP601

XILINX®

SP601 BIST



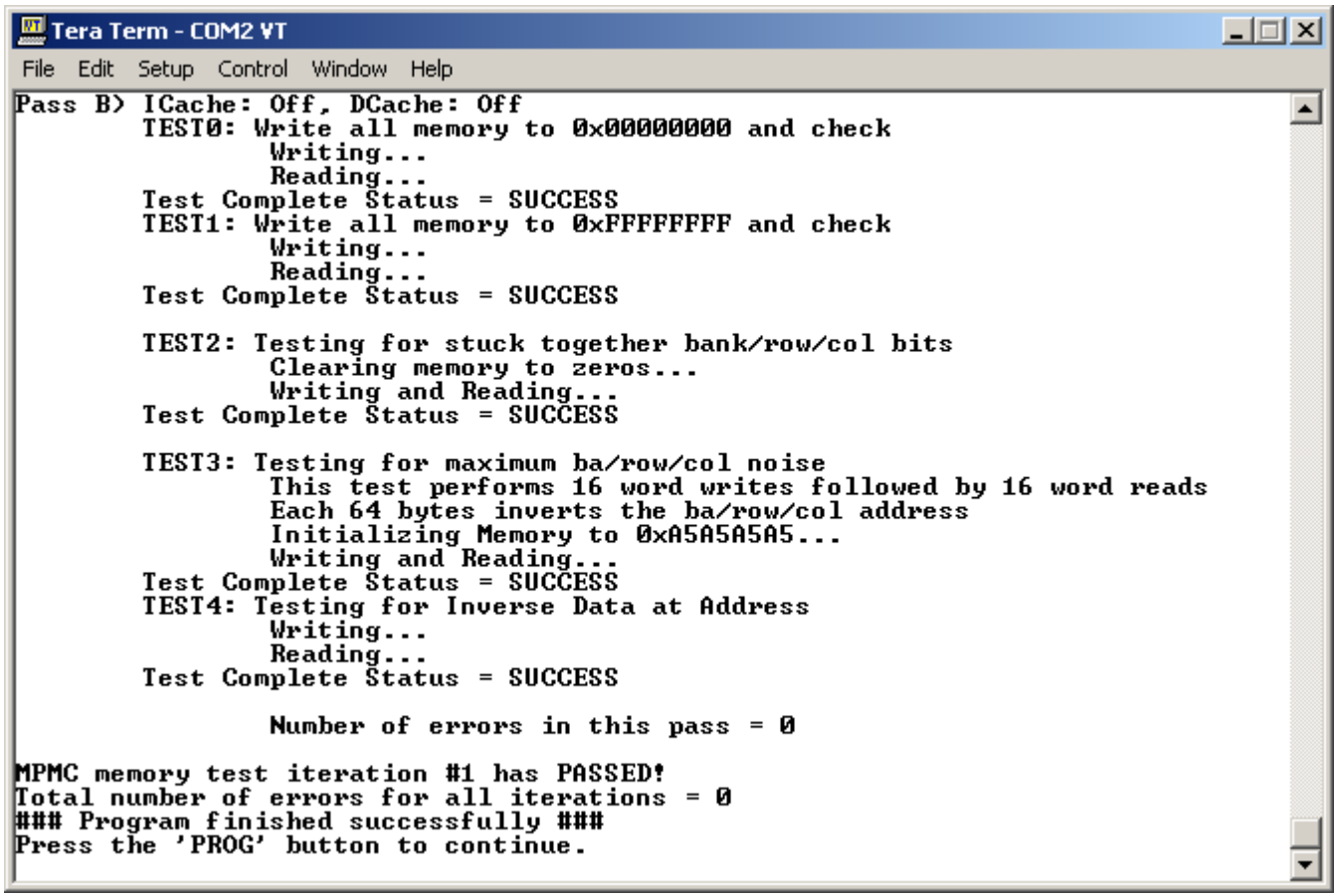
- External Memory Test running with caches on

Note: Presentation applies to the SP601

XILINX®

SP601 BIST

- Second part of External Memory test (caches off)

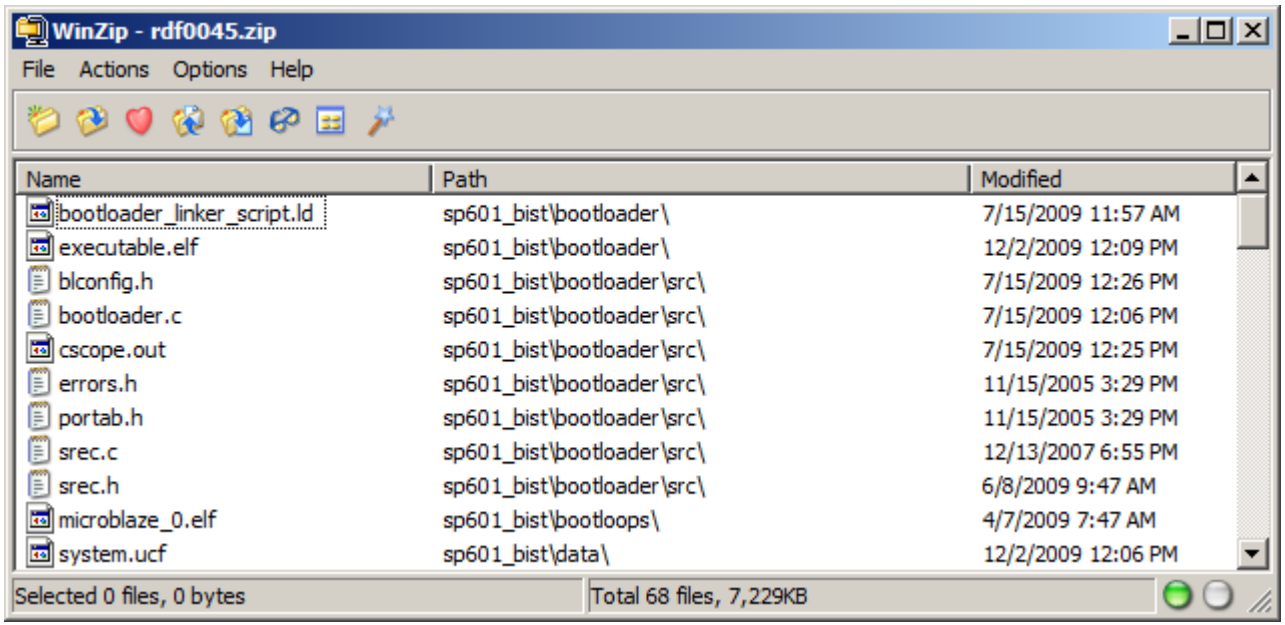


Note: Presentation applies to the SP601

Compile SP601 BIST Design

Compile SP601 BIST Design

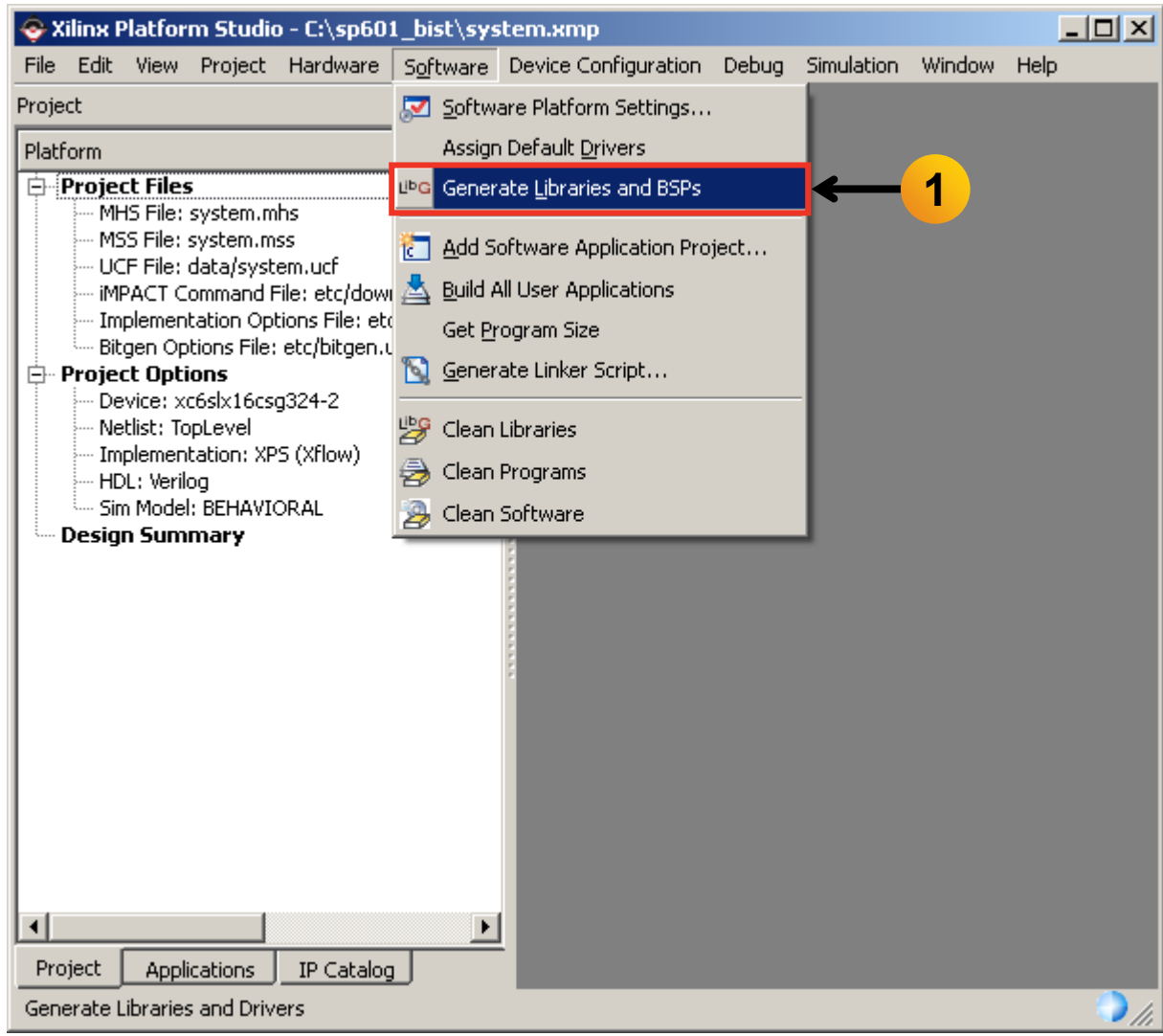
- **Unzip the rdf0045.zip file**
  - https://secure.xilinx.com/webreg/clickthrough.do?cid=139854



Note: Presentation applies to the SP601

Compile SP601 BIST Design

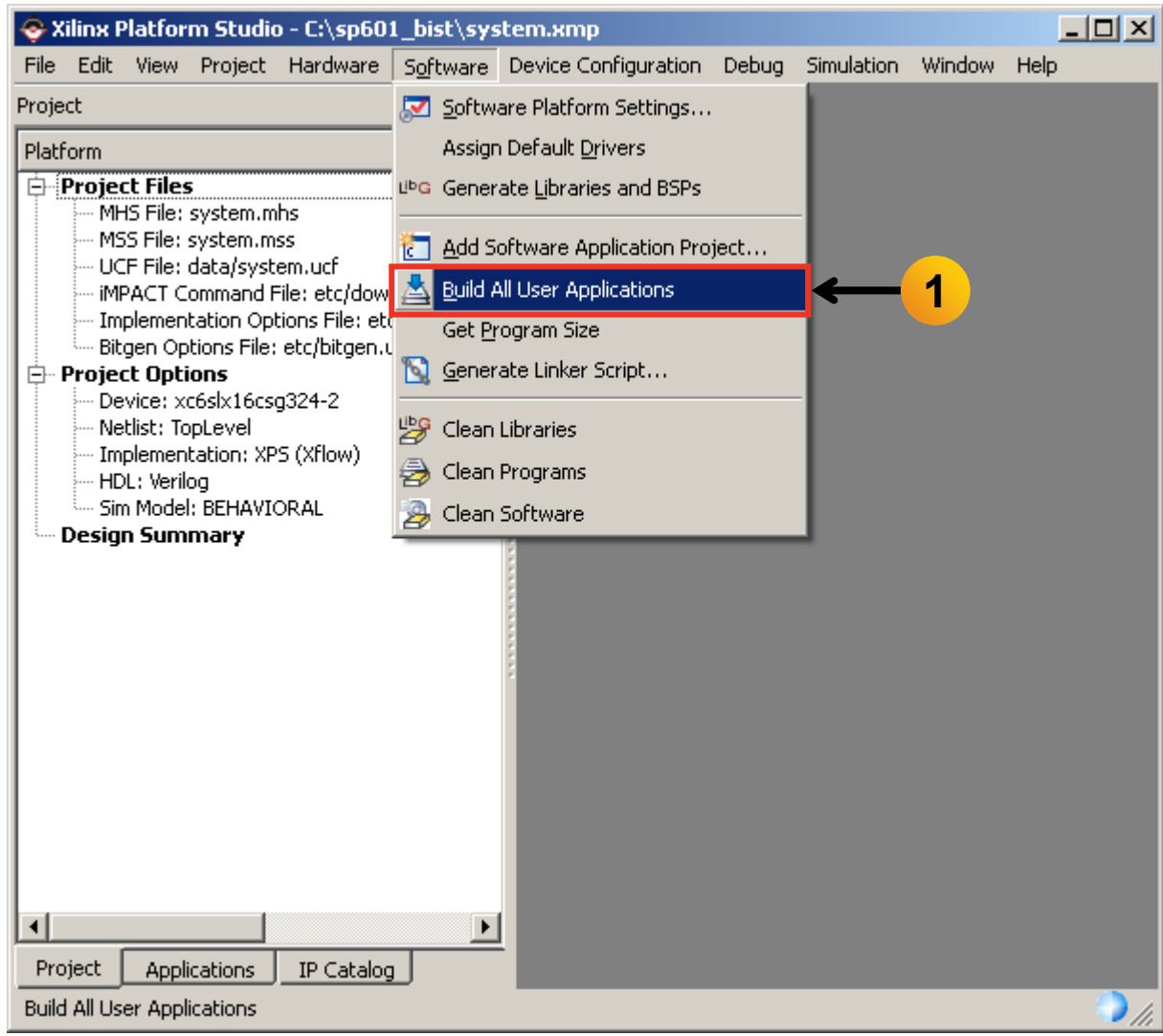
- The BIST Design can be compiled with EDK
- Open XPS project <design path>\ system.xmp
- Generate the libraries needed to create the bitstream
  - Select **Software** → **Generate Libraries and BSPs** (1)



Note: Presentation applies to the SP601

Compile SP601 BIST Design

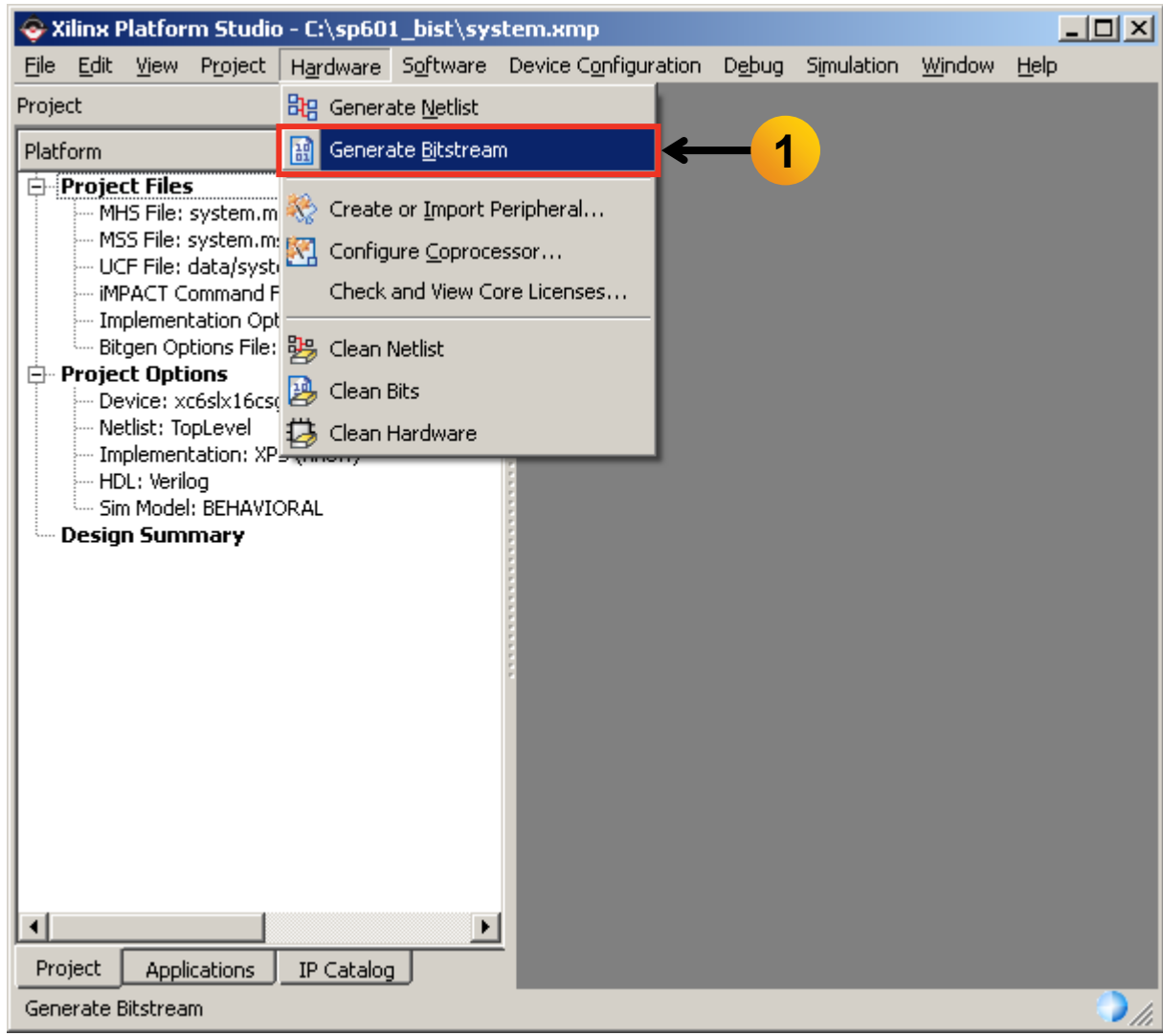
- **Compile the Software Applications and create the application ELF files**
  - Select **Software → Build All User Applications** (1)



Note: Presentation applies to the SP601

Compile SP601 BIST Design

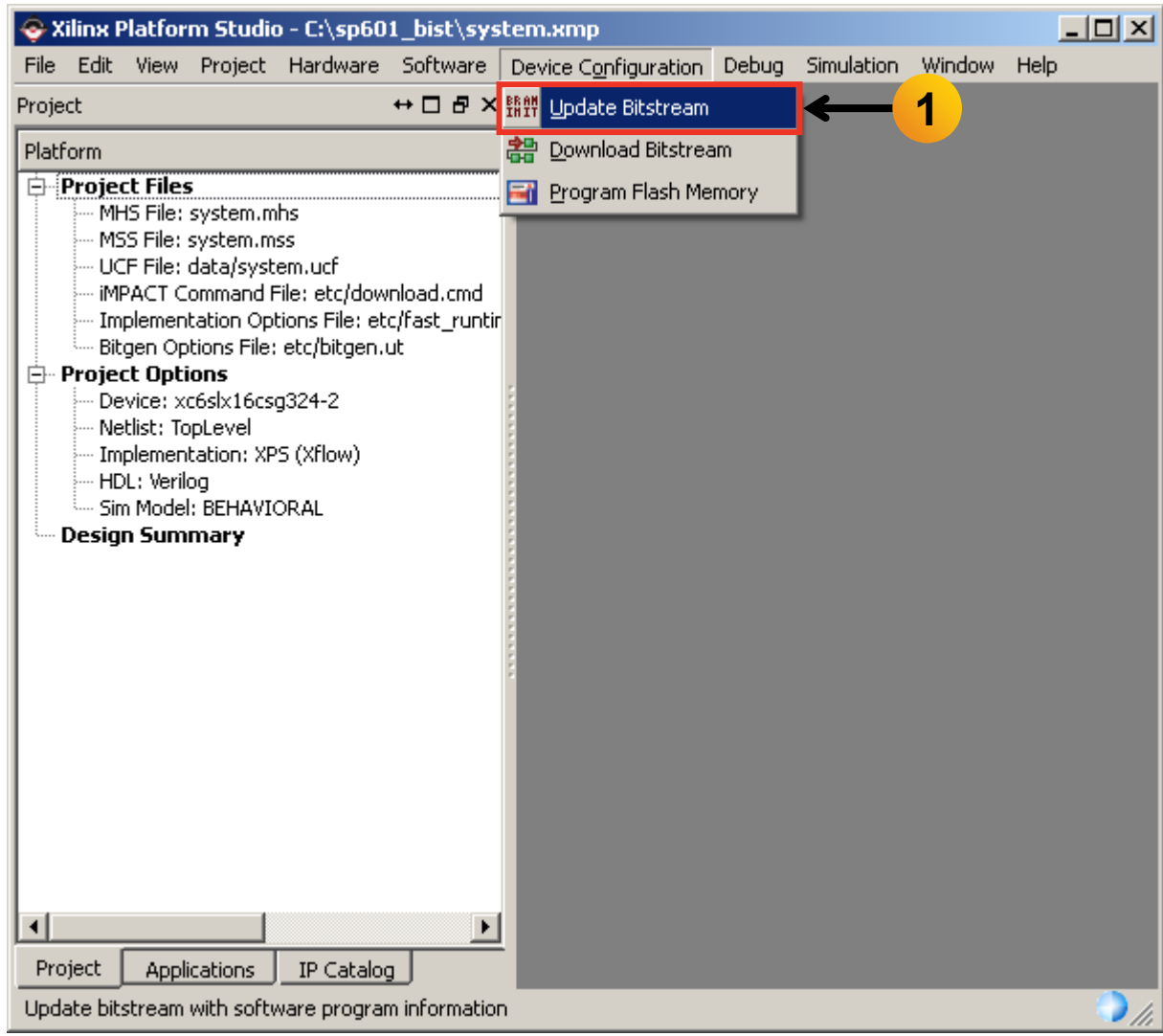
- **Create the hardware design, system.bit, located in <project directory> /implementation**
  - Select **Hardware → Generate Bitstream** (1)



Note: Presentation applies to the SP601

Compile SP601 BIST Design

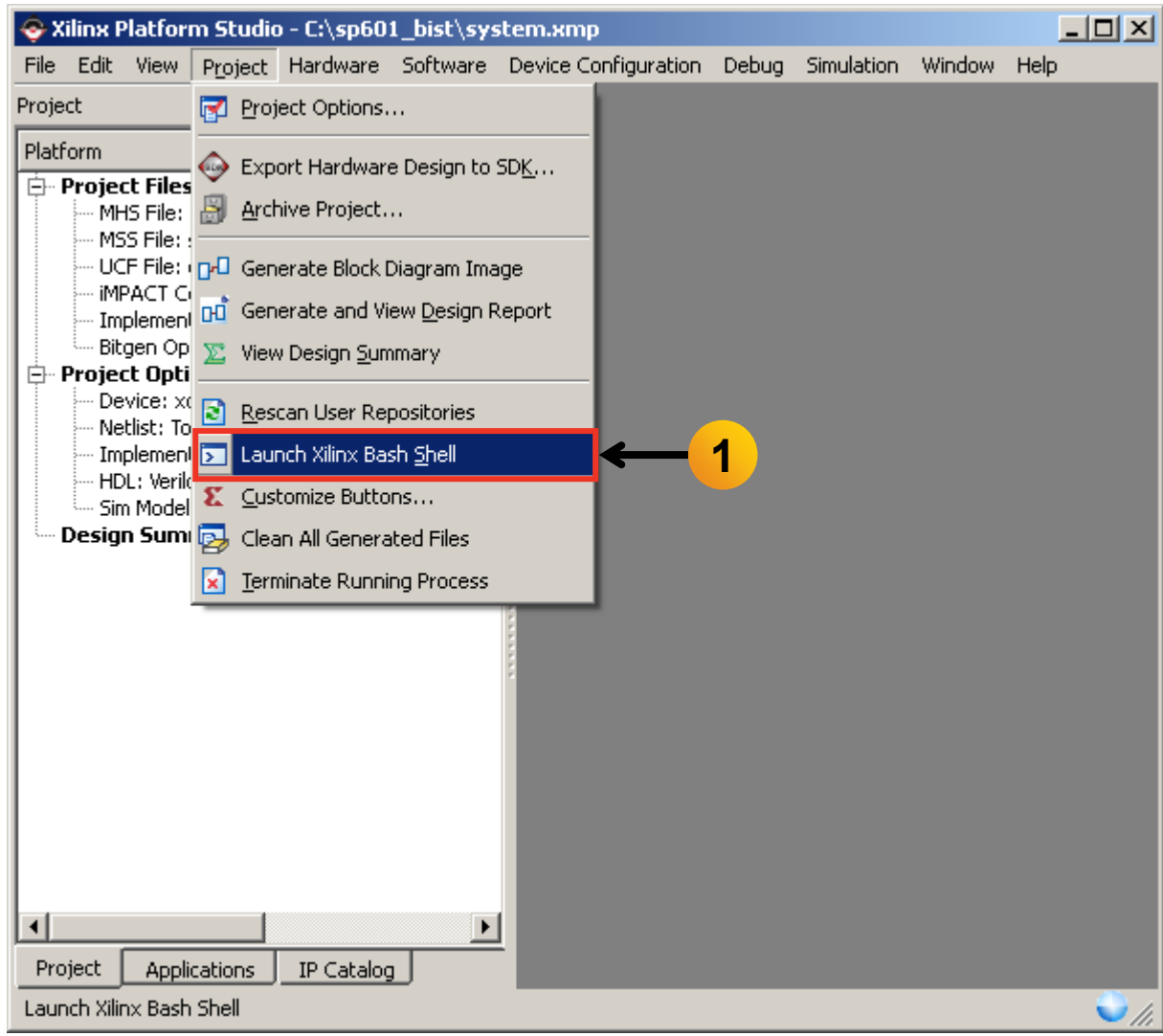
- **Init memory with the Bootloader Application ELF**
  - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
  - Select **Device Configuration → Update Bitstream** (1)



Note: Presentation applies to the SP601

Compile SP601 BIST Design

- **The bitstream must be converted to hex format (.bin) prior to programming into flash**
  - Select **Project → Launch Xilinx Bash Shell** (1)

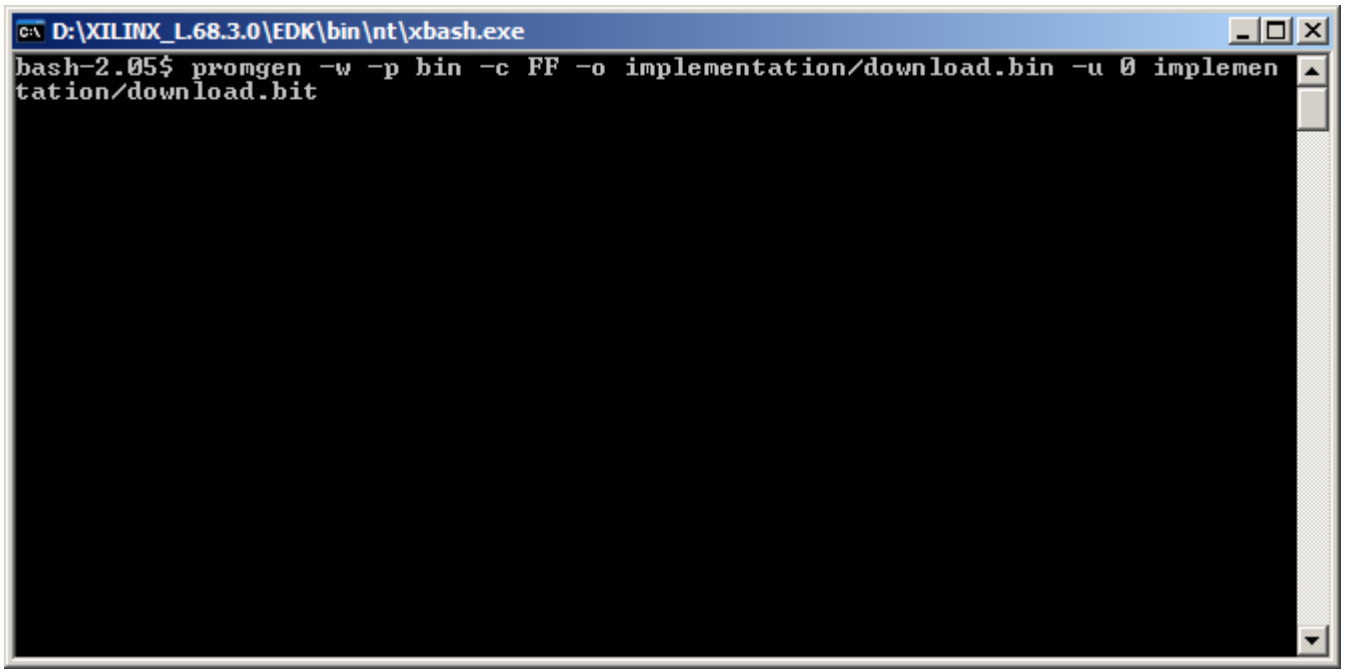


Note: Presentation applies to the SP601

Compile SP601 BIST Design

- **Generate a BIN file from the bitstream**

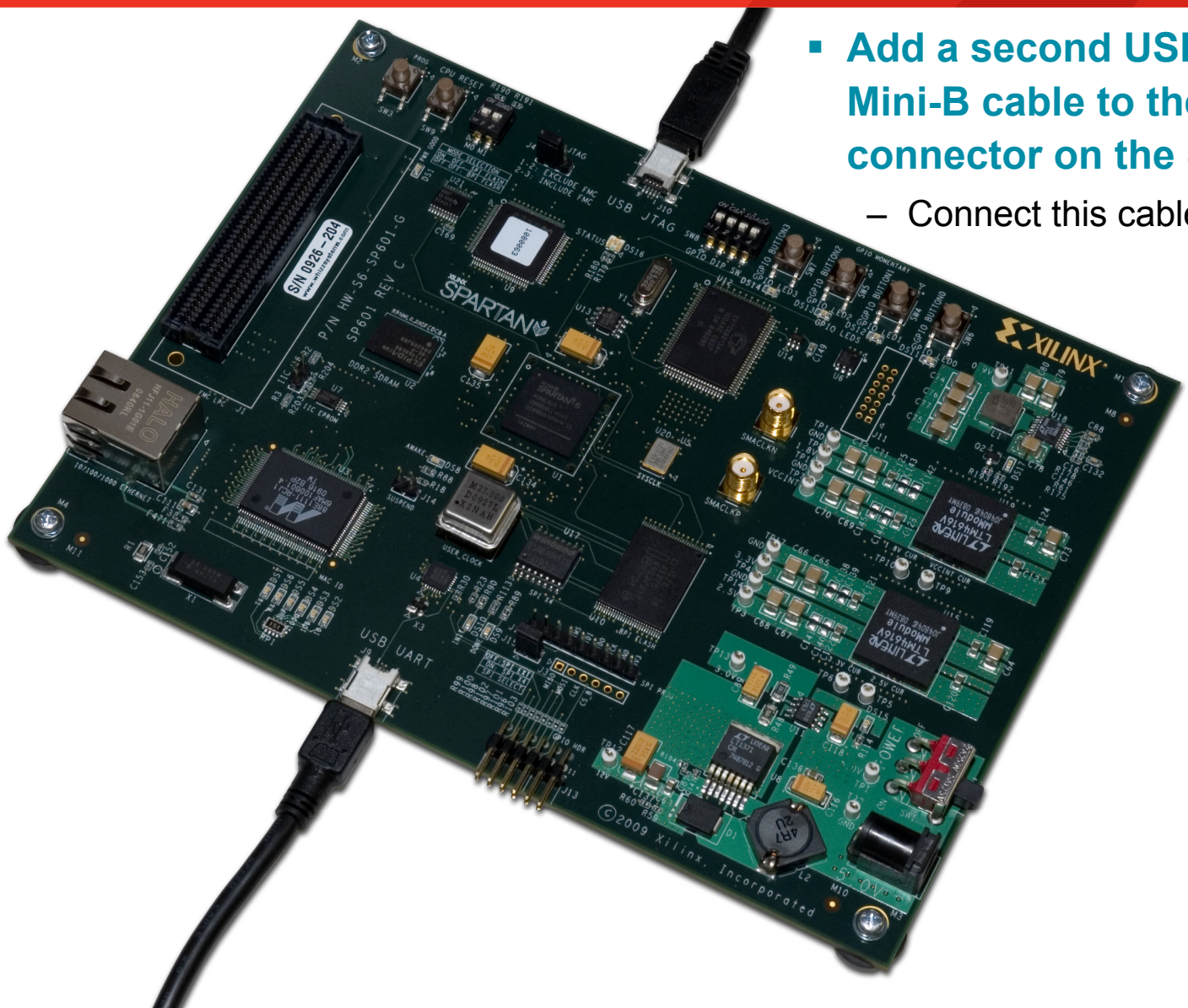
  promgen -w -p bin -c FF -o implementation/download.bin -u 0 implementation/download.bit



Note: Presentation applies to the SP601

Program SP601 BPI

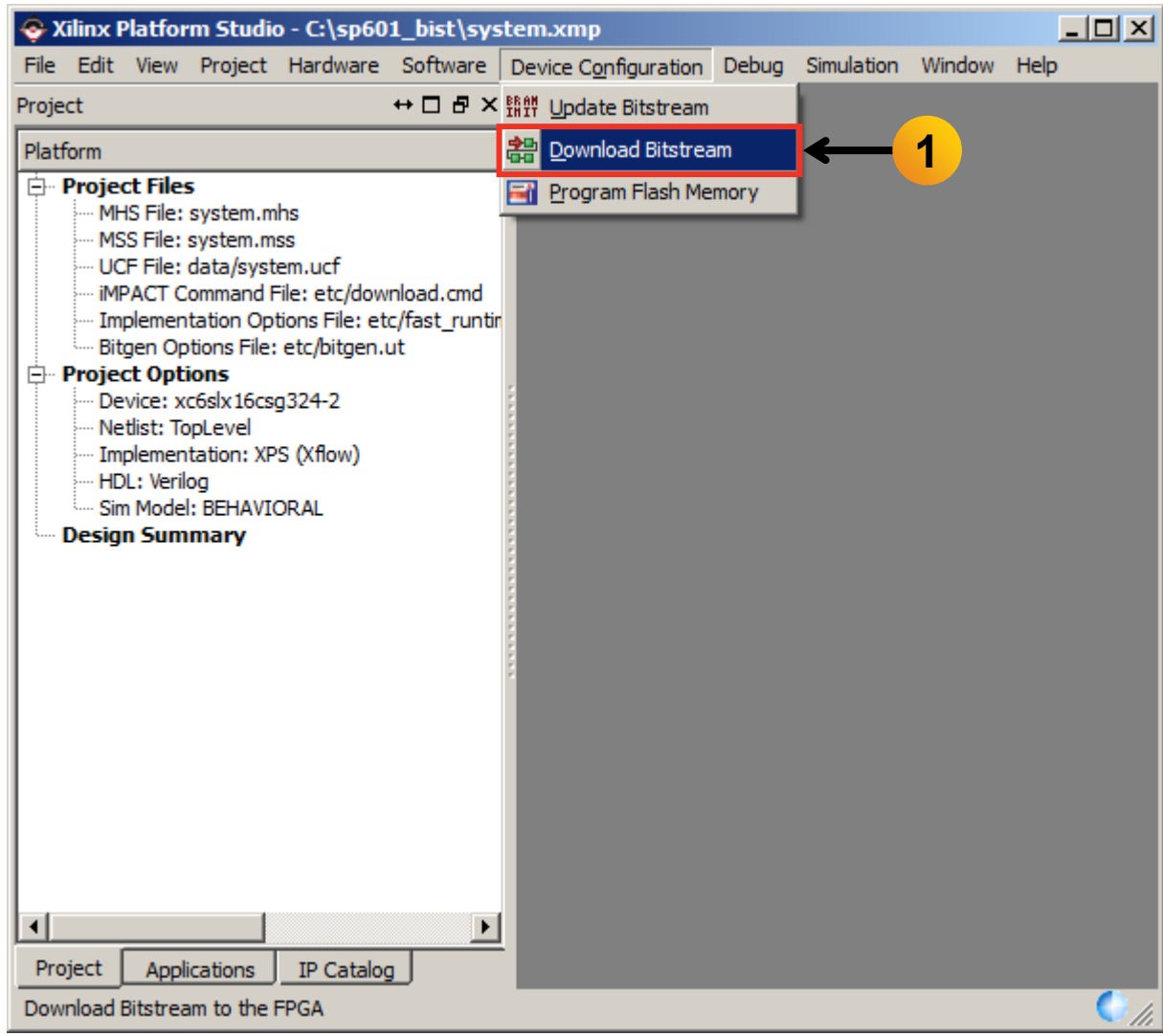
Program SP601 BPI



- **Add a second USB Type-A to Mini-B cable to the USB JTAG connector on the SP601 board**
  - Connect this cable to your PC

Program SP601 BPI

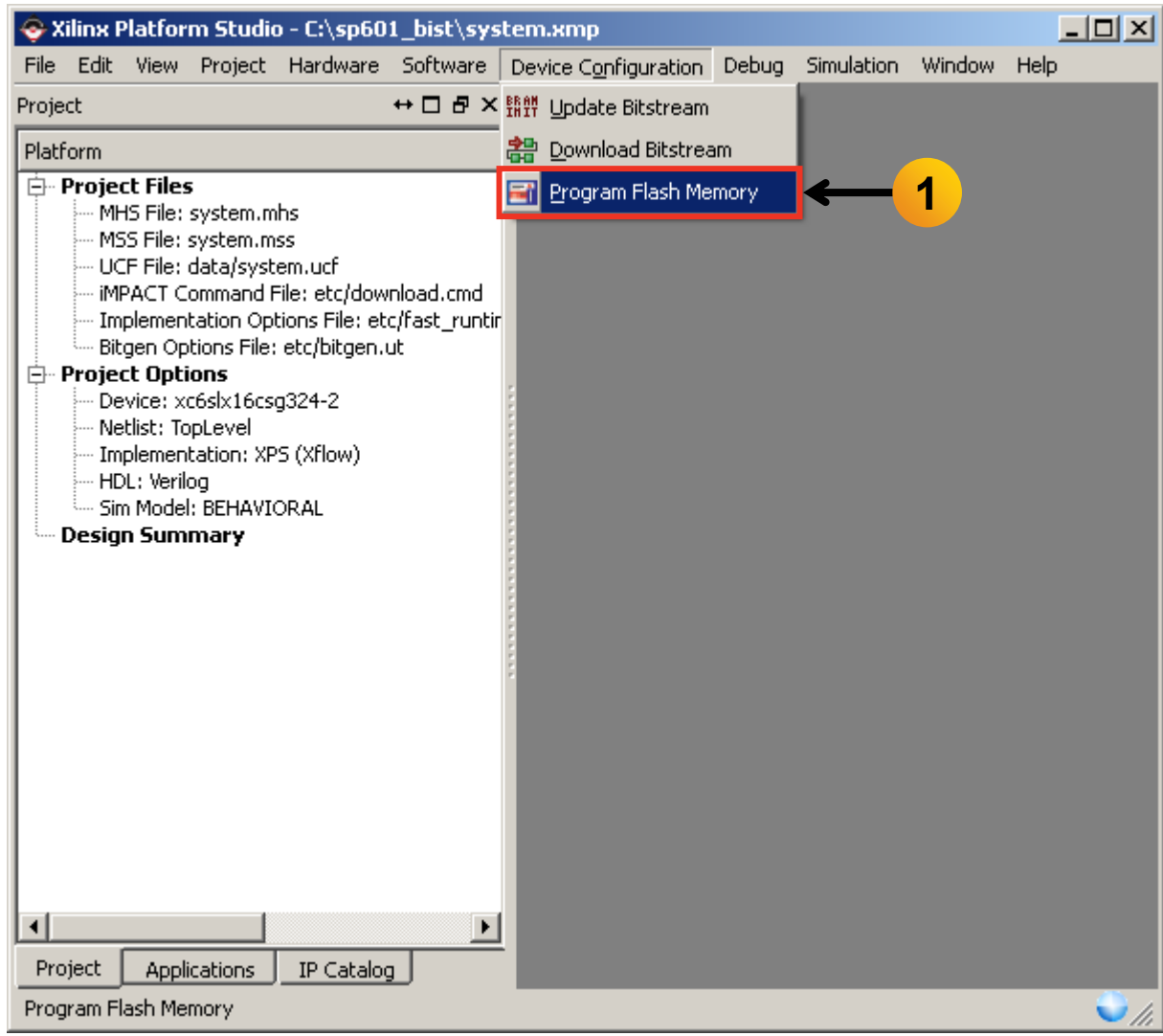
- **Download the bitstream**
  - Select **Device Configuration → Download Bitstream** (1)



Note: This step is required prior to programming the Flash with EDK

Program SP601 BPI

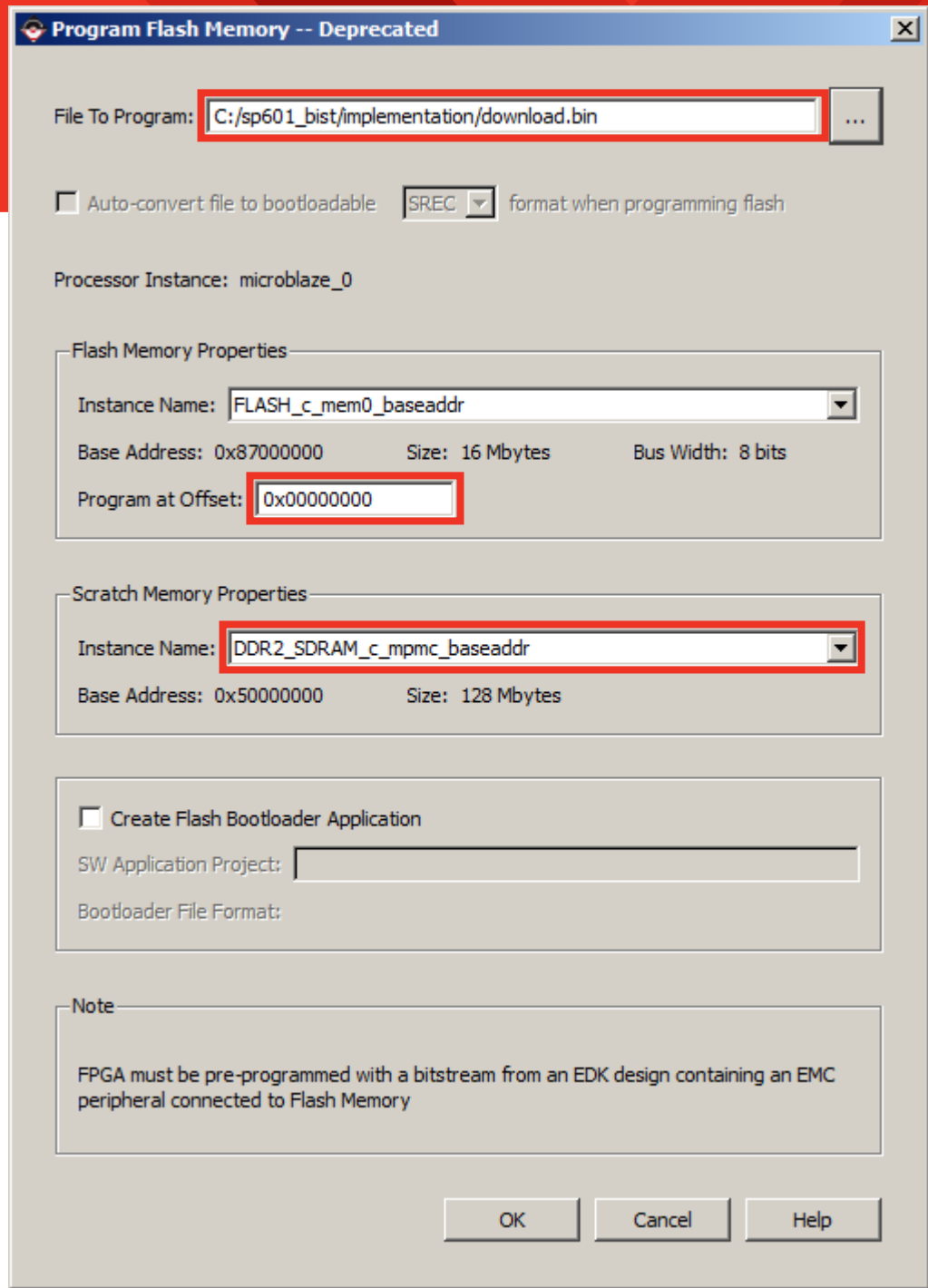
- **Program the bitstream and ELF files into BPI Flash**
  - Select **Device Configuration → Program Flash Memory** (1)



Note: This overwrites the BIST application delivered with the SP601 board

Program SP601 BPI

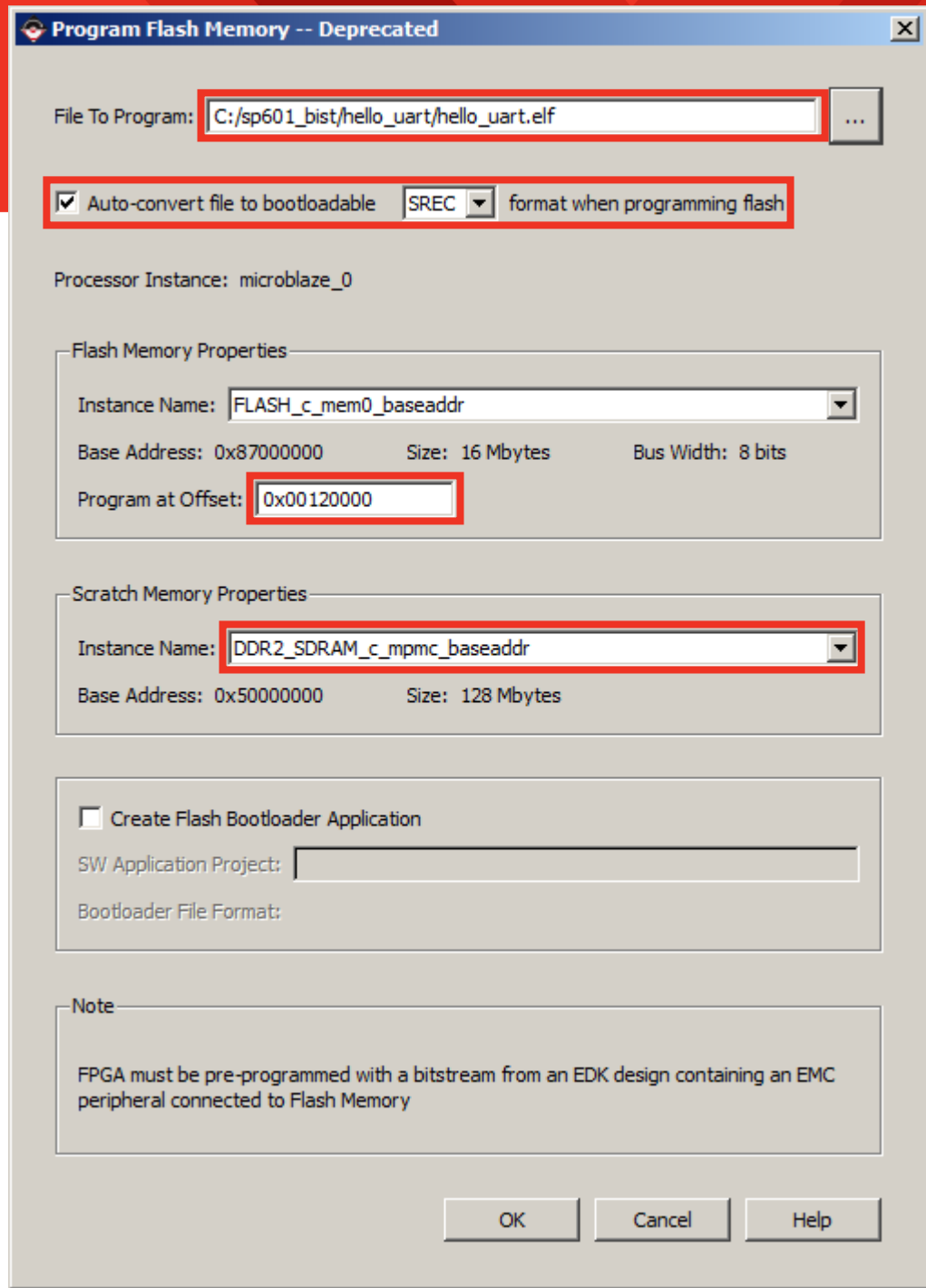
- **Program the BPI Flash with the bitstream**
  - Bitstream download.***bin***
  - Offset: **0x00000000**
  - Scratch Memory: **xps_bram_if_cntlr_1**



Note: Takes about 2 minutes

Program SP601 BPI

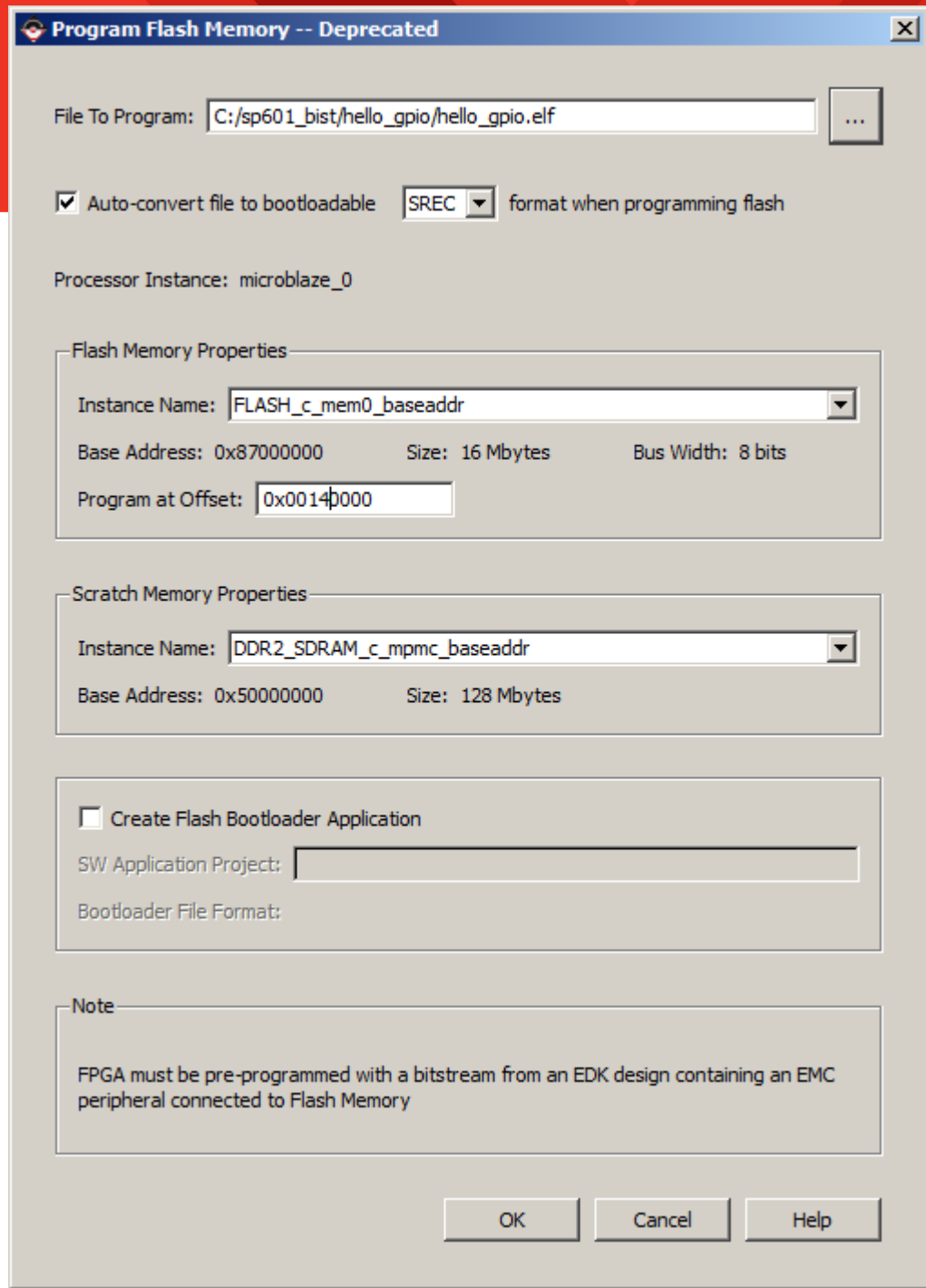
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_uart/hello_uart.elf**
  - Select Auto-convert to SREC
  - Offset: **0x00120000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Takes about a minute

Program SP601 BPI

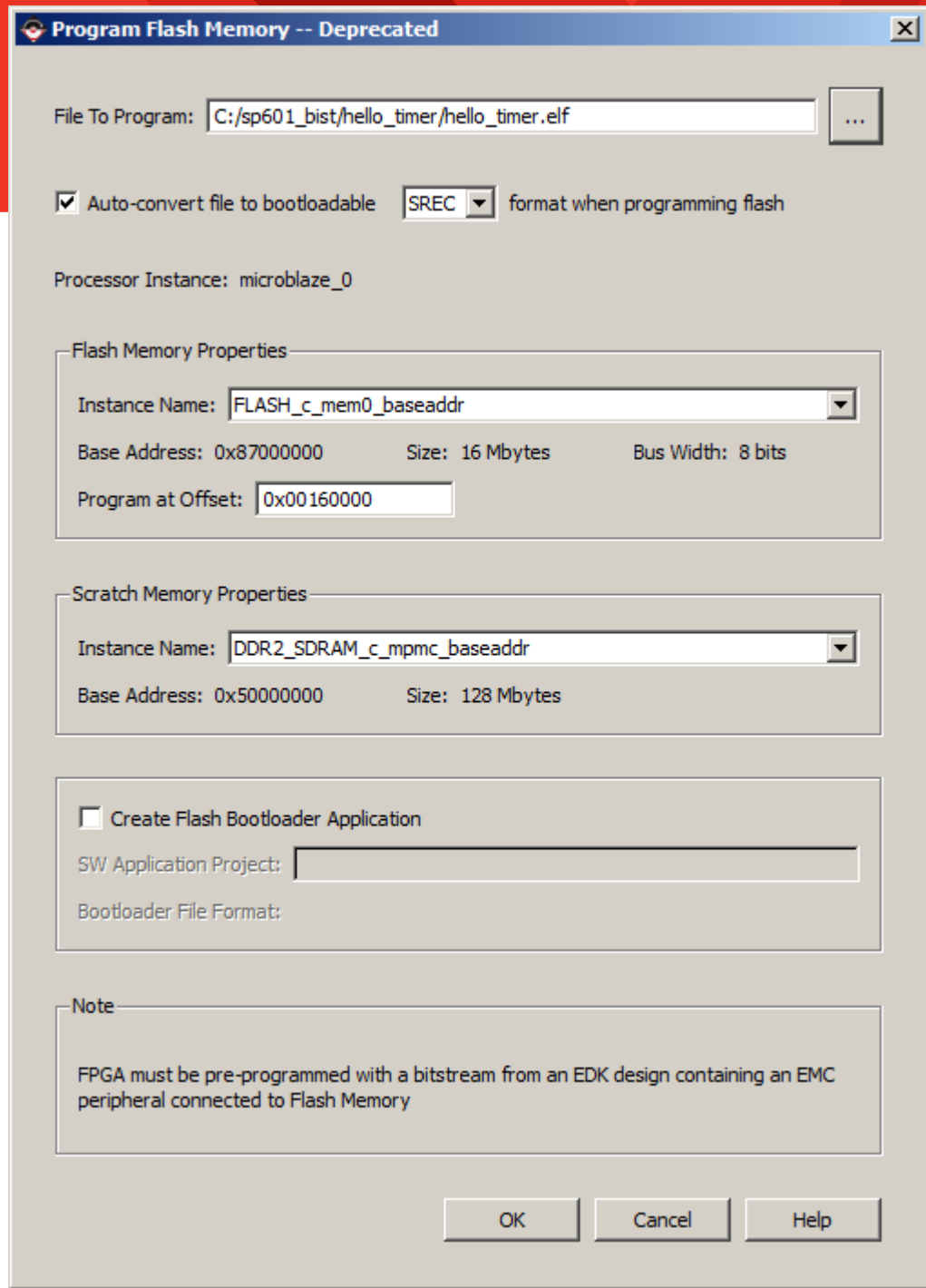
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_gpio/hello_gpio.elf**
  - Select Auto-convert to SREC
  - Offset: **0x00140000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

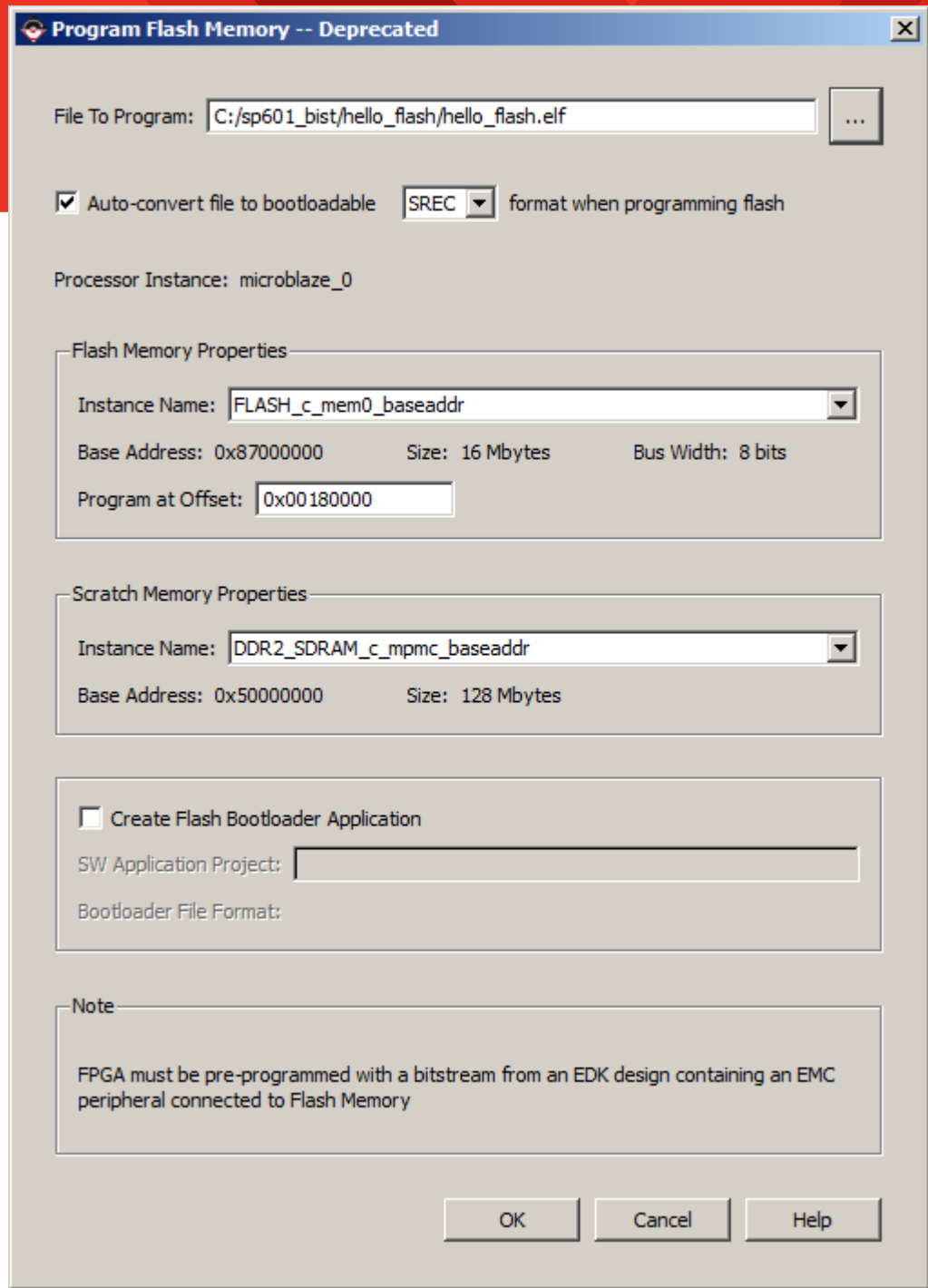
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_timer/hello_timer.elf**
  - Select Auto-convert to SREC
  - Offset: **0x00160000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

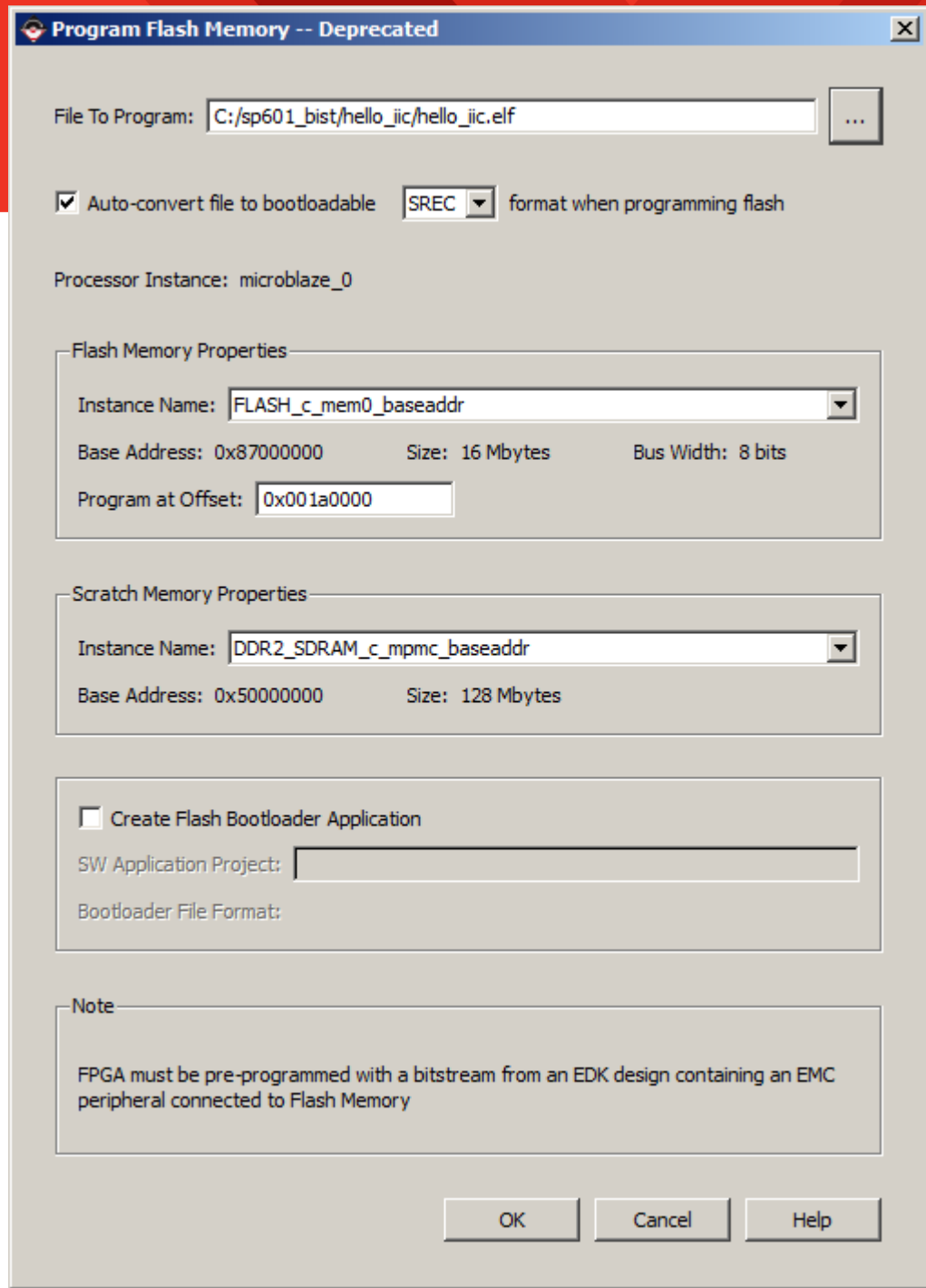
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_flash/hello_flash.elf**
  - Select Auto-convert to SREC
  - Offset: **0x00180000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

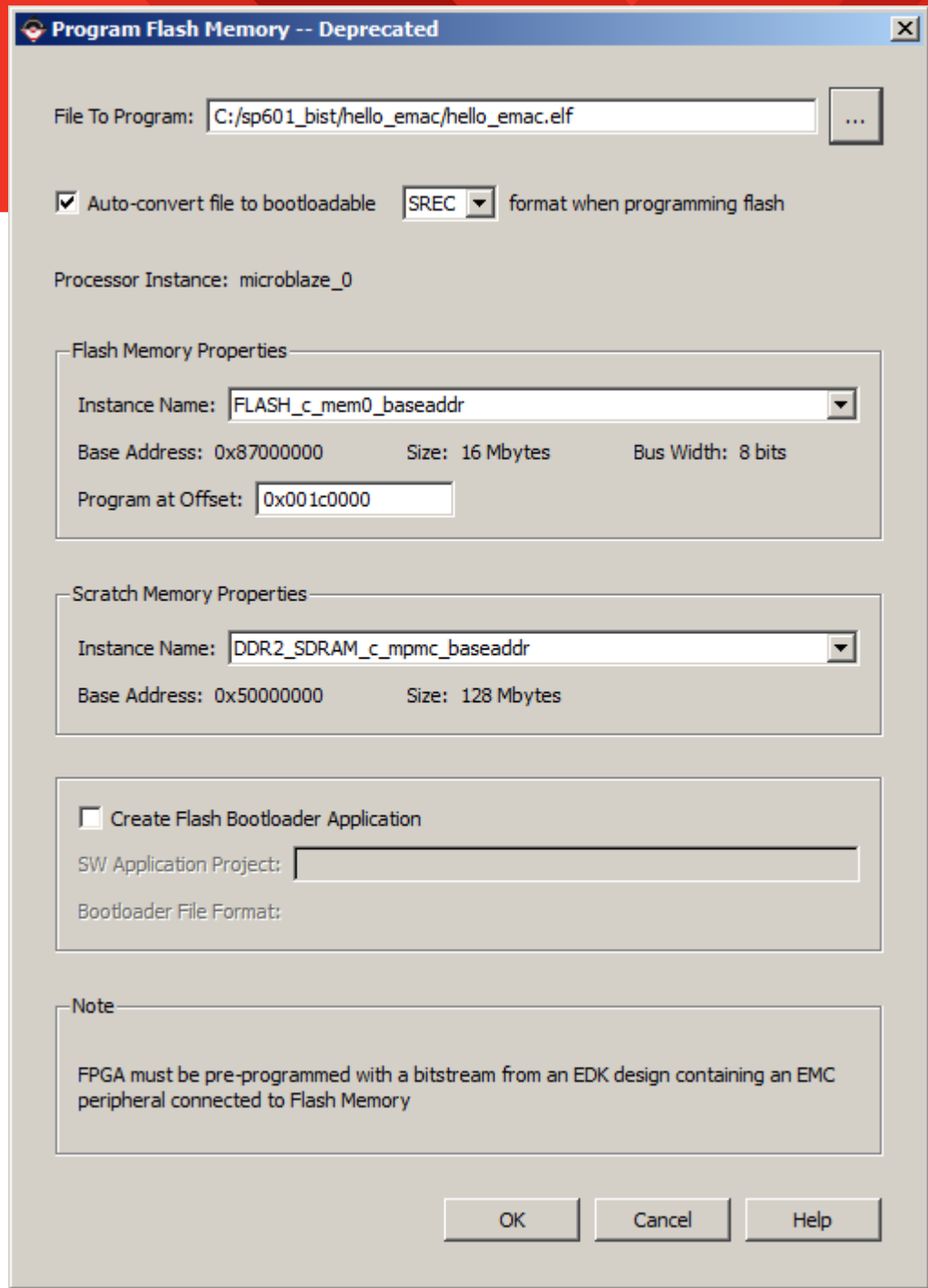
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_iic/hello_iic.elf**
  - Select Auto-convert to SREC
  - Offset: **0x001a0000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

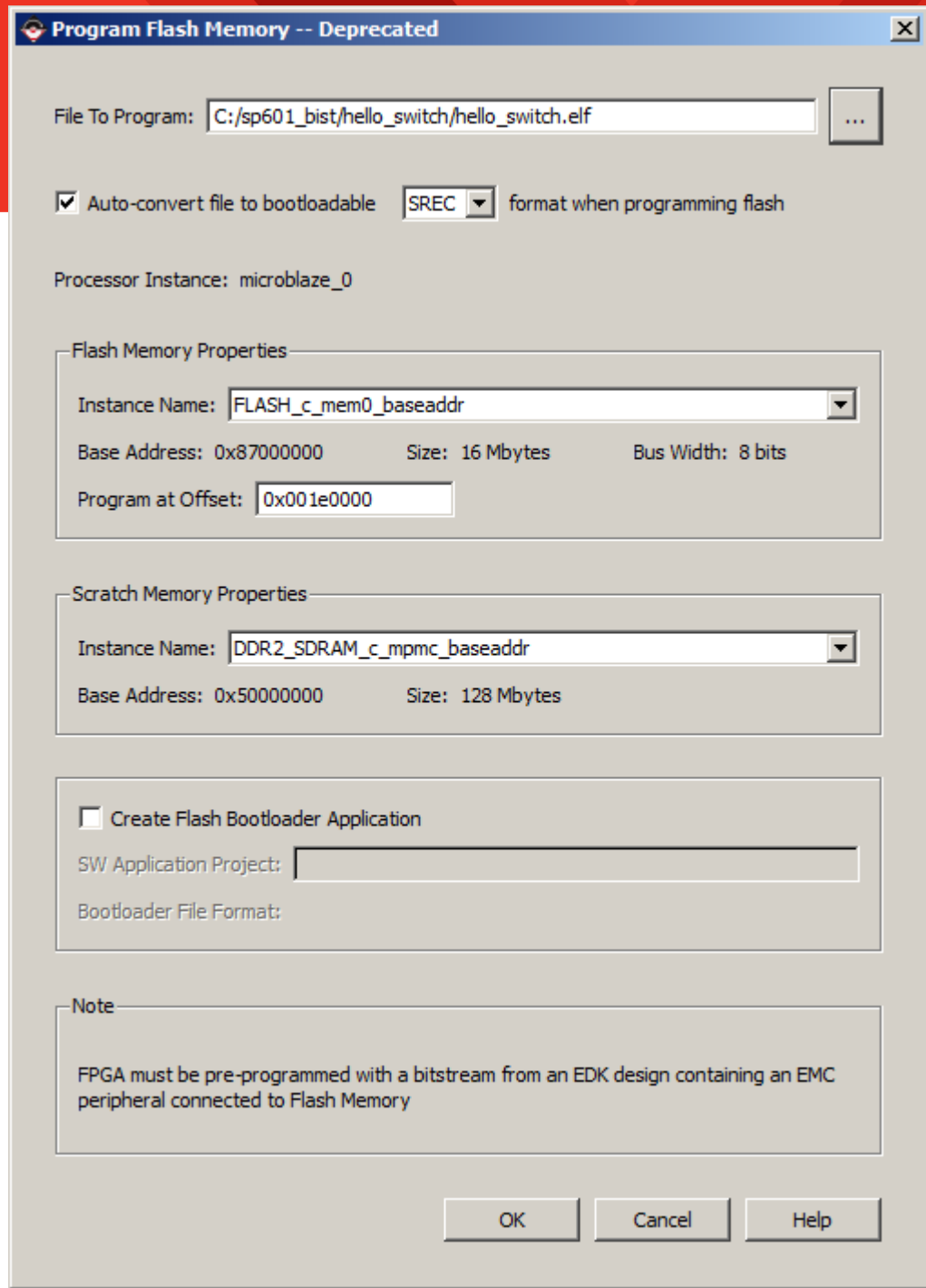
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_emac/hello_emac.elf**
  - Select Auto-convert to SREC
  - Offset: **0x001c0000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

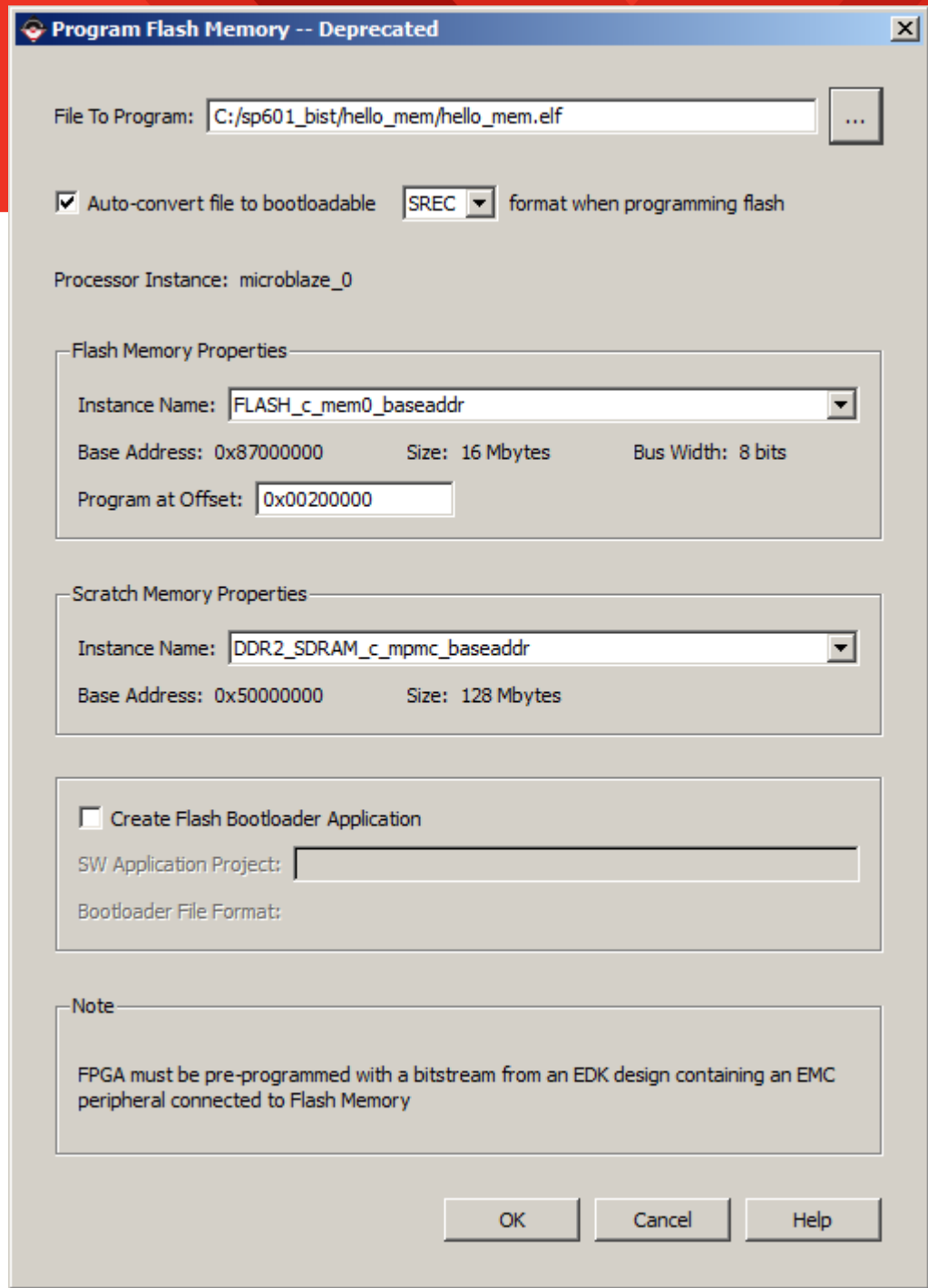
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_switch/ hello_switch.elf**
  - Select Auto-convert to SREC
  - Offset: **0x001e0000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

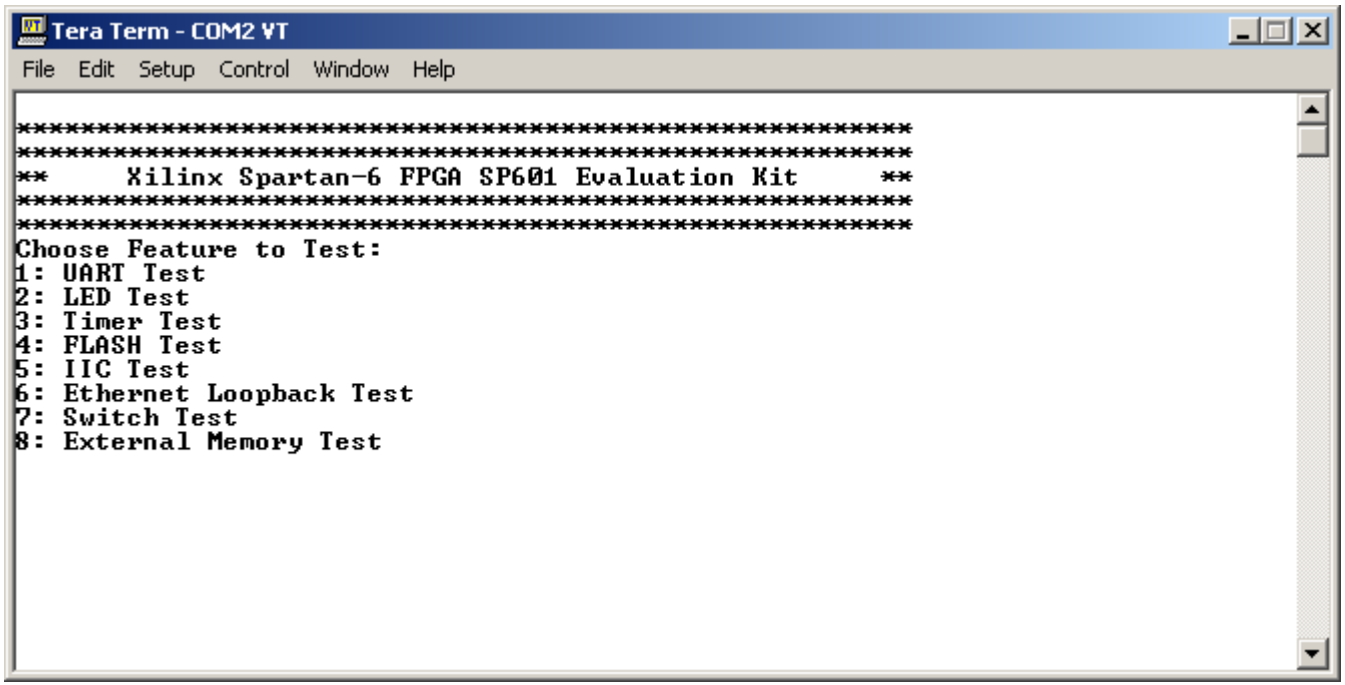
- **Program the BPI Flash with an SREC file:**
  - ELF: **hello_mem/hello_mem.elf**
  - Select Auto-convert to SREC
  - Offset: **0x00200000**
  - Scratch Memory: **DDR2_SDRAM_c_mpmc_baseaddr**



Note: Presentation applies to the SP601

Program SP601 BPI

- **Press PROG and view initial BIST screen**
  - Type "**1**" to start the UART Test



Note: Presentation applies to the SP601

References

References

- **EDK Documentation**
  - Embedded System Tools Reference Guide
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/est_rm.pdf
- **Spartan-6 Configuration**
  - Spartan-6 FPGA Configuration User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

Documentation

Documentation

- **Spartan-6**
  - Spartan-6 FPGA Family
    http://www.xilinx.com/products/spartan6/index.htm
- **SP601 Documentation**
  - Spartan-6 FPGA SP601 Evaluation Kit
    http://www.xilinx.com/products/devkits/EK-S6-SP601-G.htm
  - SP601 Getting Started Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug523.pdf
  - SP601 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf
  - SP601 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug524.pdf