

SP601 Built-In Self Test Flash Application

December 2009

Overview

- **Xilinx SP601 Board**
- **Software Requirements**
- **SP601 Setup**
- **SP601 BIST (Built-In Self Test)**
- **Compile SP601 BIST Design**
- **Program SP601 BPI**
- **References**

Note: This presentation applies to the SP601

SP601 BIST Design Description

▪ Description

- The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

▪ Reference Design IP

- EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_iic, xps_mch_emc, xps_spi, util_io_mux, util_bus_split, xps_ethernetlite
 - [Embedded System Tools Reference Guide](#) (UG111)
 - http://www.xilinx.com/ise/embedded/edk_ip.htm

▪ Reference Design Source

- rdf0045.zip

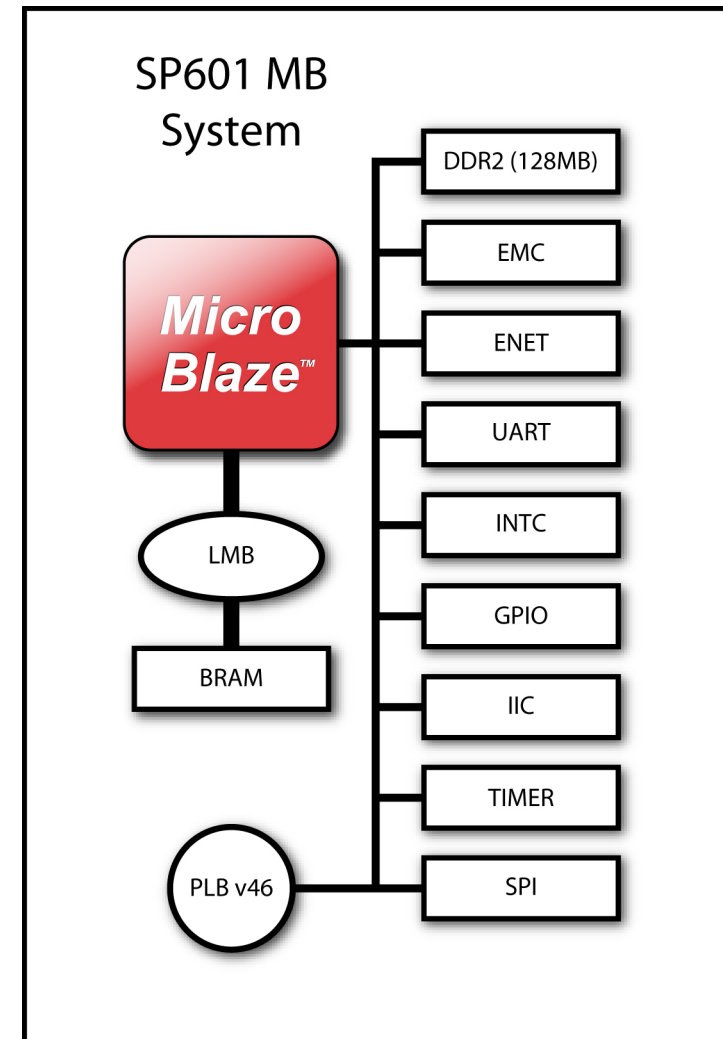
Embedded Processor Design

- **The provided embedded reference design is supported “as is”**
 - Please refer to the click through license agreement
- **Embedded reference design has been verified on the SP601 Evaluation Kit**
 - Design consists of Early Access IP
 - Design may change in subsequent releases
- **The reference design will allow users to:**
 - Re-build and verify functionality on the SP601 evaluation kit

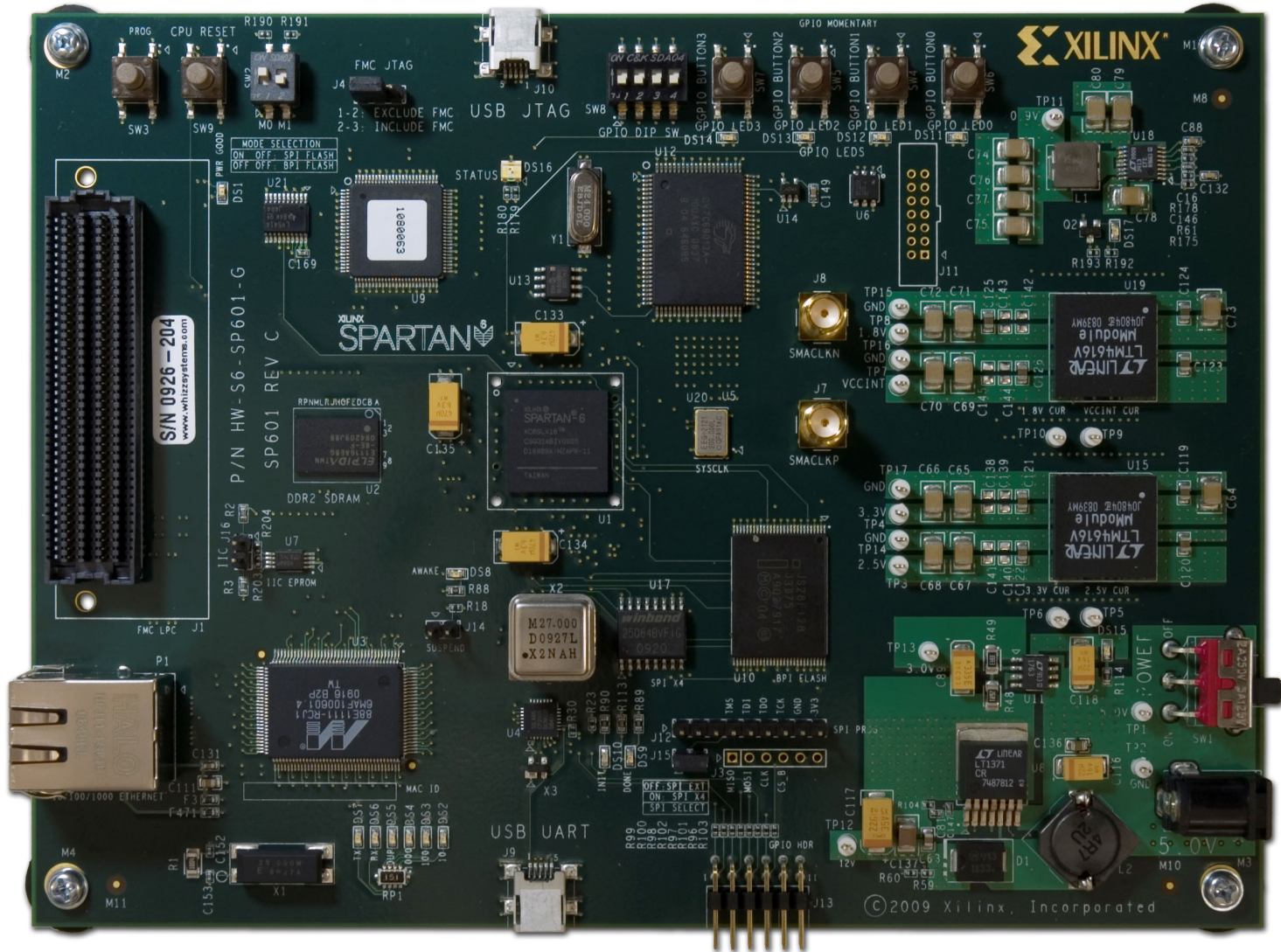
SP601 MicroBlaze Hardware

▪ The SP601 MicroBlaze Design Hardware includes:

- DDR2 Interface (128 MB)
- BRAM
- External Memory Controller (EMC)
 - Flash Memory
- Networking
- UART
- Interrupt Controller
- GPIO (IIC, LEDs and LCD)
- PLB Arbiter
- SPI



Xilinx SP601 Board



ISE Software Requirement

- **Xilinx ISE 11.4 software**

- Install the Webpack for the Spartan-6 LX16 devices
- Run XilinxUpdate and download the Webpack devices



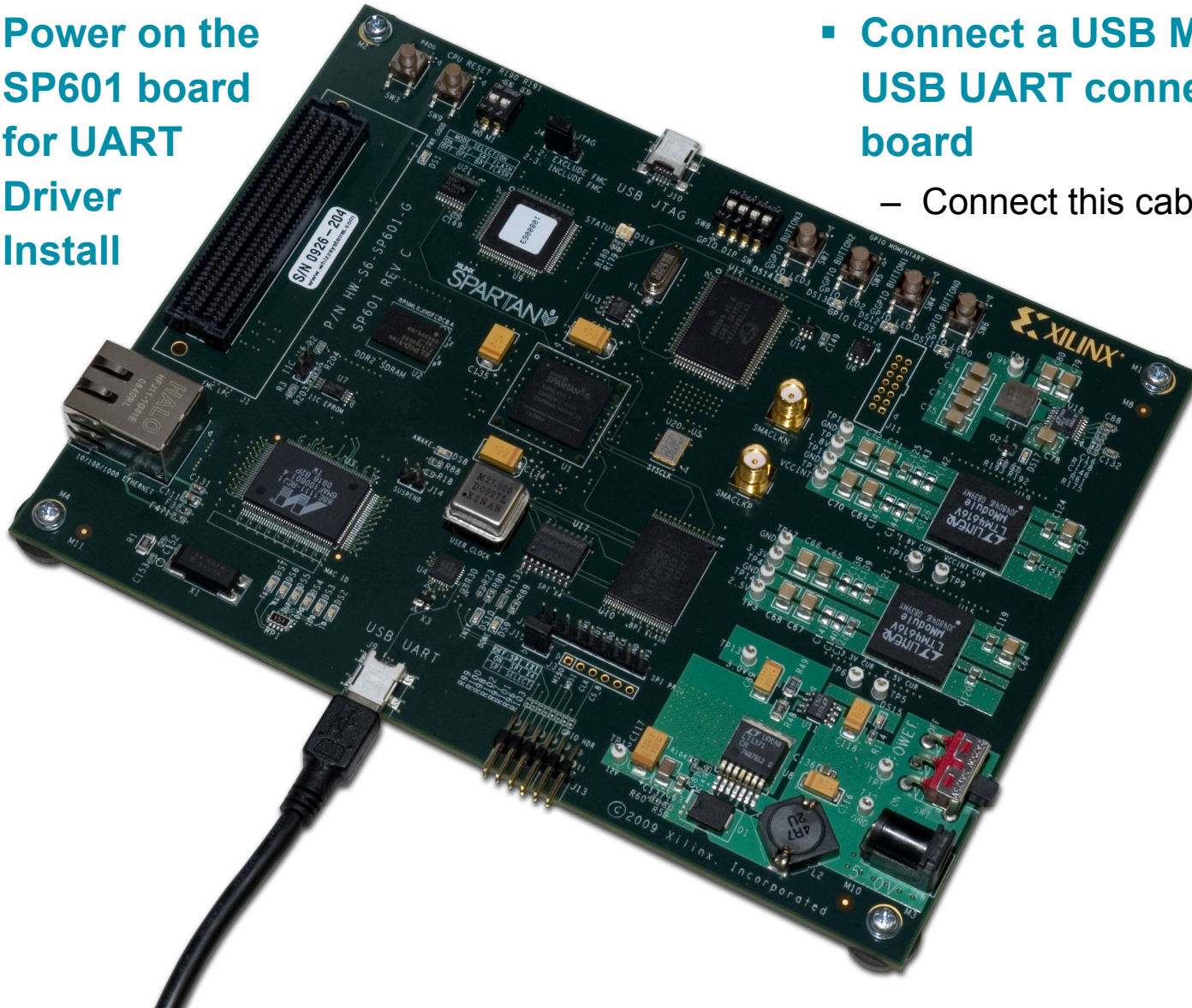
EDK Software Requirement

- Xilinx EDK 11.4 software



SP601 Setup

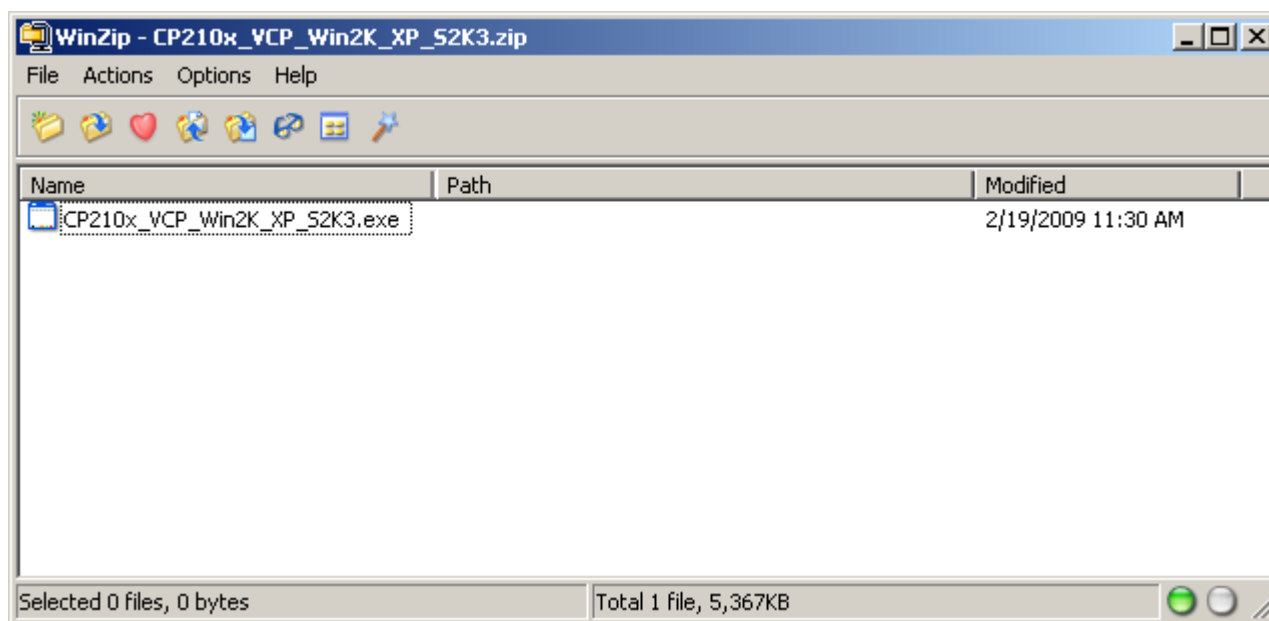
- Power on the SP601 board for UART Driver Install
- Connect a USB Mini-B Cable to the USB UART connector on the SP601 board
 - Connect this cable to your PC



SP601 Setup

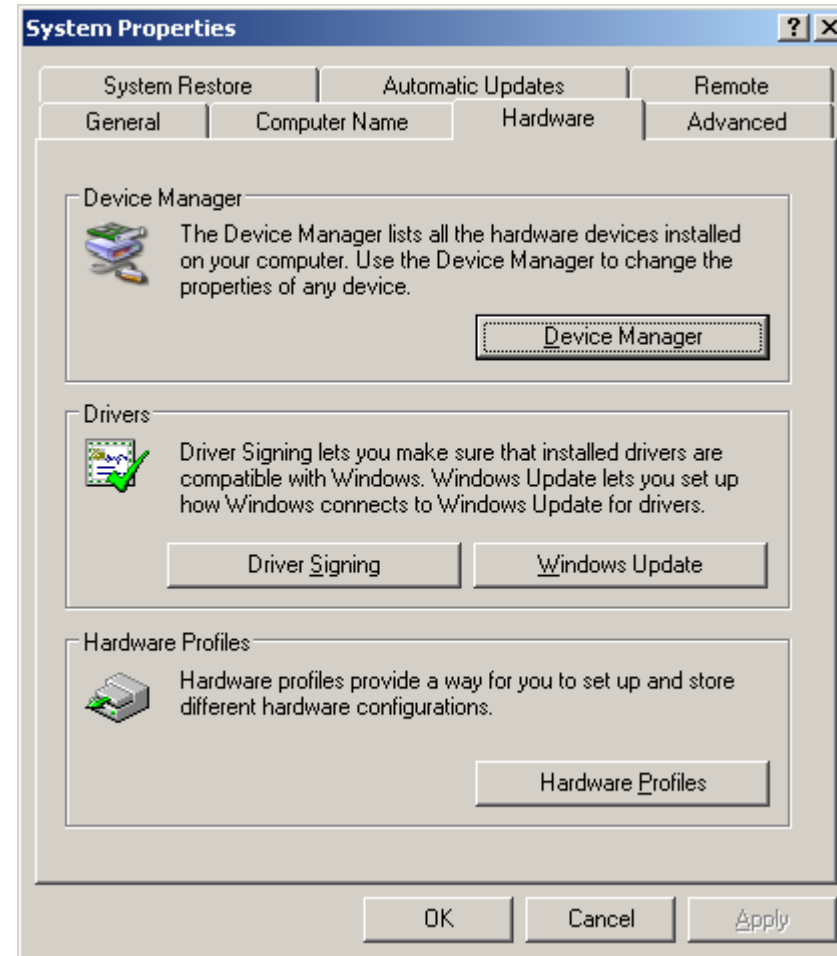
■ Install USB UART Drivers

- https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip



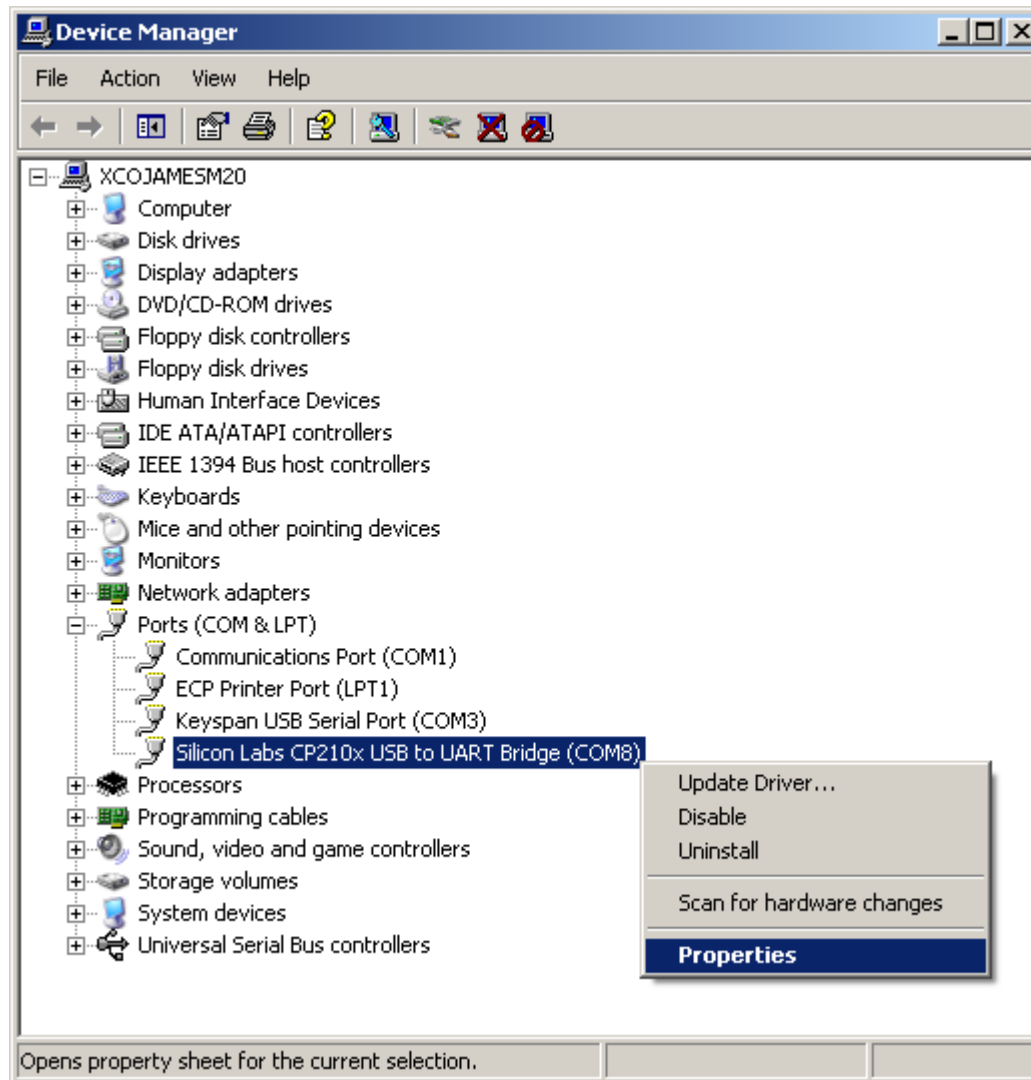
SP601 Setup

- **Right-click on My Computer and select Properties**
 - Select the Hardware tab
 - Click on Device Manager



SP601 Setup

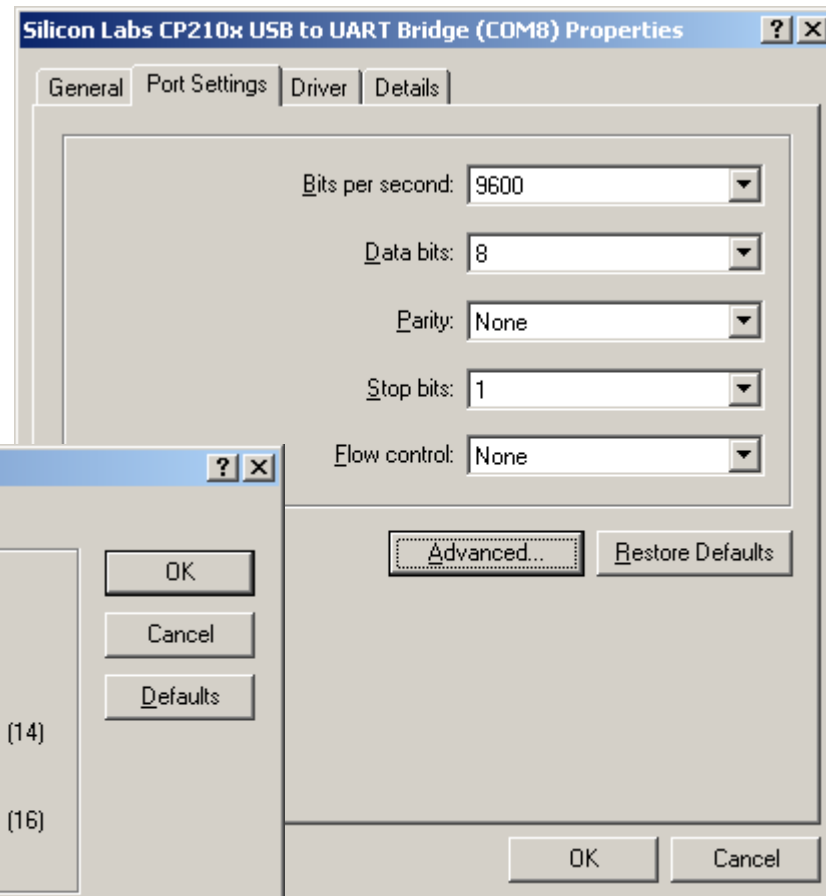
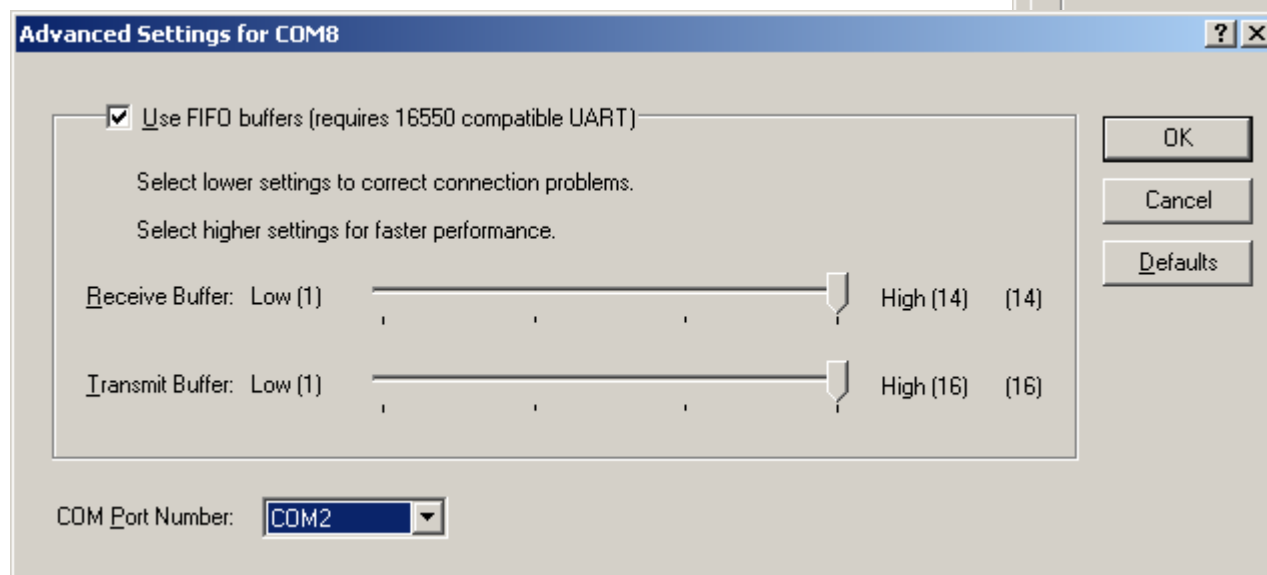
- **Expand the Ports Hardware**
 - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select **Properties**



SP601 Setup

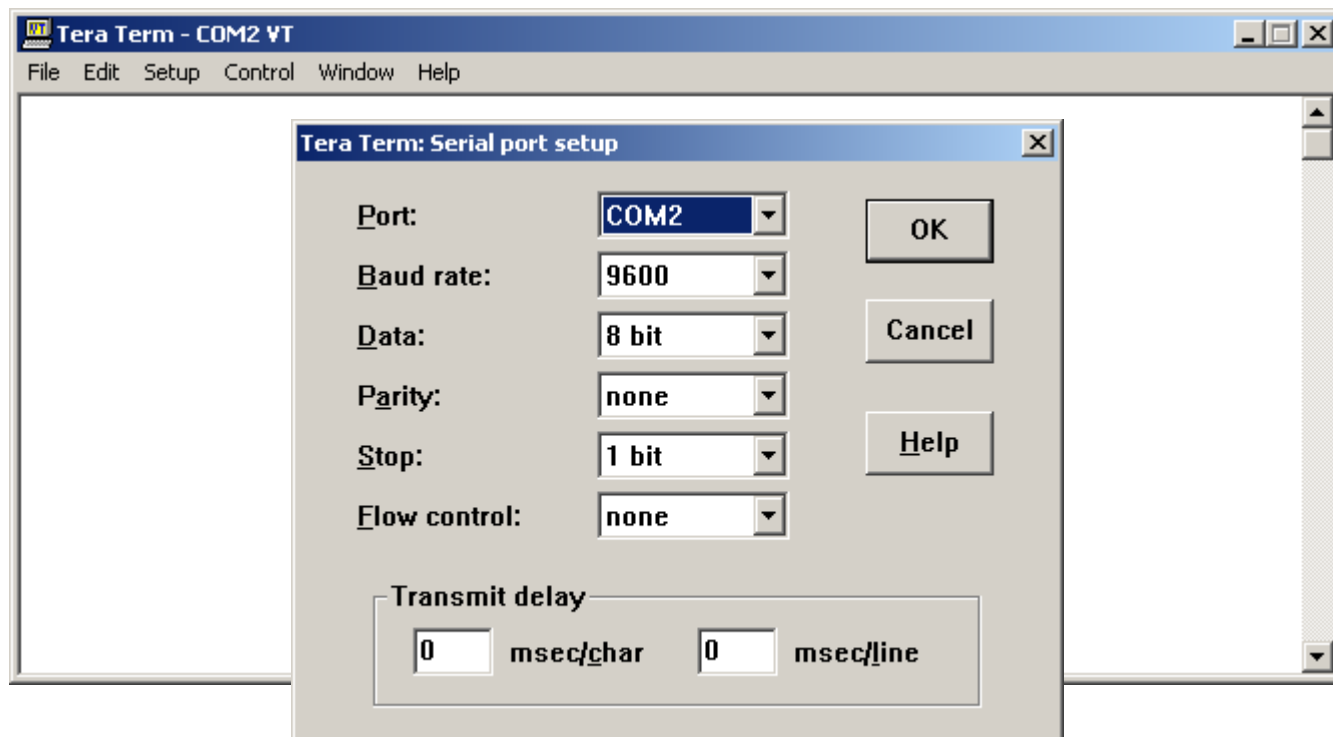
■ Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



SP601 Setup

- **Board Power must be on before starting Tera Term**
- **Start the Terminal Program**
 - Select your USB Com Port
 - Set the baud to 9600

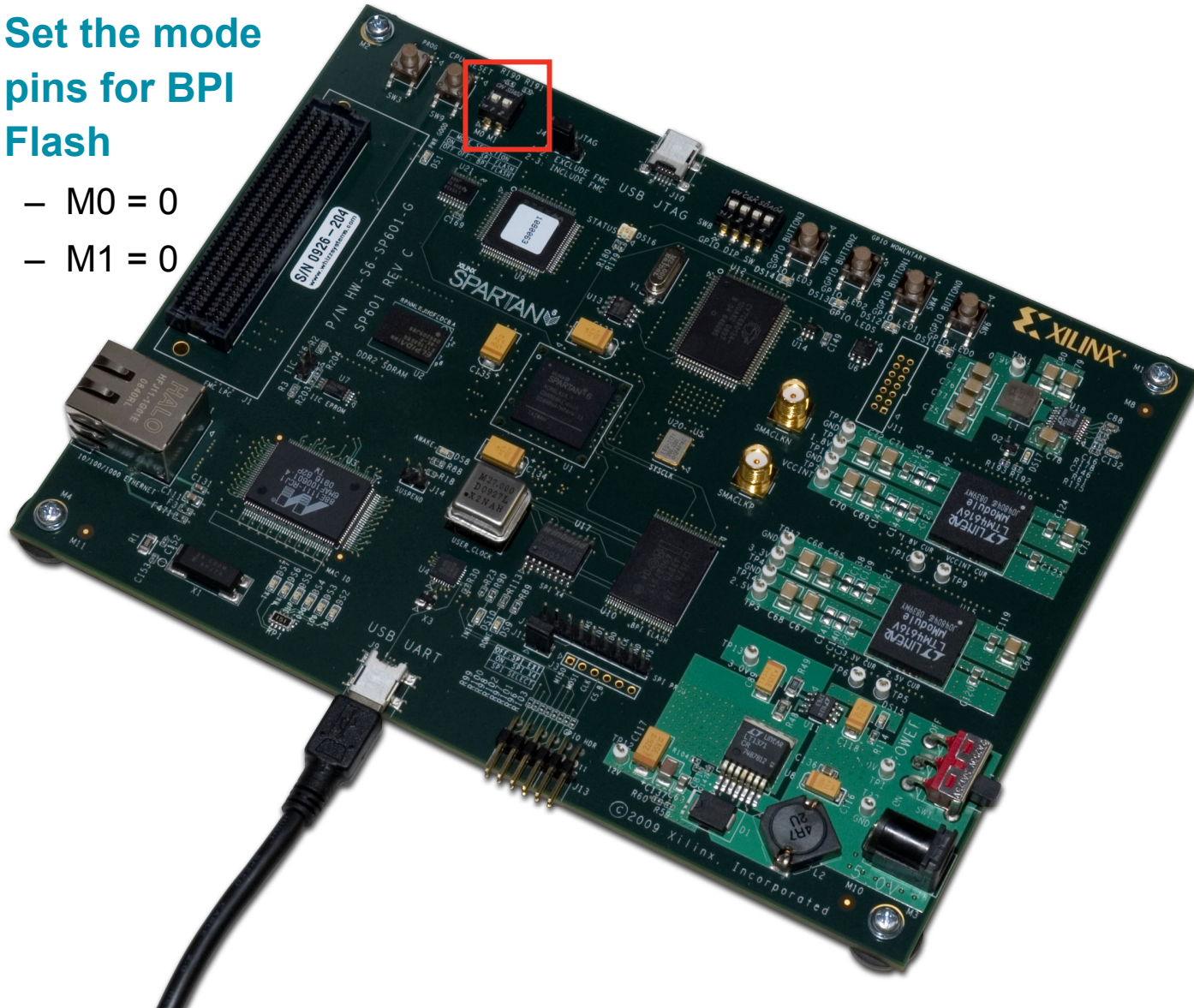


Note: Tera Term may need to be restarted if board power is cycled

SP601 Setup

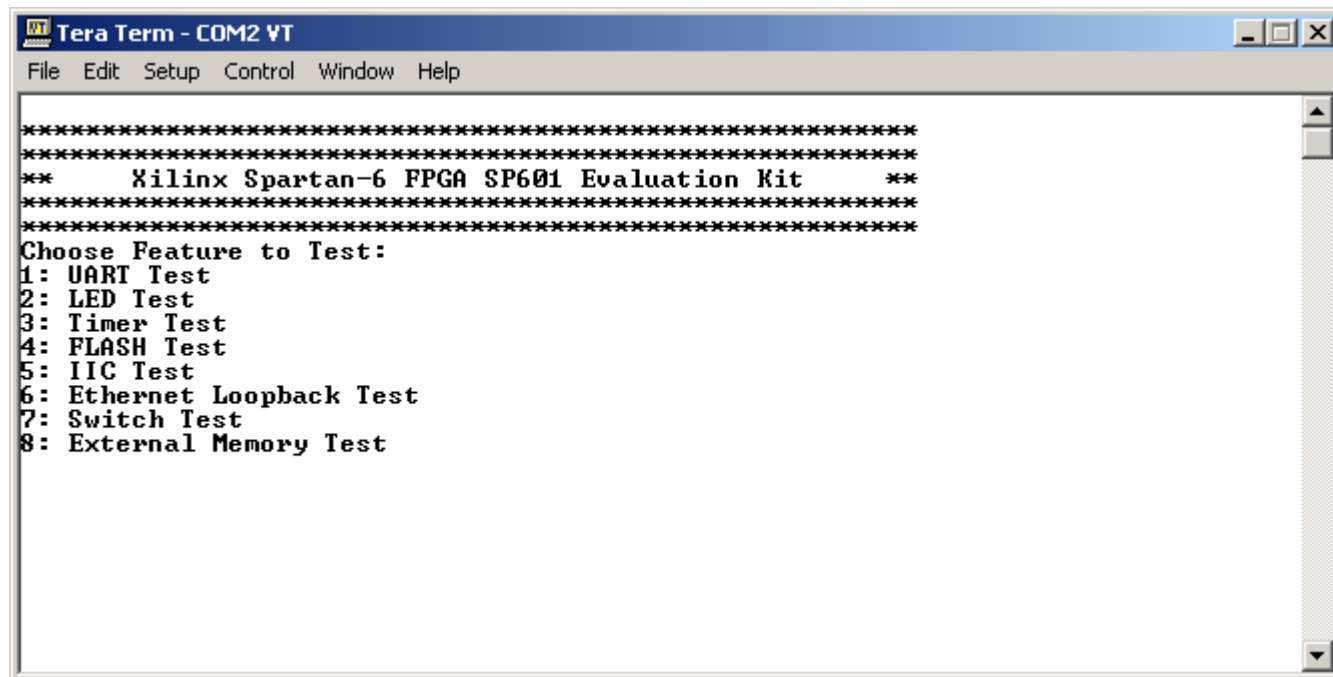
- Set the mode pins for BPI Flash

- M0 = 0
- M1 = 0



SP601 BIST

- Press PROG and view initial BIST screen
 - Type “1” to start the UART Test



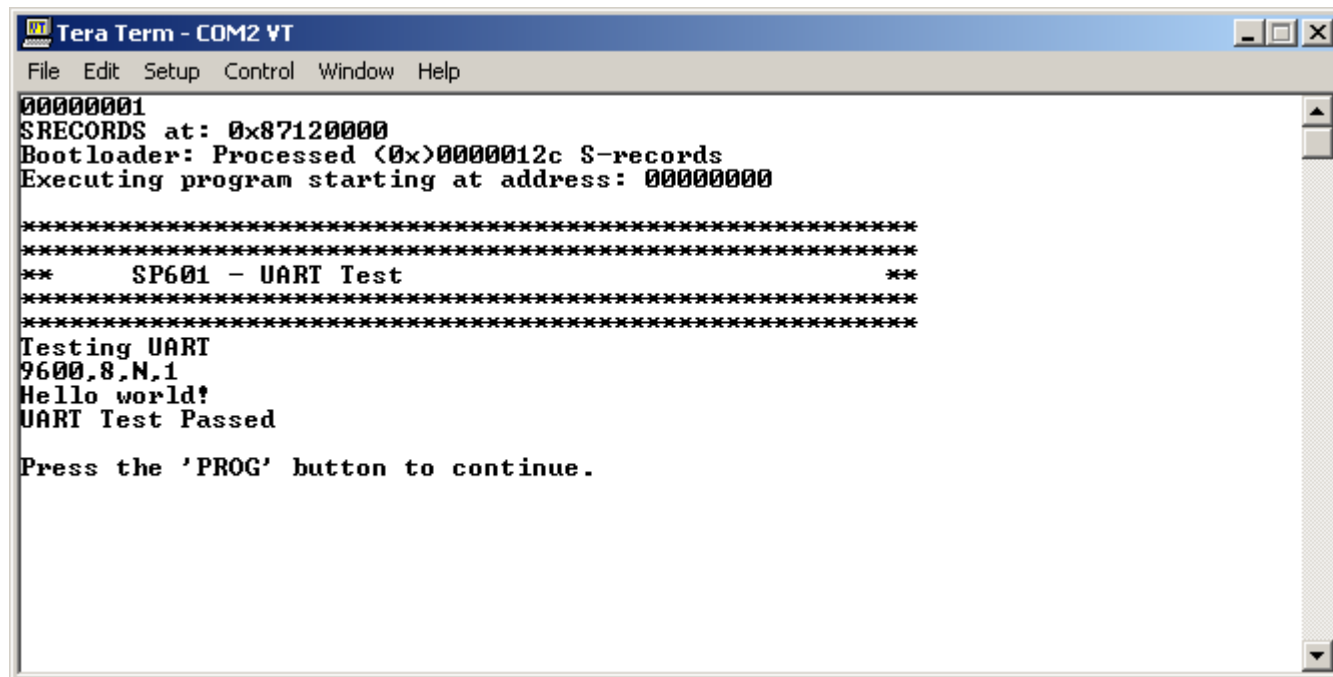
```
Tera Term - COM2 VT
File Edit Setup Control Window Help

*****
*****
**      Xilinx Spartan-6 FPGA SP601 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
```


SP601 BIST

- **UART Test completed**

- Press **PROG** and type **2** to begin LED Test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
00000001
SRECORDS at: 0x87120000
Bootloader: Processed (0x)0000012c S-records
Executing program starting at address: 00000000

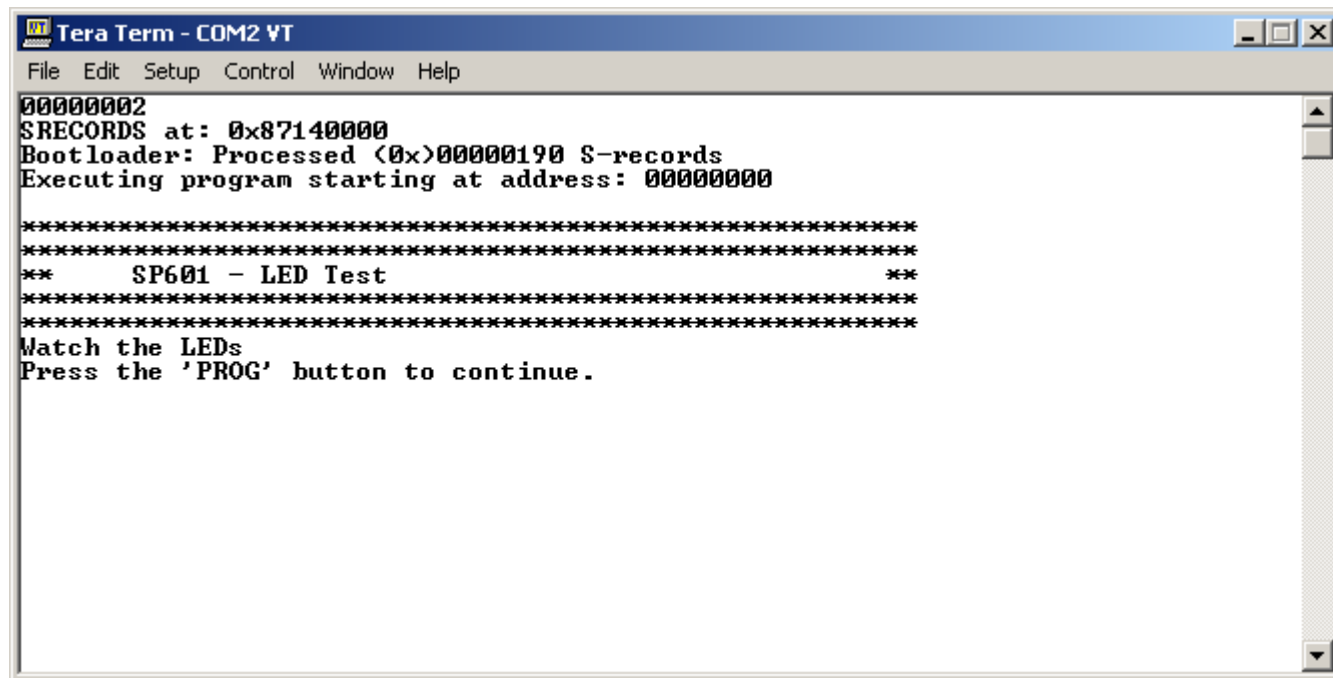
*****
*****
**      SP601 - UART Test      **
*****
*****
Testing UART
9600,8,N,1
Hello world!
UART Test Passed

Press the 'PROG' button to continue.
```

SP601 BIST

- LED Test completed

- Press **PROG** and type **3** to begin Timer Test



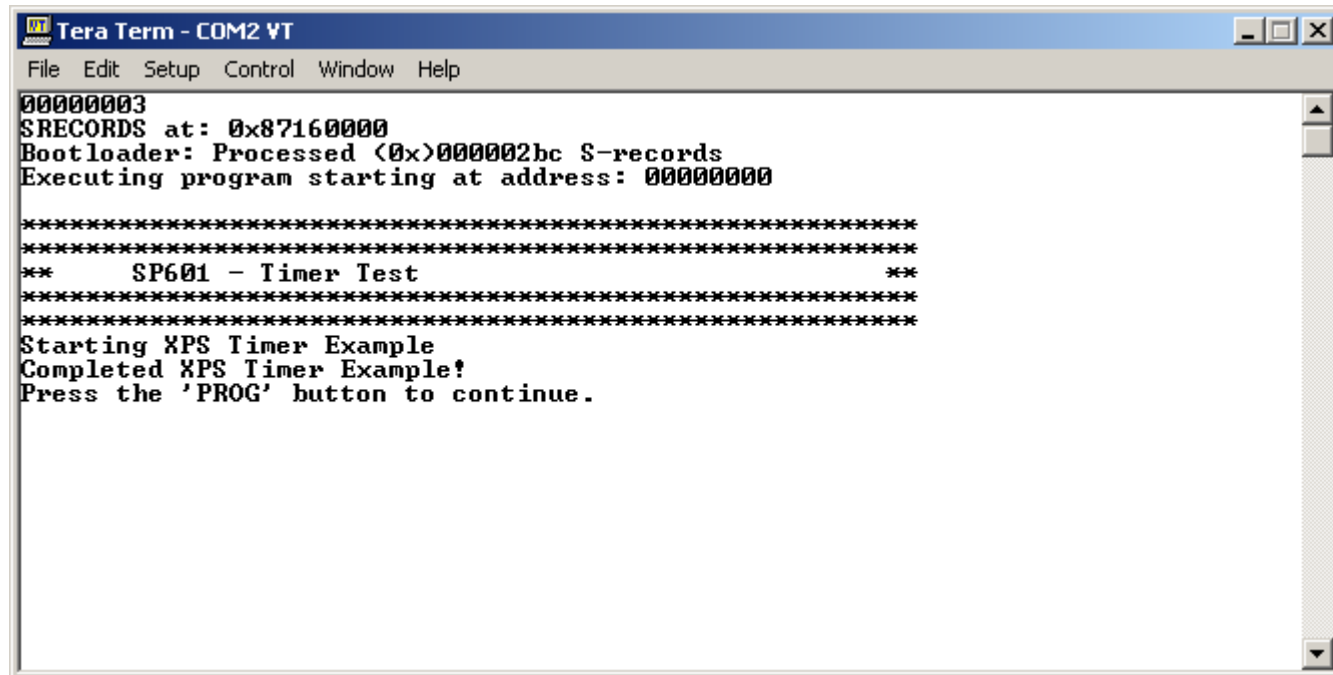
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
000000002
SRECORDS at: 0x87140000
Bootloader: Processed (0x)00000190 S-records
Executing program starting at address: 00000000

*****
*****
**      SP601 - LED Test      **
*****
*****
Watch the LEDs
Press the 'PROG' button to continue.
```

SP601 BIST

- **Timer Test completed**

- Press **PROG** and type **4** to begin Flash test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
00000003
SRECORDS at: 0x87160000
Bootloader: Processed (0x)000002bc S-records
Executing program starting at address: 00000000

*****
*****
**      SP601 - Timer Test      **
*****
*****
Starting XPS Timer Example
Completed XPS Timer Example!
Press the 'PROG' button to continue.
```

Note: Do not press PROG until this test completes

- Flash Test completed

- Press **PROG** and type **5** to begin IIC EEPROM Test

```

Tera Term - COM2 VT
File Edit Setup Control Window Help

00000004
SRECORDS at: 0x87180000
Bootloader: Processed (0x)000003e8 S-records
Executing program starting at address: 00000000

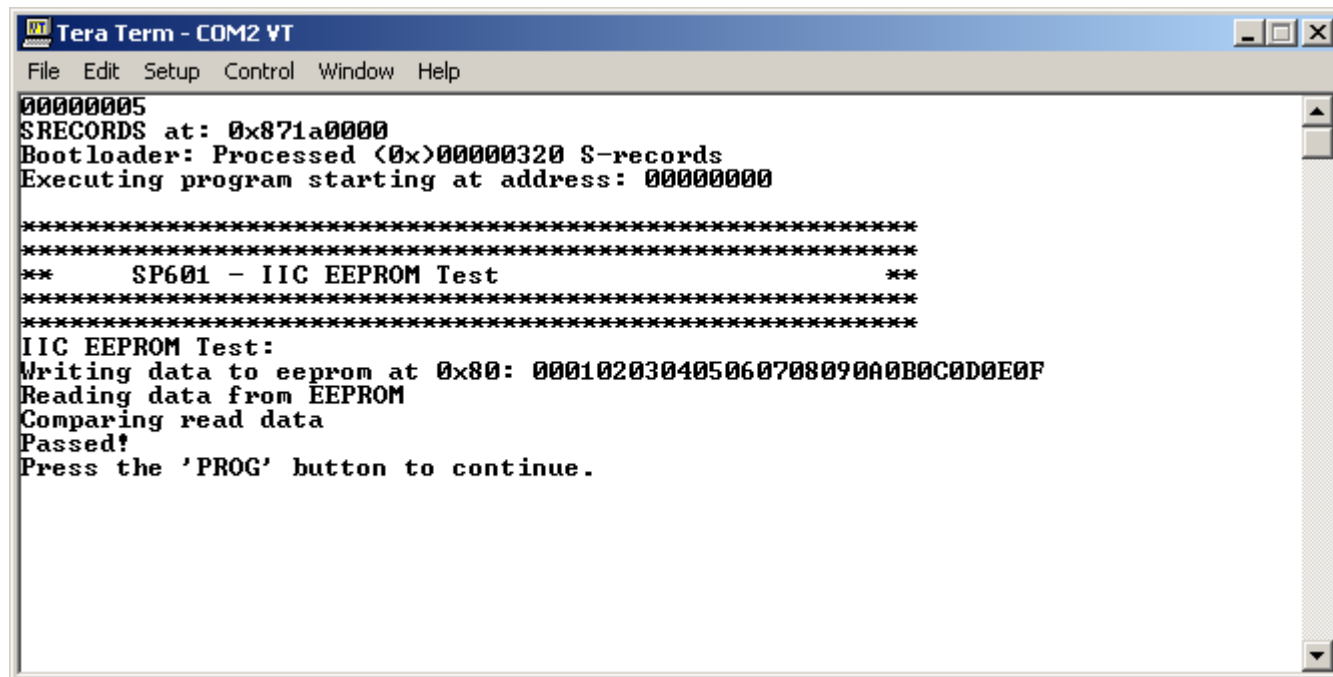
*****
*****
**      SP601 - FLASH Test      **
*****
*****
-- Initialized the Flash library successfully --
-- Unlocked all the blocks successfully --
-- Erased the Flash memory contents at offset 0x0300000 successfully --
-- Writing: 000102030405060708090A0B0C0D0E0F101112131415161718191A1B1C1D1E1F2021
22232425262728292A2B2C2D2E2F303132333435363738393A3B3C3D3E3F40414243444546474849
4A4B4C4D4E4F505152535455565758595A5B5C5D5E5F606162636465666768696A6B6C6D6E6F7071
72737475767778797A7B7C7D7E7F808182838485868788898A8B8C8D8E8F90919293949596979899
9A9B9C9D9E9F0A01A2A3A4A5A6A7A8A9AABACADAEAFB0B1B2B3B4B5B6B7B8B9BABBBBCBDBEBFC0C1
C2C3C4C5C6C7C8C9CACBCCDCECFD0D1D2D3D4D5D6D7D8D9DADBDCDDDEDFE0E1E2E3E4E5E6E7E8E9
EAECEDEEEFF0F1F2F3F4F5F6F7F8F9FAFBFCFDFEFF
-- Write operation at offset 0x0300000 completed successfully --
-- Read operation completed successfully --
-- Data comparison successful --
Press the 'PROG' button to continue.

```

SP601 BIST

- IIC EEPROM Test completed

- Press **PROG** and type **6** to begin Ethernetlite Test



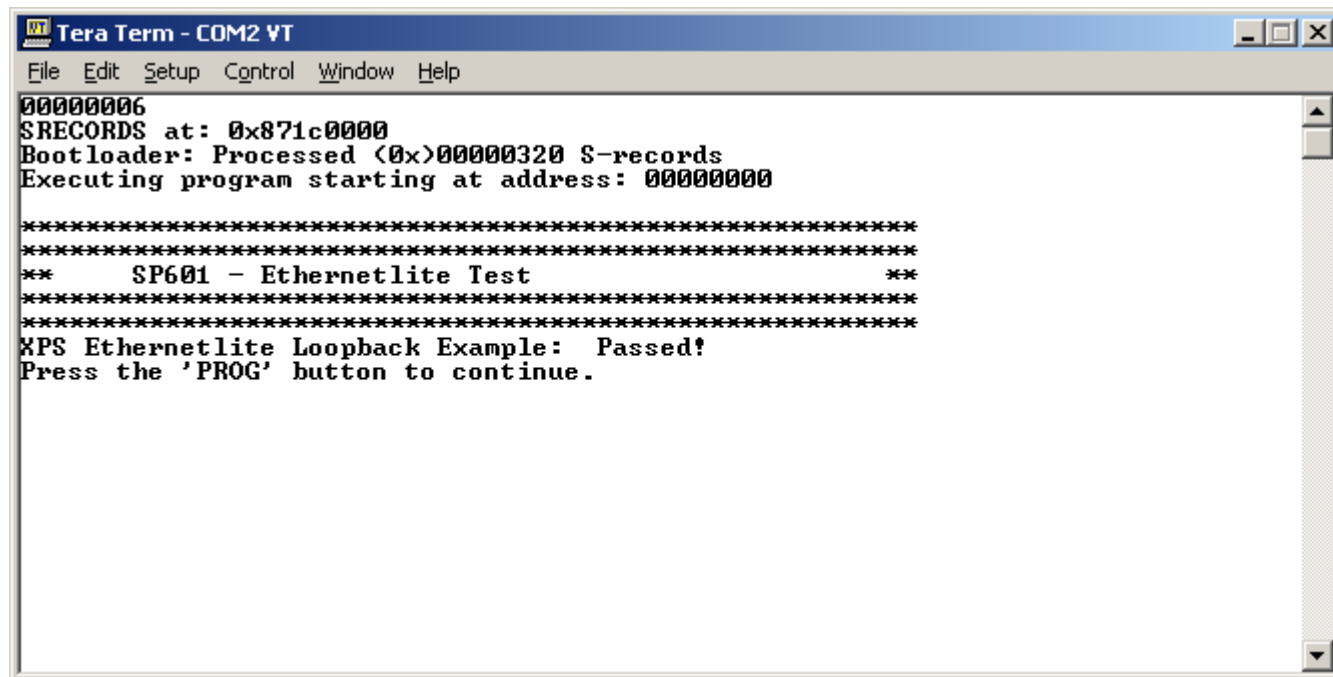
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
00000005
SRECORDS at: 0x871a0000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      SP601 - IIC EEPROM Test      **
*****
*****
IIC EEPROM Test:
Writing data to eeprom at 0x80: 000102030405060708090A0B0C0D0E0F
Reading data from EEPROM
Comparing read data
Passed!
Press the 'PROG' button to continue.
```

SP601 BIST

- Ethernetlite Test completed

- Press **PROG** and type **7** to begin GPIO Switch Test



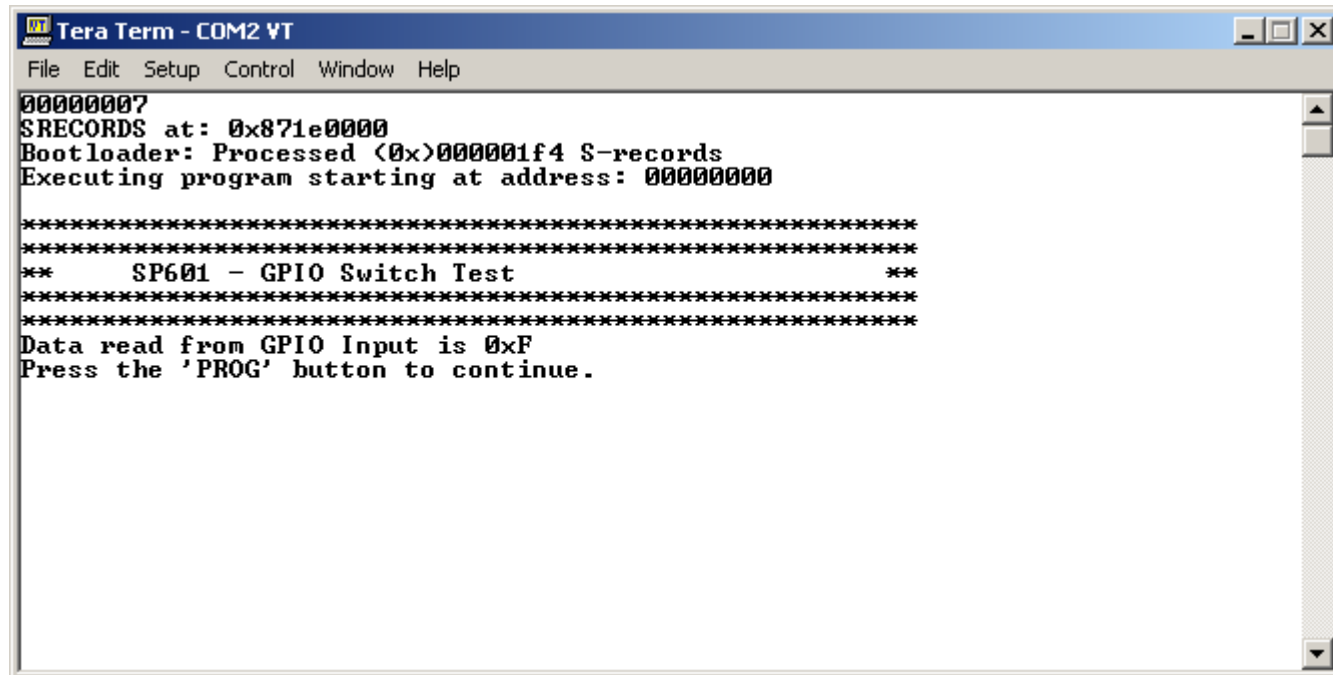
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
00000006
SRECORDS at: 0x871c0000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      SP601 - Ethernetlite Test      **
*****
*****
XPS Ethernetlite Loopback Example: Passed!
Press the 'PROG' button to continue.
```

SP601 BIST

- **GPIO Switch Test completed**

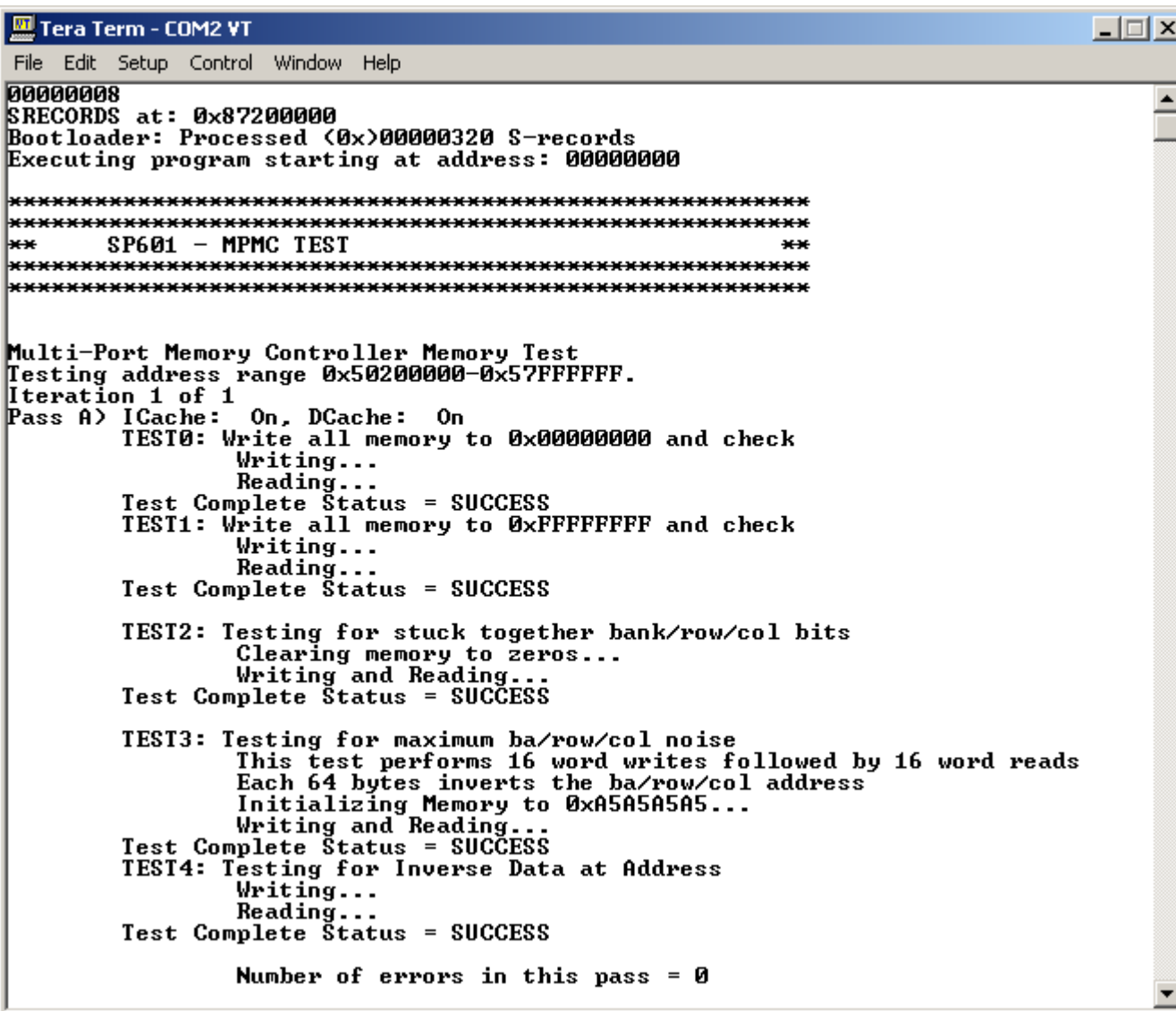
- Press **PROG** and type **8** to begin External Memory Test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
00000000?
SRECORDS at: 0x871e0000
Bootloader: Processed (0x)000001f4 S-records
Executing program starting at address: 00000000

*****
*****
**      SP601 - GPIO Switch Test      **
*****
*****
Data read from GPIO Input is 0xF
Press the 'PROG' button to continue.
```

SP601 BIST



```
Tera Term - COM2 VT
File Edit Setup Control Window Help

00000008
$RECORDS at: 0x87200000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      SP601 - MPMC TEST      **
*****
*****

Multi-Port Memory Controller Memory Test
Testing address range 0x50200000-0x57FFFFFF.
Iteration 1 of 1
Pass A) ICache: On, DCache: On
TEST0: Write all memory to 0x00000000 and check
      Writing...
      Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
      Writing...
      Reading...
Test Complete Status = SUCCESS

TEST2: Testing for stuck together bank/row/col bits
      Clearing memory to zeros...
      Writing and Reading...
Test Complete Status = SUCCESS

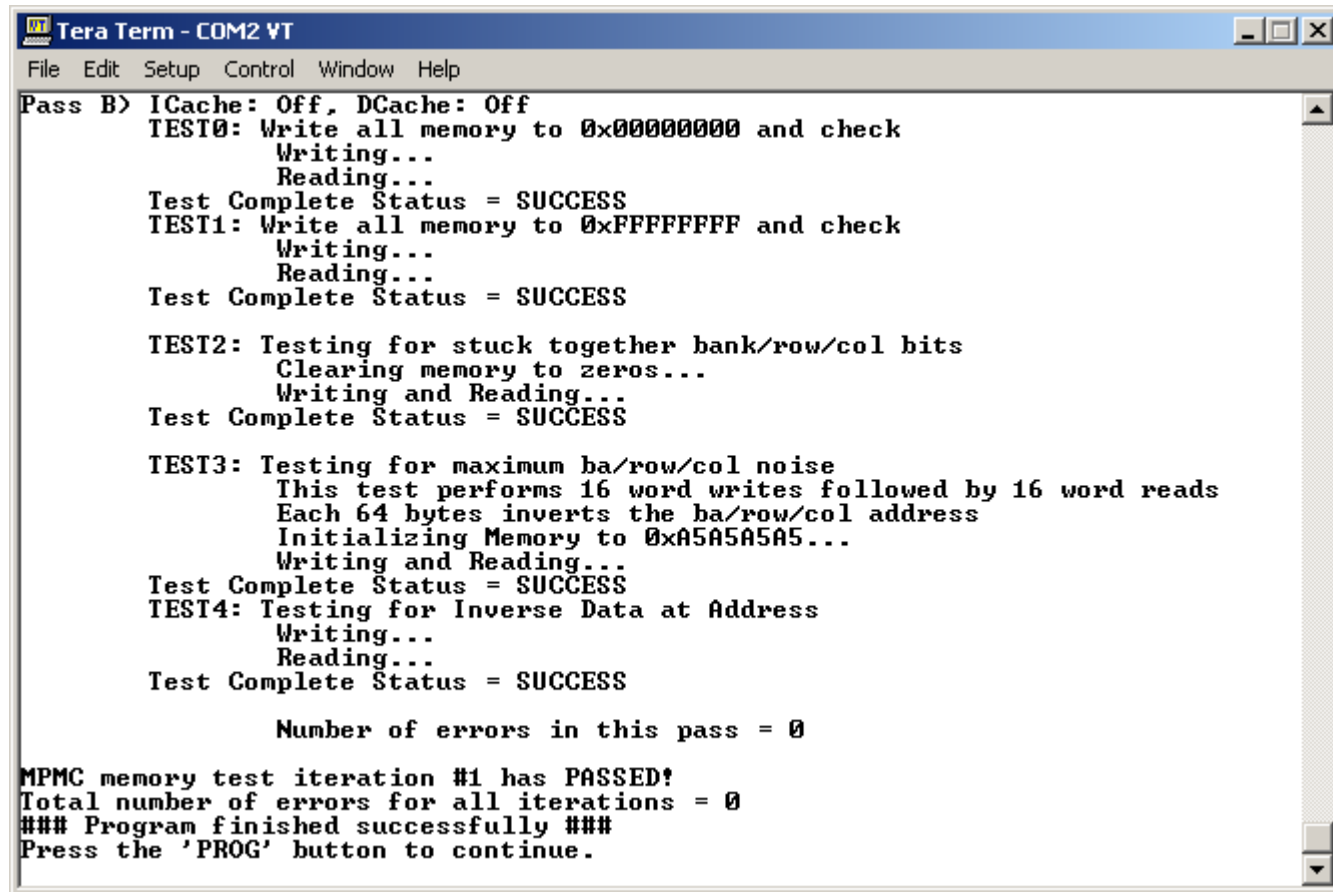
TEST3: Testing for maximum ba/row/col noise
      This test performs 16 word writes followed by 16 word reads
      Each 64 bytes inverts the ba/row/col address
      Initializing Memory to 0xA5A5A5A5...
      Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
      Writing...
      Reading...
Test Complete Status = SUCCESS

      Number of errors in this pass = 0
```

- External Memory Test running with caches on

SP601 BIST

- Second part of External Memory test (caches off)



```
Tera Term - COM2 VT
File Edit Setup Control Window Help

Pass B> ICache: Off, DCache: Off
TEST0: Write all memory to 0x00000000 and check
      Writing...
      Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
      Writing...
      Reading...
Test Complete Status = SUCCESS

TEST2: Testing for stuck together bank/row/col bits
      Clearing memory to zeros...
      Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
      This test performs 16 word writes followed by 16 word reads
      Each 64 bytes inverts the ba/row/col address
      Initializing Memory to 0xA5A5A5A5...
      Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
      Writing...
      Reading...
Test Complete Status = SUCCESS

      Number of errors in this pass = 0

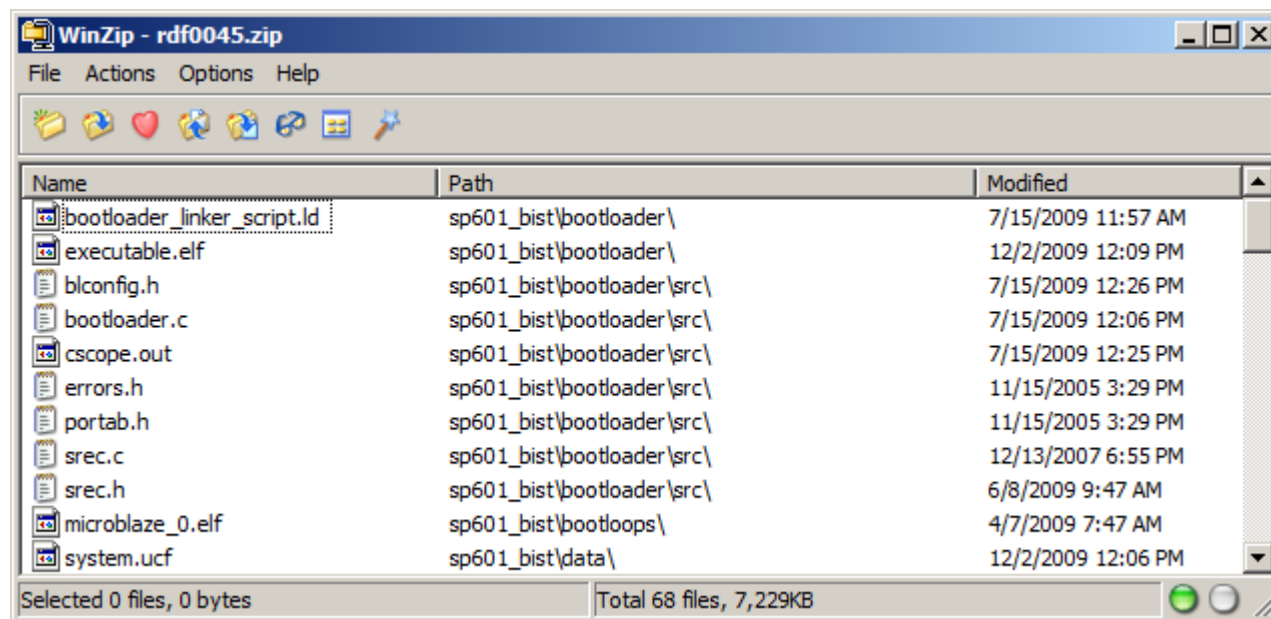
MPMC memory test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
Press the 'PROG' button to continue.
```

Compile SP601 BIST Design

Compile SP601 BIST Design

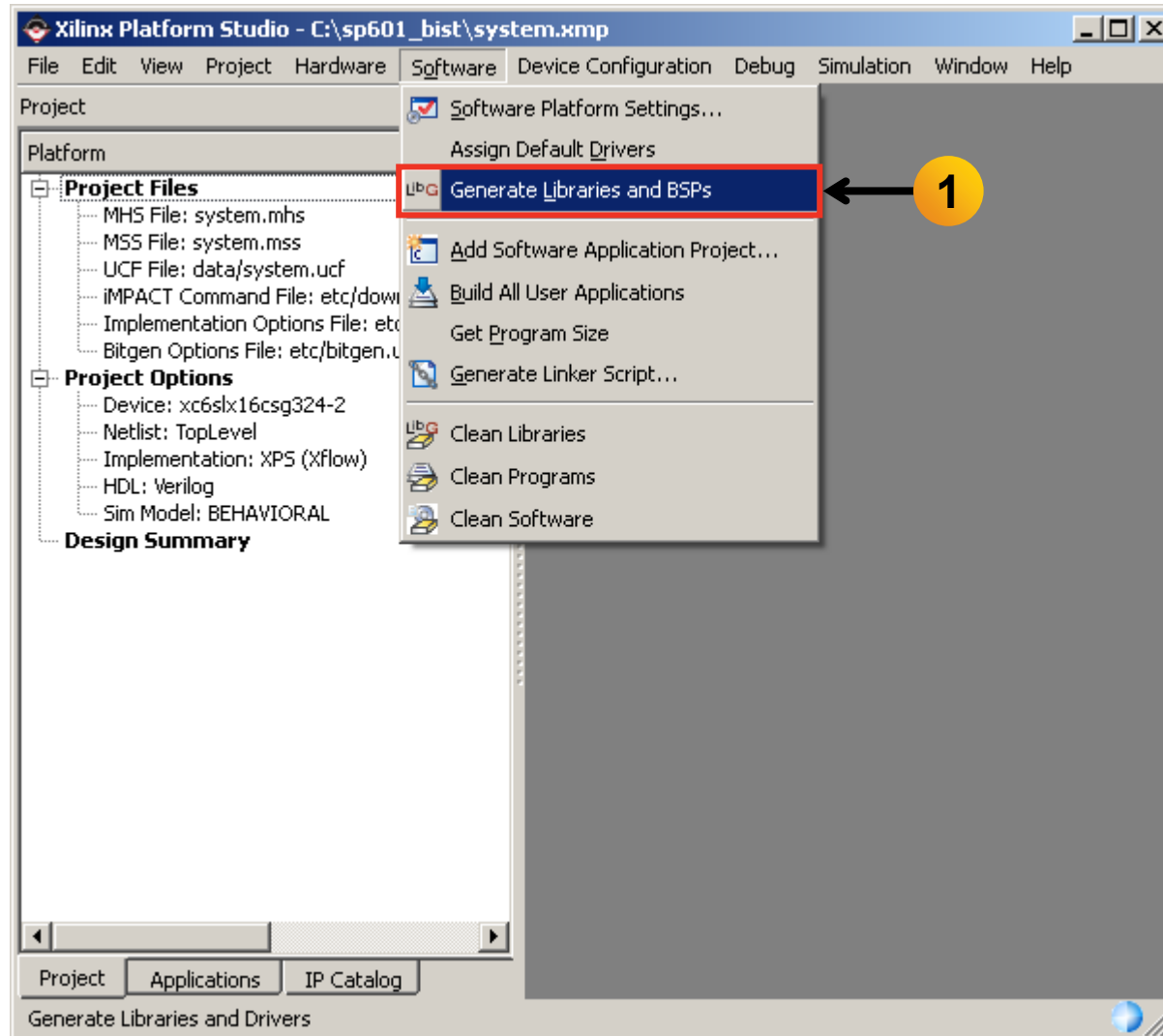
- Unzip the rdf0045.zip file

- <https://secure.xilinx.com/webreg/clickthrough.do?cid=139854>



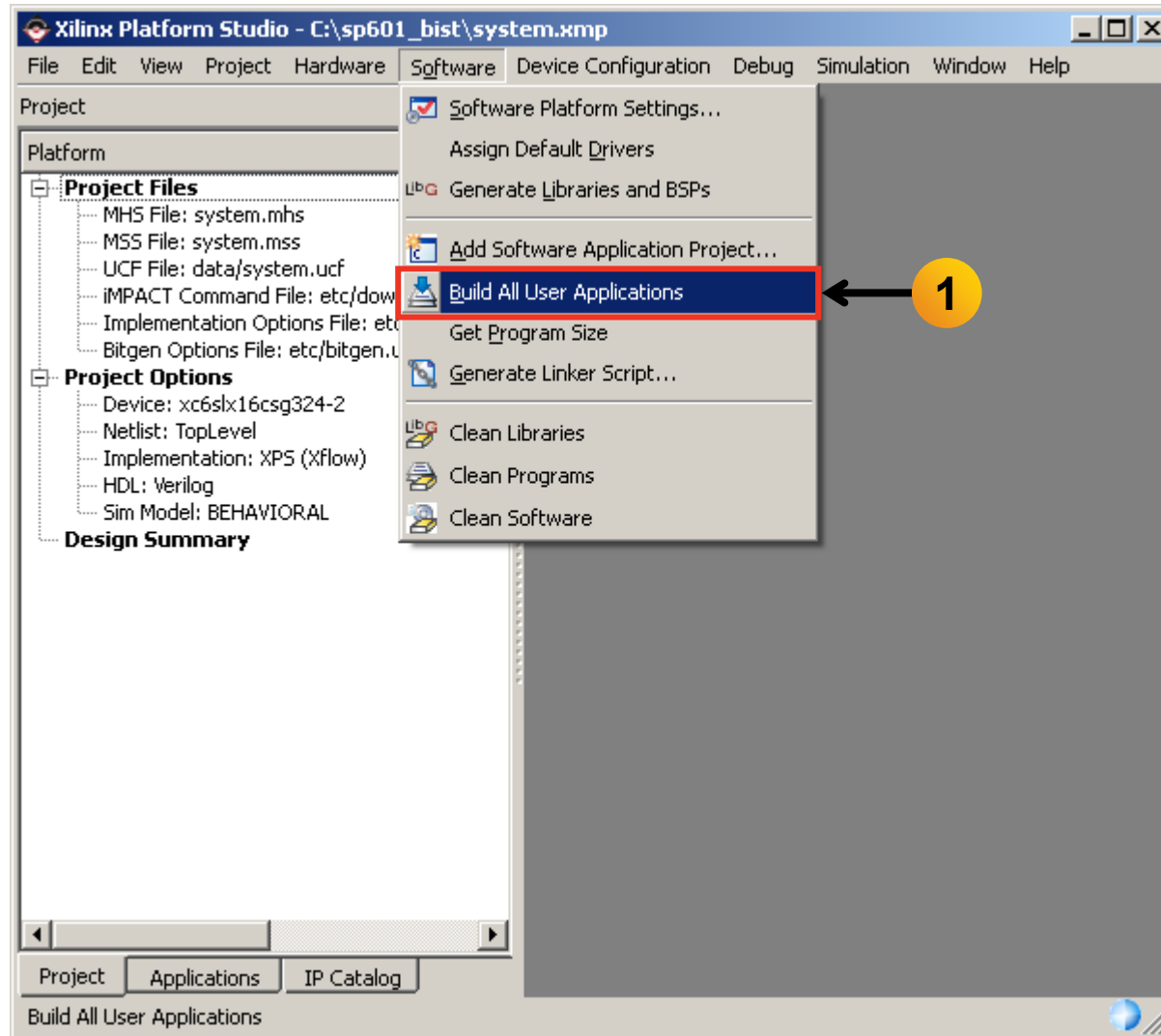
Compile SP601 BIST Design

- The BIST Design can be compiled with EDK
- Open XPS project <design path>\system.xmp
- Generate the libraries needed to create the bitstream
 - Select **Software** → **Generate Libraries and BSPs** (1)



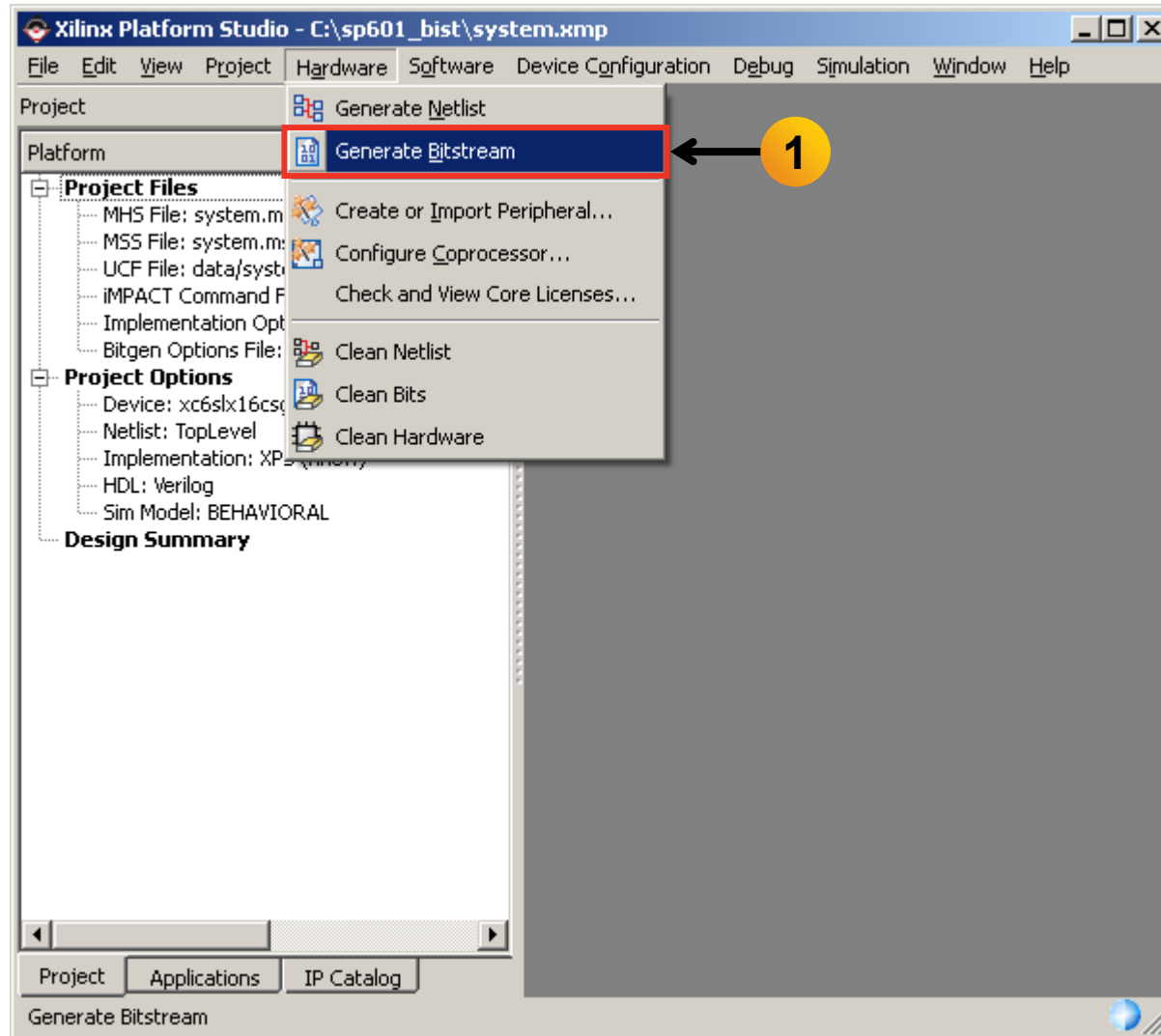
Compile SP601 BIST Design

- **Compile the Software Applications and create the application ELF files**
 - Select **Software** → **Build All User Applications** (1)



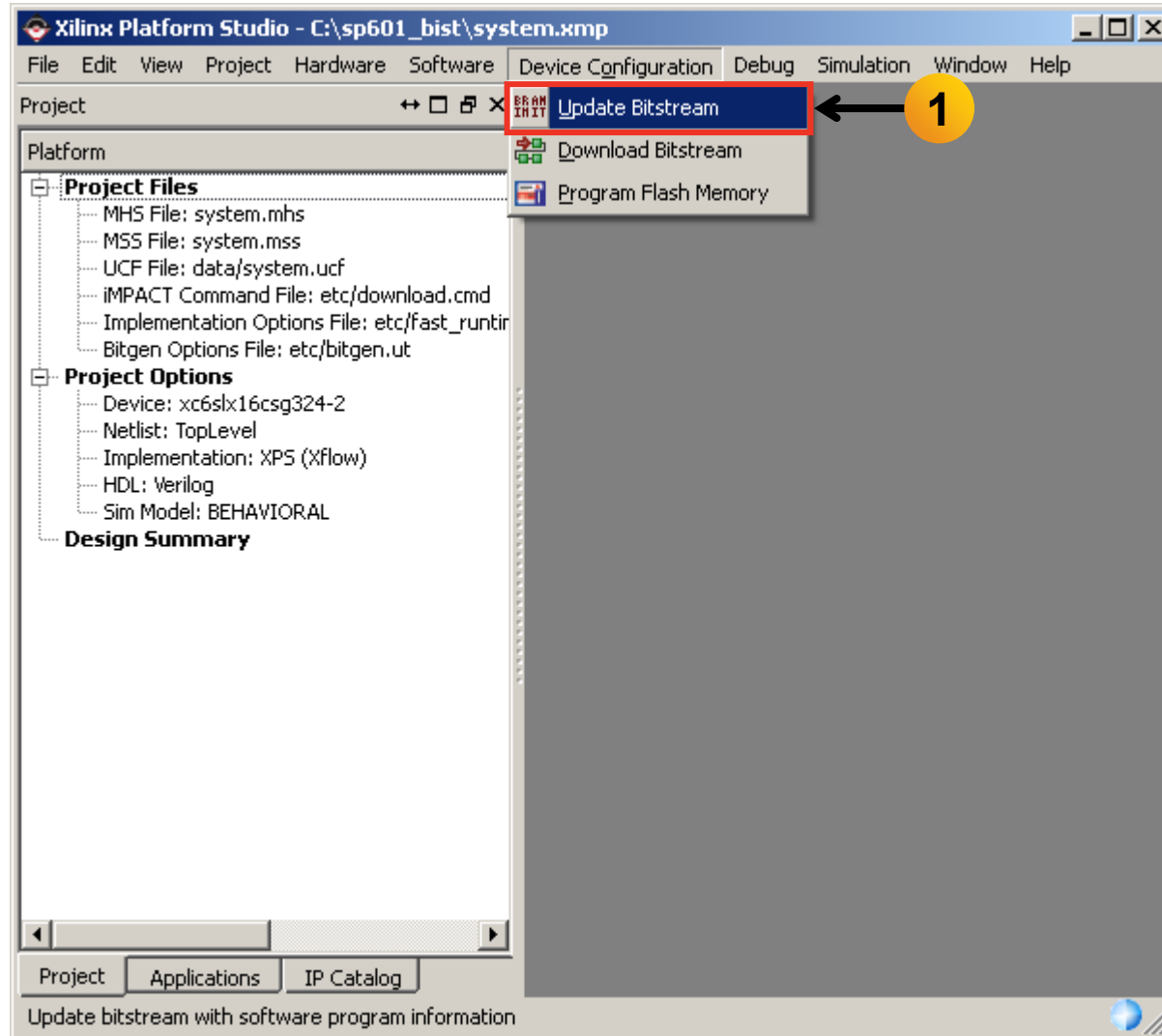
Compile SP601 BIST Design

- Create the hardware design, system.bit, located in <project directory>/implementation
 - Select Hardware → **Generate Bitstream** (1)



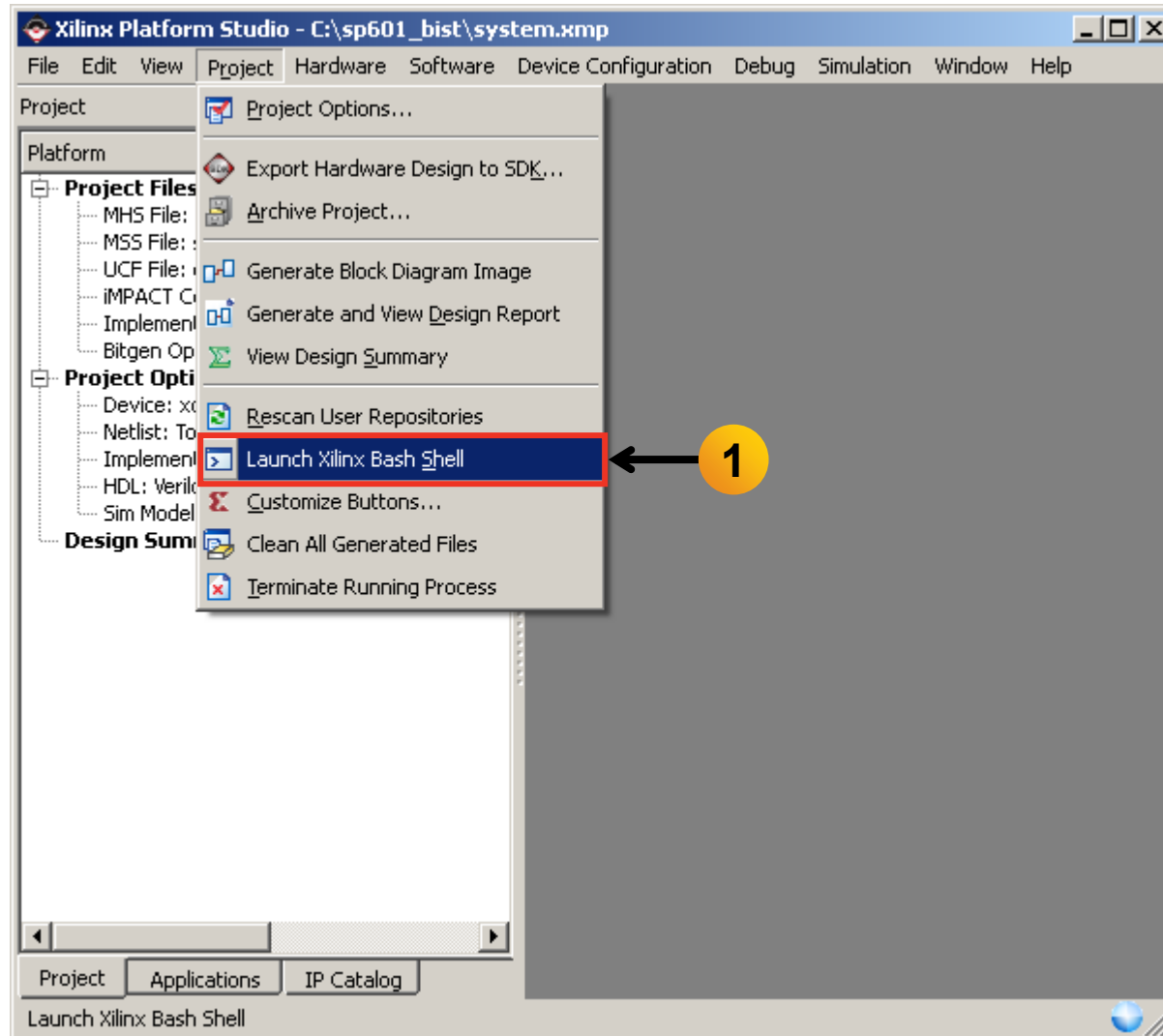
Compile SP601 BIST Design

- **Init memory with the Bootloader Application ELF**
 - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
 - Select **Device Configuration** → **Update Bitstream** (1)



Compile SP601 BIST Design

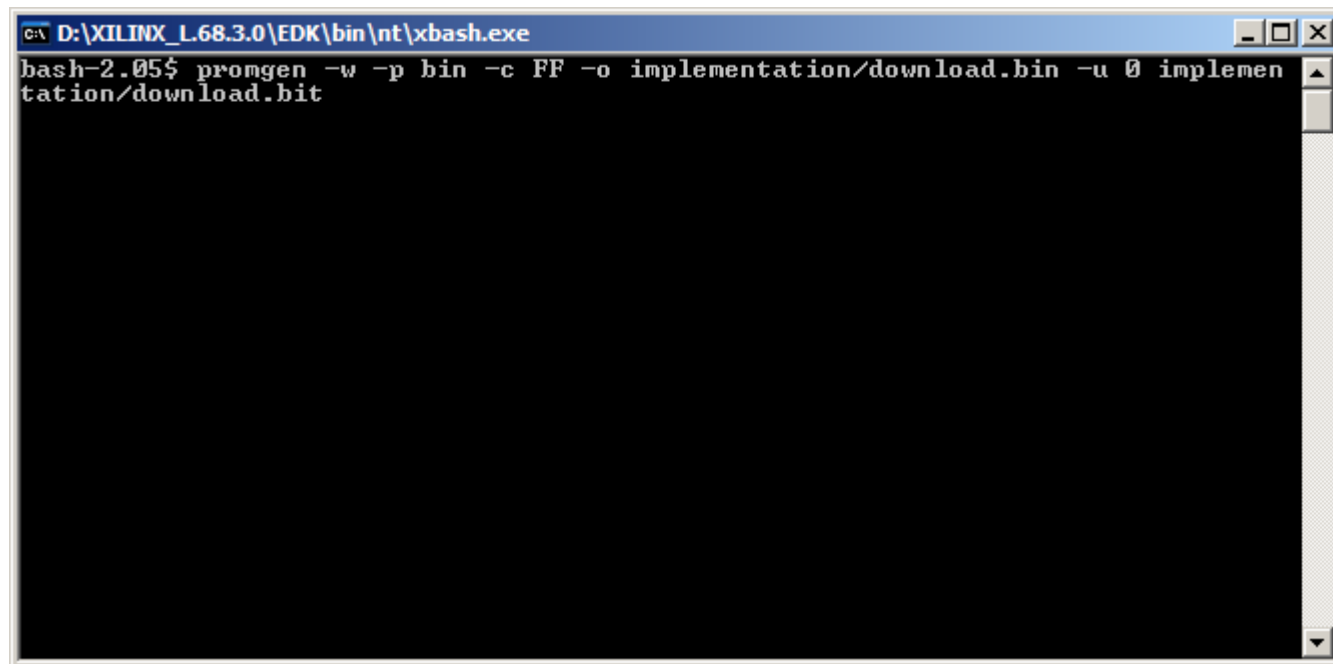
- The bitstream must be converted to hex format (.bin) prior to programming into flash
 - Select **Project** → **Launch Xilinx Bash Shell** (1)



Compile SP601 BIST Design

- **Generate a BIN file from the bitstream**

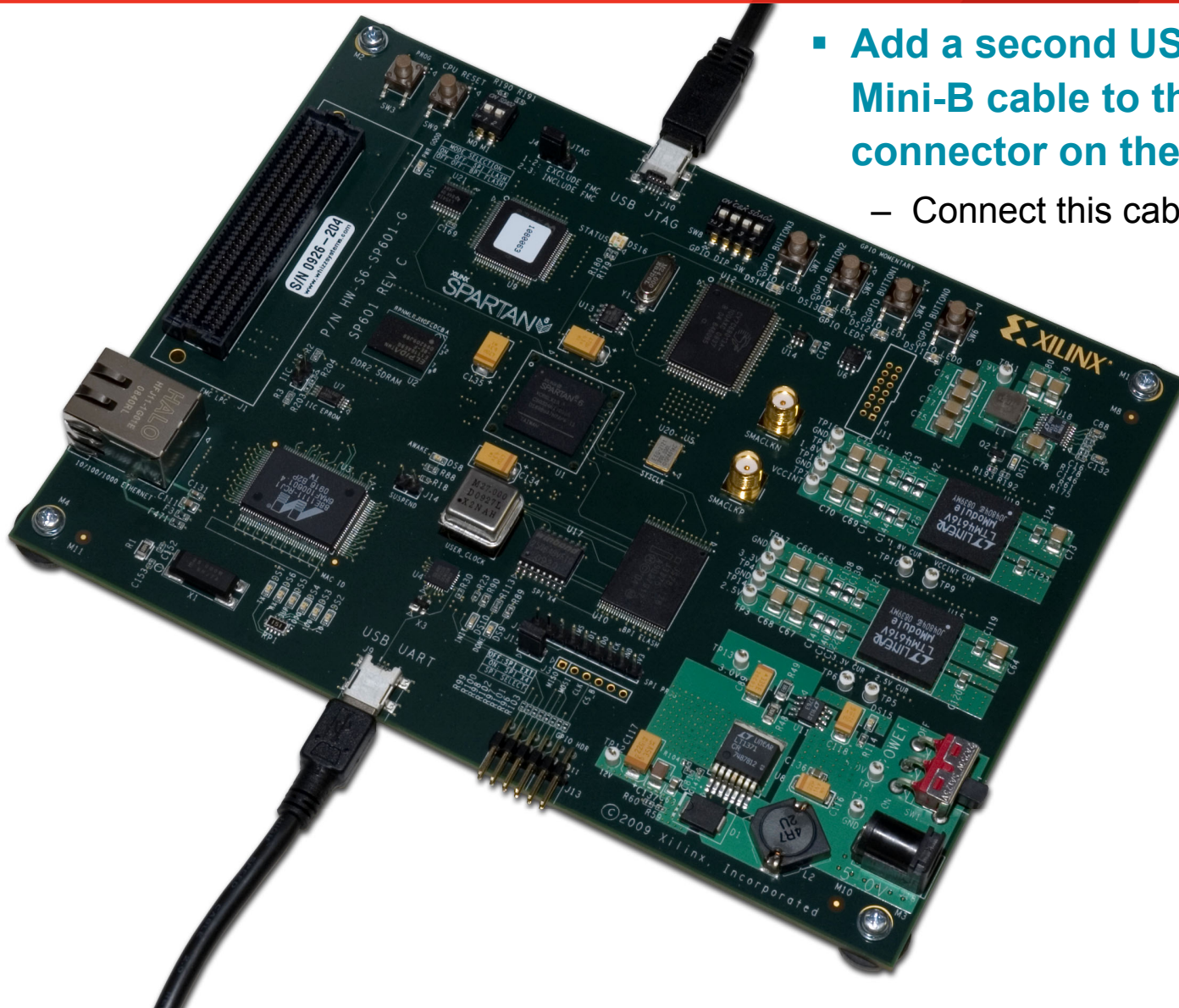
**promgen -w -p bin -c FF -o implementation/download.bin -u 0
implementation/download.bit**



A screenshot of a Windows command prompt window titled "D:\XILINX_L68.3.0\EDK\bin\nt\xbash.exe". The window shows a terminal session where the command `promgen -w -p bin -c FF -o implementation/download.bin -u 0 implementation/download.bit` has been entered and executed. The prompt is `bash-2.05$`. The command output is not visible, suggesting it completed successfully.

Program SP601 BPI

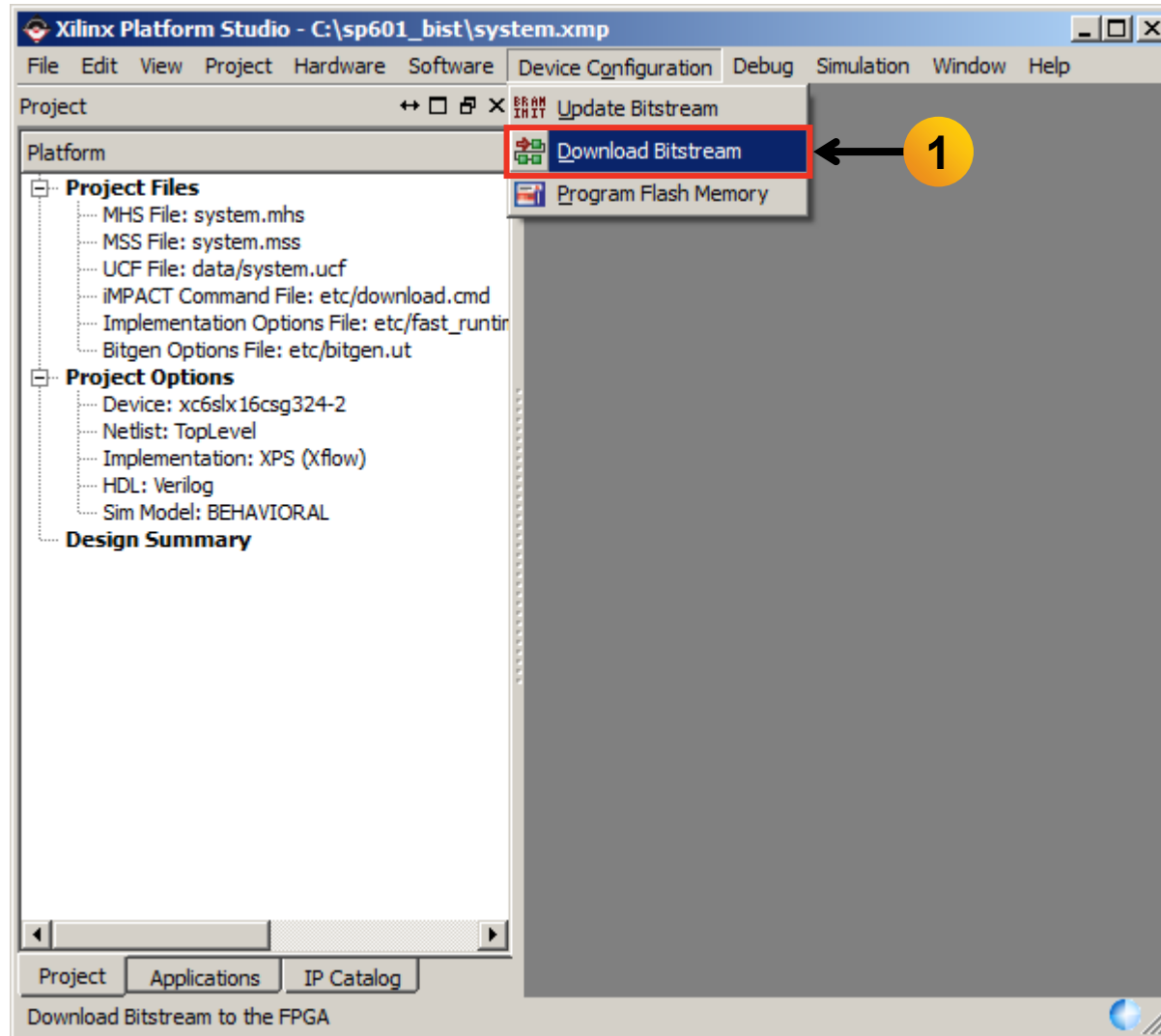
Program SP601 BPI



- Add a second USB Type-A to Mini-B cable to the USB JTAG connector on the SP601 board
 - Connect this cable to your PC

Program SP601 BPI

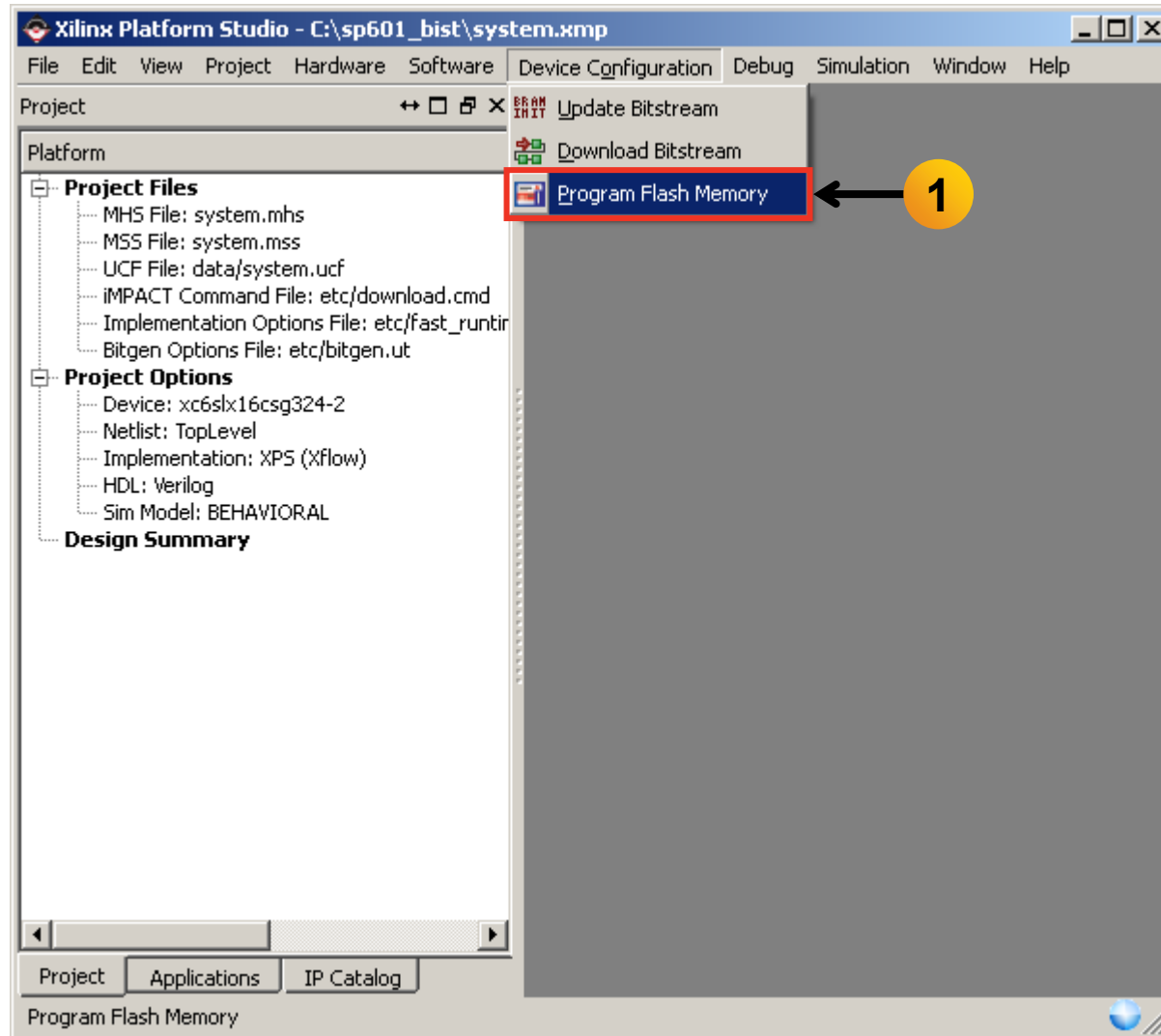
- **Download the bitstream**
 - Select **Device Configuration** → **Download Bitstream** (1)



Note: This step is required prior to programming the Flash with EDK

Program SP601 BPI

- Program the bitstream and ELF files into BPI Flash
 - Select **Device Configuration** → **Program Flash Memory** (1)



Note: This overwrites the BIST application delivered with the SP601 board

Program SP601 BPI

■ Program the BPI Flash with the bitstream

- Bitstream download.*bin*
- Offset: **0x00000000**
- Scratch Memory:
xps_bram_if_cntlr_1

Program Flash Memory -- Deprecated

File To Program:

☐ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Note: Takes about 2 minutes

Program SP601 BPI

■ Program the BPI Flash with an SREC file:

- ELF:
hello_uart/hello_uart.elf
- Select Auto-convert to SREC
- Offset: **0x00120000**
- Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

The screenshot shows the 'Program Flash Memory' dialog box with the following settings highlighted by red boxes:

- File To Program:** C:/sp601_bist/hello_uart/hello_uart.elf
- Auto-convert file to bootloadable:** ☒ (checked)
- Format:** SREC (selected in the dropdown)
- format when programming flash:** (checked)
- Processor Instance:** microblaze_0
- Flash Memory Properties:**
 - Instance Name:** FLASH_c_mem0_baseaddr
 - Base Address:** 0x87000000
 - Size:** 16 Mbytes
 - Bus Width:** 8 bits
 - Program at Offset:** 0x00120000
- Scratch Memory Properties:**
 - Instance Name:** DDR2_SDRAM_c_mpmc_baseaddr
 - Base Address:** 0x50000000
 - Size:** 128 Mbytes
- Create Flash Bootloader Application:** ☐ (unchecked)
- SW Application Project:** (empty text field)
- Bootloader File Format:** (empty text field)

Note: FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

Buttons: OK, Cancel, Help

Note: Takes about a minute

Program SP601 BPI

- Program the BPI Flash with an SREC file:
 - ELF:
hello_gpio/hello_gpio.elf
 - Select Auto-convert to SREC
 - Offset: **0x00140000**
 - Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Depreciated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Program SP601 BPI

■ Program the BPI Flash with an SREC file:

- ELF:
hello_timer/hello_timer.elf
- Select Auto-convert to SREC
- Offset: **0x00160000**
- Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Deprecated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Program SP601 BPI

- Program the BPI Flash with an SREC file:
 - ELF:
hello_flash/hello_flash.elf
 - Select Auto-convert to SREC
 - Offset: **0x00180000**
 - Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Deprecated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Program SP601 BPI

- Program the BPI Flash with an SREC file:
 - ELF:
hello_iic/hello_iic.elf
 - Select Auto-convert to SREC
 - Offset: **0x001a0000**
 - Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Deprecated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Program SP601 BPI

- Program the BPI Flash with an SREC file:
 - ELF:
hello_emac/hello_emac.elf
 - Select Auto-convert to SREC
 - Offset: **0x001c0000**
 - Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Depreciated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Note: Presentation applies to the SP601

Program SP601 BPI

■ Program the BPI Flash with an SREC file:

- ELF:
**hello_switch/
hello_switch.elf**
- Select Auto-convert to SREC
- Offset: **0x001e0000**
- Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Depreciated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Program SP601 BPI

■ Program the BPI Flash with an SREC file:

- ELF:
hello_mem/hello_mem.elf
- Select Auto-convert to SREC
- Offset: **0x00200000**
- Scratch Memory:
DDR2_SDRAM_c_mpmc_baseaddr

Program Flash Memory -- Deprecated

File To Program: ...

☒ Auto-convert file to bootloadable format when programming flash

Processor Instance: microblaze_0

Flash Memory Properties

Instance Name:

Base Address: 0x87000000 Size: 16 Mbytes Bus Width: 8 bits

Program at Offset:

Scratch Memory Properties

Instance Name:

Base Address: 0x50000000 Size: 128 Mbytes

☐ Create Flash Bootloader Application

SW Application Project:

Bootloader File Format:

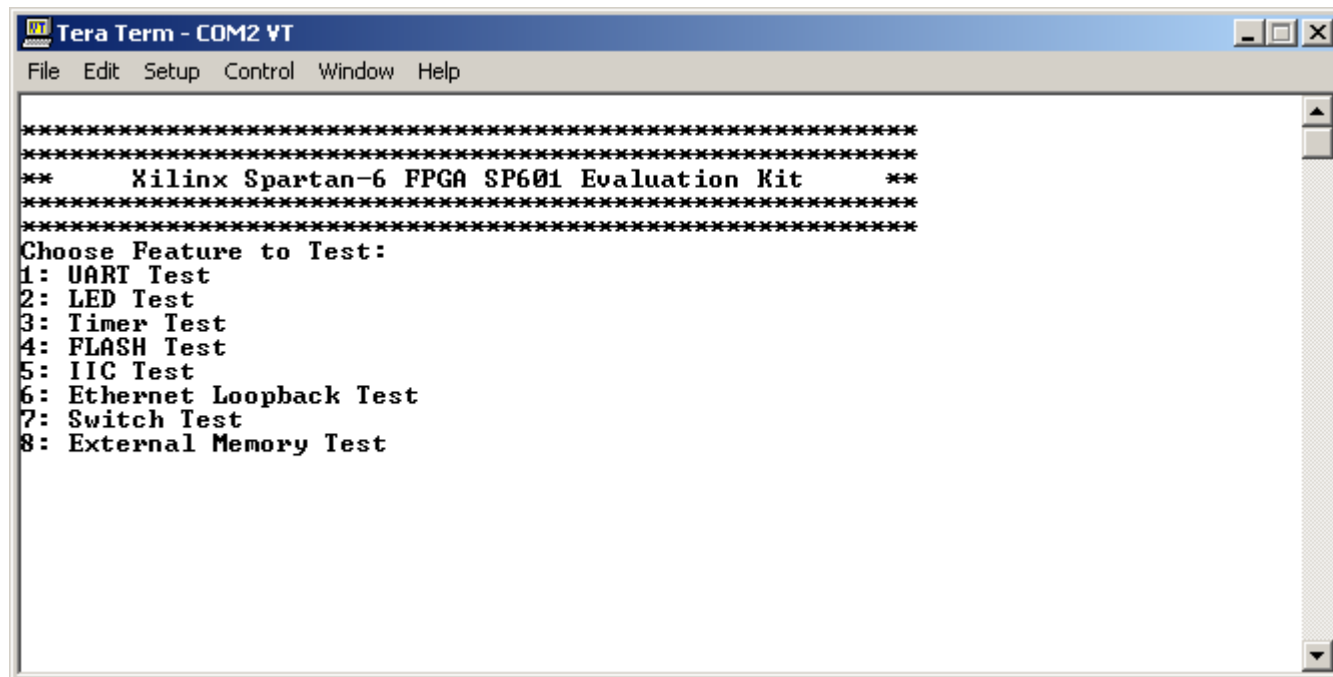
Note

FPGA must be pre-programmed with a bitstream from an EDK design containing an EMC peripheral connected to Flash Memory

OK Cancel Help

Program SP601 BPI

- Press PROG and view initial BIST screen
 - Type “1” to start the UART Test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help

*****
*****
**      Xilinx Spartan-6 FPGA SP601 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
```

References

References

- **EDK Documentation**

- Embedded System Tools Reference Guide

http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/est_rm.pdf

- **Spartan-6 Configuration**

- Spartan-6 FPGA Configuration User Guide

http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

Documentation

Documentation

- **Spartan-6**

- Spartan-6 FPGA Family

- <http://www.xilinx.com/products/spartan6/index.htm>

- **SP601 Documentation**

- Spartan-6 FPGA SP601 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-S6-SP601-G.htm>

- SP601 Getting Started Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug523.pdf

- SP601 Hardware User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf

- SP601 Reference Design User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug524.pdf