ML605 PCIe x4 Gen2 Design Creation

December 2009

XTP045

Overview

- Virtex-6 PCIe x4 Gen2 Capability
- Xilinx ML605 Board
- Software Requirements
- Generate PCIe Core
- Compile PCIe Core
- Program Platform Flash with PCIe Design
- ML605 Setup
- Running the PCIe x4 Gen2 Design
- References
  - IP Release Notes Guide XTP025

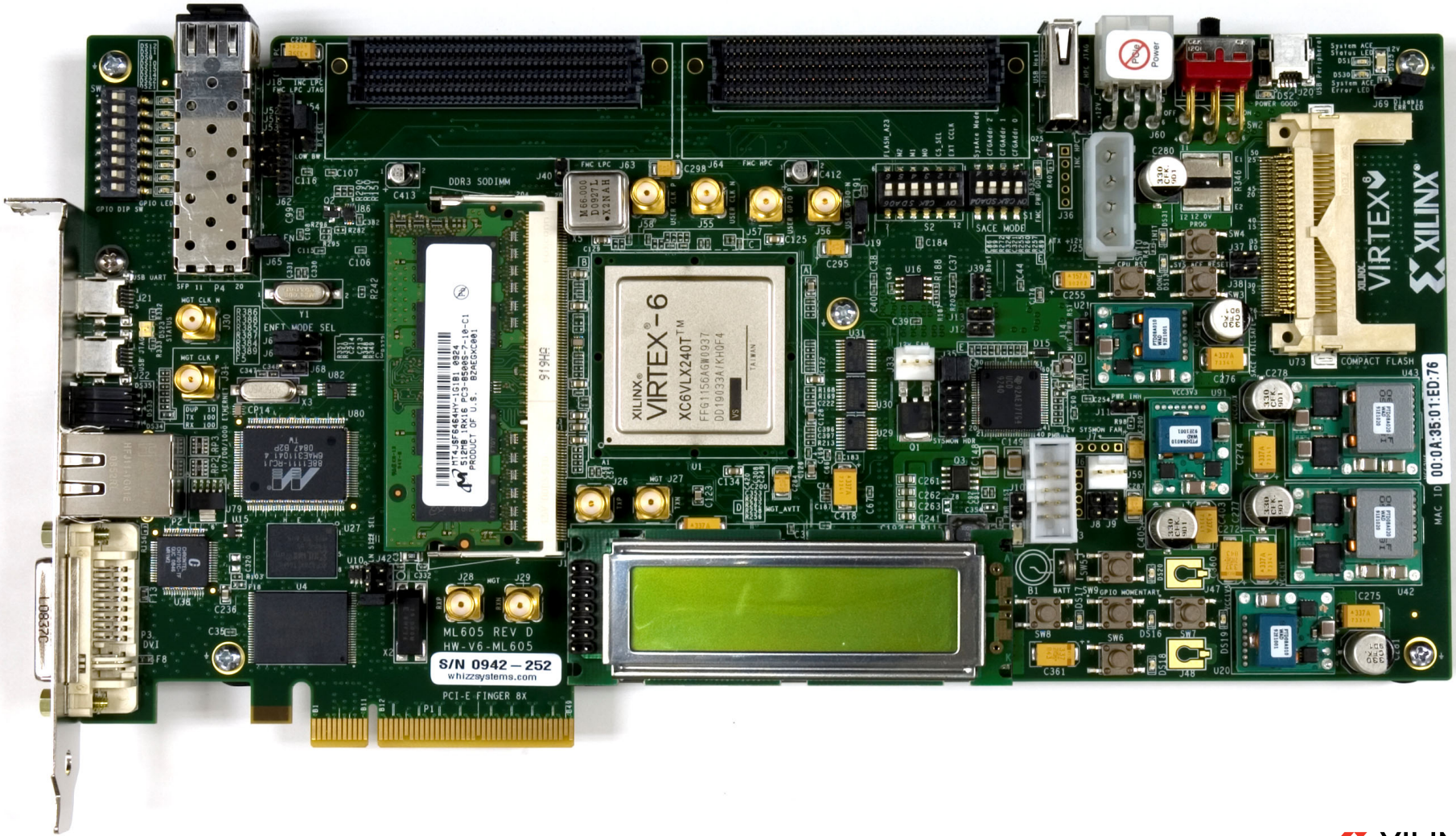
Note: This presentation applies to the ML605

Virtex-6 PCIe x4 Gen2 Capability

- **Integrated Block for PCI Express**
  - PCI Express Base 2.0 Specification
- **Generation 2 (5 GT/s) data rates**
  - x4, x2, or x1 Gen2 lane width
  - x8 Gen2 not supported in -1 parts
- **Configurable for Endpoint or Root Port Applications**
  - ML605 configured for Endpoint Applications
- **GTX Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
  - 128 / 256 / 512 / 1024 bytes
- **Configurable BAR spaces**
  - Up to 6 x 32 bit, 3 x 64 bit, or a combination
  - Memory or IO
  - BAR and ID filtering
- **Management and Statistics Interface**

Note: Presentation applies to the ML605

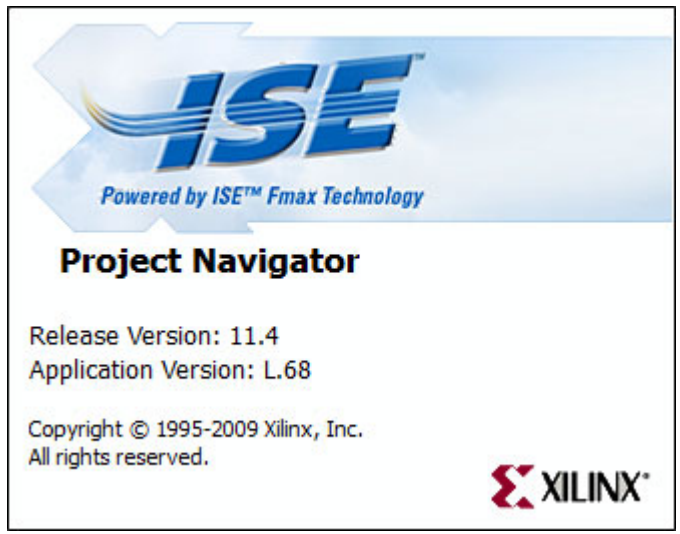
Xilinx ML605 Board



Note: Presentation applies to the ML605

ISE Software Requirement

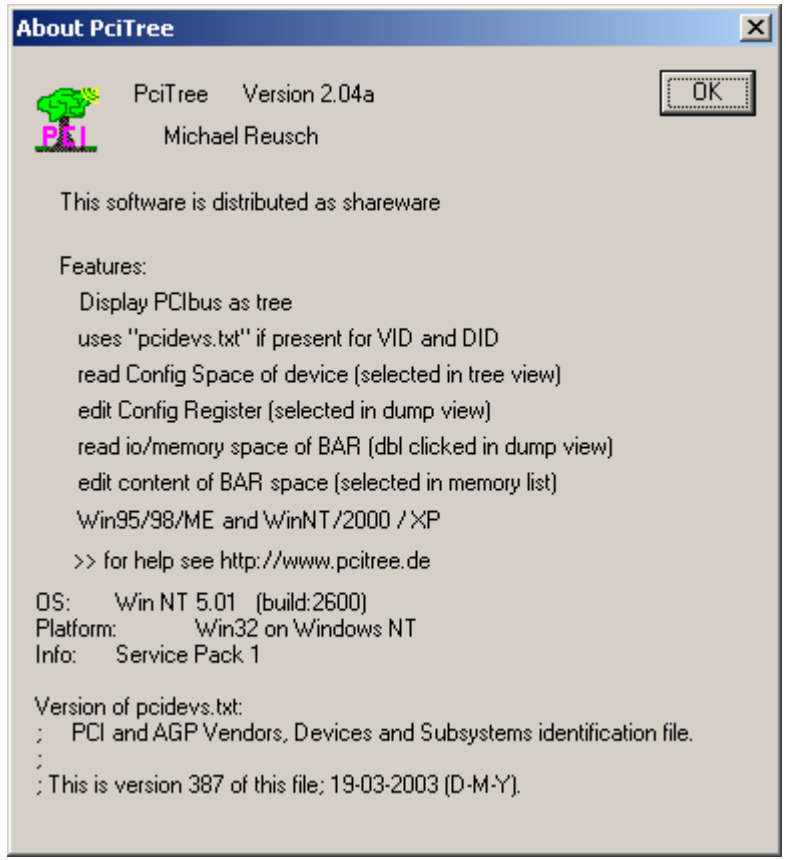
- Xilinx ISE 11.4 software



Note: Presentation applies to the ML605

PciTree Software Requirement

- **PciTree Bus Viewer**
  - Free download
  - HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory



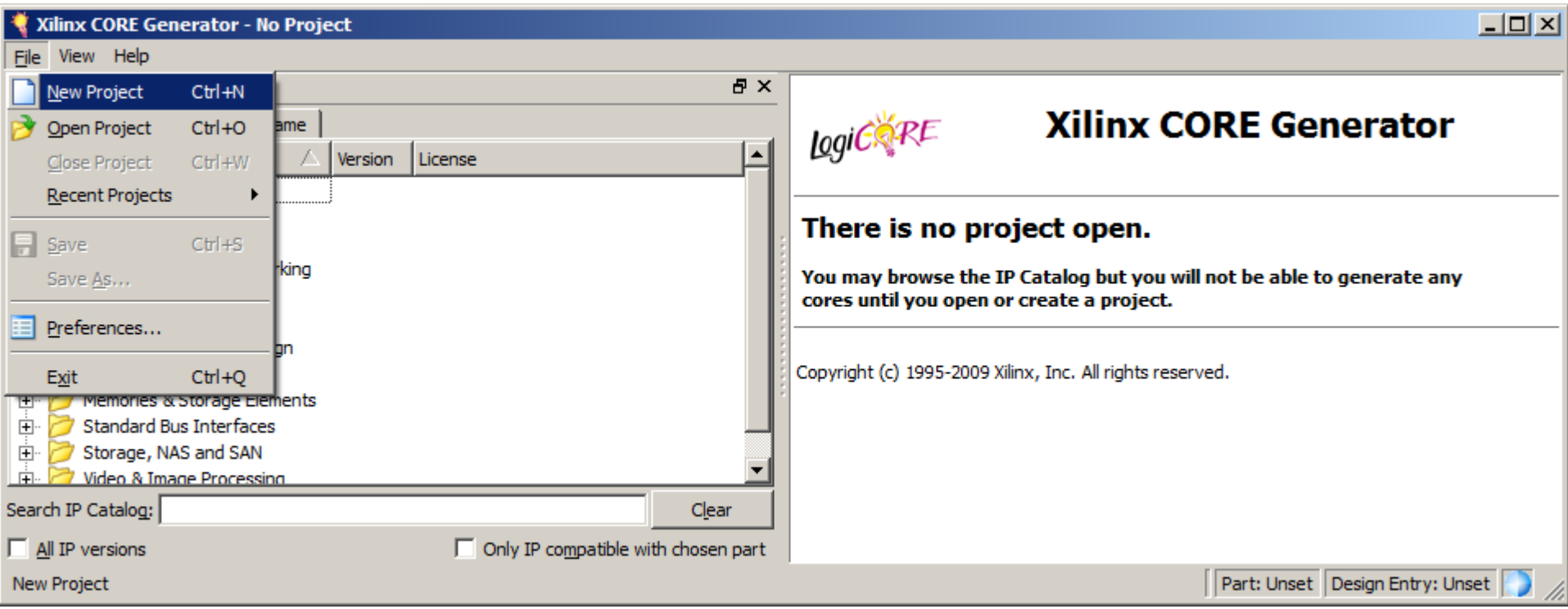
Note: Presentation applies to the ML605

Generate PCIe Core

- **Open the CORE Generator**

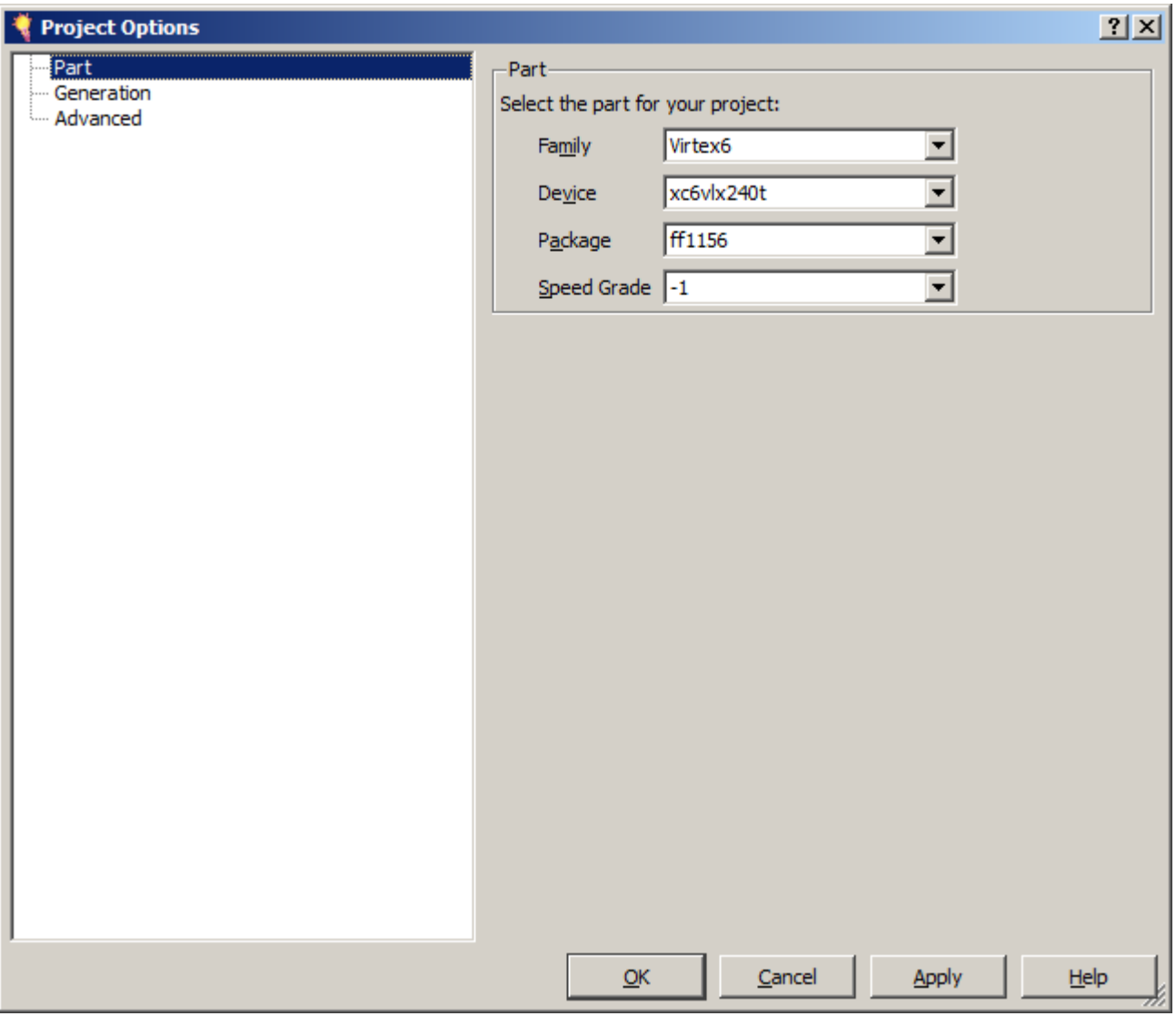
  Start → All Programs → Xilinx ISE Design Suite 11 → ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**



Note: Pre-built design: https://secure.xilinx.com/webreg/clickthrough.do?cid=139967

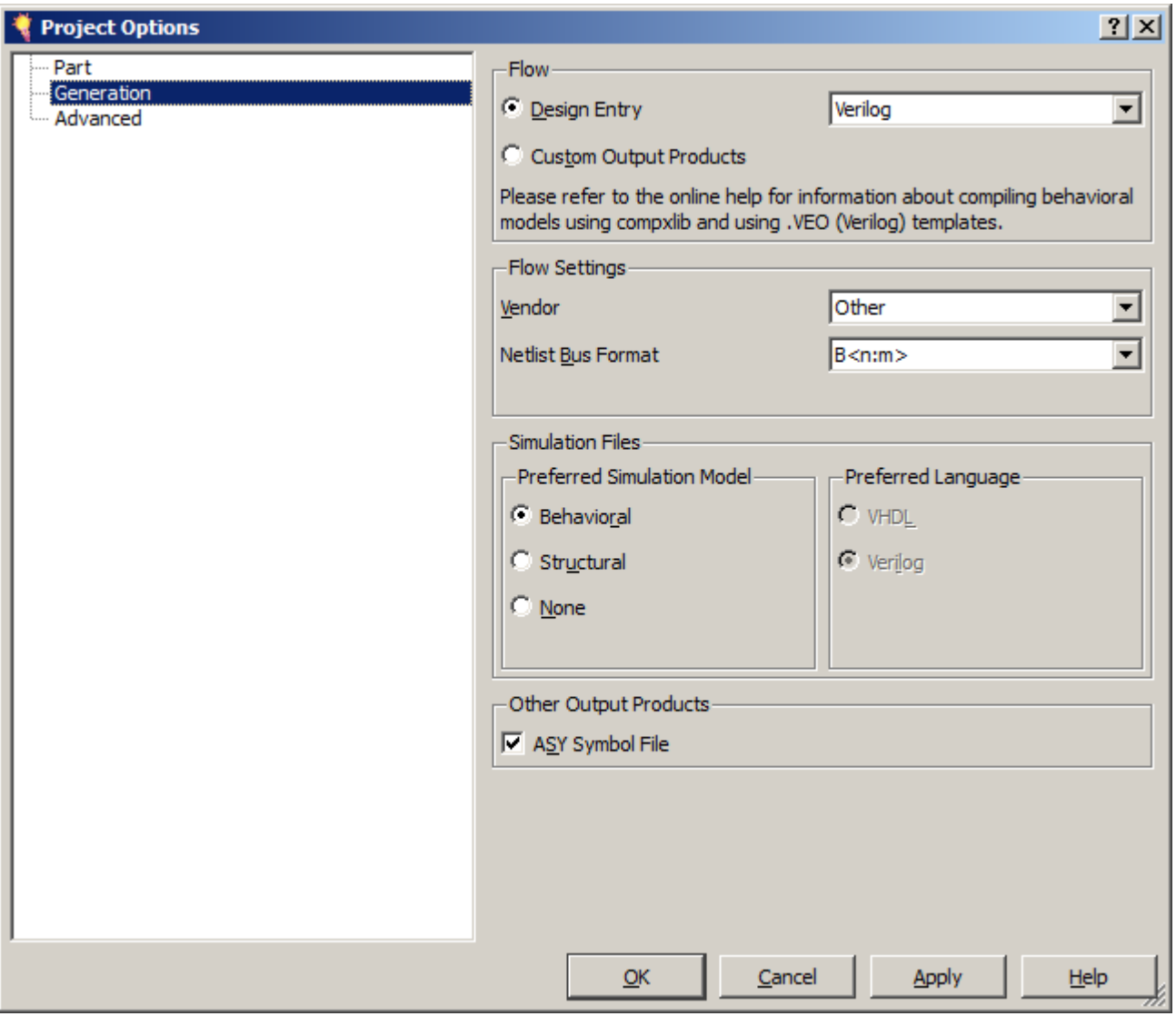
Generate PCIe Core



- Create a project directory: ml605_pcie_x4_gen2
- Name the project: ml605_pcie_x4_gen2.cgp
- The Project options will appear
- Set the Part (as seen here):
  - Family: Virtex6
  - Device: xc6vlx240t
  - Package: ff1156
  - Speed Grade: -1

Note: Presentation applies to the ML605

Generate PCIe Core



- Select Generation
- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the ML605

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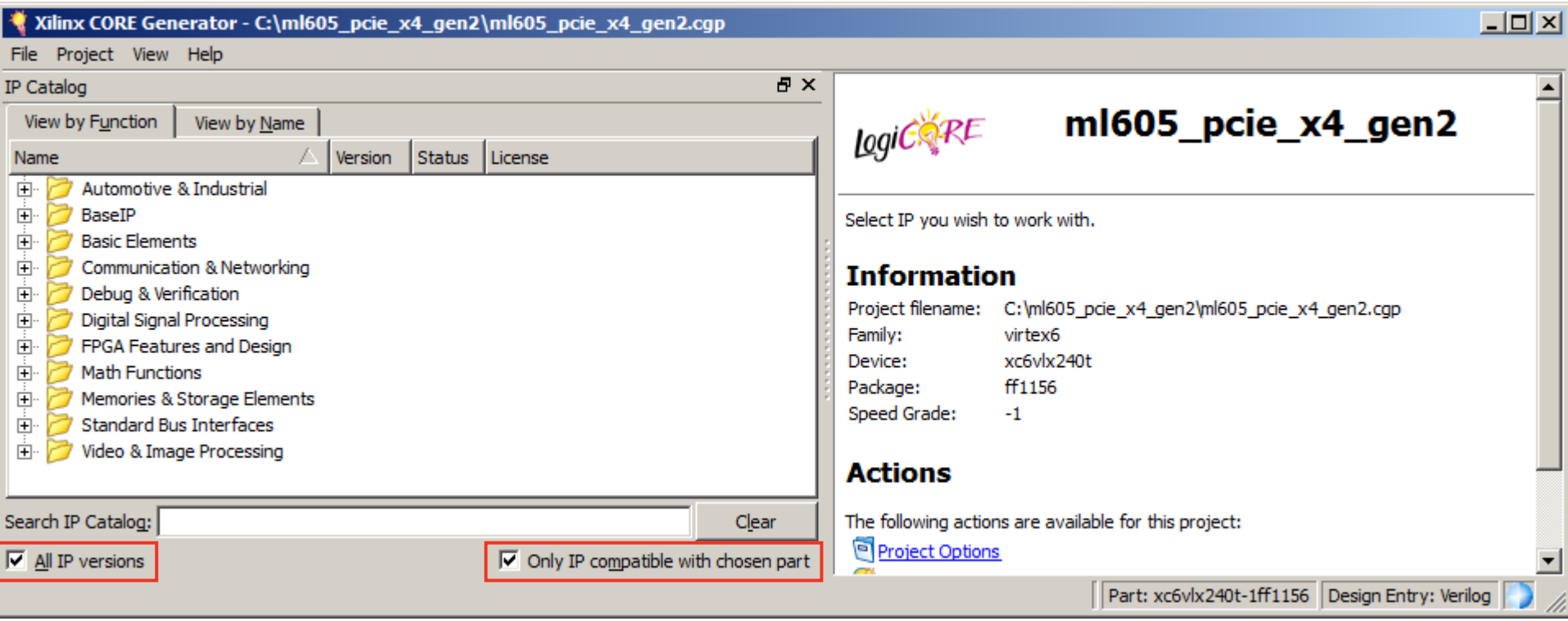
Generate PCIe Core

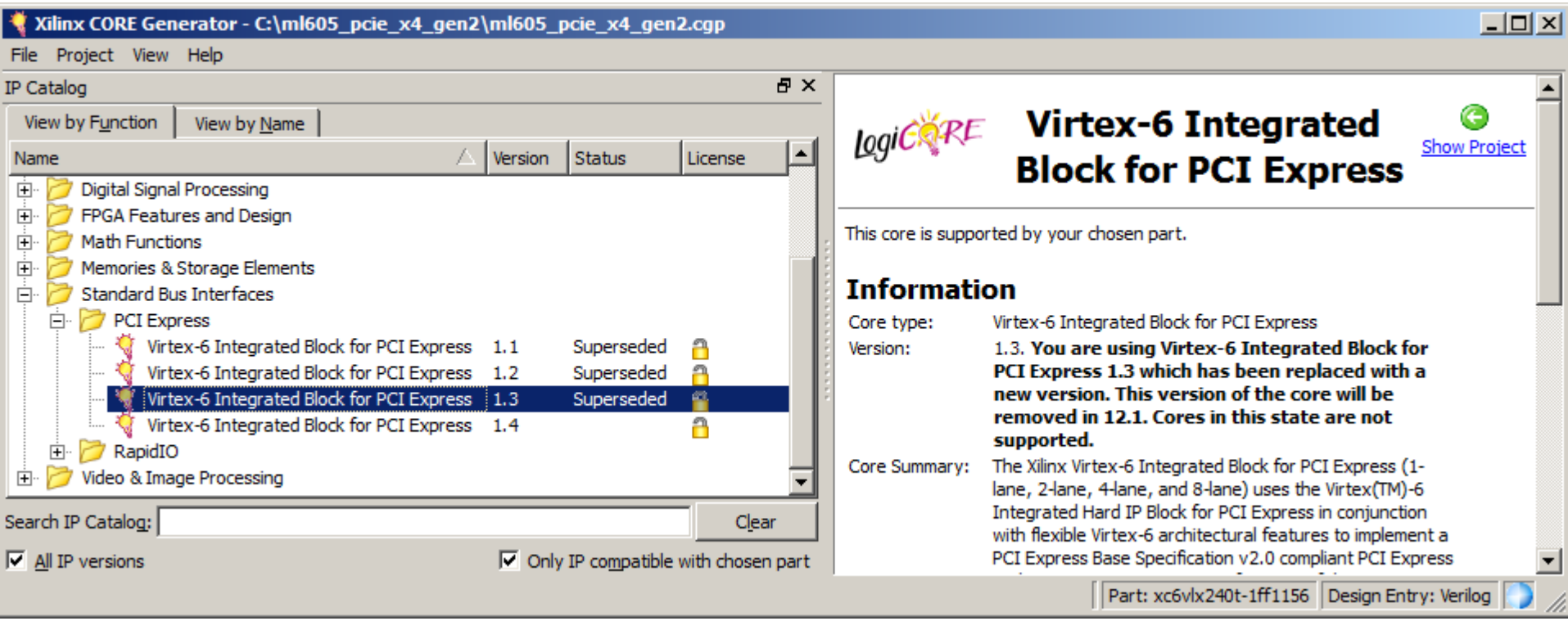
- **Select**
  - **All IP versions**
  - **Only IP compatible with chosen part**



Note: Presentation applies to the ML605

Generate PCIe Core

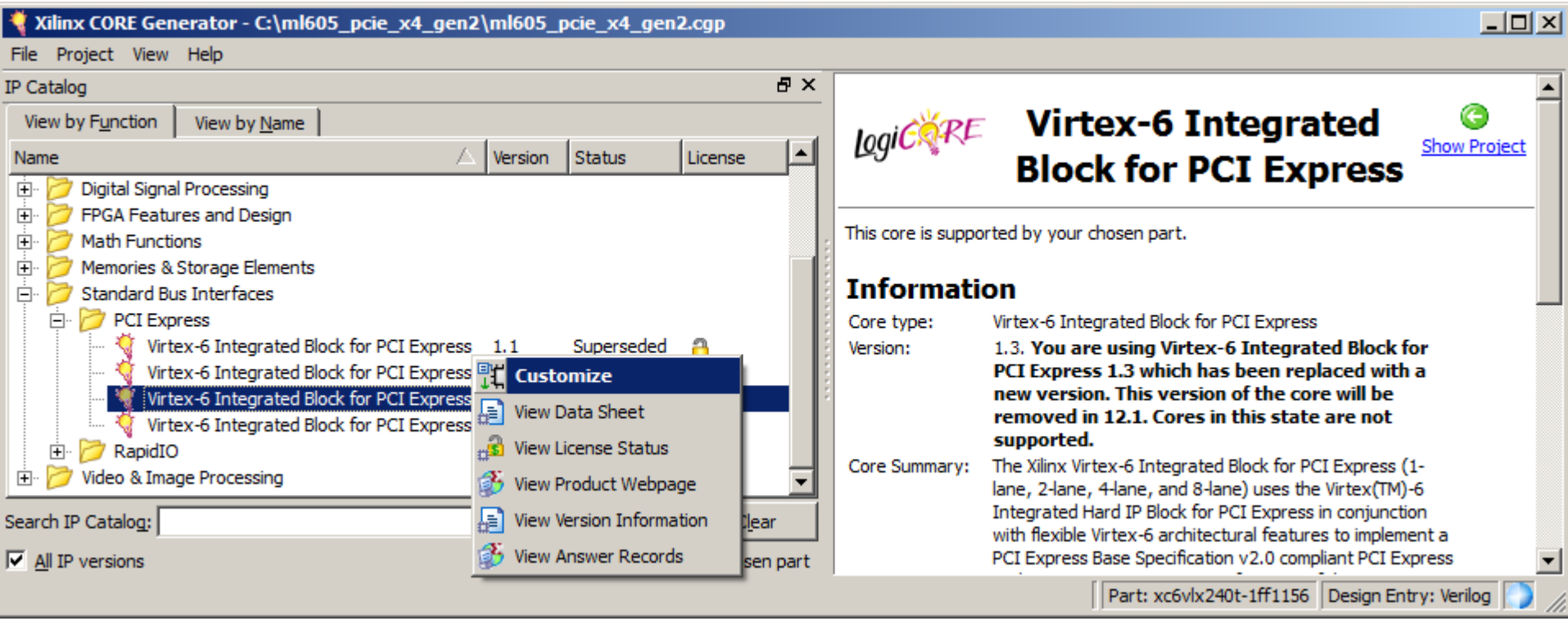
- **Select**
  - Virtex-6 Integrated Block for PCI Express, **Version 1.3**



Note: Version 1.3 is required for XC6VLX240T-1CES FPGAs with PCIe x4 Gen 2

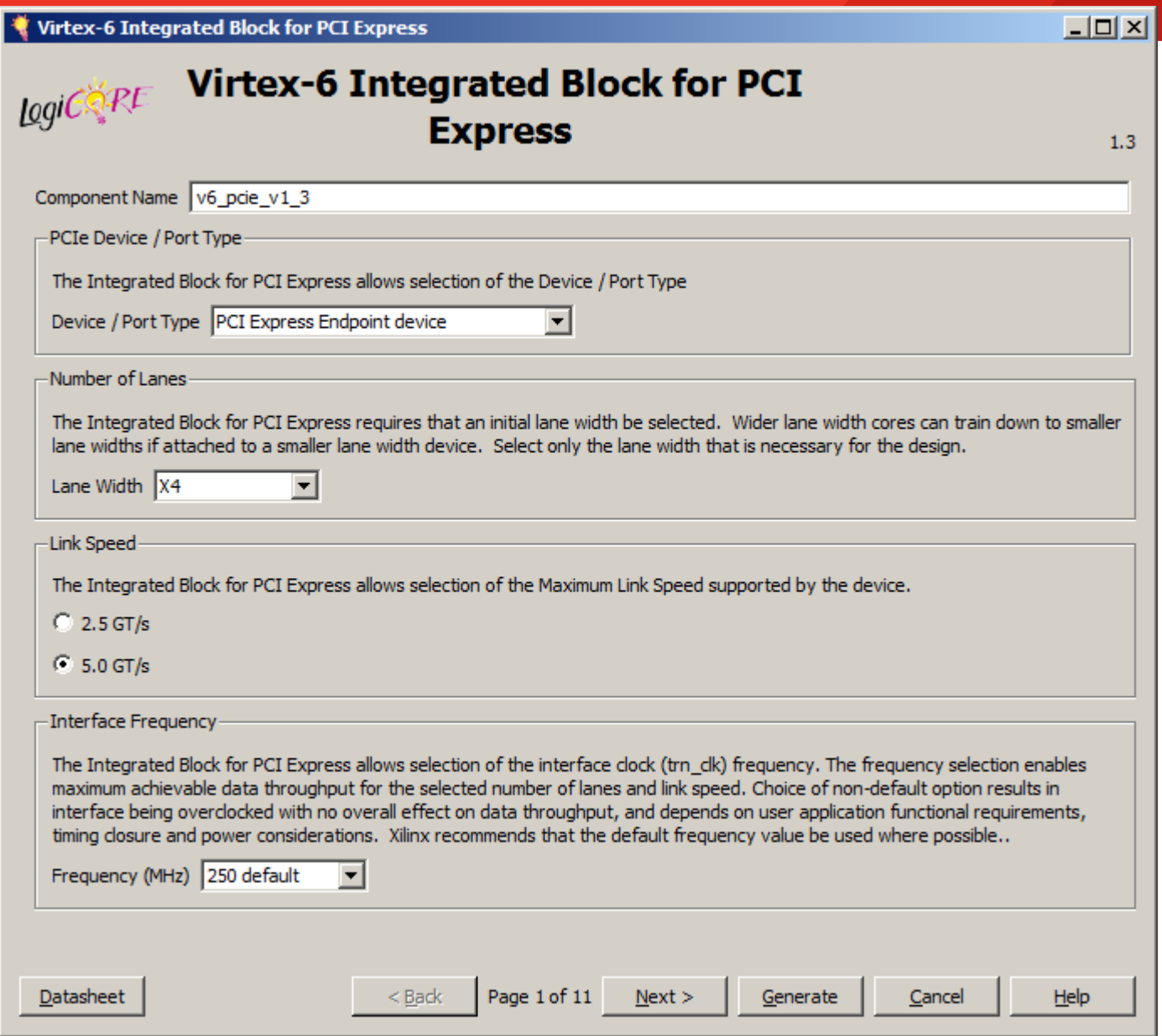
Generate PCIe Core

- **Right click on the Virtex-6 Integrated Block for PCI Express, Version 1.3**
  - Select **Customize**



Note: Presentation applies to the ML605

Generate PCIe Core



- Set the lane Width to X4
- Set the Link Speed to 5.0 GT/s
- Click Next

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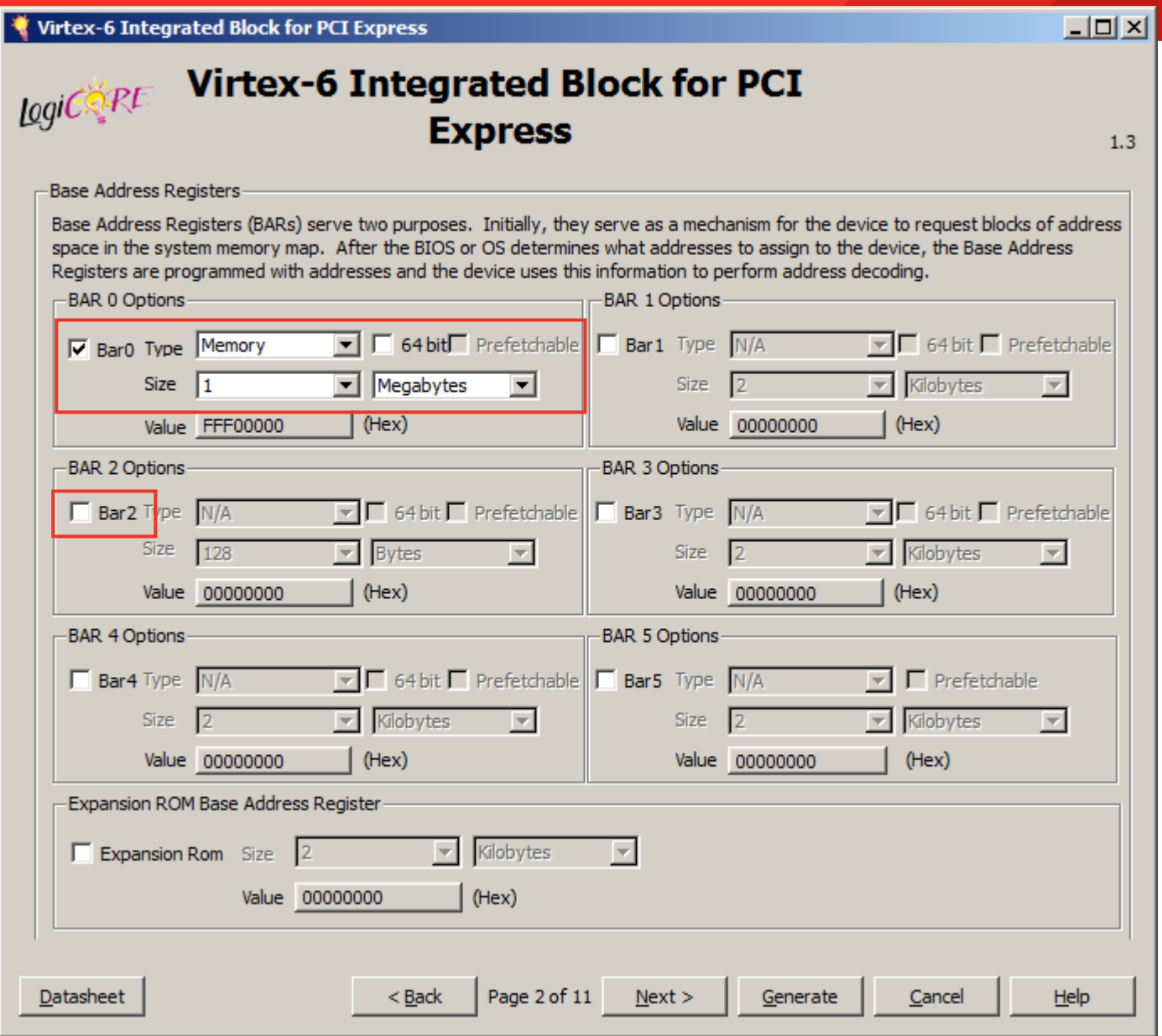
Generate PCIe Core



- **BAR 0**
  - Set to 1 Megabytes
- **BAR 2**
  - Deselect BAR 2
- **Click Next**

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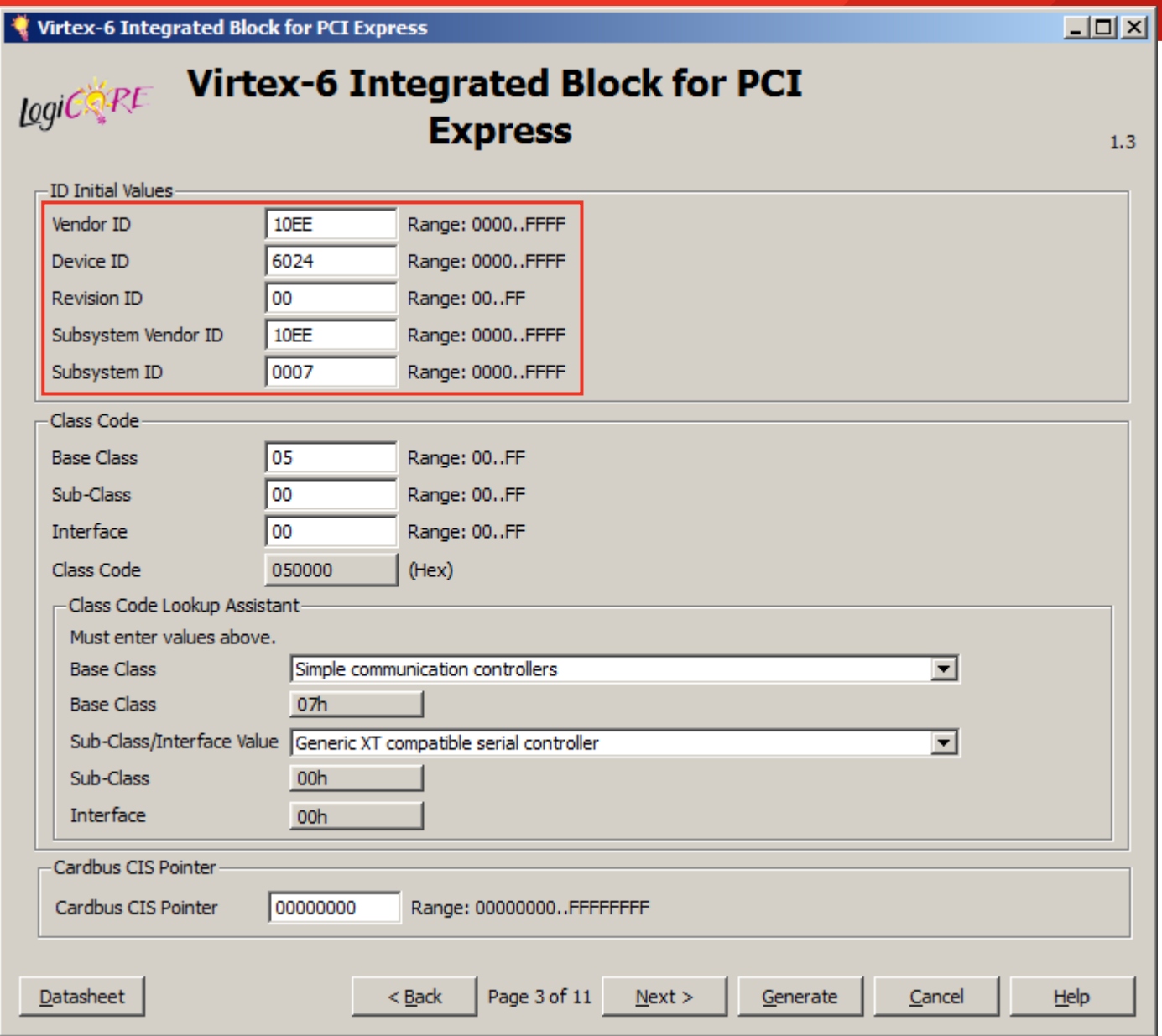
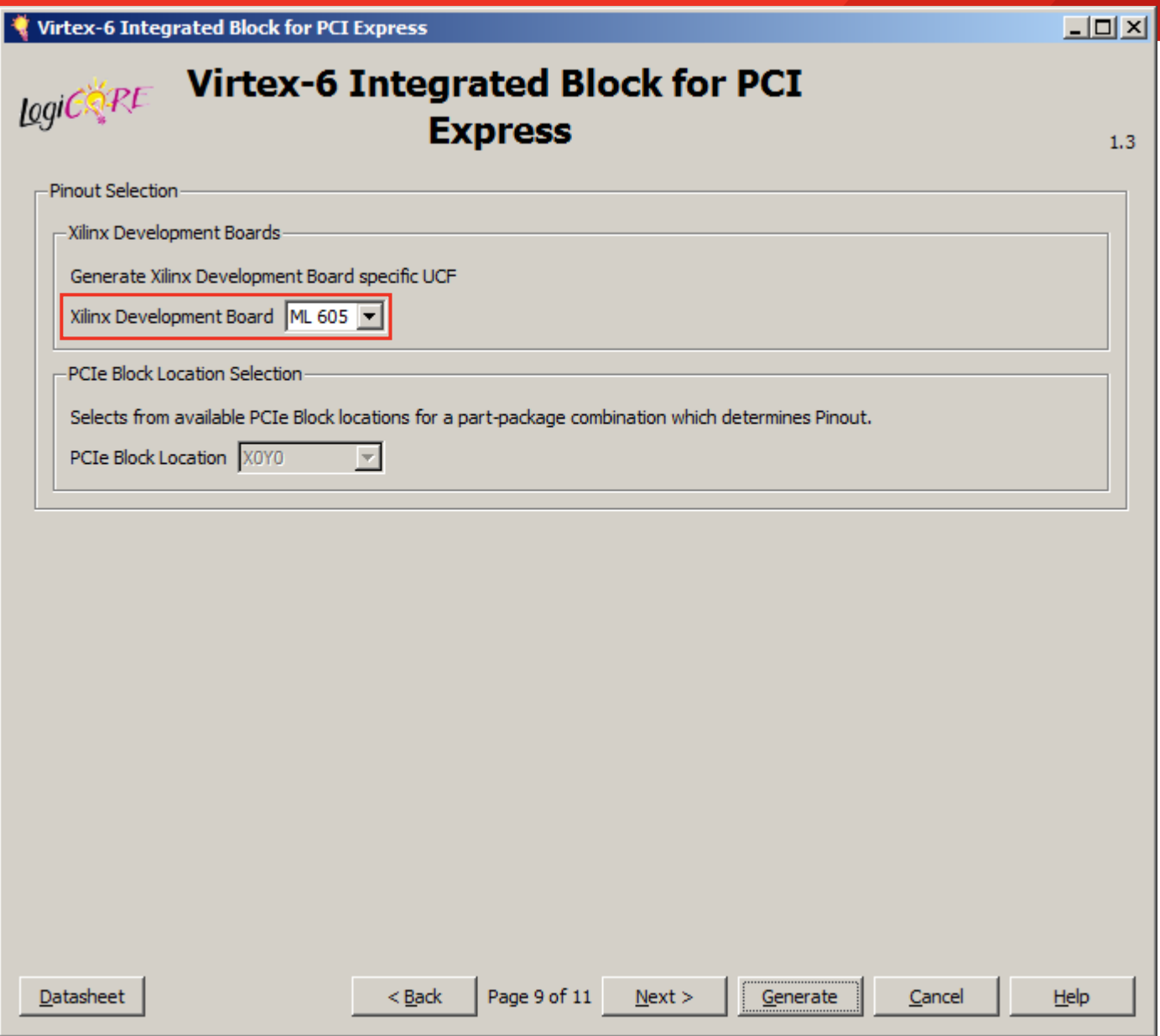
Generate PCIe Core



- **Note ID Initial Values**
  - Vendor ID = **10EE**
  - Device ID = **6024**
  - Revision ID = **00**
  - Subsystem Vendor ID = **10EE**
  - Subsystem ID = **0007**
- **Click Next 6 times**

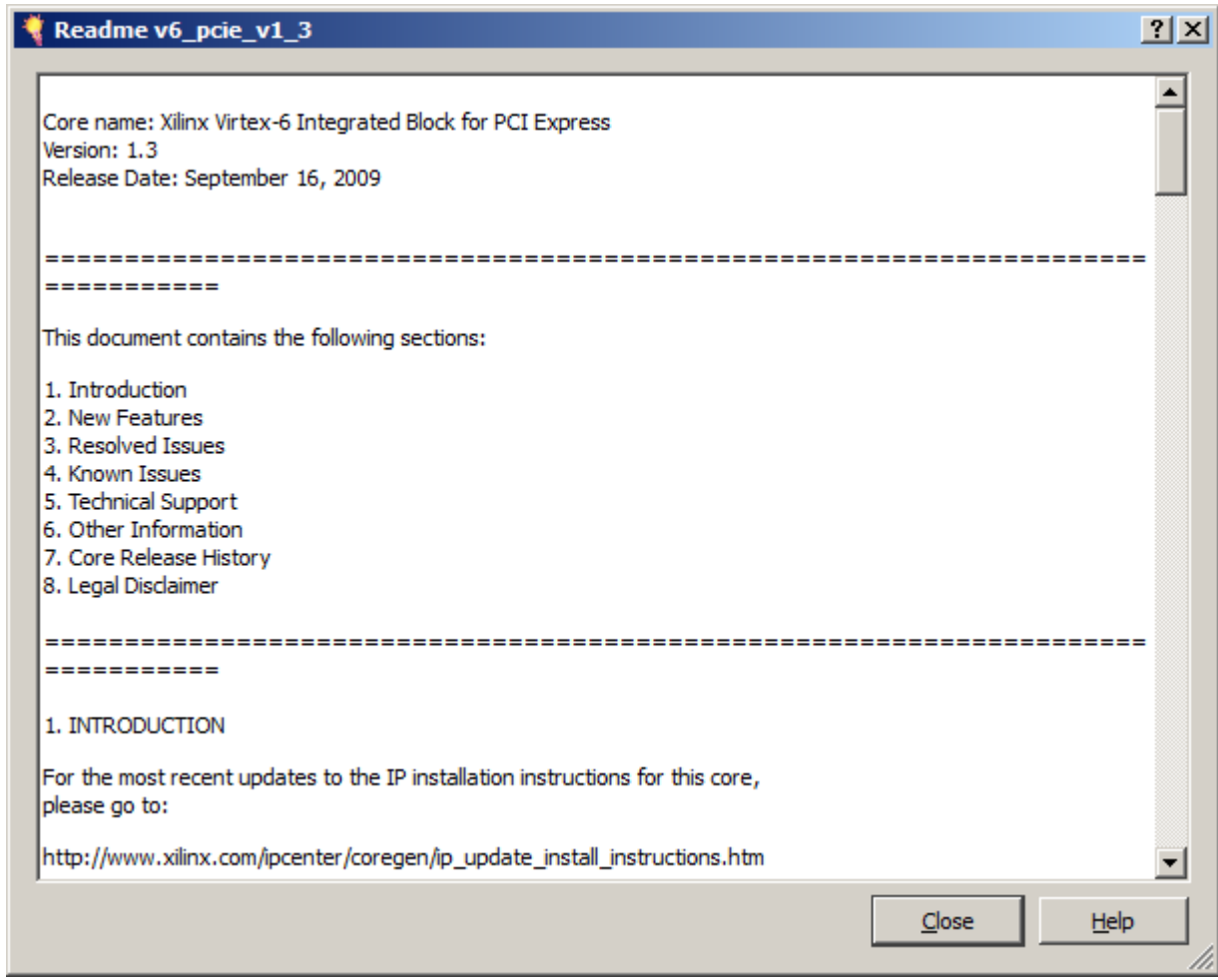
Generate PCIe Core



- **On Page 9**
  - Select ML605
- **Click Generate**

Generate PCIe Core

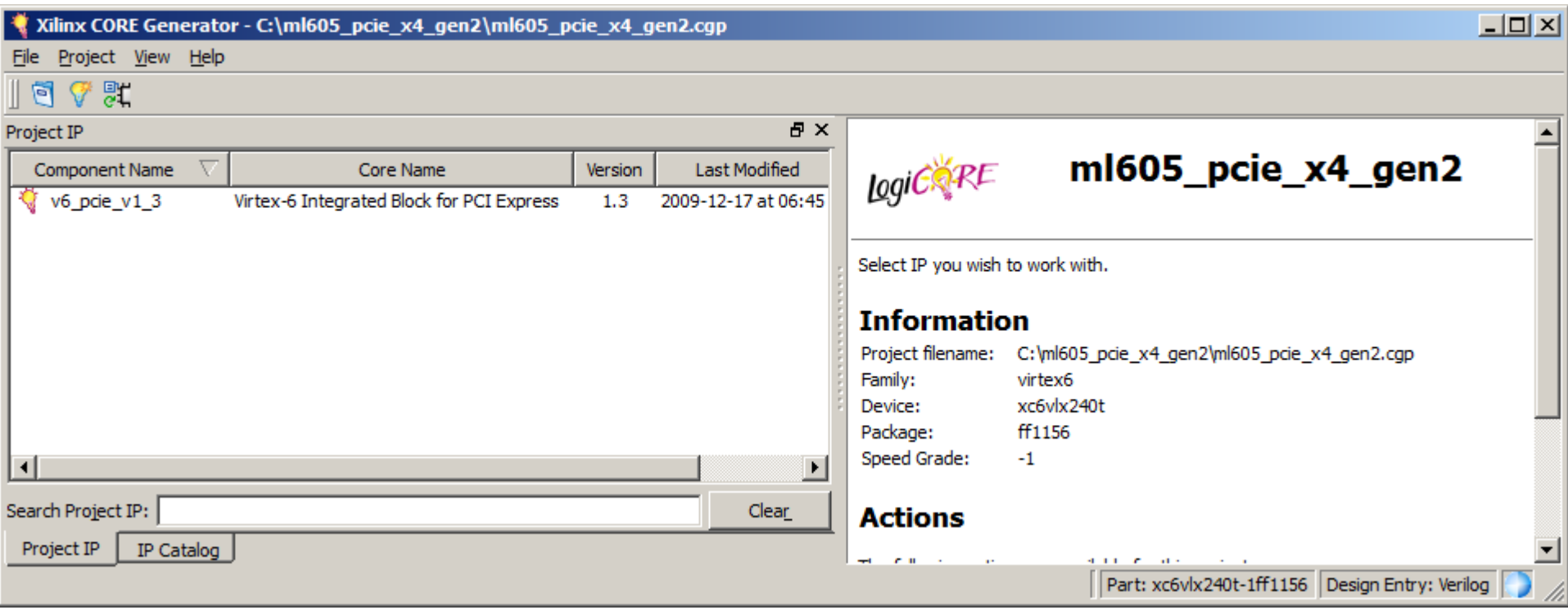
- After the PCIe core finishes generating, click OK on the Readme File window



Note: Presentation applies to the ML605

Generate PCIe Core

- The v6_pcie_v1_3 IP appears under the Project IP tab



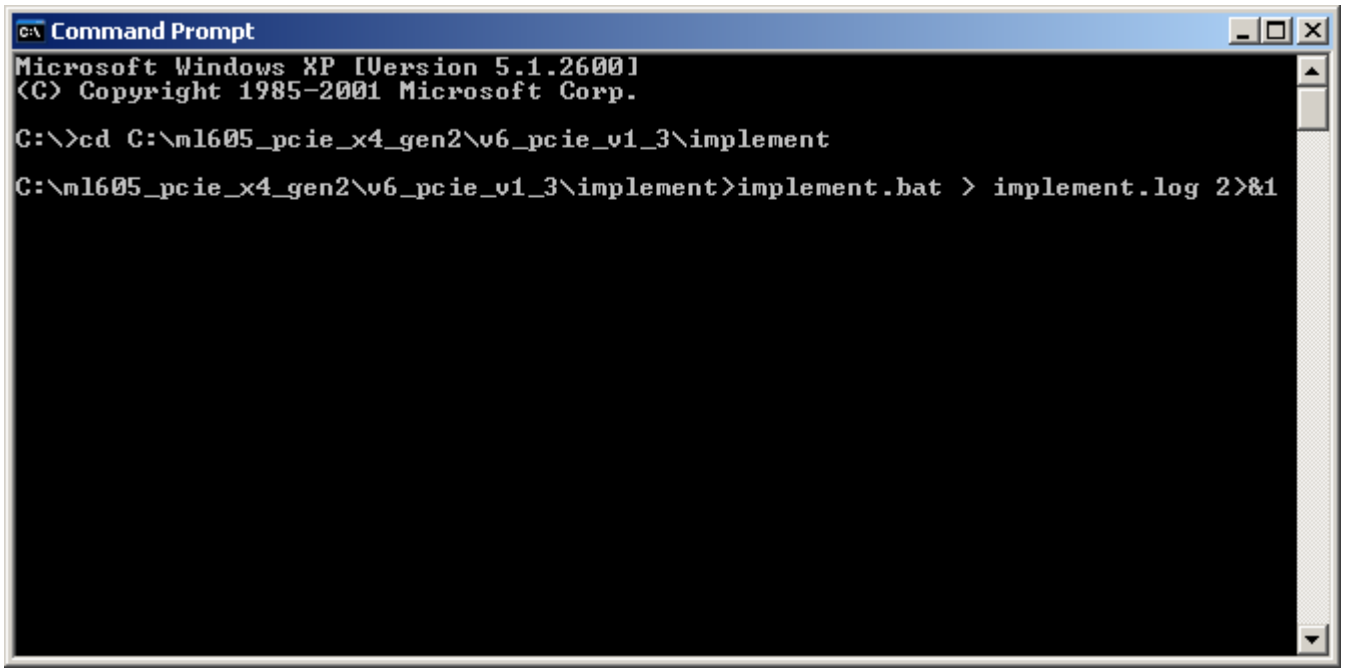
Note: Presentation applies to the ML605

Compile PCIe Core

- **Type these commands in a windows command shell:**

  cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement

  implement.bat > implement.log 2>&1



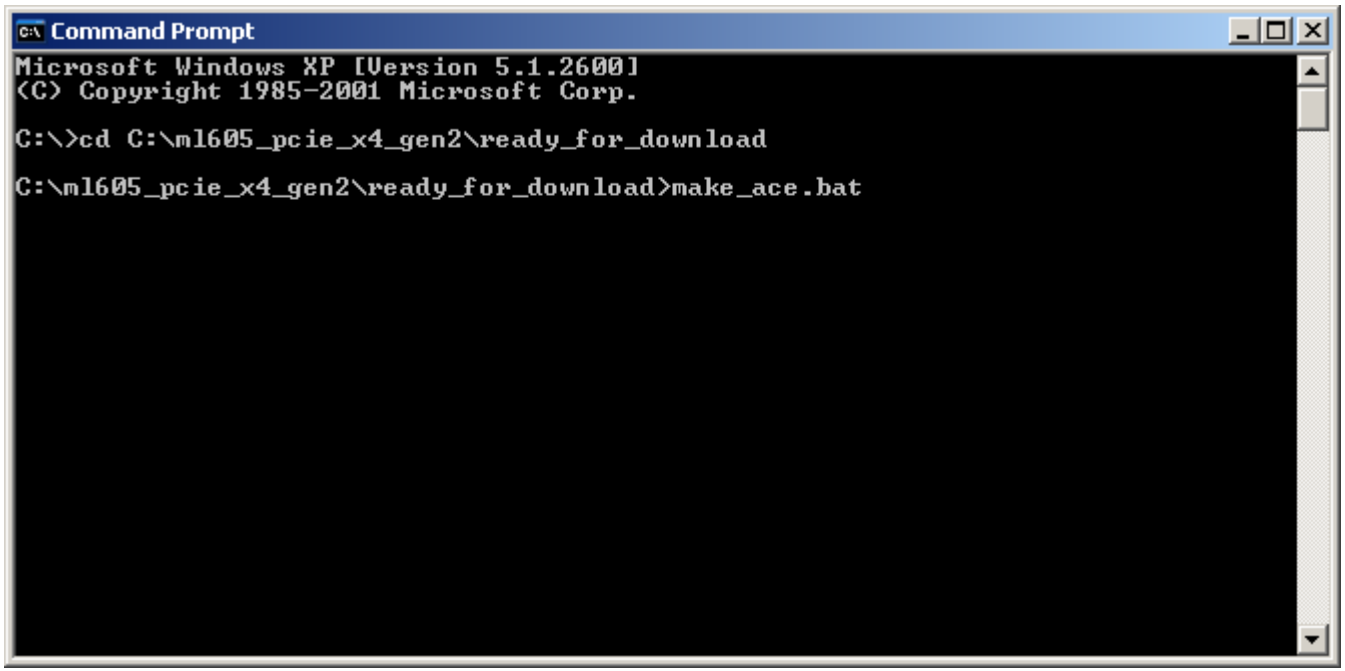
Note: Presentation applies to the ML605

Create PCIe ACE File (Optional)

- **Type these commands in a windows command shell:**

  cd C:\ml605_pcie_x4_gen2\ready_for_download

  make_ace.bat



Note: The make_ace.bat file is included with RDF0009

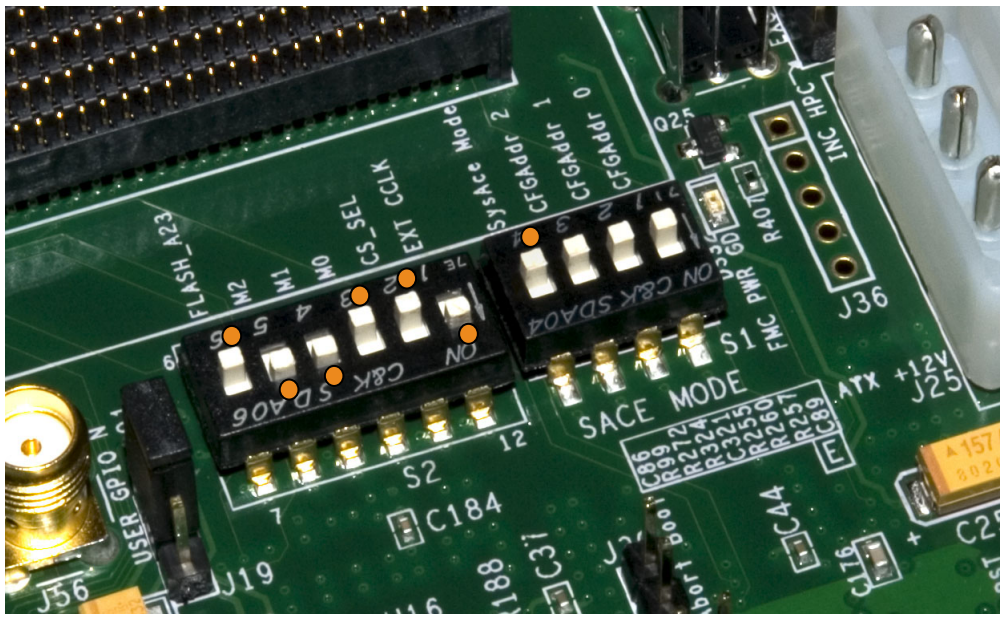
Program Platform Flash with PCIe Design

- **Power on the ML605**
- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board**
  - Connect this cable to your PC

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Set S2 to 011001 (1 = on, Position 6 → Position 1)**
  - This selects Slave SelectMAP (Positions 5, 4, and 3), Platform Flash (2) and EXT CCLK (1, for PCIe compliance)
- **Set S1 to 0XXX (X = Don't care, Position 4 → Position 1)**
  - This disables the Compact Flash

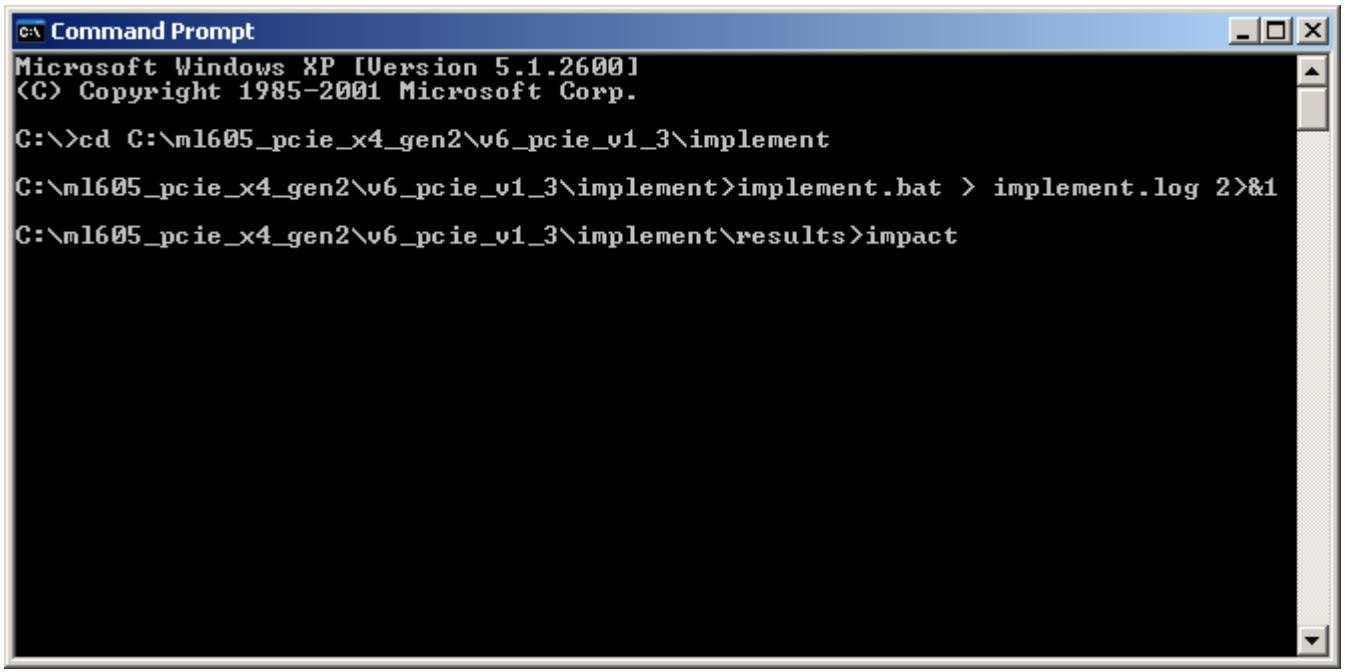


Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Run iMPACT:**

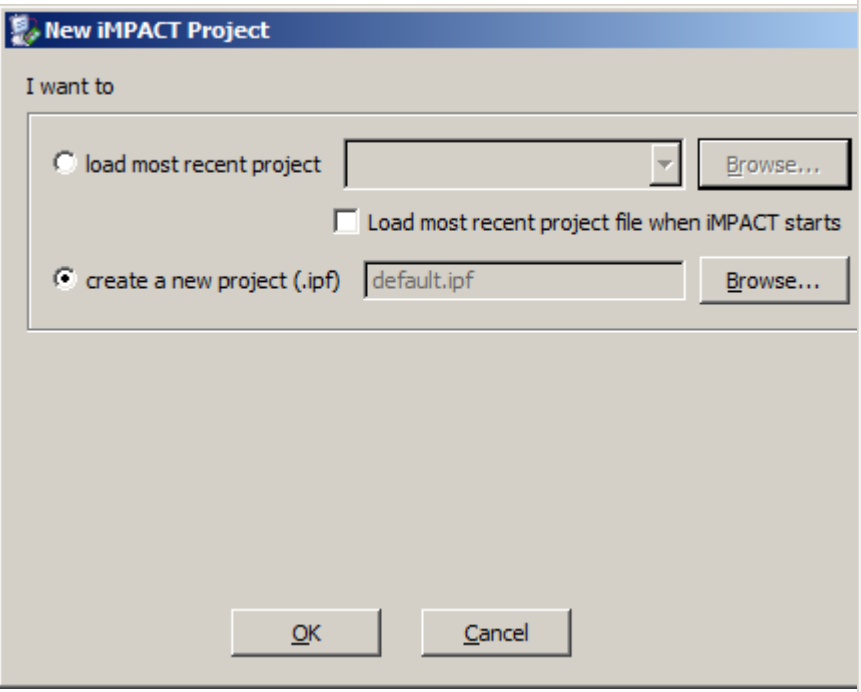
  impact

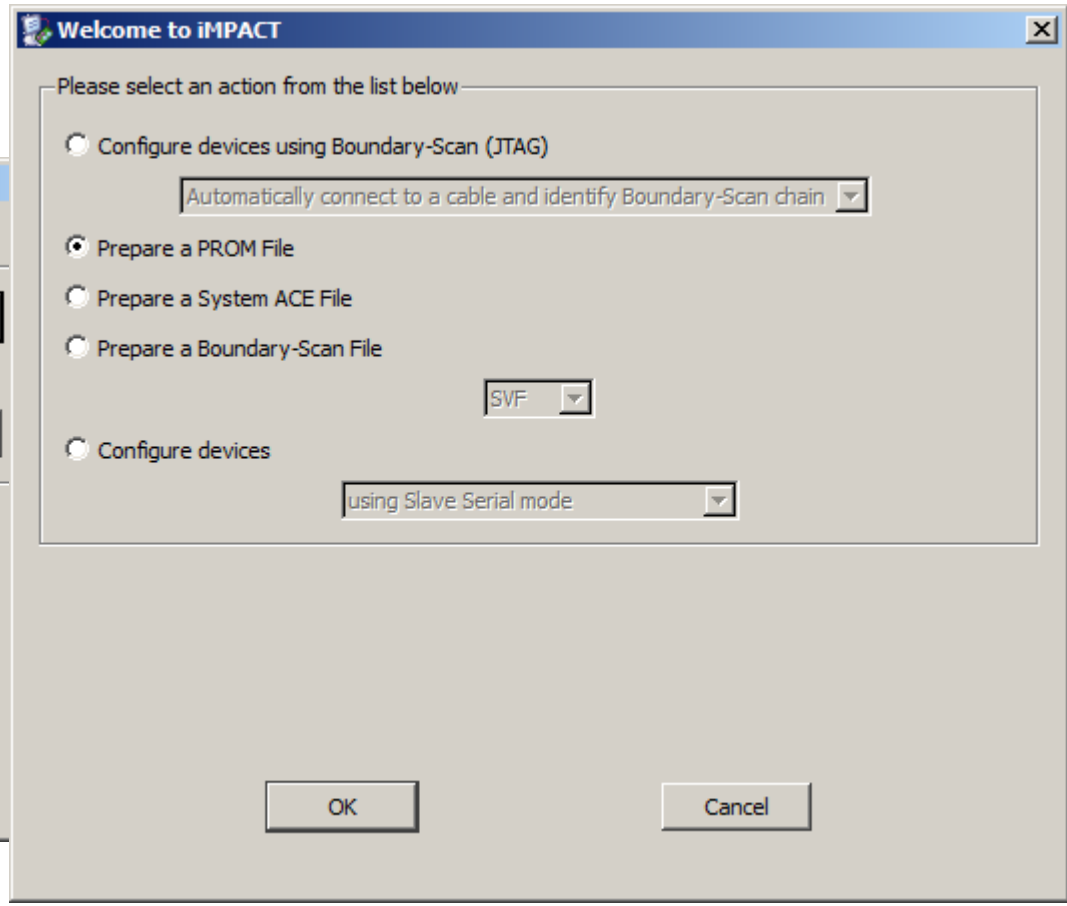


Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **Select**
  - Create a new project
  - Prepare a PROM File

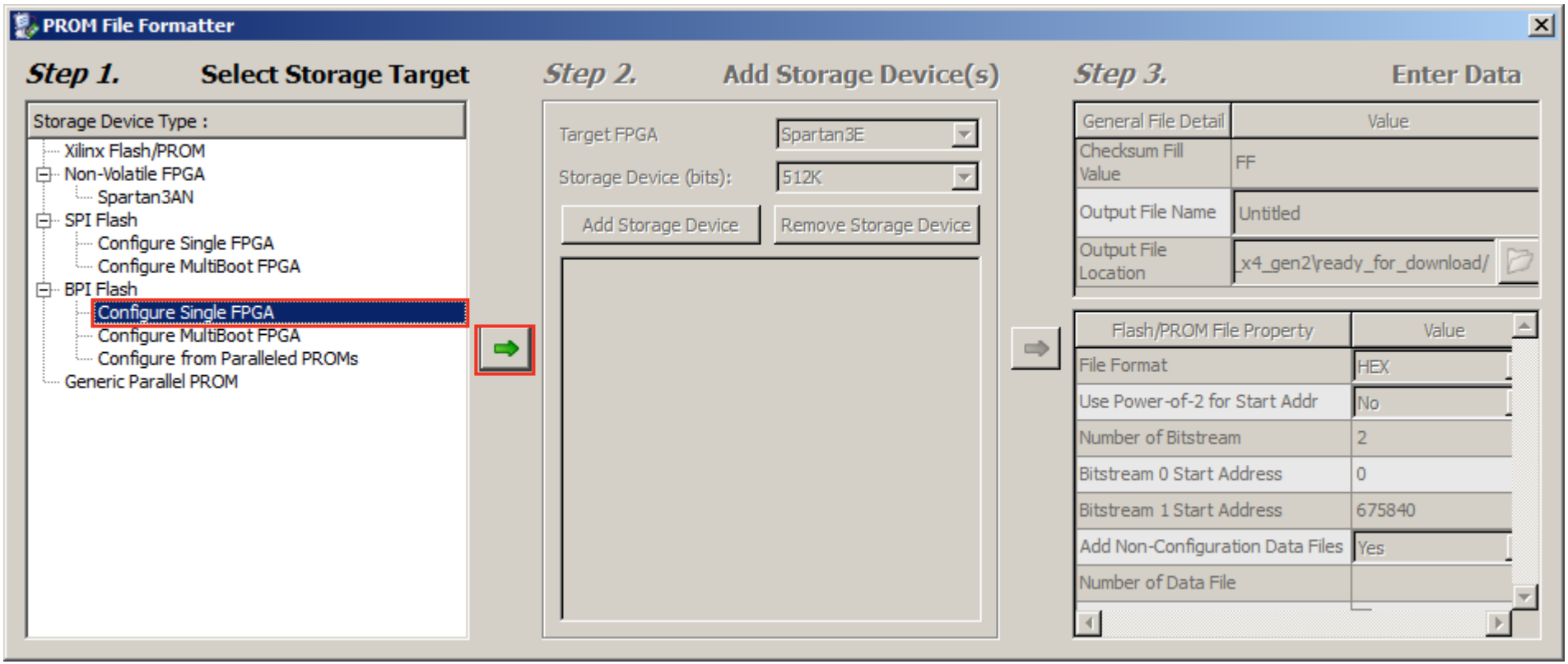




Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

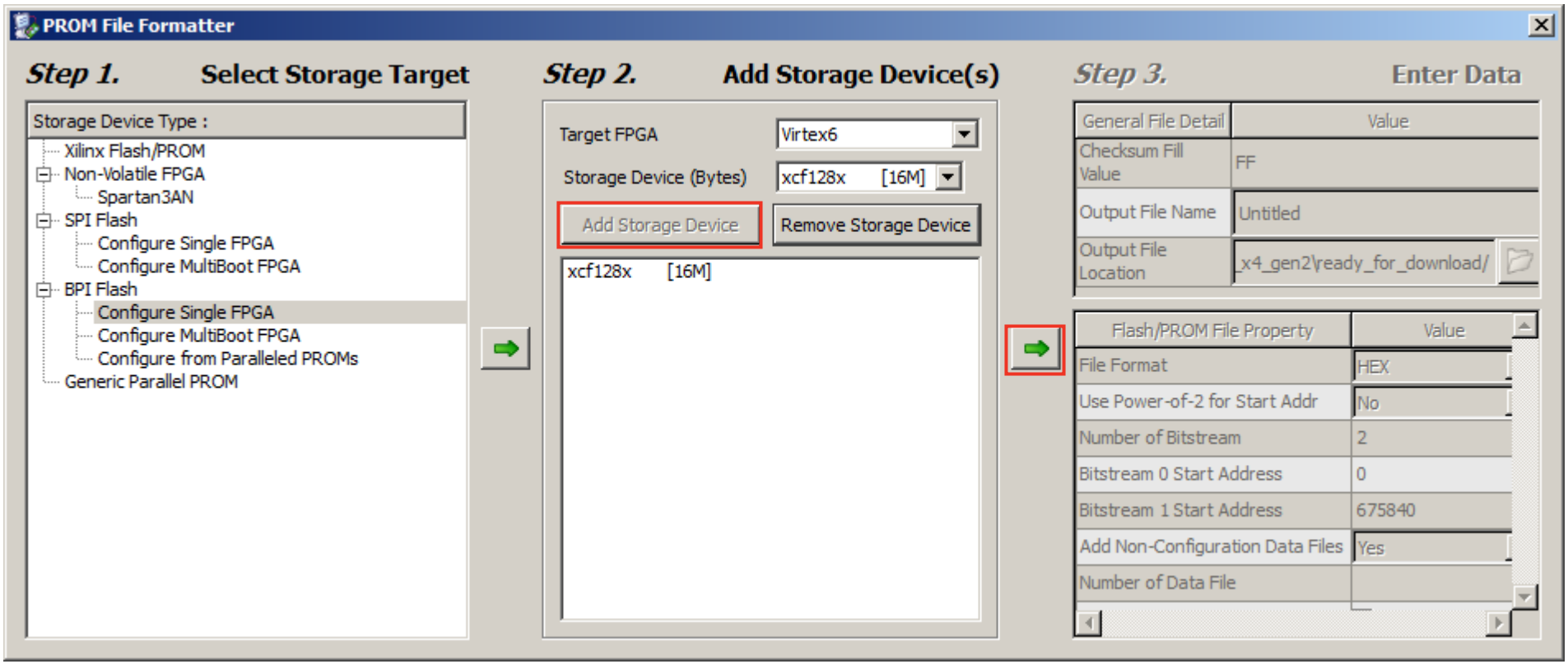
- **To generate a PROM file for the XCF128X Platform Flash, select:**
  - BPI – Configure Single FPGA



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

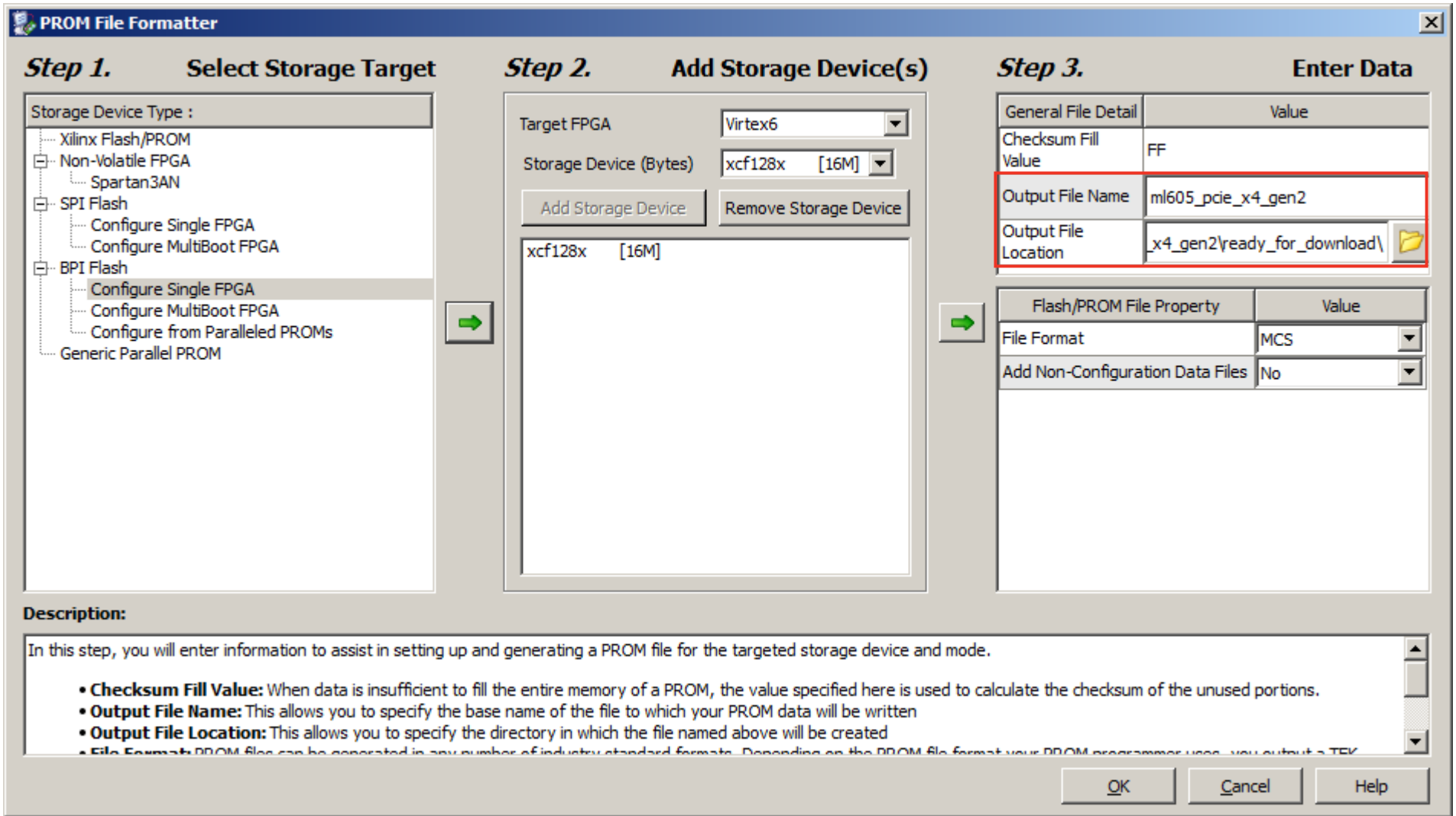
- Add xcf128x



Note: Presentation applies to the ML605

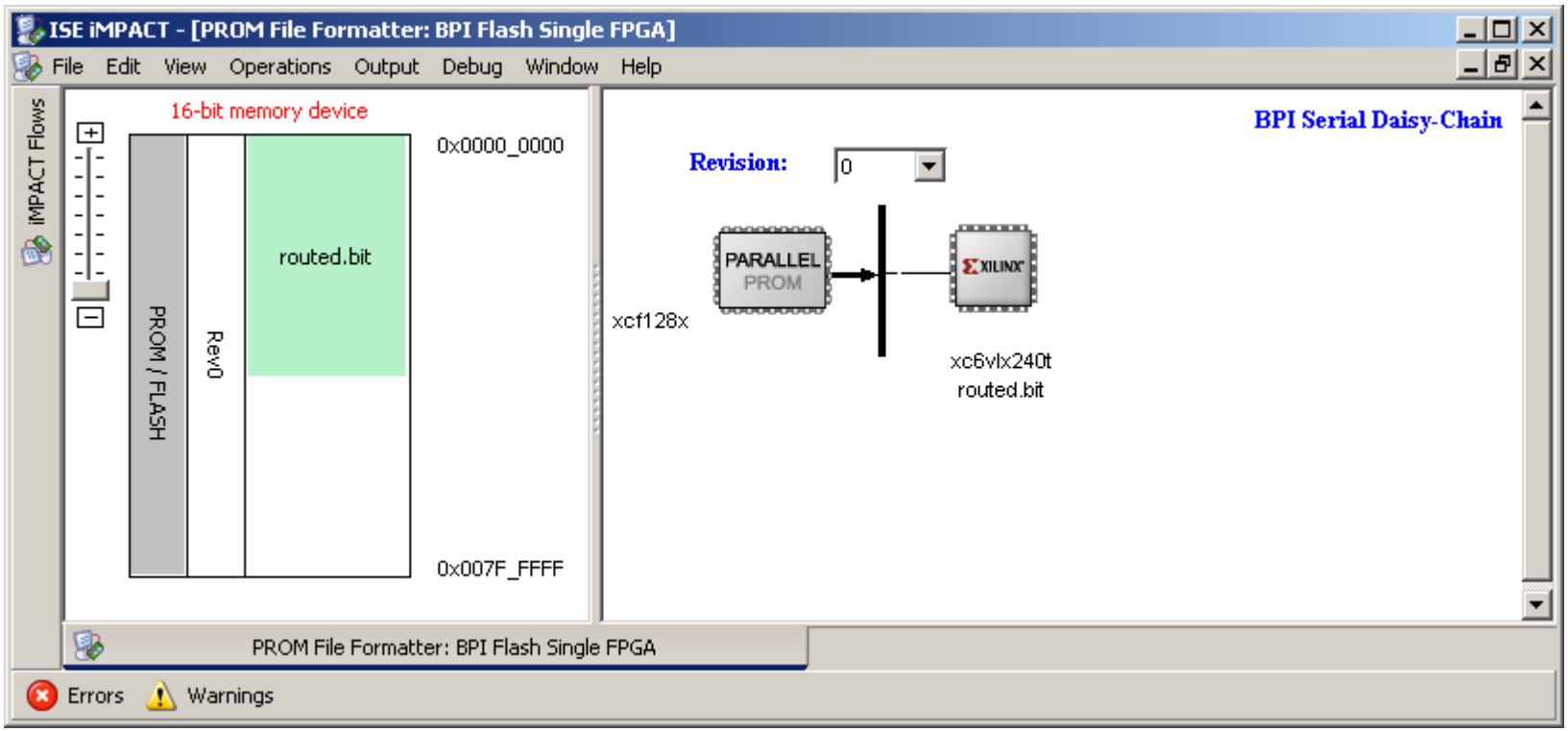
Program Platform Flash with PCIe Design

- Set file name and location as desired and click OK



Program Platform Flash with PCIe Design

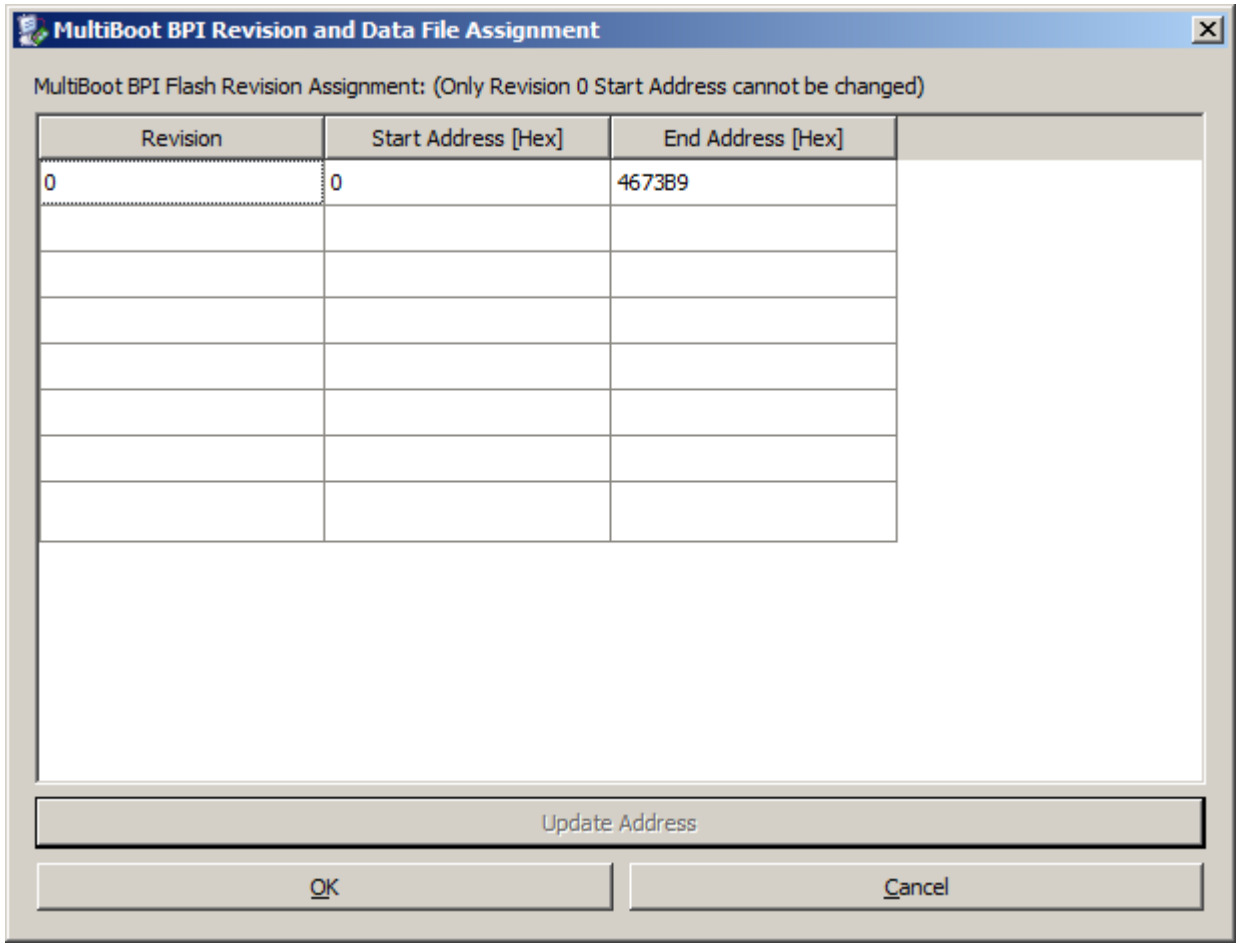
- Add routed.bit from the <design path>\v6_pcie_v1_3\implement\results



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- Click OK on this dialog

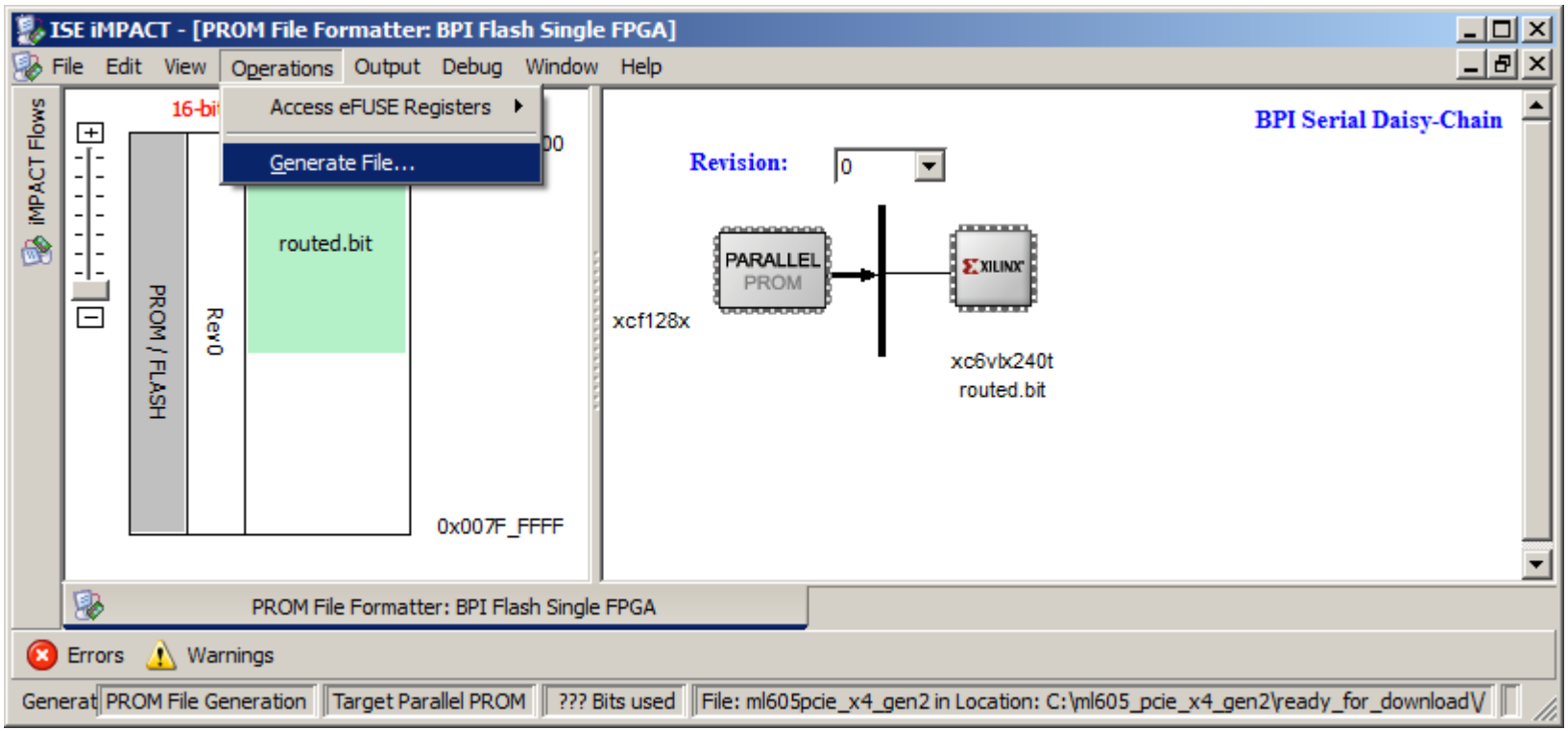


Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- From the iMPACT menu, select

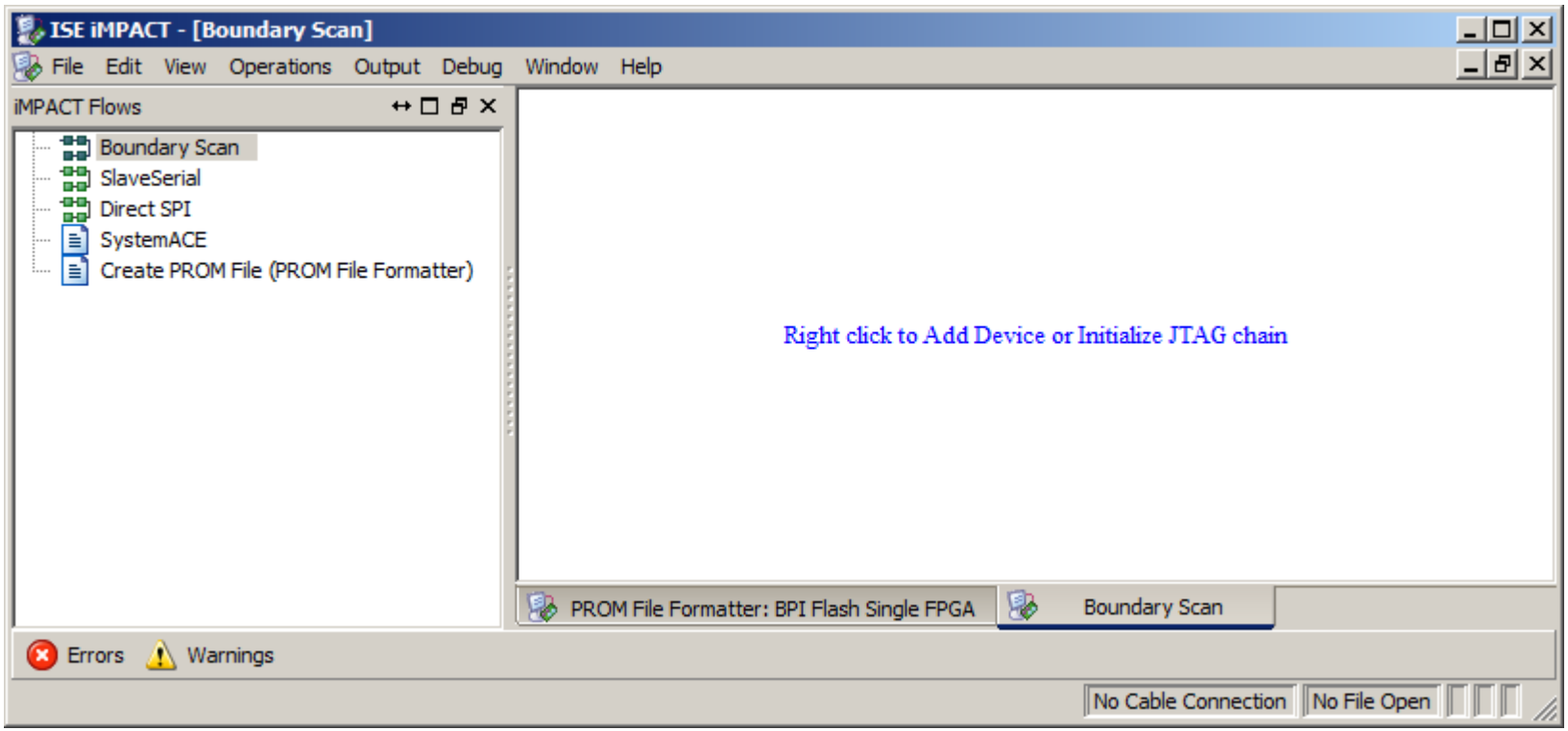
  Operations → Generate File…



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- After generation completes, under the iMPACT Flows, double click on Boundary Scan

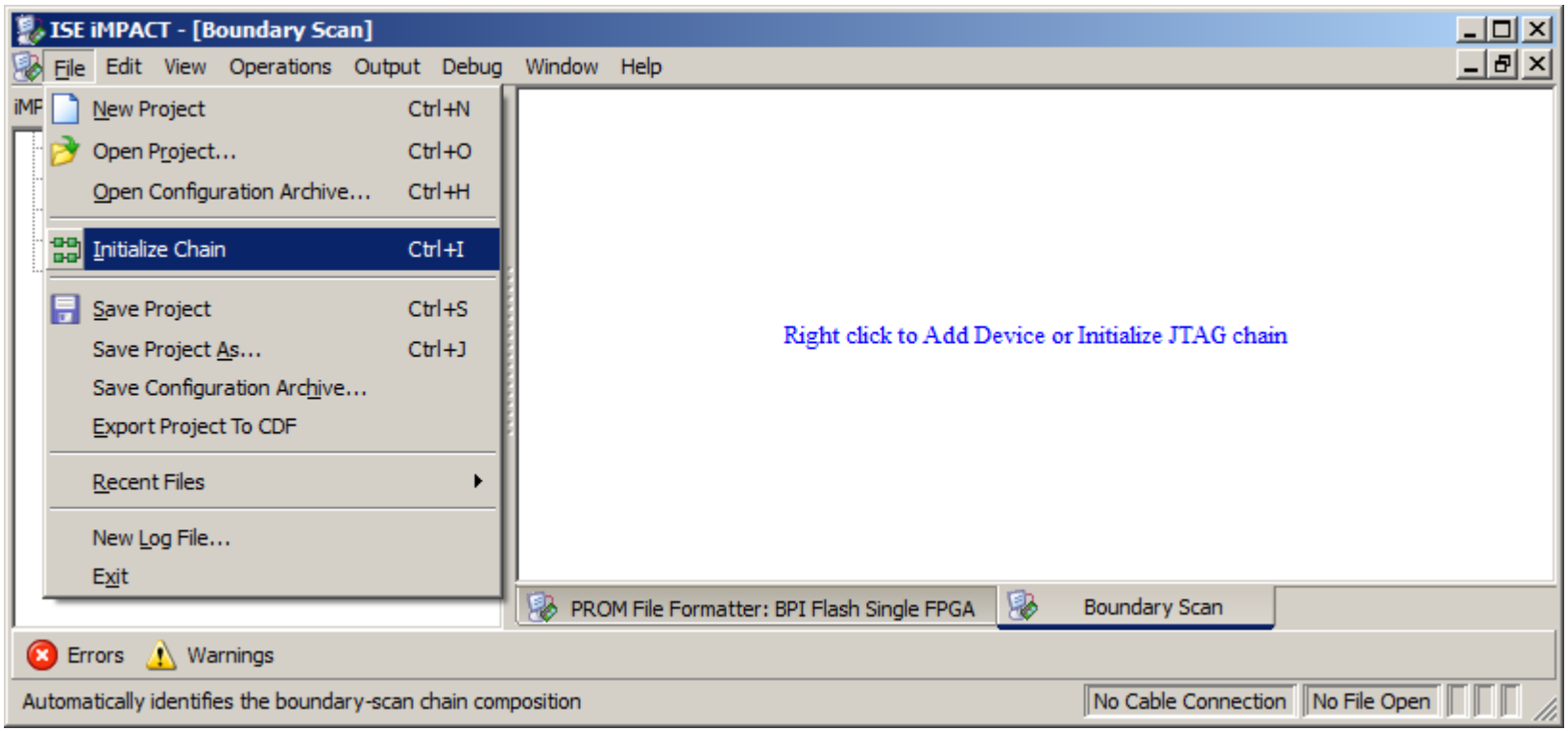


Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- **From the iMPACT menu, select**

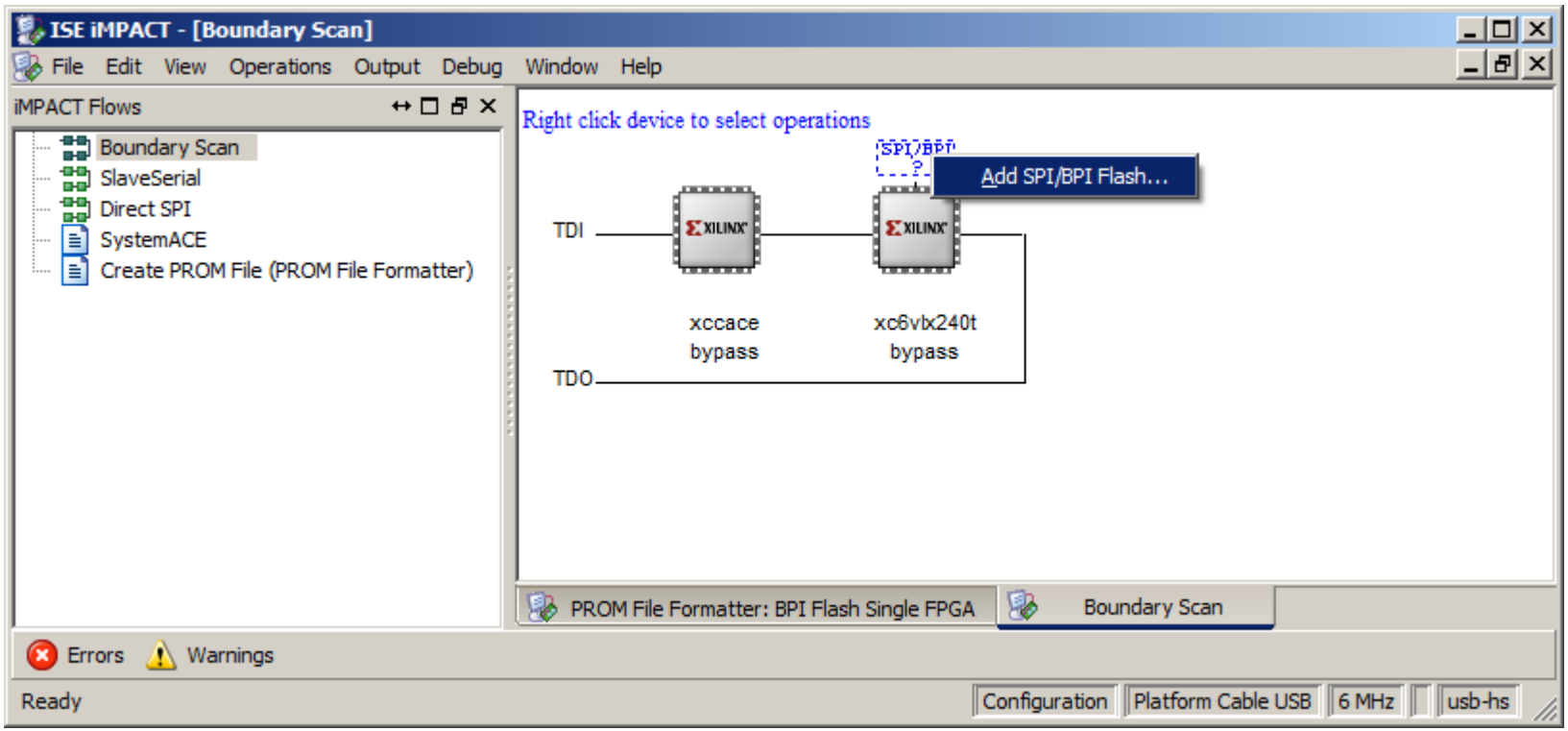
  File → Initialize Chain



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

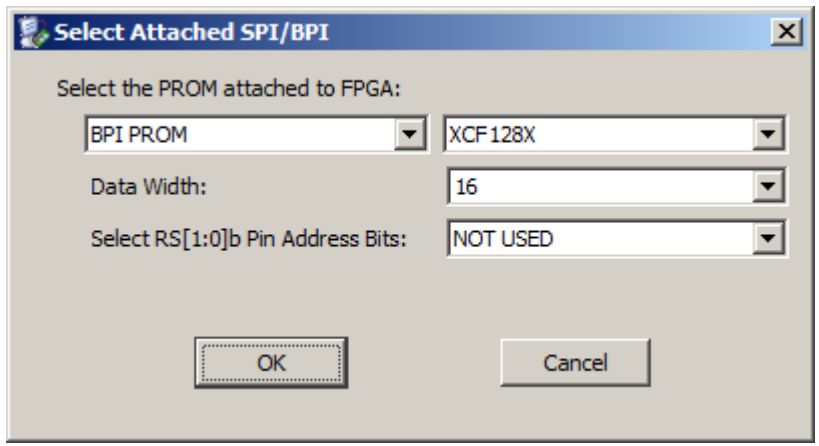
- **Right click on the SPI/BPI ? and select Add SPI/BPI Flash…**
  - Add <design path>\ready_for_download\ml605_pcie_x4_gen2.mcs



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

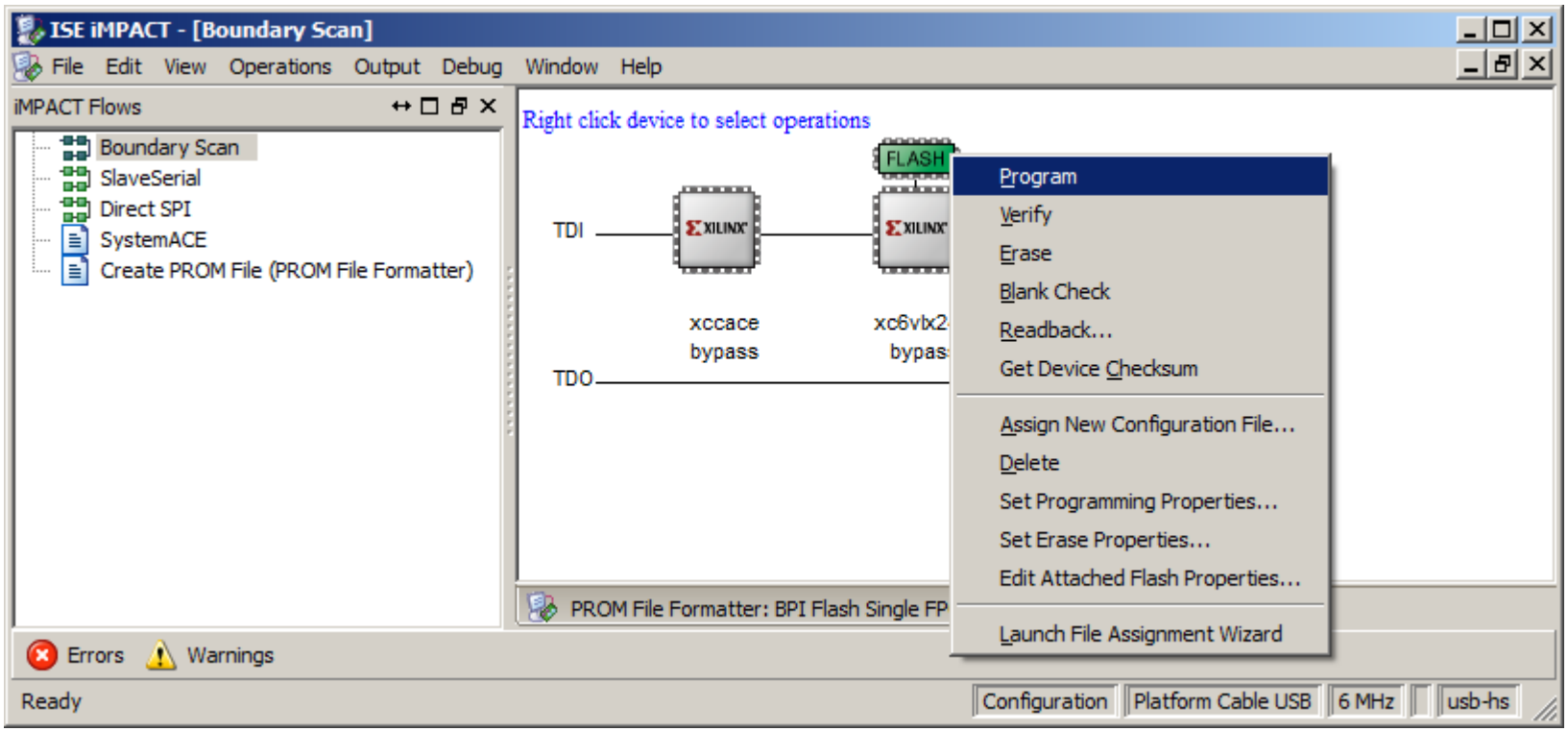
- Click OK for this dialog



Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

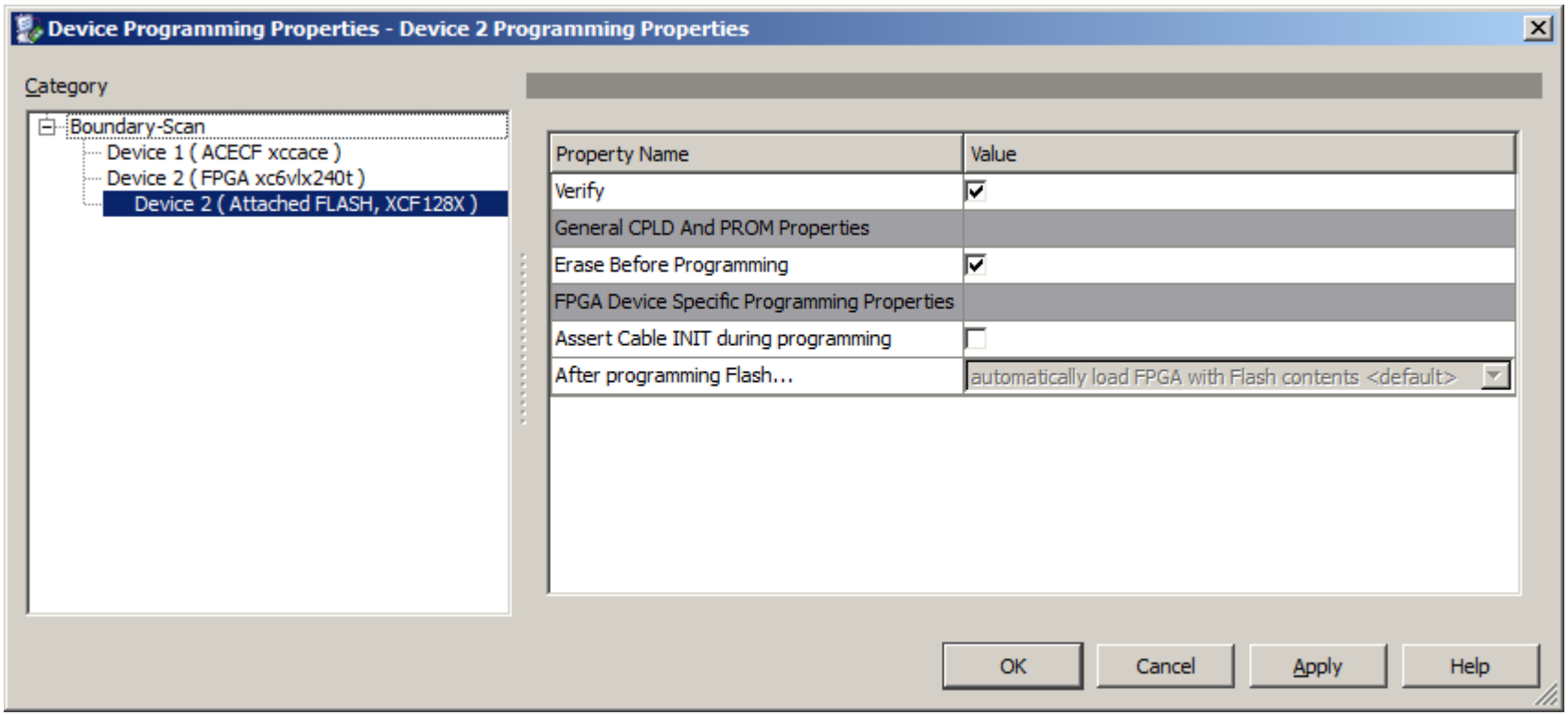
- Right click on the Flash and select Program



Note: Takes about 12 minutes

Program Platform Flash with PCIe Design

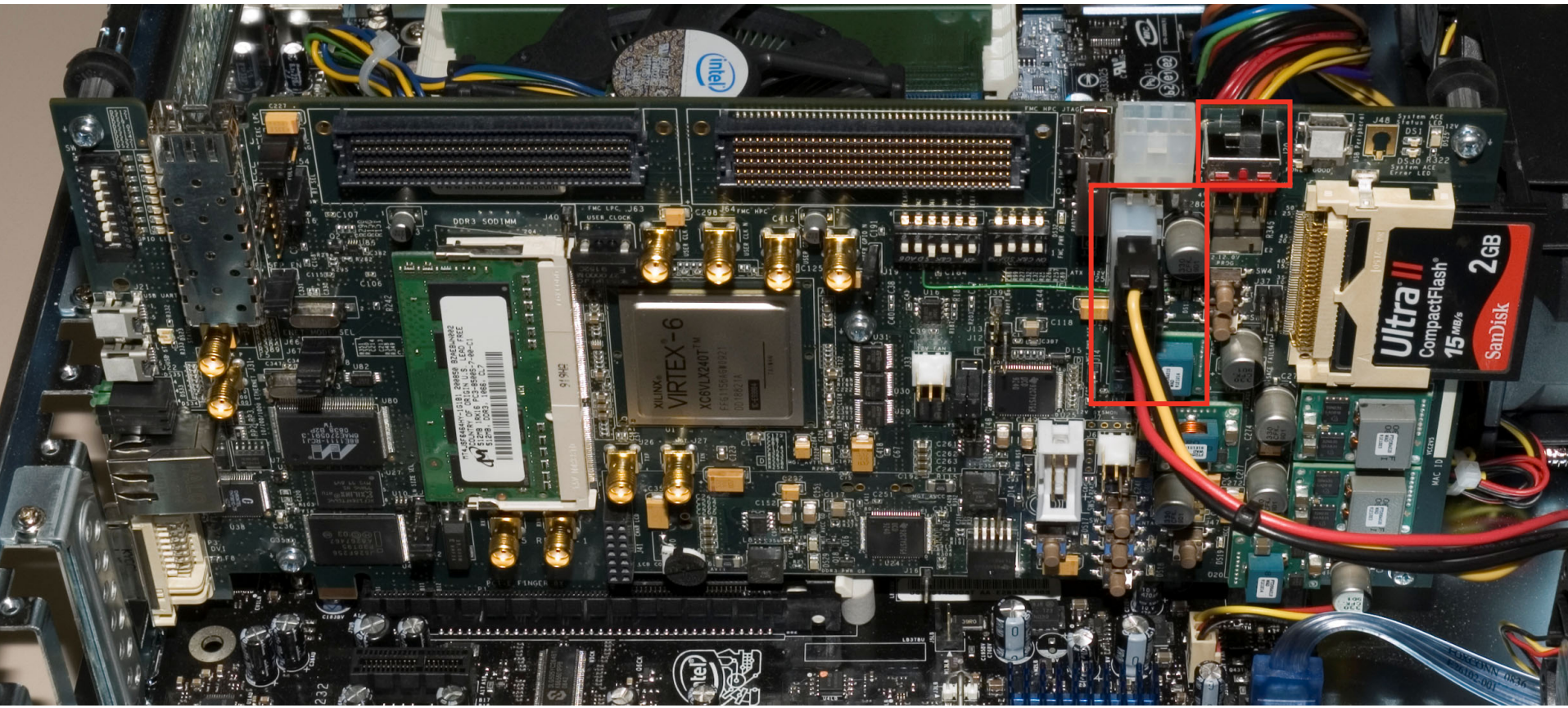
- **Erase Before Programming must be selected**



Note: Presentation applies to the ML605

Hardware Setup

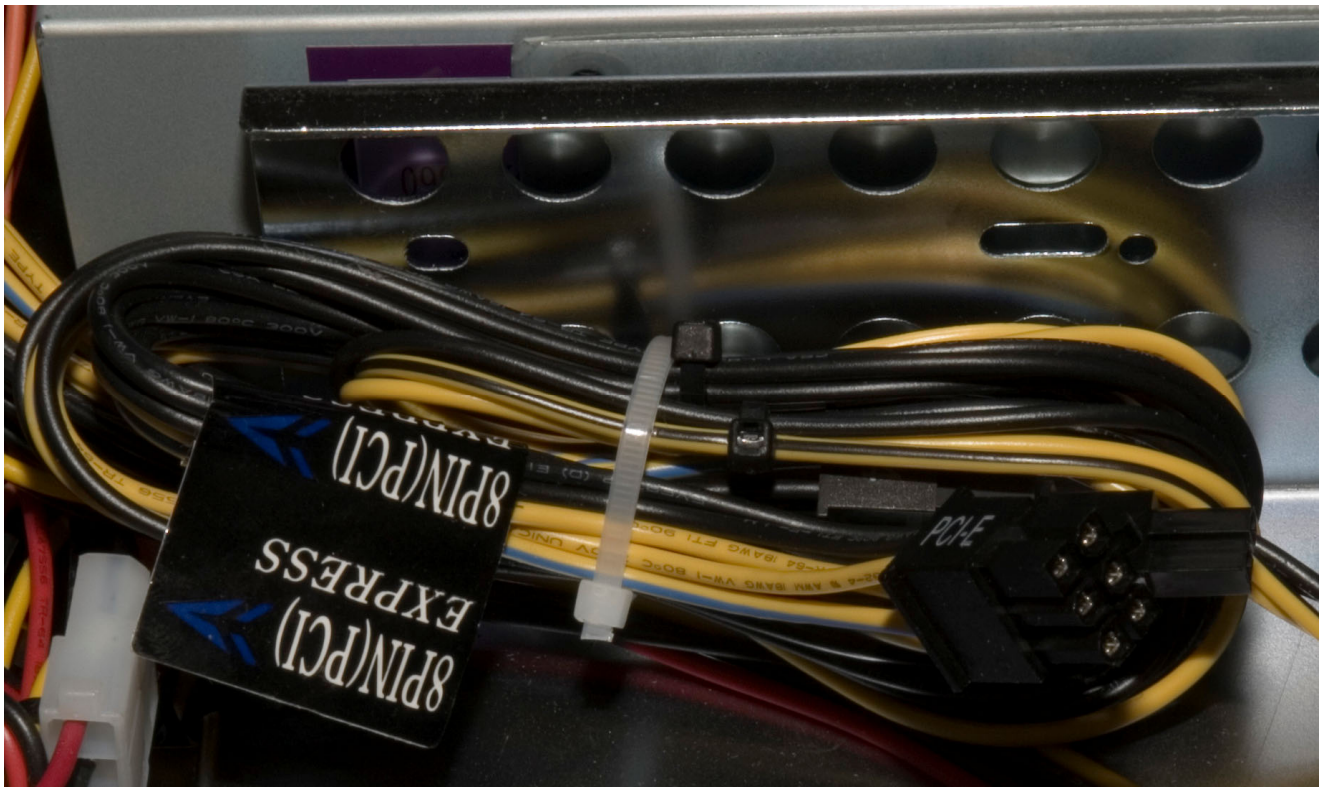
- **Insert the ML605 Board into a PCIe x4 slot (x16 shown)**
  - Connect PC power to J25, turn on Power Switch



Note: Presentation applies to the ML605

Hardware Setup

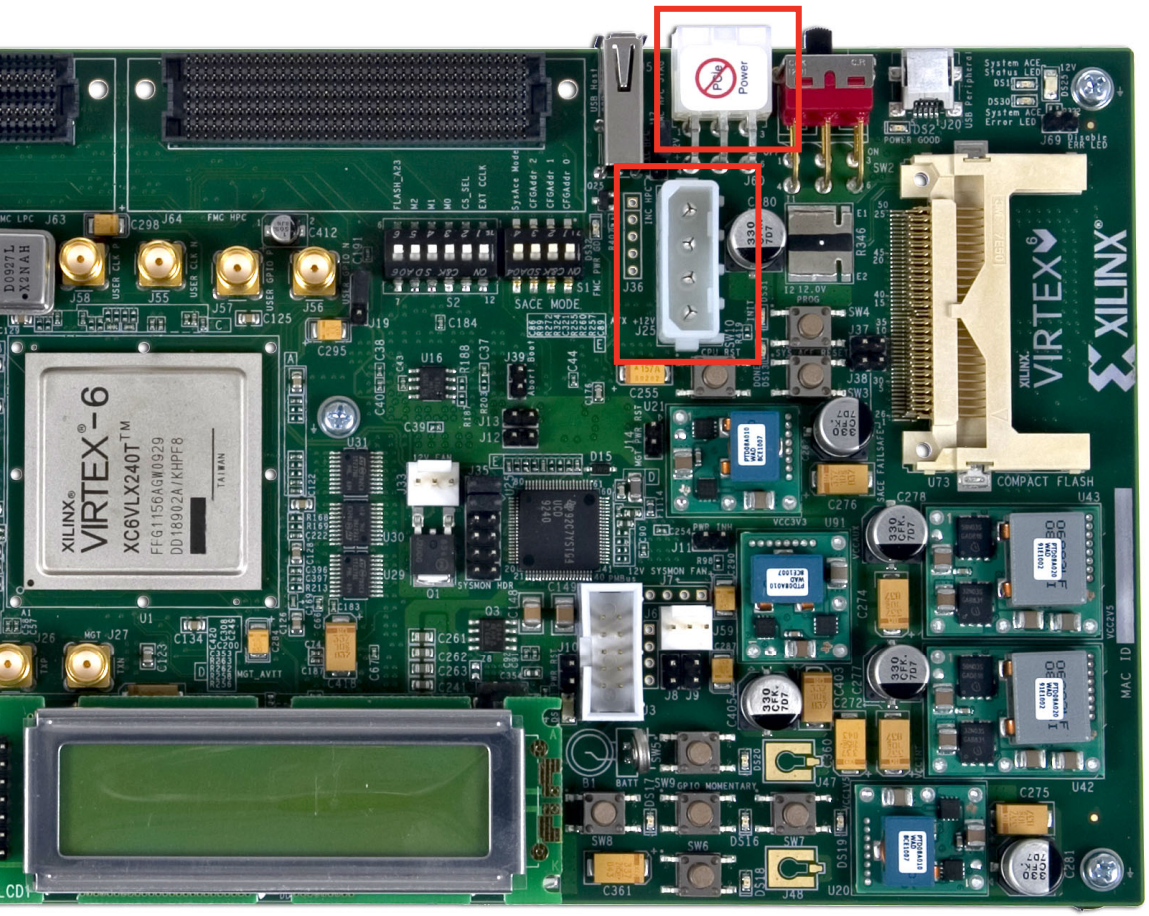
- Do *not* use the PCIe connector from the PC power supply



Note: Presentation applies to the ML605

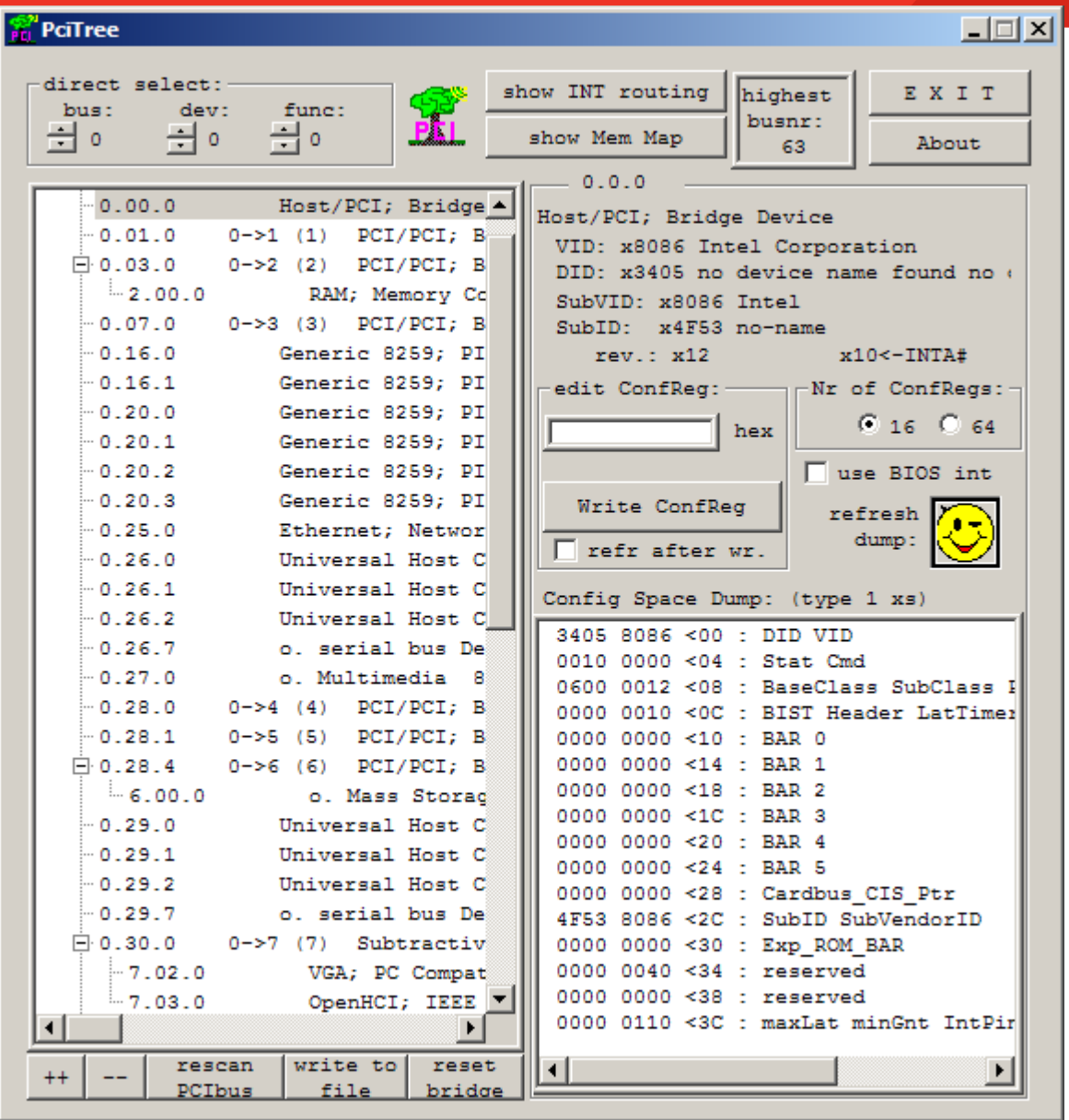
Hardware Setup

- Do not connect both the ML605 power brick connector (J60) and the four pin ATX power connector at the same time



Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



- Power on the PC
- Start PciTree

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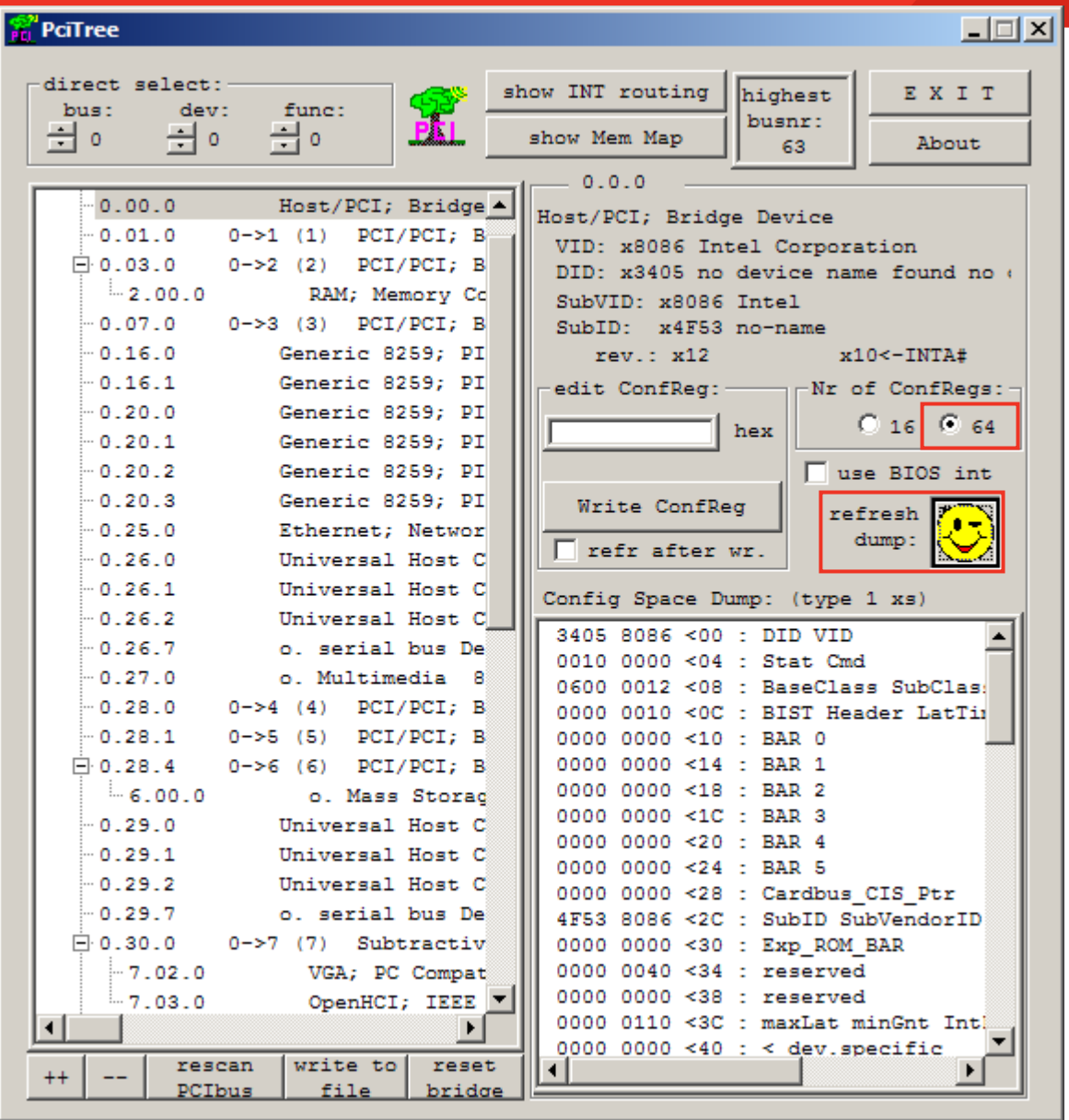
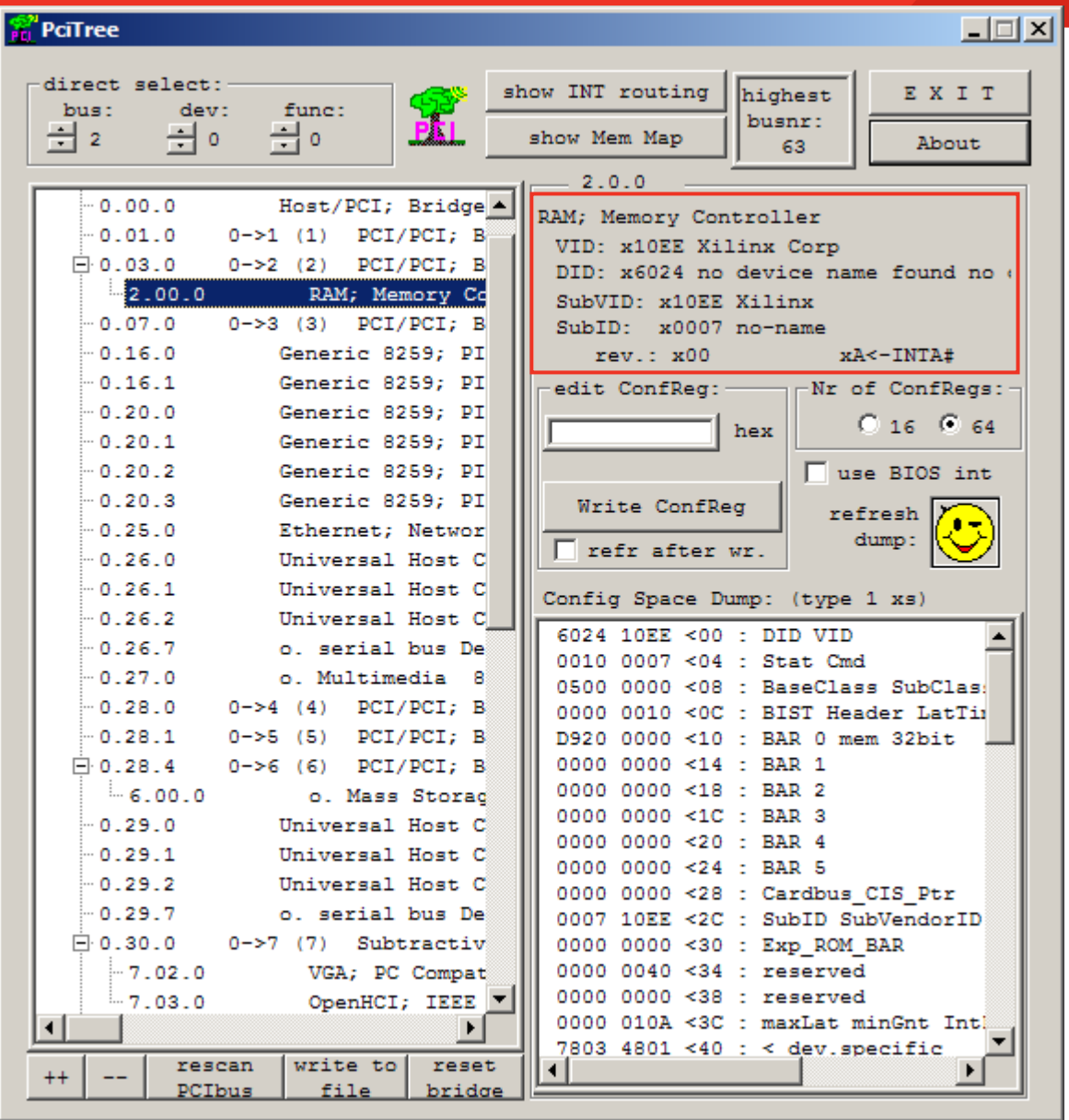
Running the PCIe x4 Gen2 Design



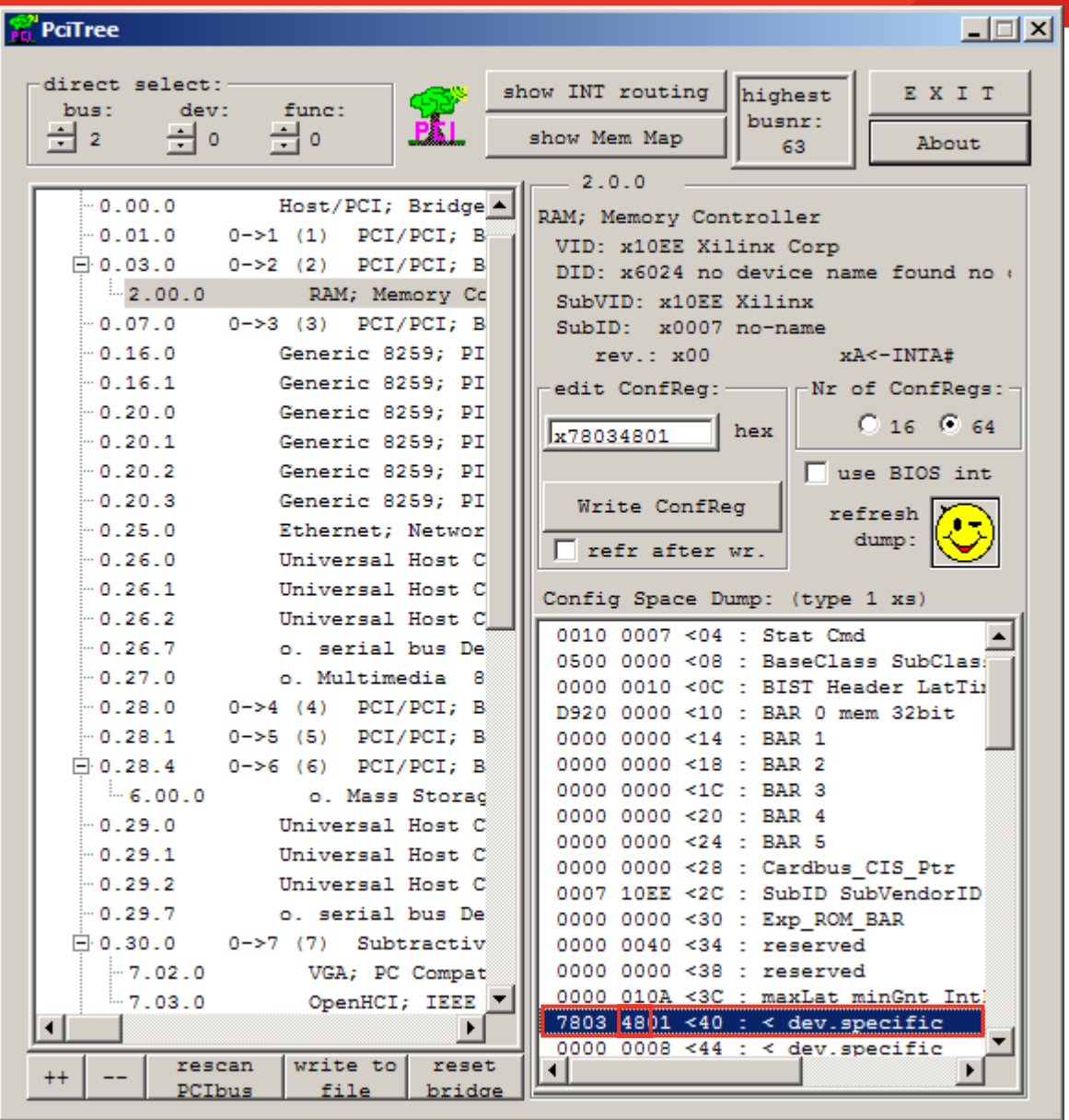
- Set Number of Configuration Registers to 64
- Click on Refresh dump

Running the PCIe x4 Gen2 Design



- **Locate the Xilinx Device**
  - Vendor ID is **0x10EE**
  - The x4 Gen2 configuration will have a Device ID of **0x6024**

Running the PCIe x4 Gen2 Design



- **Navigate the linked list in configuration space to locate the PCIe Capabilities Structure**
  - See UG517 for details
- **With the Xilinx device selected, select Register 0x40**
  - Register 0x40 points to the next structure
  - 0x48 is the address of the next structure

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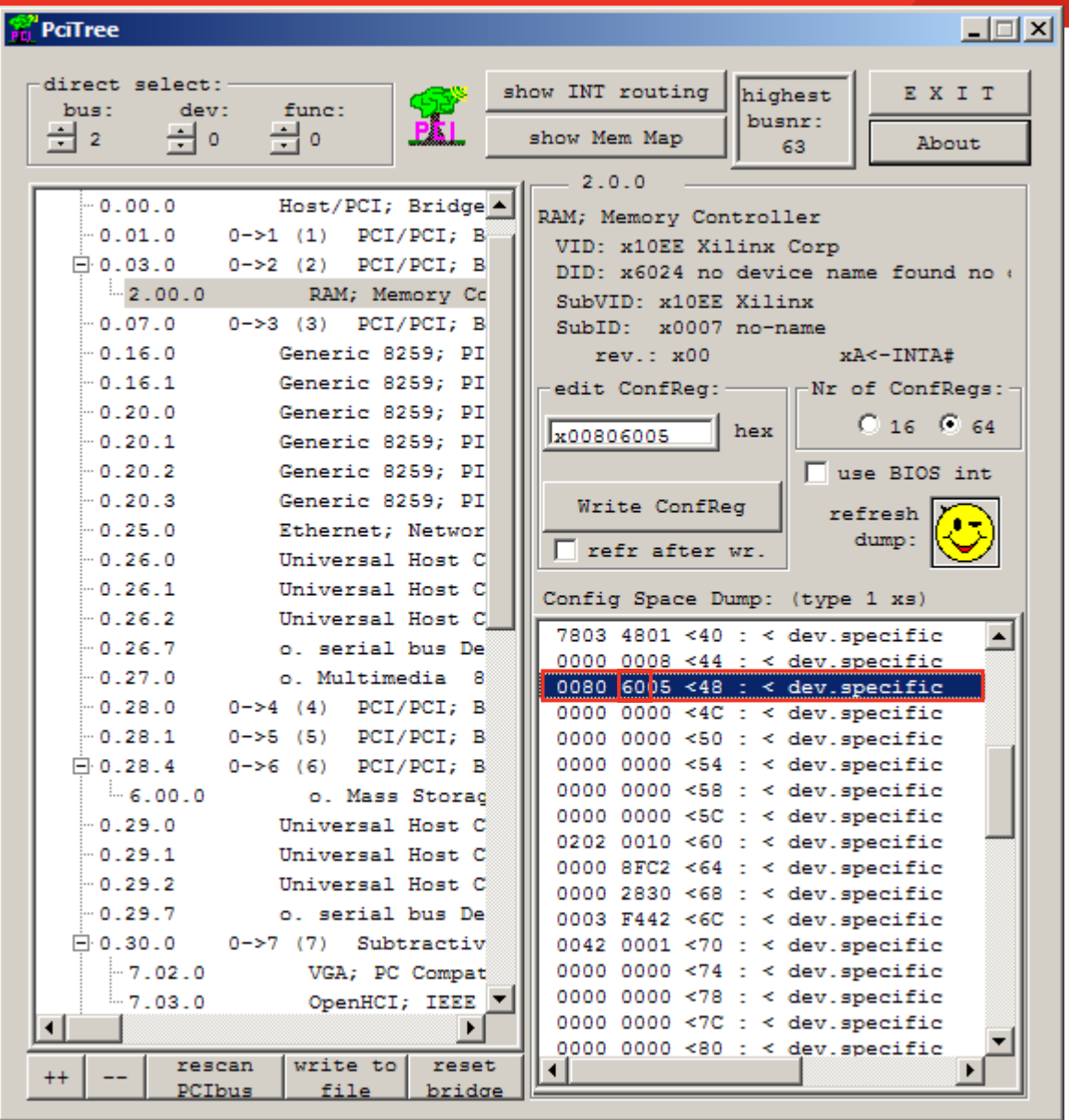
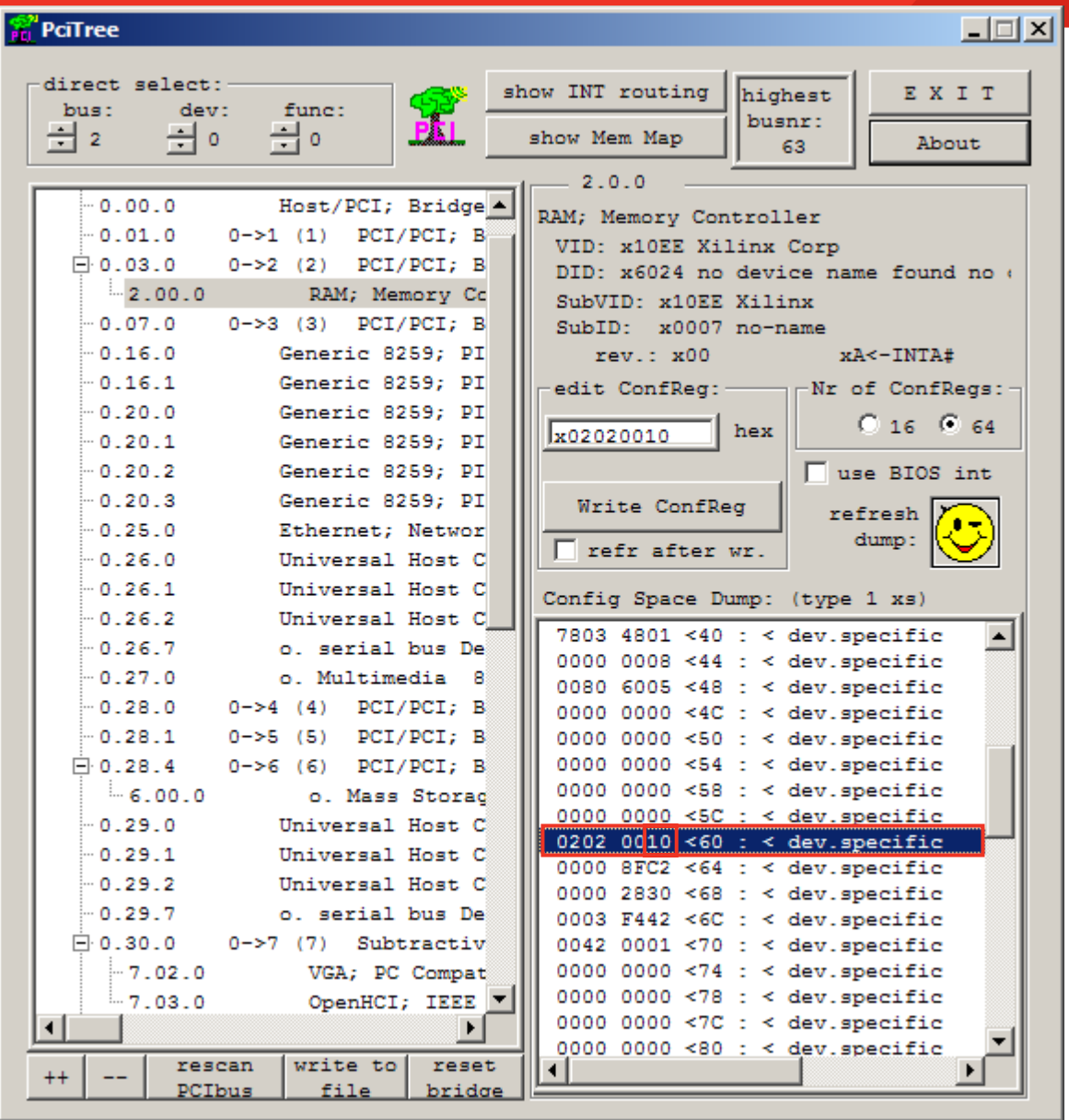
Running the PCIe x4 Gen2 Design



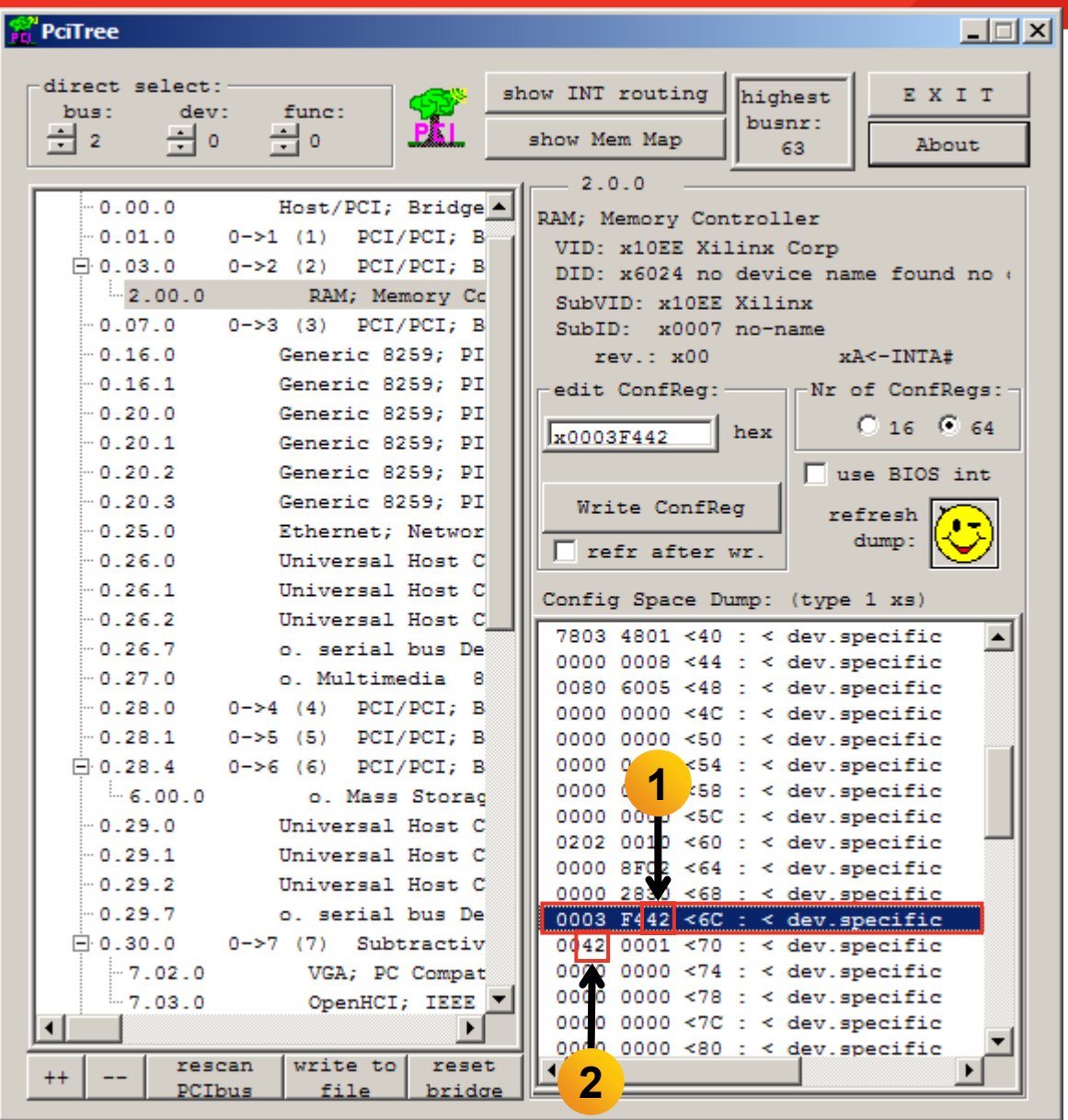
- **Select Register 0x48**
  - Register 0x48 points to the next structure
  - 0x60 is the address of the next structure

Running the PCIe x4 Gen2 Design



- **Register 0x60**
  - 0x60 is a type 0x10, indicating PCIe Capabilities Structure
  - Last Structure

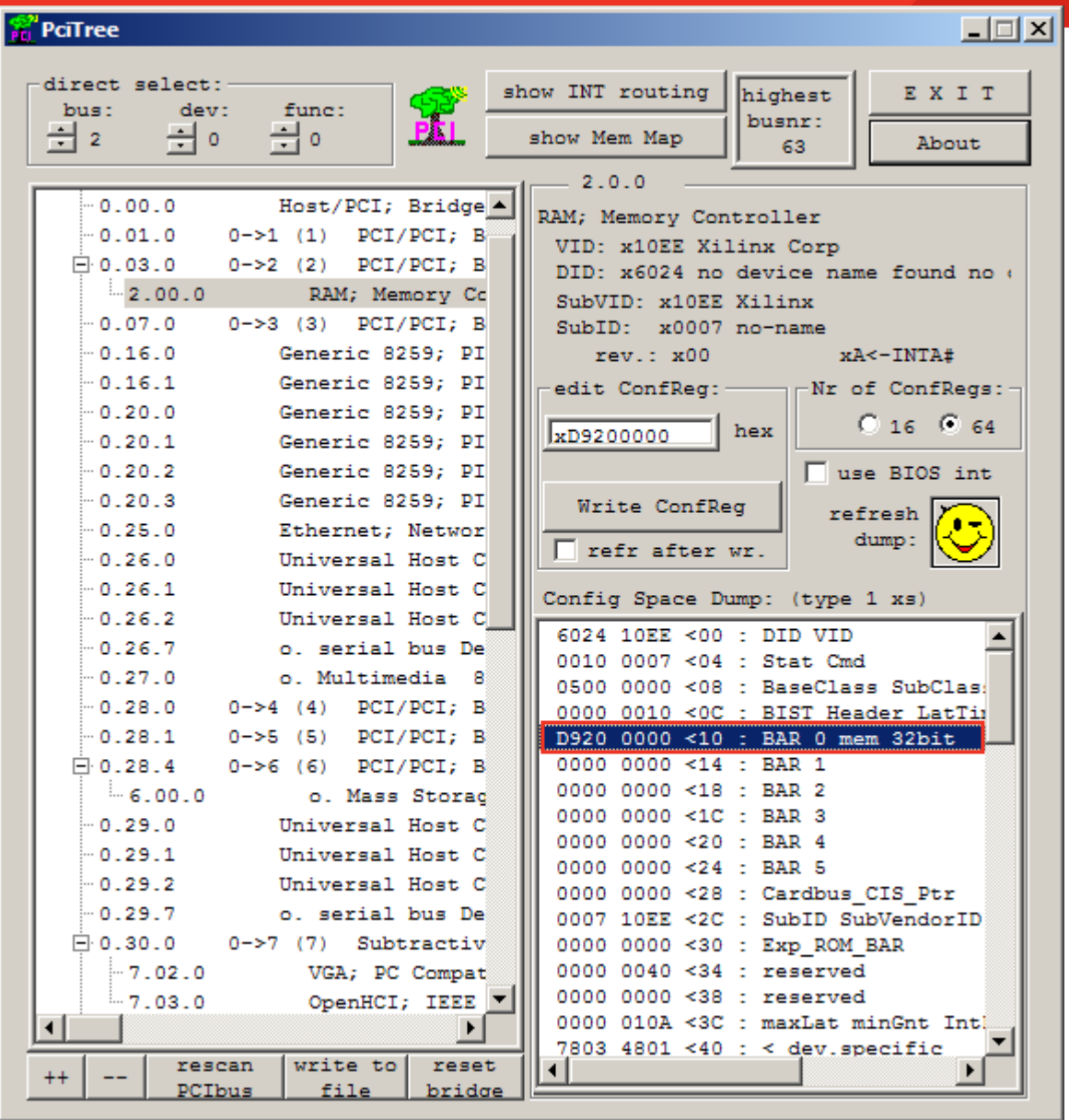
Running the PCIe x4 Gen2 Design



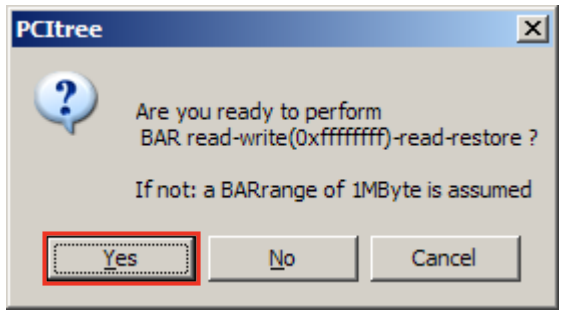
- **Register 0x6C**
  - Link Capabilities Register
  - Indicates the maximum number of lanes and speed (Gen1, Gen2) for device
  - The value 0x42 shows this is an x4 Gen2 device (1)
- **Link Status Register**
  - 0x70
  - Shows the current link status
  - This design, in a Gen2 chassis, trained to x4 Gen2 (2)

XILINX

Running the PCIe x4 Gen2 Design

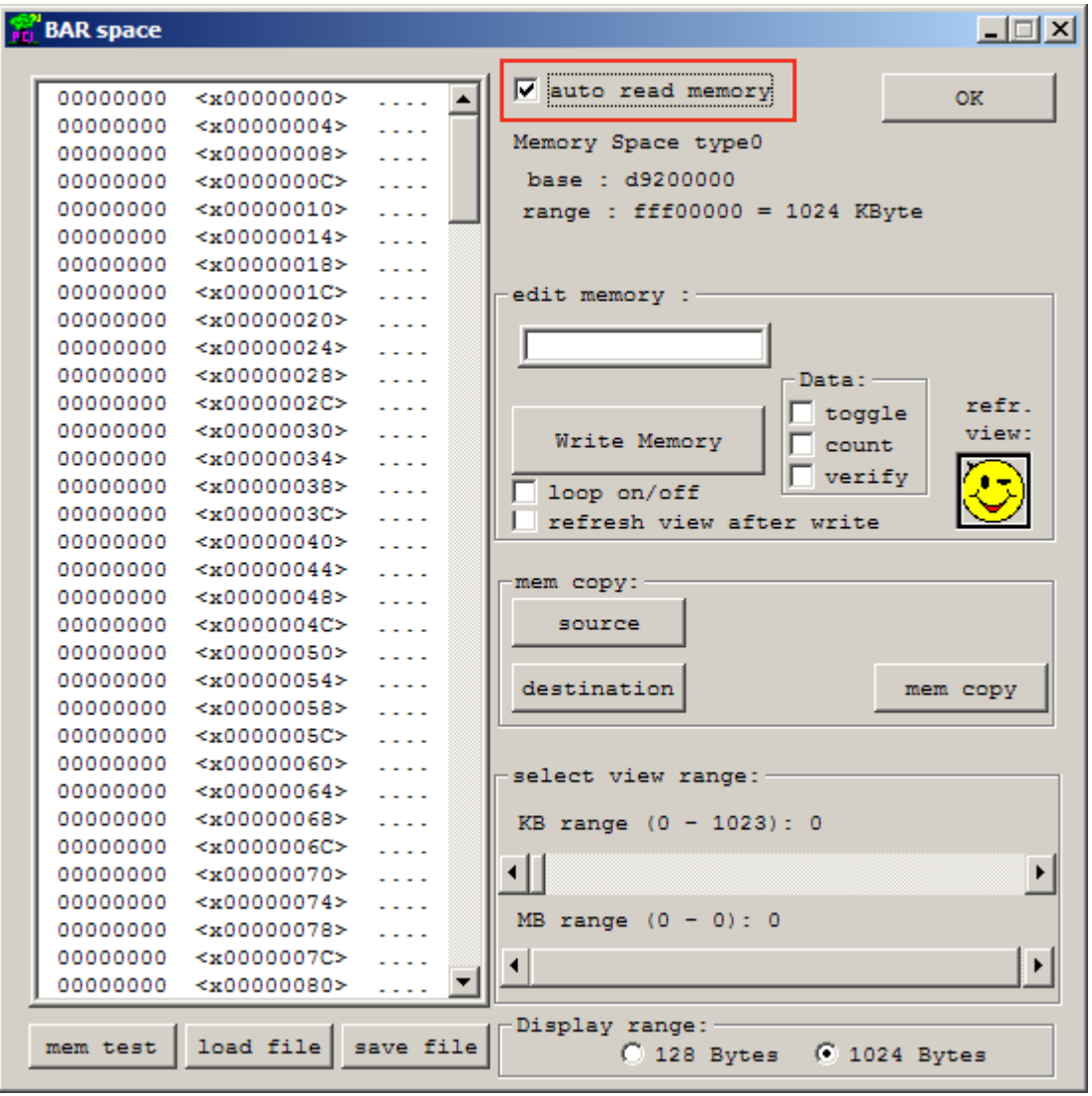


- **Double-click on BAR 0**
  - BAR 0 Address is machine dependent
- **Click Yes on the Dialog box seen below**



XILINX

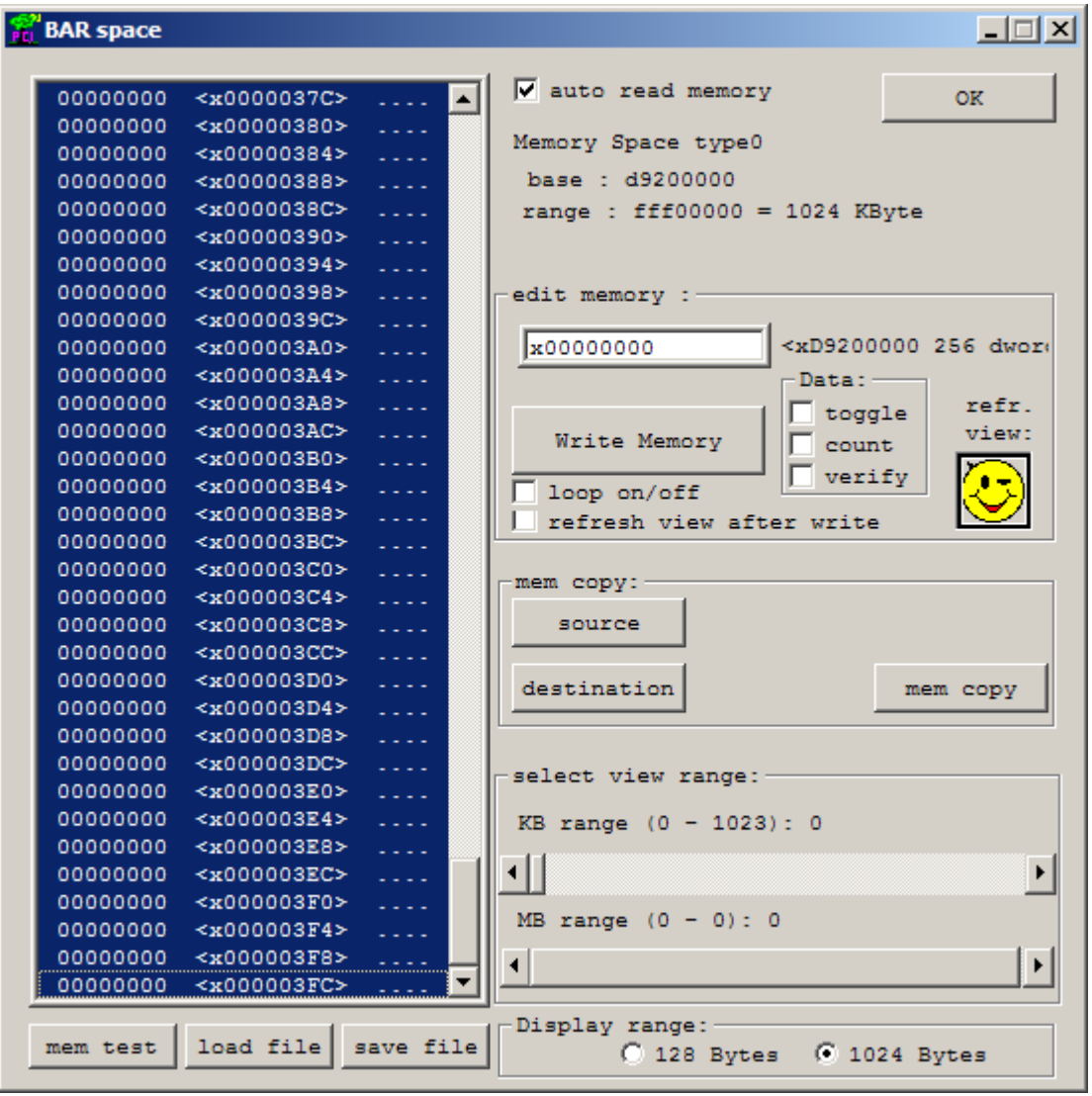
Running the PCIe x4 Gen2 Design



- Select auto read memory

Note: Presentation applies to the ML605

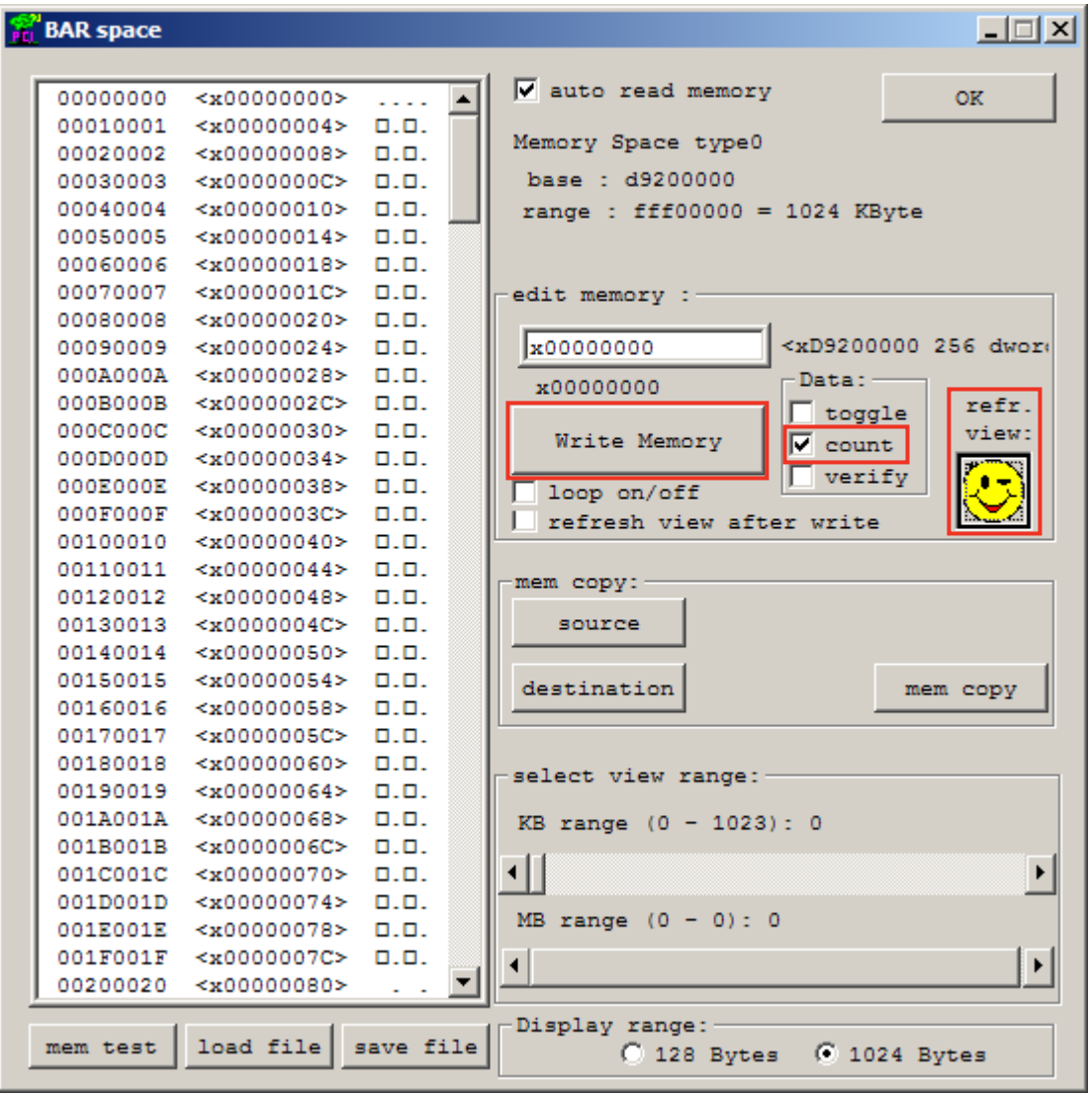
Running the PCIe x4 Gen2 Design



- **Click on the first memory location**
  - Type <Shift-End> to select 1024 Bytes

Note: Presentation applies to the ML605

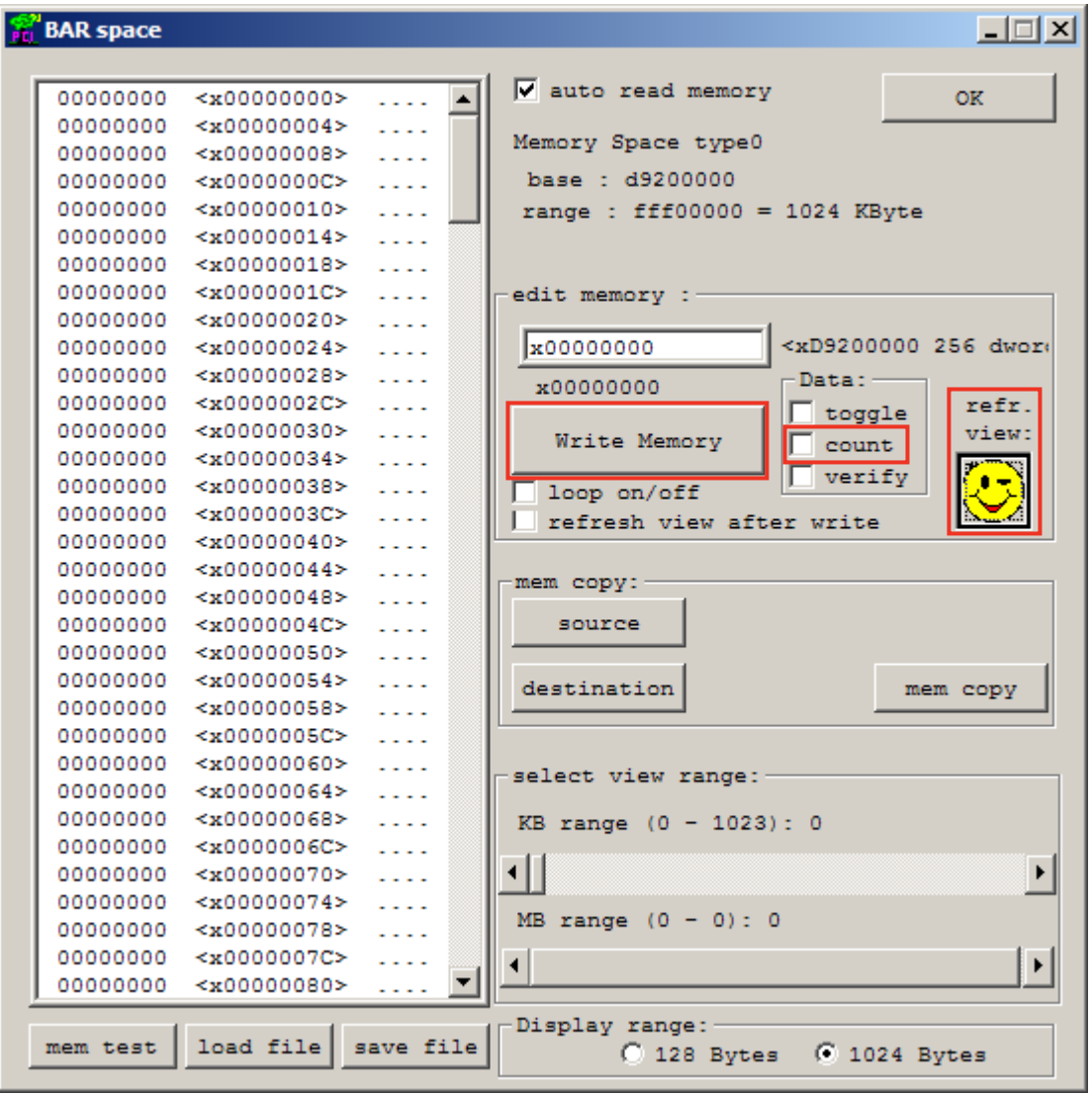
Running the PCIe x4 Gen2 Design



- **Write Memory**
  - Select count
  - Click Write Memory
  - Click refr view
- **View results – counting up to FF**

Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



- **Restore Memory**
  - Deselect count
  - Click Write Memory
  - Click refr view
- **Memory is reset to zeros**

Note: Presentation applies to the ML605

Virtex-6 PCIe x4 Gen2 Capability

- **ML605 Supports PCIe Gen1 and Gen2 Capability**
  - x4, x2, or x1 Gen2 lane width
  - x8 Gen2 not supported in -1 parts
- **LogiCORE PIO Example Design**
  - RDF0009.zip
- **LogiCORE Integrated Block for PCI Express**
  - See UG517 for details

Note: Presentation applies to the ML605

References

References

- **PCIe Base Specification**
  - PCI SIG Web Site

    http://www.pcisig.com/home
- **Virtex-6 PCIe**
  - PCIe Product Overview

    http://www.xilinx.com/products/ipcenter/V6_PCI_Express_Block.htm
  - Virtex-6 FPGA Integrated Block v1.3 for PCI Express User Guide

    http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ug517.pdf
  - Virtex-6 FPGA Integrated Block v1.3 for PCI Express Data Sheet

    http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ds715.pdf
  - IP Release Notes Guide

    http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

Documentation

Documentation

- **Virtex-6**
  - Virtex-6 FPGA Family
    http://www.xilinx.com/products/virtex6/index.htm
- **ML605 Documentation**
  - Virtex-6 FPGA ML605 Evaluation Kit
    http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm
  - ML605 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf
  - ML605 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf