

ML605 PCIe x4 Gen2 Design Creation

December 2009

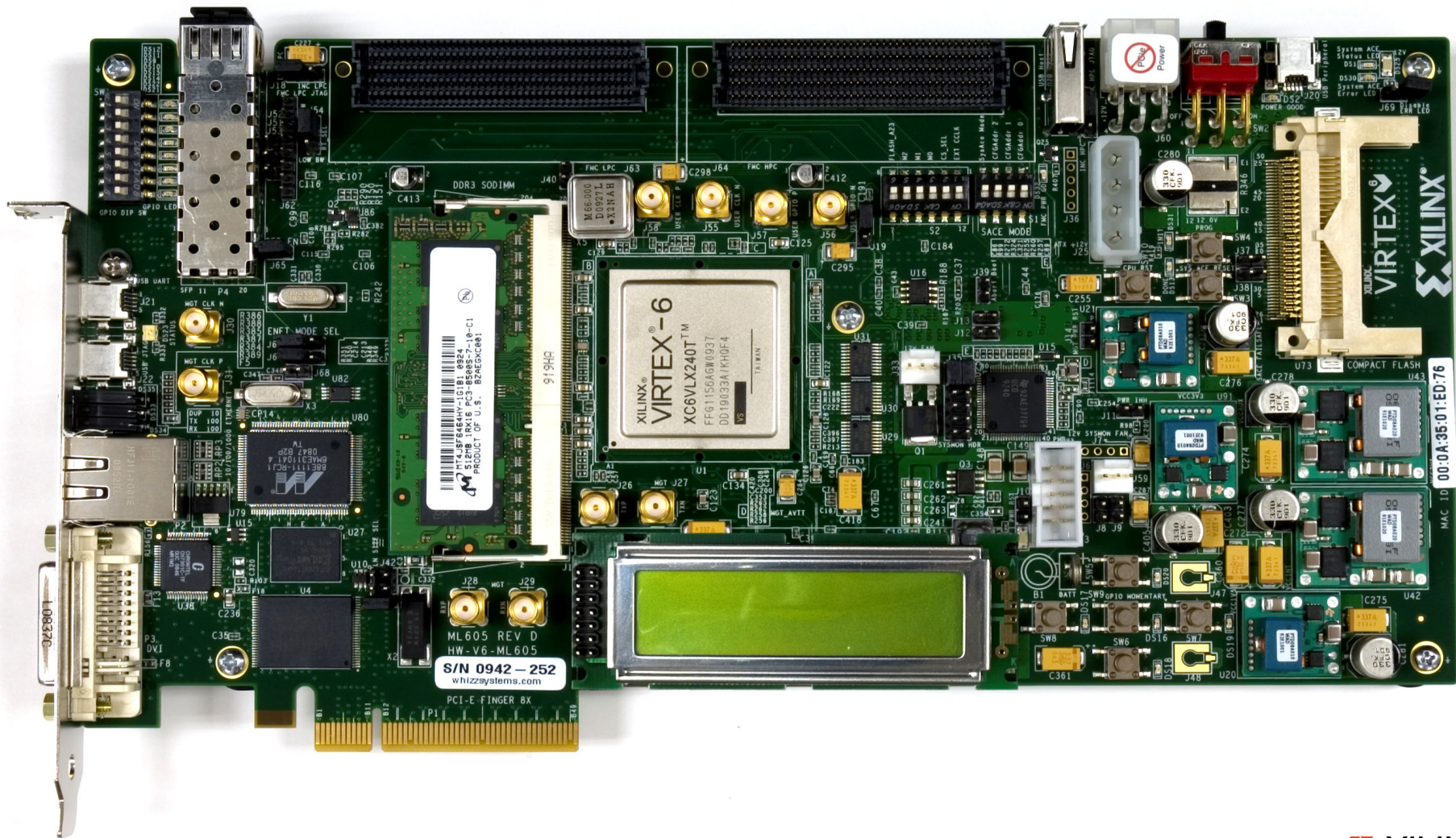
Overview

- **Virtex-6 PCIe x4 Gen2 Capability**
- **Xilinx ML605 Board**
- **Software Requirements**
- **Generate PCIe Core**
- **Compile PCIe Core**
- **Program Platform Flash with PCIe Design**
- **ML605 Setup**
- **Running the PCIe x4 Gen2 Design**
- **References**
 - IP Release Notes Guide [XTP025](#)

Virtex-6 PCIe x4 Gen2 Capability

- **Integrated Block for PCI Express**
 - PCI Express Base 2.0 Specification
- **Generation 2 (5 GT/s) data rates**
 - x4, x2, or x1 Gen2 lane width
 - x8 Gen2 not supported in -1 parts
- **Configurable for Endpoint or Root Port Applications**
 - ML605 configured for Endpoint Applications
- **GTX Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
 - 128 / 256 / 512 / 1024 bytes
- **Configurable BAR spaces**
 - Up to 6 x 32 bit, 3 x 64 bit, or a combination
 - Memory or IO
 - BAR and ID filtering
- **Management and Statistics Interface**

Xilinx ML605 Board



ISE Software Requirement

- Xilinx ISE 11.4 software



PciTree Software Requirement

■ PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory

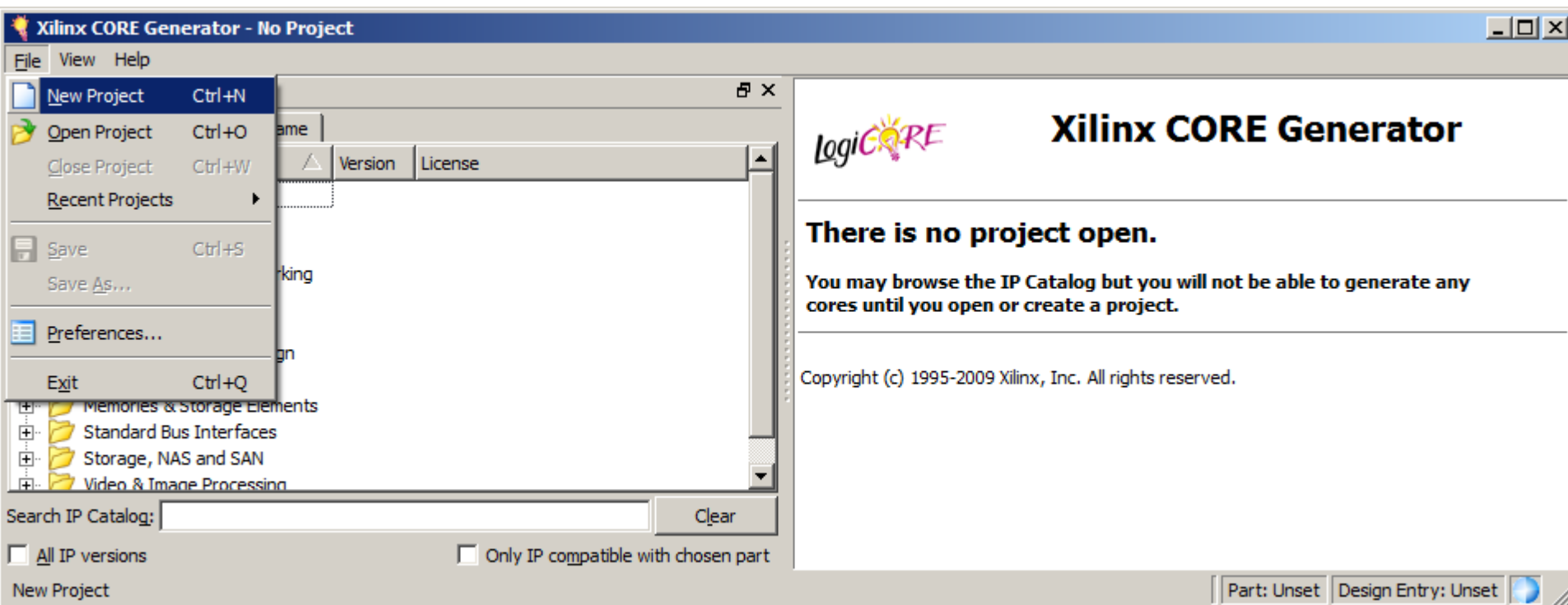


Generate PCIe Core

- **Open the CORE Generator**

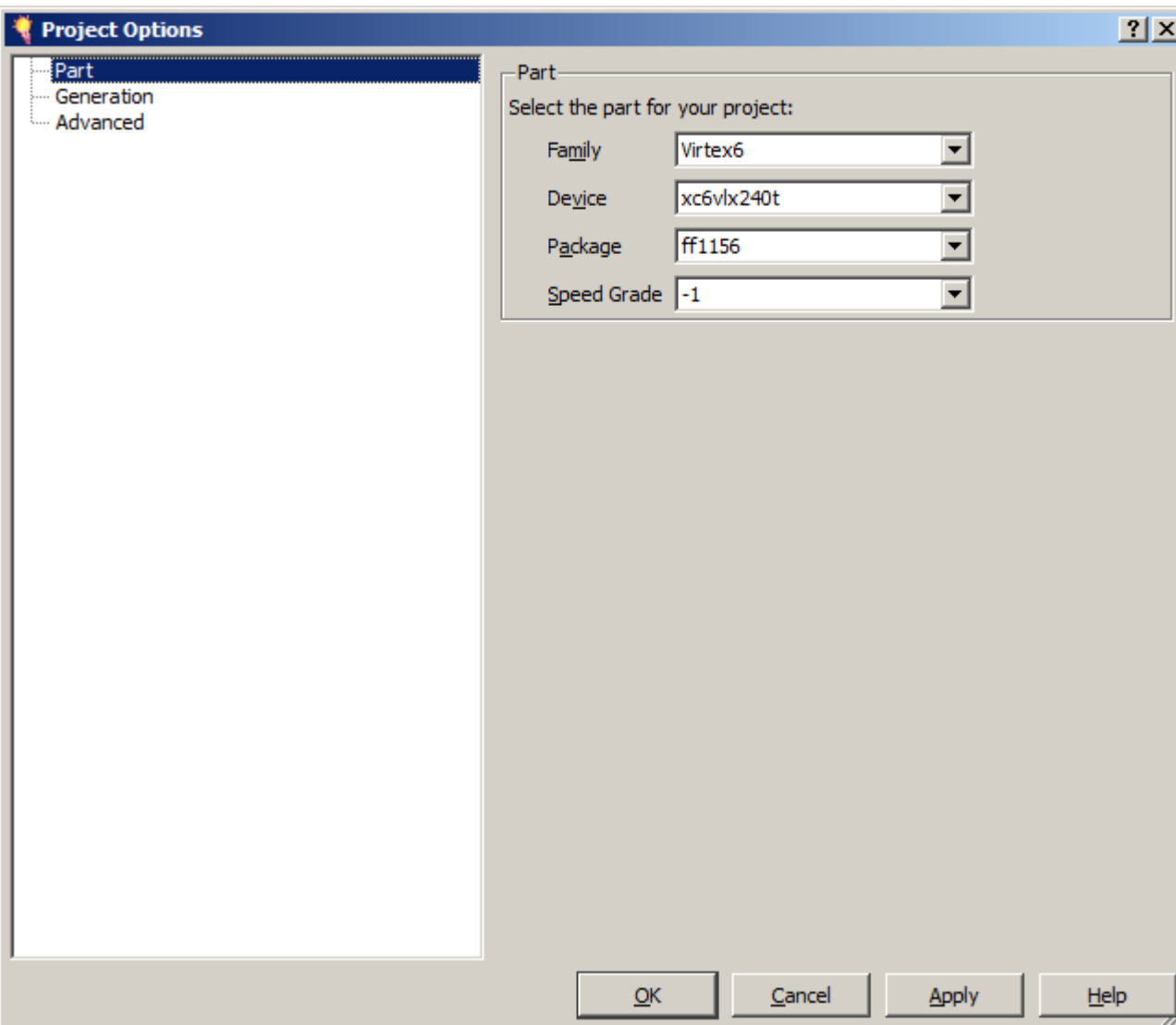
Start → All Programs → Xilinx ISE Design Suite 11 →
ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**



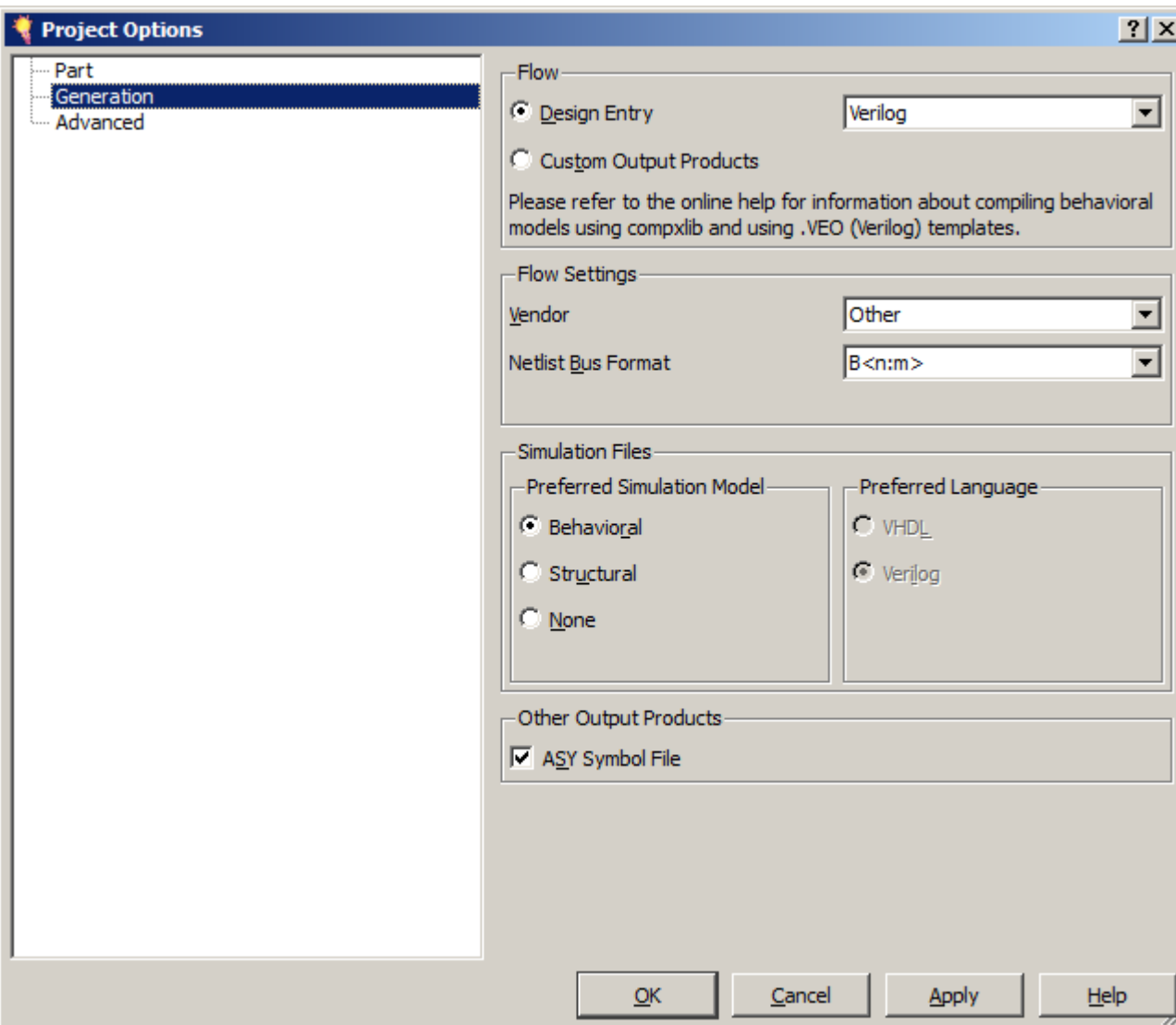
Note: Pre-built design: <https://secure.xilinx.com/webreg/clickthrough.do?cid=139967>

Generate PCIe Core



- Create a project directory:
`ml605_pcie_x4_gen2`
- Name the project:
`ml605_pcie_x4_gen2.cgp`
- The Project options will appear
- Set the Part (as seen here):
 - Family: Virtex6
 - Device: xc6vlx240t
 - Package: ff1156
 - Speed Grade: -1

Generate PCIe Core



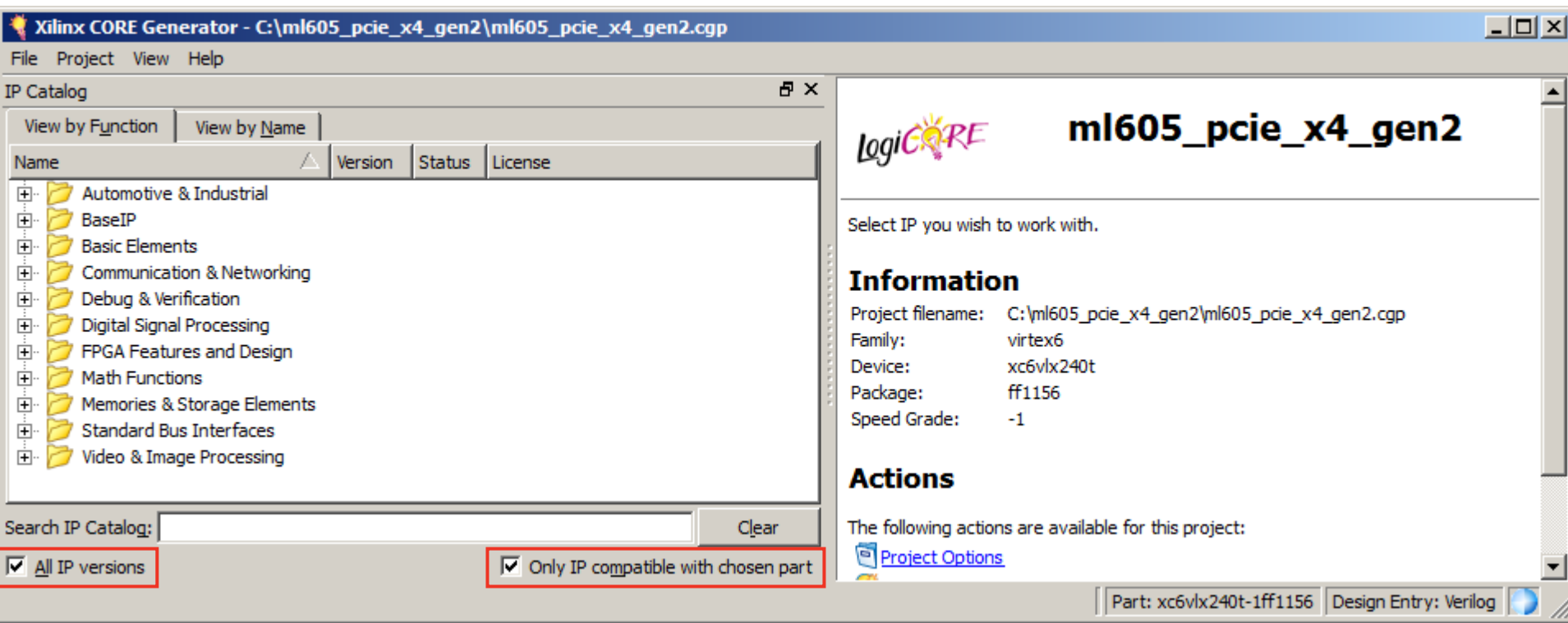
- Select Generation
- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the ML605

Generate PCIe Core

■ Select

- All IP versions
- Only IP compatible with chosen part



Generate PCIe Core

■ Select

- Virtex-6 Integrated Block for PCI Express, **Version 1.3**

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog on the left lists various IP blocks, with 'Virtex-6 Integrated Block for PCI Express' version 1.3 selected. The right pane displays the details for this core, including a warning that version 1.3 is superseded and will be removed in 12.1.

Xilinx CORE Generator - C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp

File Project View Help

IP Catalog

View by Function View by Name

Name	Version	Status	License
Digital Signal Processing			
FPGA Features and Design			
Math Functions			
Memories & Storage Elements			
Standard Bus Interfaces			
PCI Express			
Virtex-6 Integrated Block for PCI Express	1.1	Superseded	
Virtex-6 Integrated Block for PCI Express	1.2	Superseded	
Virtex-6 Integrated Block for PCI Express	1.3	Superseded	
Virtex-6 Integrated Block for PCI Express	1.4		
RapidIO			
Video & Image Processing			

Search IP Catalog: [] Clear

☒ All IP versions ☒ Only IP compatible with chosen part

LogiCORE **Virtex-6 Integrated Block for PCI Express** [Show Project](#)

This core is supported by your chosen part.

Information

Core type: Virtex-6 Integrated Block for PCI Express

Version: 1.3. **You are using Virtex-6 Integrated Block for PCI Express 1.3 which has been replaced with a new version. This version of the core will be removed in 12.1. Cores in this state are not supported.**

Core Summary: The Xilinx Virtex-6 Integrated Block for PCI Express (1-lane, 2-lane, 4-lane, and 8-lane) uses the Virtex(TM)-6 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-6 architectural features to implement a PCI Express Base Specification v2.0 compliant PCI Express

Part: xc6vlx240t-1ff1156 Design Entry: Verilog

Note: Version 1.3 is required for XC6VLX240T-1CES FPGAs with PCIe x4 Gen 2

Generate PCIe Core

- Right click on the Virtex-6 Integrated Block for PCI Express, Version 1.3
 - Select Customize

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog on the left lists various IP blocks, with 'Virtex-6 Integrated Block for PCI Express' selected. A right-click context menu is open over the selected item, showing options like 'Customize', 'View Data Sheet', 'View License Status', 'View Product Webpage', 'View Version Information', and 'View Answer Records'. The 'Customize' option is highlighted. The main panel on the right displays the details for the 'Virtex-6 Integrated Block for PCI Express'. It includes a 'Show Project' button, a status message, and an 'Information' section with details about the core type, version, and summary.

Xilinx CORE Generator - C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp

File Project View Help

IP Catalog

View by Function View by Name

Name	Version	Status	License
Digital Signal Processing			
FPGA Features and Design			
Math Functions			
Memories & Storage Elements			
Standard Bus Interfaces			
PCI Express			
Virtex-6 Integrated Block for PCI Express	1.1	Superseded	
Virtex-6 Integrated Block for PCI Express			
Virtex-6 Integrated Block for PCI Express			
Virtex-6 Integrated Block for PCI Express			
RapidIO			
Video & Image Processing			

Search IP Catalog:

☒ All IP versions

LogiCORE **Virtex-6 Integrated Block for PCI Express** [Show Project](#)

This core is supported by your chosen part.

Information

Core type: Virtex-6 Integrated Block for PCI Express

Version: 1.3. **You are using Virtex-6 Integrated Block for PCI Express 1.3 which has been replaced with a new version. This version of the core will be removed in 12.1. Cores in this state are not supported.**

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Part: xc6vlx240t-1ff1156 Design Entry: Verilog

Generate PCIe Core

Virtex-6 Integrated Block for PCI Express

logiCORE **Virtex-6 Integrated Block for PCI Express** 1.3

Component Name

PCIe Device / Port Type

The Integrated Block for PCI Express allows selection of the Device / Port Type

Device / Port Type

Number of Lanes

The Integrated Block for PCI Express requires that an initial lane width be selected. Wider lane width cores can train down to smaller lane widths if attached to a smaller lane width device. Select only the lane width that is necessary for the design.

Lane Width

Link Speed

The Integrated Block for PCI Express allows selection of the Maximum Link Speed supported by the device.

☐ 2.5 GT/s

☒ 5.0 GT/s

Interface Frequency

The Integrated Block for PCI Express allows selection of the interface clock (trn_clk) frequency. The frequency selection enables maximum achievable data throughput for the selected number of lanes and link speed. Choice of non-default option results in interface being overclocked with no overall effect on data throughput, and depends on user application functional requirements, timing closure and power considerations. Xilinx recommends that the default frequency value be used where possible..

Frequency (MHz)

[Datasheet](#) [< Back](#) Page 1 of 11 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

- Set the lane Width to X4
- Set the Link Speed to 5.0 GT/s
- Click Next

Generate PCIe Core

Virtex-6 Integrated Block for PCI Express

logiCORE Virtex-6 Integrated Block for PCI Express 1.3

Base Address Registers

Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses to assign to the device, the Base Address Registers are programmed with addresses and the device uses this information to perform address decoding.

BAR 0 Options

☒ Bar0 Type: Memory ☐ 64 bit ☐ Prefetchable
Size: 1 Megabytes
Value: FFF00000 (Hex)

BAR 1 Options

☐ Bar1 Type: N/A ☐ 64 bit ☐ Prefetchable
Size: 2 Kilobytes
Value: 00000000 (Hex)

BAR 2 Options

☐ Bar2 Type: N/A ☐ 64 bit ☐ Prefetchable
Size: 128 Bytes
Value: 00000000 (Hex)

BAR 3 Options

☐ Bar3 Type: N/A ☐ 64 bit ☐ Prefetchable
Size: 2 Kilobytes
Value: 00000000 (Hex)

BAR 4 Options

☐ Bar4 Type: N/A ☐ 64 bit ☐ Prefetchable
Size: 2 Kilobytes
Value: 00000000 (Hex)

BAR 5 Options

☐ Bar5 Type: N/A ☐ Prefetchable
Size: 2 Kilobytes
Value: 00000000 (Hex)

Expansion ROM Base Address Register

☐ Expansion Rom Size: 2 Kilobytes
Value: 00000000 (Hex)

[Datasheet](#) [< Back](#) Page 2 of 11 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

- **BAR 0**
 - Set to 1 Megabytes
- **BAR 2**
 - Deselect BAR 2
- **Click Next**

Generate PCIe Core

Virtex-6 Integrated Block for PCI Express

LogiCORE Virtex-6 Integrated Block for PCI Express 1.3

ID Initial Values

Vendor ID	10EE	Range: 0000..FFFF
Device ID	6024	Range: 0000..FFFF
Revision ID	00	Range: 00..FF
Subsystem Vendor ID	10EE	Range: 0000..FFFF
Subsystem ID	0007	Range: 0000..FFFF

Class Code

Base Class	05	Range: 00..FF
Sub-Class	00	Range: 00..FF
Interface	00	Range: 00..FF
Class Code	050000	(Hex)

Class Code Lookup Assistant

Must enter values above.

Base Class	Simple communication controllers
Base Class	07h
Sub-Class/Interface Value	Generic XT compatible serial controller
Sub-Class	00h
Interface	00h

Cardbus CIS Pointer

Cardbus CIS Pointer	00000000	Range: 00000000..FFFFFFFF
---------------------	----------	---------------------------


Datasheet < Back Page 3 of 11 Next > Generate Cancel Help

■ Note ID Initial Values

- Vendor ID = **10EE**
- Device ID = **6024**
- Revision ID = **00**
- Subsystem Vendor ID = **10EE**
- Subsystem ID = **0007**

■ Click Next 6 times

Generate PCIe Core

 **Virtex-6 Integrated Block for PCI Express** 1.3

Pinout Selection

Xilinx Development Boards

Generate Xilinx Development Board specific UCF

Xilinx Development Board **ML 605**

PCIe Block Location Selection

Selects from available PCIe Block locations for a part-package combination which determines Pinout.

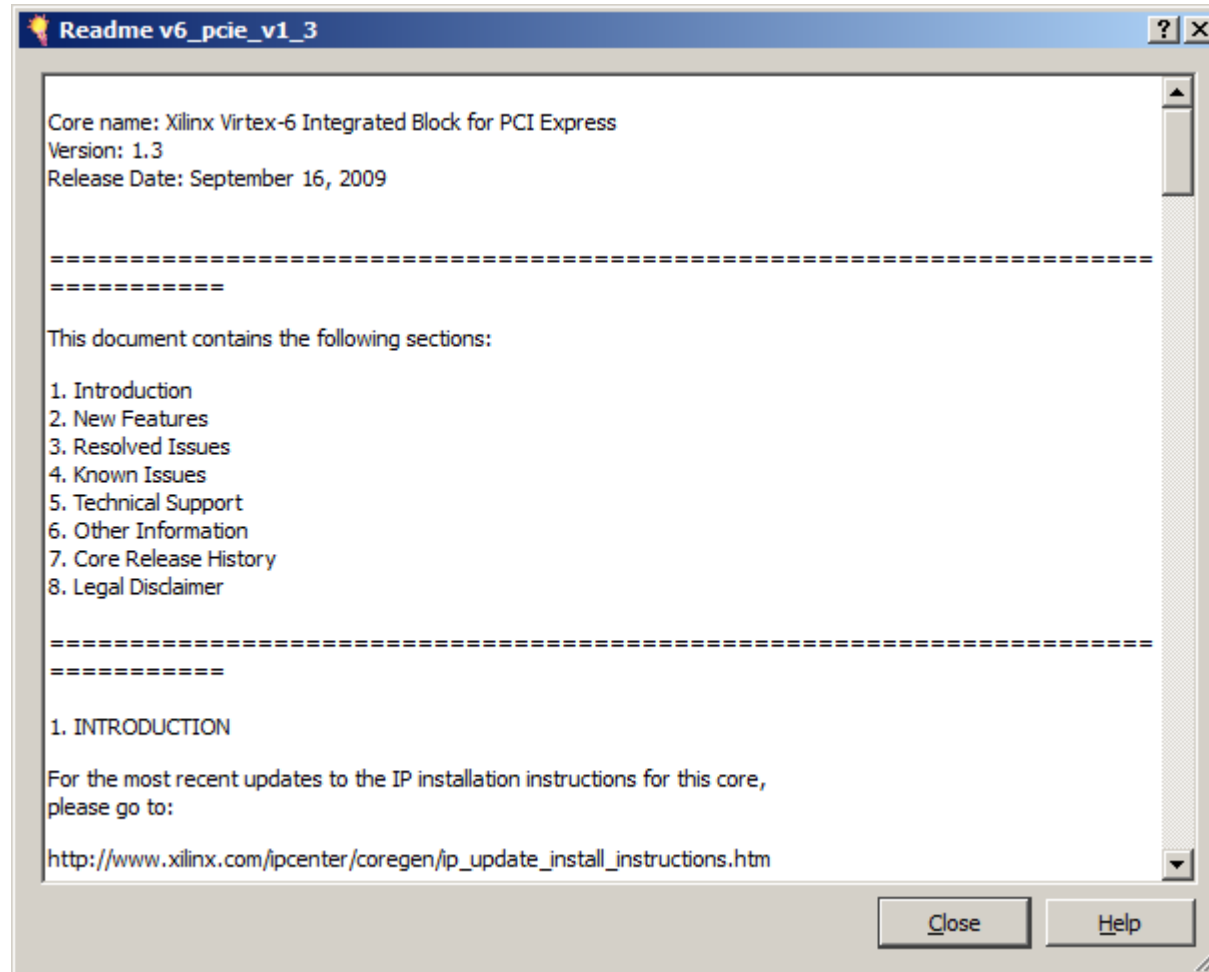
PCIe Block Location **X0Y0**

[Datasheet](#) [< Back](#) Page 9 of 11 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

- On Page 9
 - Select ML605
- Click Generate

Generate PCIe Core

- After the PCIe core finishes generating, click OK on the Readme File window



Generate PCIe Core

- The v6_pcie_v1_3 IP appears under the Project IP tab

The screenshot shows the Xilinx CORE Generator window titled "Xilinx CORE Generator - C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp". The "Project IP" tab is active, displaying a table of available IP cores. The table has four columns: "Component Name", "Core Name", "Version", and "Last Modified". One IP core is listed: "v6_pcie_v1_3" with the core name "Virtex-6 Integrated Block for PCI Express", version "1.3", and last modified date "2009-12-17 at 06:45". Below the table is a "Search Project IP:" text box and a "Clear" button. At the bottom left are "Project IP" and "IP Catalog" buttons. The right pane shows the "LogiCORE" logo and the core name "ml605_pcie_x4_gen2". It includes a "Select IP you wish to work with." instruction, an "Information" section with project details (filename, family, device, package, speed grade), and an "Actions" section. The status bar at the bottom right shows "Part: xc6vlx240t-1ff1156" and "Design Entry: Verilog".

Component Name	Core Name	Version	Last Modified
v6_pcie_v1_3	Virtex-6 Integrated Block for PCI Express	1.3	2009-12-17 at 06:45

Search Project IP: Clear

Project IP IP Catalog

LogiCORE ml605_pcie_x4_gen2

Select IP you wish to work with.

Information

Project filename: C:\ml605_pcie_x4_gen2\ml605_pcie_x4_gen2.cgp
Family: virtex6
Device: xc6vlx240t
Package: ff1156
Speed Grade: -1

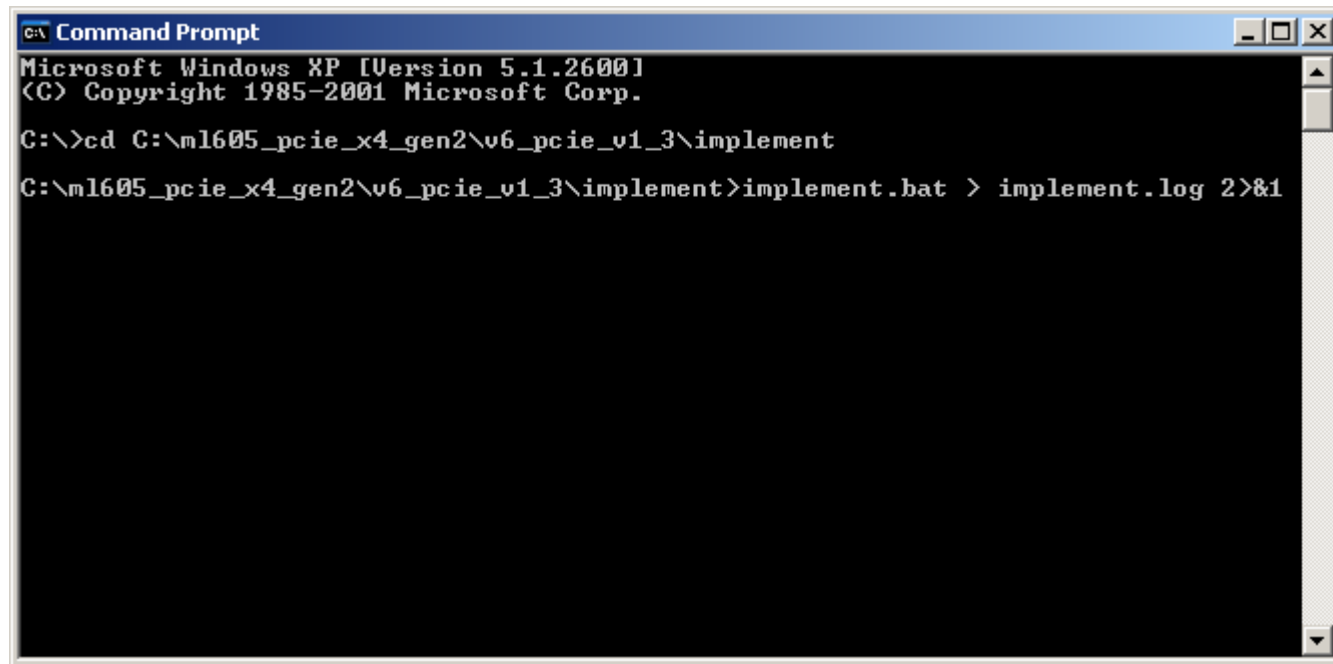
Actions

Part: xc6vlx240t-1ff1156 Design Entry: Verilog

Compile PCIe Core

- Type these commands in a windows command shell:

```
cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement  
implement.bat > implement.log 2>&1
```

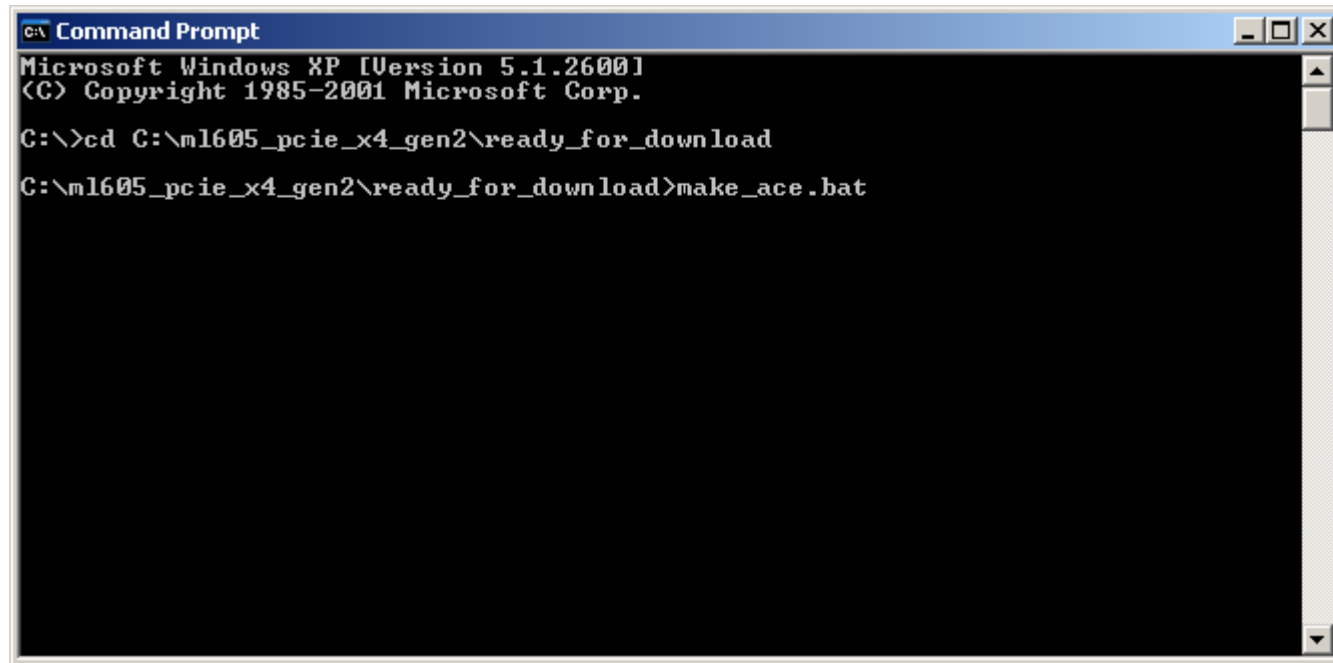


```
C:\> Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement  
C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement>implement.bat > implement.log 2>&1
```

Create PCIe ACE File (Optional)

- Type these commands in a windows command shell:

```
cd C:\ml605_pcie_x4_gen2\ready_for_download  
make_ace.bat
```



The screenshot shows a Windows Command Prompt window titled "C:\ Command Prompt". The window displays the following text:

```
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd C:\ml605_pcie_x4_gen2\ready_for_download  
C:\ml605_pcie_x4_gen2\ready_for_download>make_ace.bat
```

Note: The make_ace.bat file is included with [RDF0009](#)

Program Platform Flash with PCIe Design

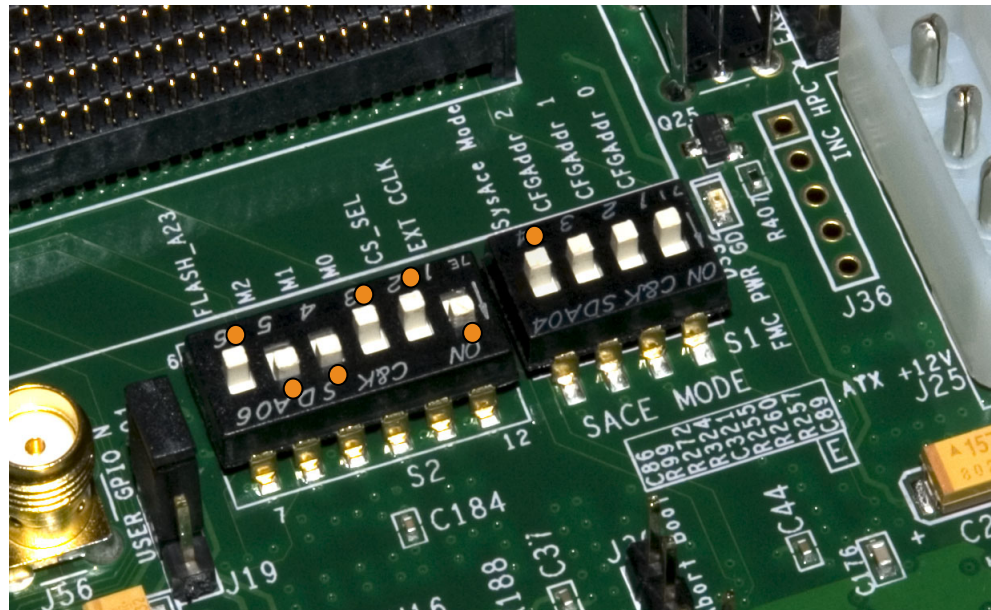
- Power on the ML605
- Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board
 - Connect this cable to your PC



Note: Presentation applies to the ML605

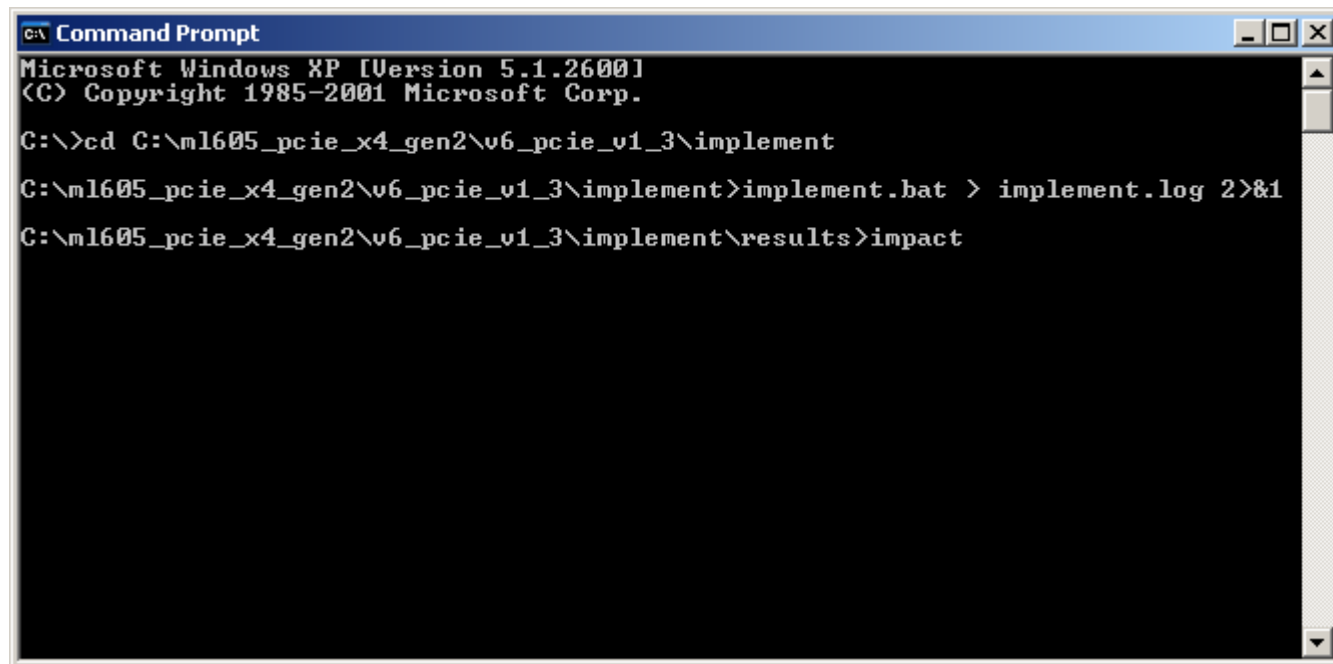
Program Platform Flash with PCIe Design

- **Set S2 to 011001 (1 = on, Position 6 → Position 1)**
 - This selects Slave SelectMAP (Positions 5, 4, and 3), Platform Flash (2) and EXT CCLK (1, for PCIe compliance)
- **Set S1 to 0XXX (X = Don't care, Position 4 → Position 1)**
 - This disables the Compact Flash



Program Platform Flash with PCIe Design

- Run iMPACT:
impact



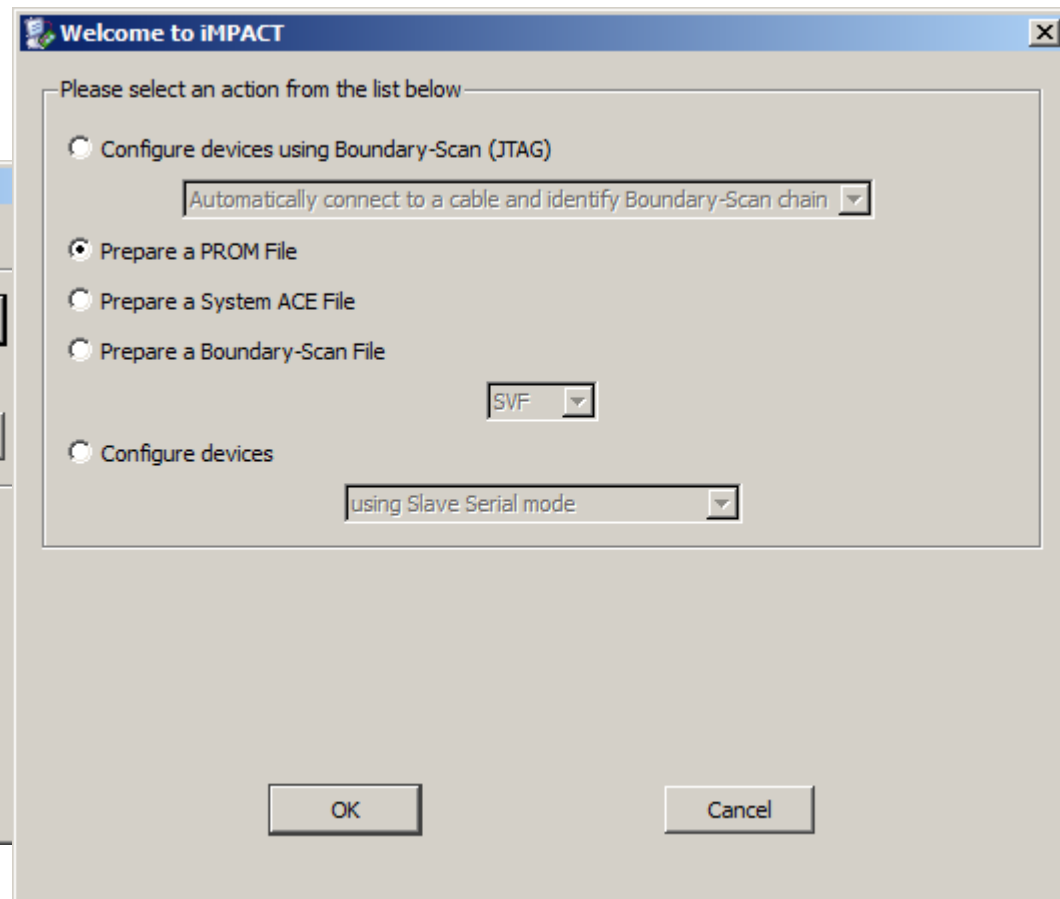
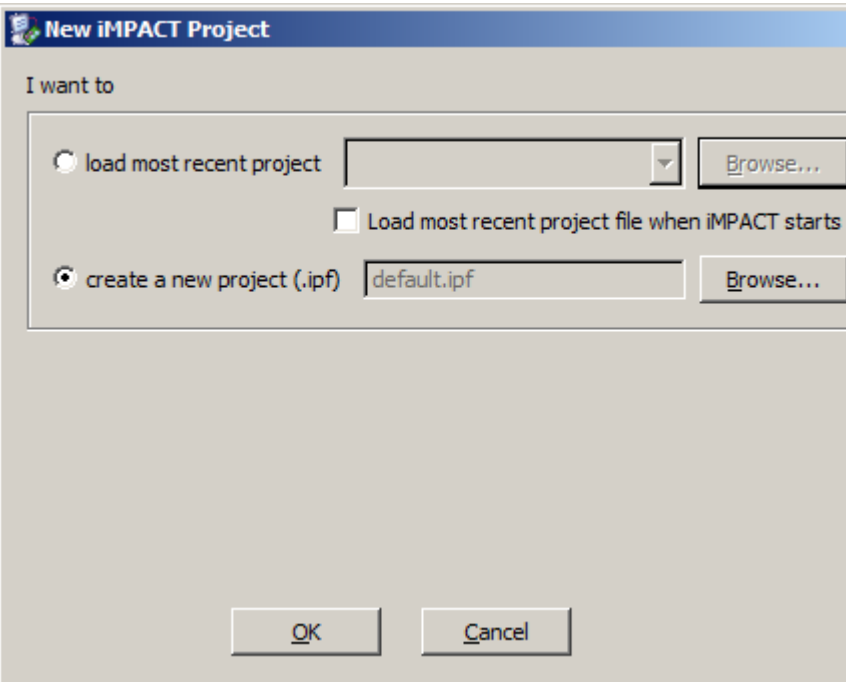
```
Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement
C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement>implement.bat > implement.log 2>&1
C:\ml605_pcie_x4_gen2\v6_pcie_v1_3\implement\results>impact
```

Program Platform Flash with PCIe Design

■ Select

- Create a new project
- Prepare a PROM File



Program Platform Flash with PCIe Design

- To generate a PROM file for the XCF128X Platform Flash, select:
 - BPI – Configure Single FPGA

The screenshot shows the PROM File Formatter application window. It is divided into three main steps:

- Step 1. Select Storage Target:** A tree view under "Storage Device Type:" shows the following options:
 - Xilinx Flash/PROM
 - Non-Volatile FPGA
 - Spartan3AN
 - SPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - BPI Flash
 - Configure Single FPGA** (highlighted with a red box)
 - Configure MultiBoot FPGA
 - Configure from Paralleled PROMs
 - Generic Parallel PROMA green arrow button is located to the right of the BPI Flash section.
- Step 2. Add Storage Device(s):** This section contains two dropdown menus: "Target FPGA" (set to "Spartan3E") and "Storage Device (bits):" (set to "512K"). Below these are "Add Storage Device" and "Remove Storage Device" buttons. A large empty box is at the bottom.
- Step 3. Enter Data:** This section contains two tables.

General File Detail	
	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	_x4_gen2\ready_for_download/

Flash/PROM File Property	
	Value
File Format	HEX
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

Program Platform Flash with PCIe Design

- Add xcf128x

PROM File Formatter

Step 1. Select Storage Target

Storage Device Type :

- Xilinx Flash/PROM
 - Non-Volatile FPGA
 - Spartan3AN
 - SPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - BPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - Configure from Paralleled PROMs
 - Generic Parallel PROM

➔

Step 2. Add Storage Device(s)

Target FPGA: Virtex6

Storage Device (Bytes): xcf128x [16M]

Add Storage Device Remove Storage Device

xcf128x [16M]

➔

Step 3. Enter Data

General File Detail	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	_x4_gen2\ready_for_download/

Flash/PROM File Property	Value
File Format	HEX
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

Note: Presentation applies to the ML605

Program Platform Flash with PCIe Design

- Set file name and location as desired and click OK

PROM File Formatter

Step 1. Select Storage Target

Storage Device Type :

- Xilinx Flash/PROM
 - Non-Volatile FPGA
 - Spartan3AN
 - SPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - BPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - Configure from Paralleled PROMs
 - Generic Parallel PROM

Step 2. Add Storage Device(s)


Target FPGA: Virtex6

Storage Device (Bytes): xcf128x [16M]

Add Storage Device Remove Storage Device

xcf128x [16M]

Step 3. Enter Data

General File Detail	Value
Checksum Fill Value	FF
Output File Name	ml605_pcie_x4_gen2
Output File Location	_x4_gen2\ready_for_download\ 

Flash/PROM File Property	Value
File Format	MCS
Add Non-Configuration Data Files	No

Description:

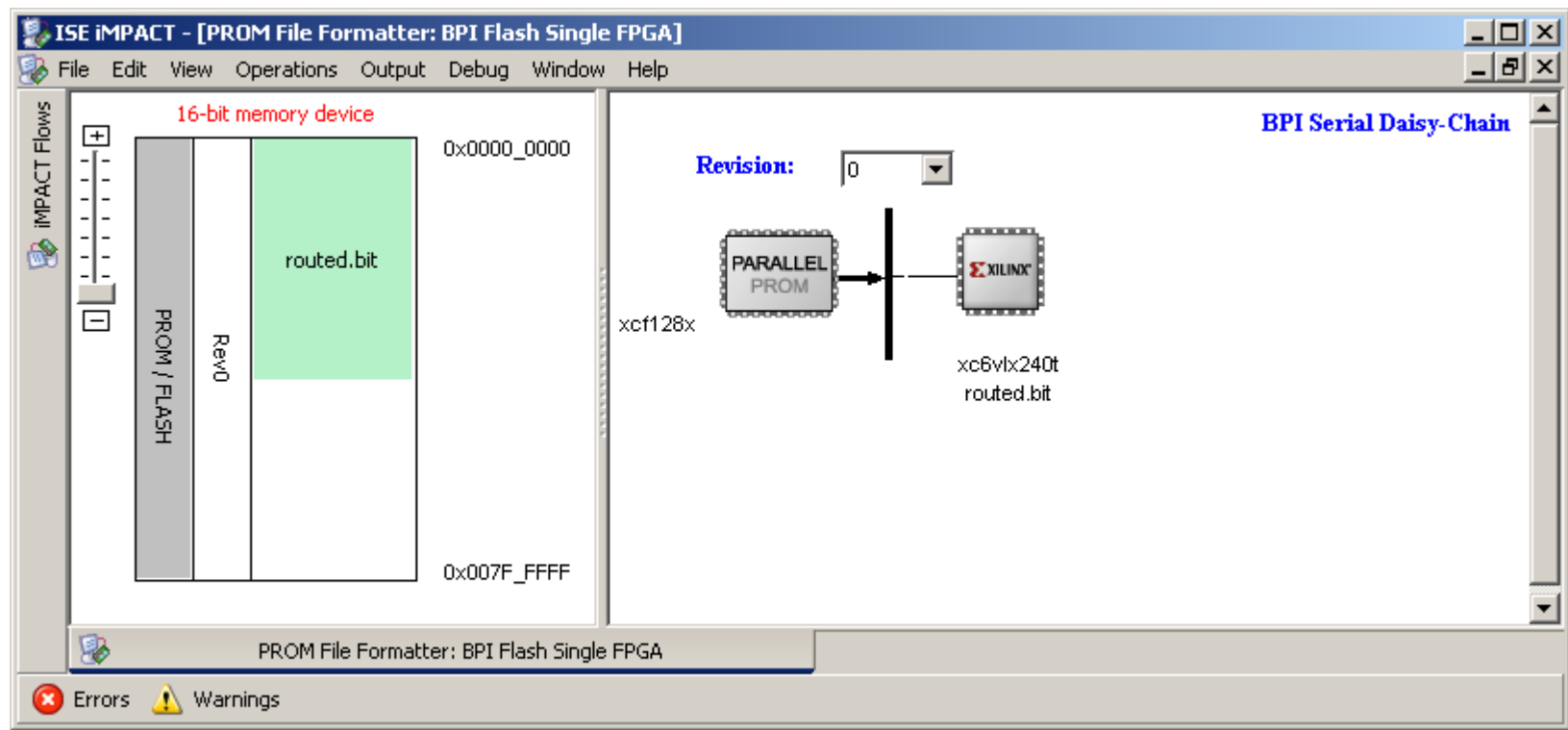
In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.

- Checksum Fill Value:** When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
- Output File Name:** This allows you to specify the base name of the file to which your PROM data will be written
- Output File Location:** This allows you to specify the directory in which the file named above will be created
- File Format:** PROM files can be generated in any number of industry standard formats. Depending on the PROM file format your PROM programmer uses, you output a .TEK

OK Cancel Help

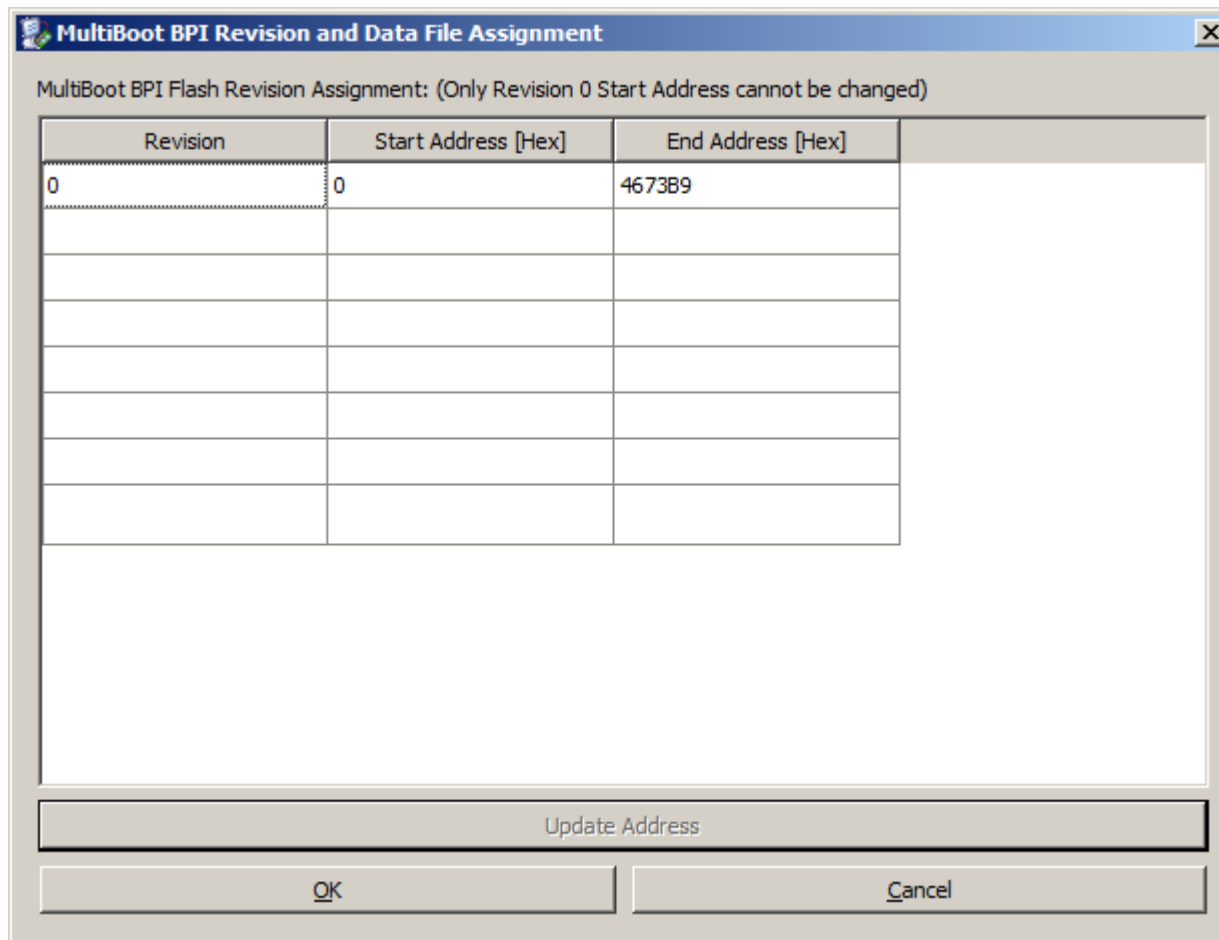
Program Platform Flash with PCIe Design

- Add routed.bit from the <design path>\v6_pcie_v1_3\implement\results



Program Platform Flash with PCIe Design

- Click OK on this dialog



MultiBoot BPI Revision and Data File Assignment

MultiBoot BPI Flash Revision Assignment: (Only Revision 0 Start Address cannot be changed)

Revision	Start Address [Hex]	End Address [Hex]
0	0	4673B9

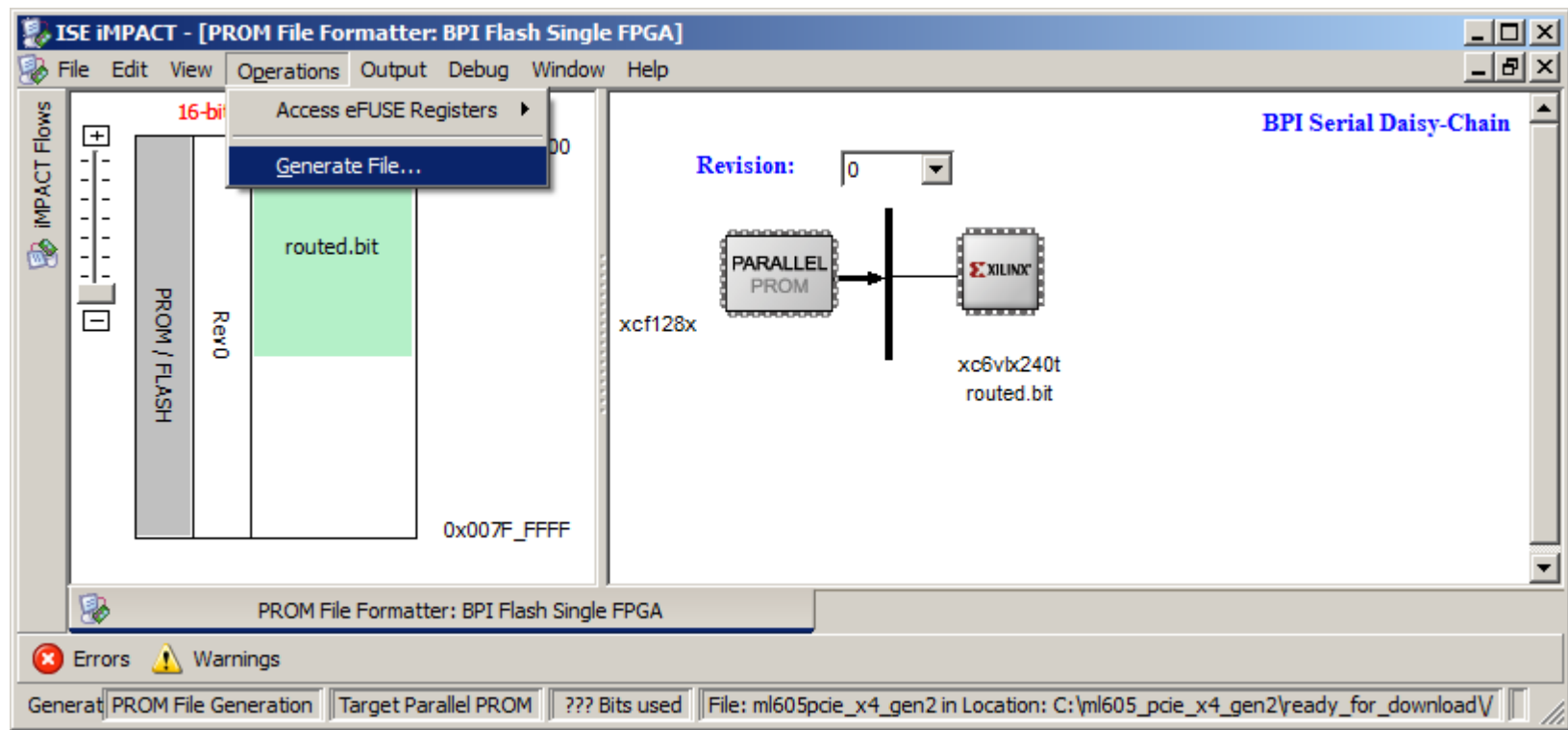
Update Address

OK Cancel

Note: Presentation applies to the ML605

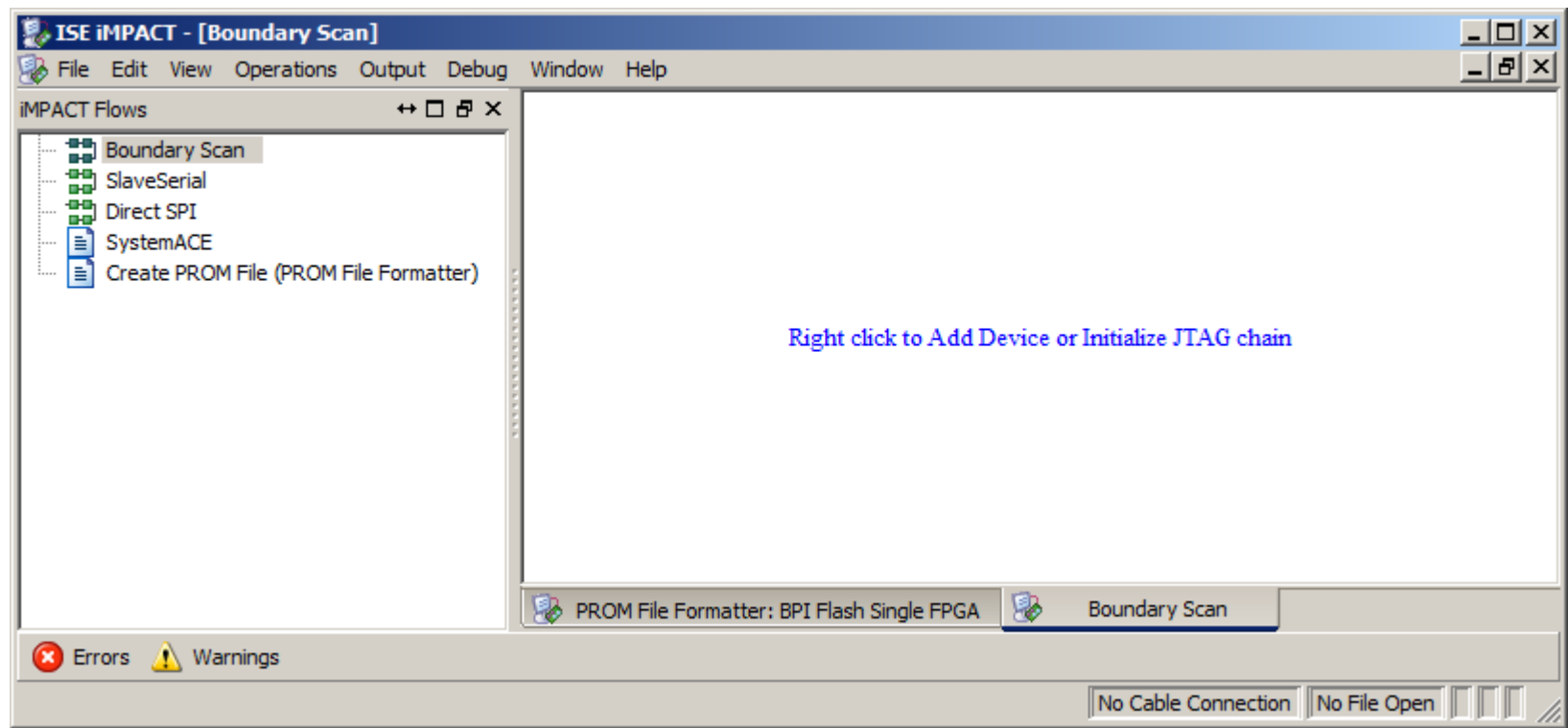
Program Platform Flash with PCIe Design

- From the iMPACT menu, select
Operations → Generate File...



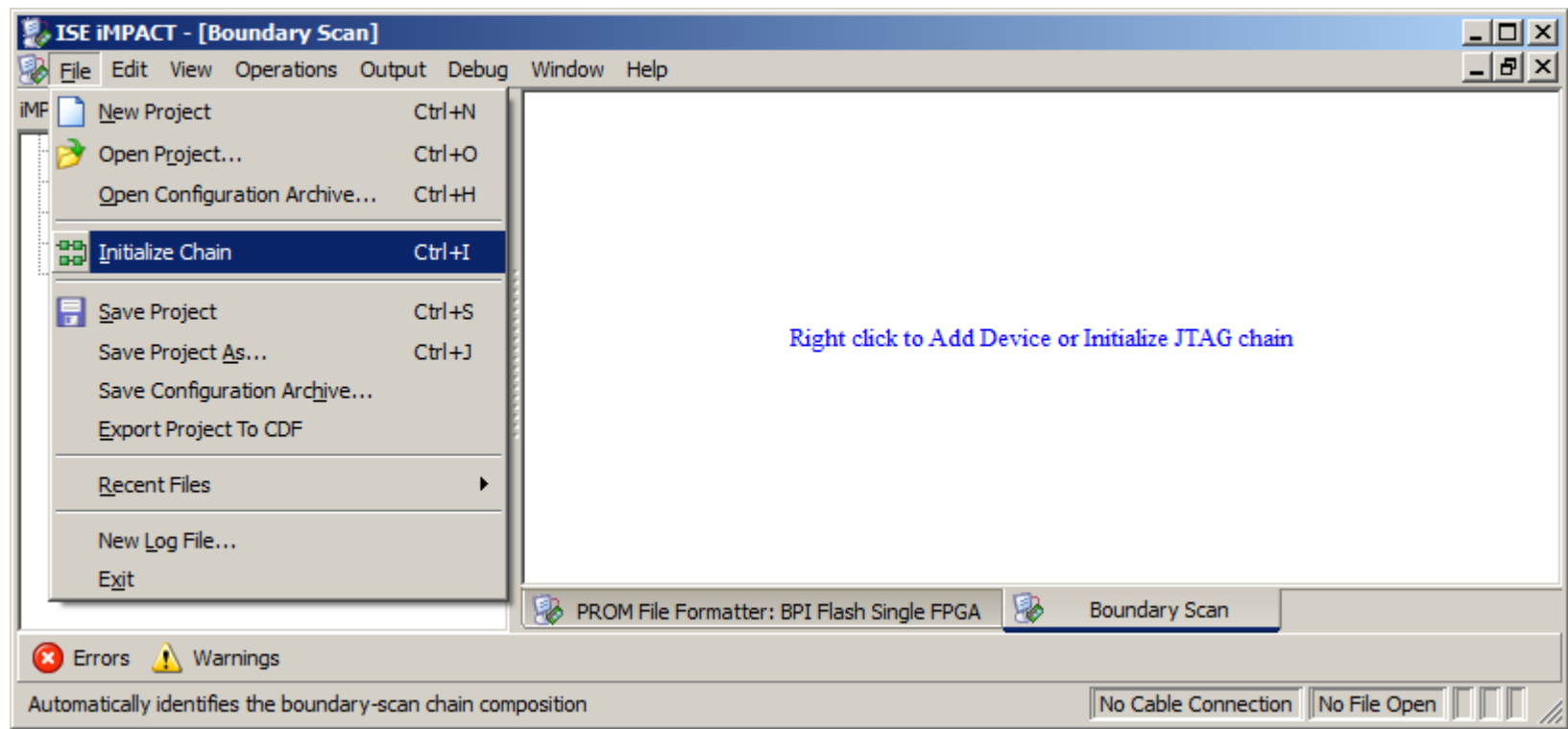
Program Platform Flash with PCIe Design

- After generation completes, under the iMPACT Flows, double click on Boundary Scan



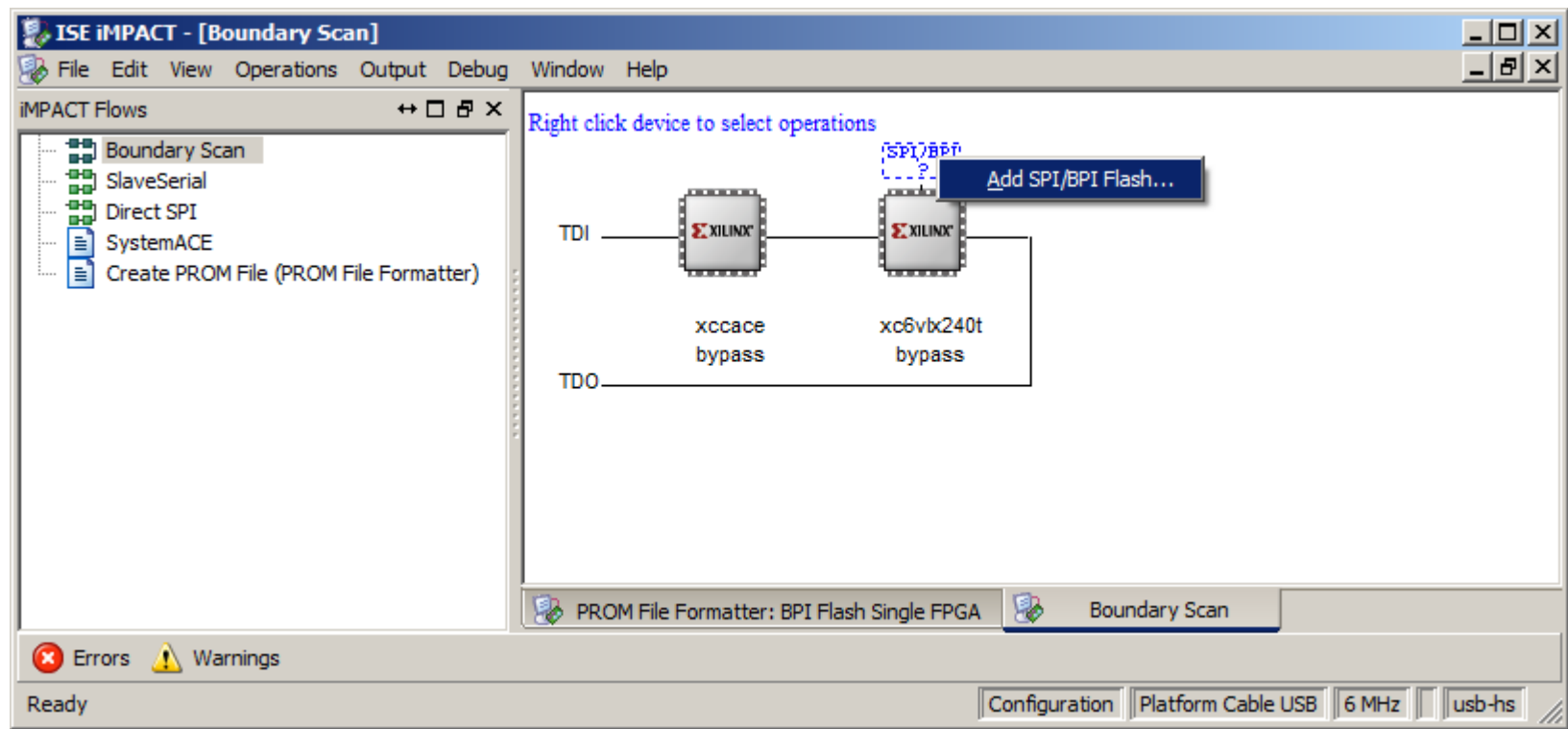
Program Platform Flash with PCIe Design

- From the iMPACT menu, select **File → Initialize Chain**



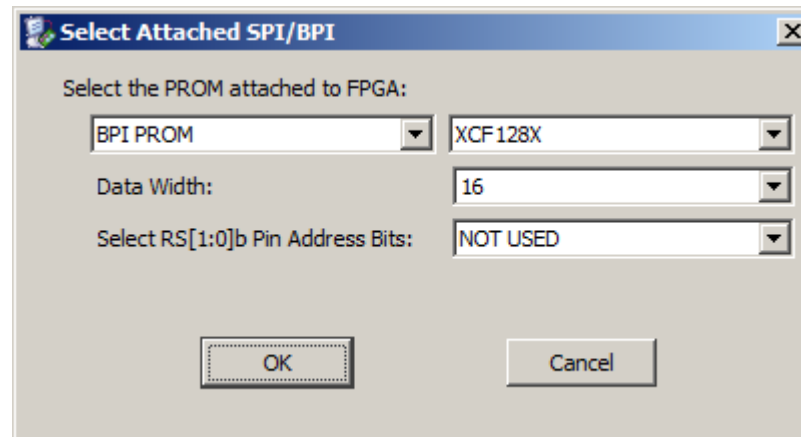
Program Platform Flash with PCIe Design

- Right click on the SPI/BPI ? and select Add SPI/BPI Flash...
 - Add <design path>\ready_for_download\ml605_pcie_x4_gen2.mcs



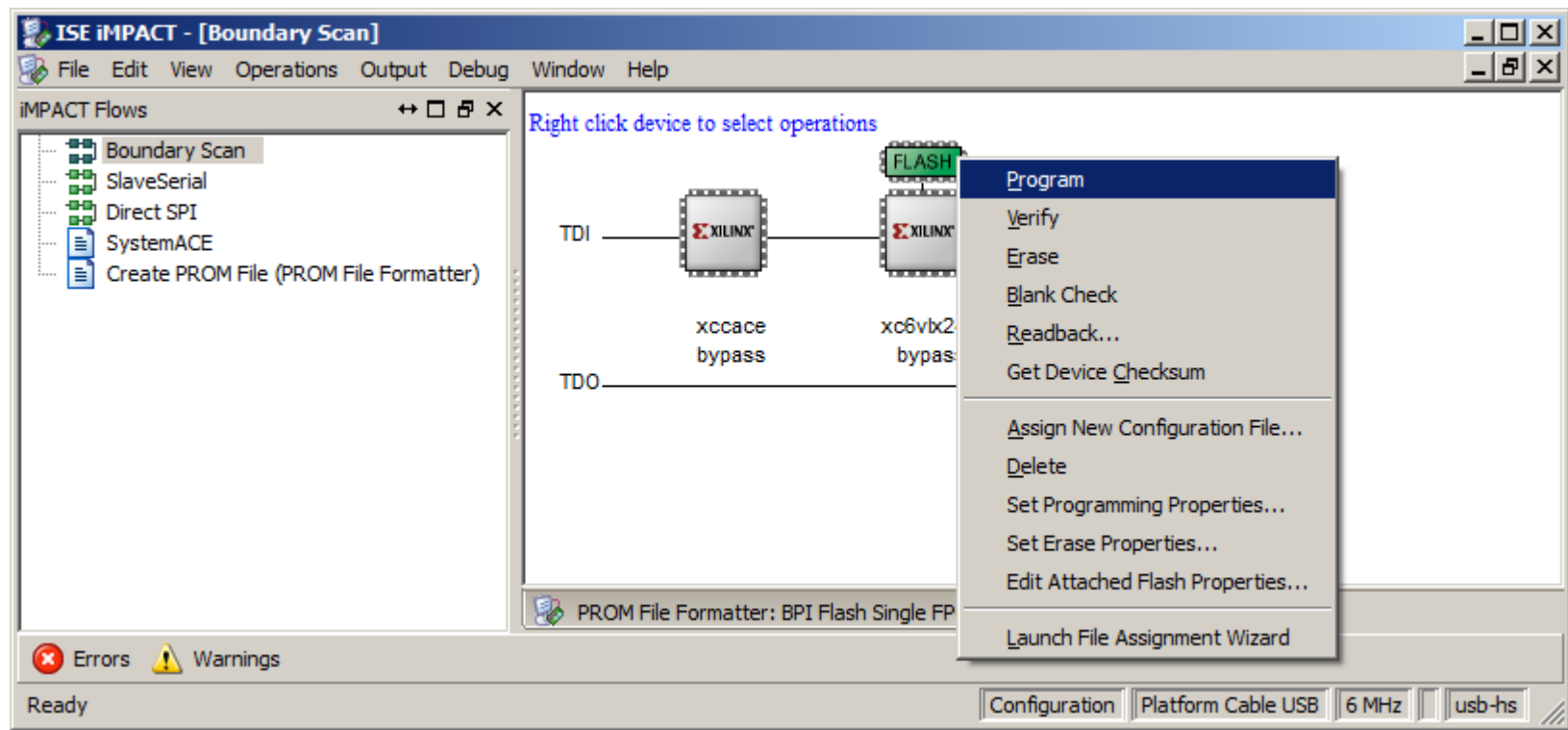
Program Platform Flash with PCIe Design

- Click OK for this dialog



Program Platform Flash with PCIe Design

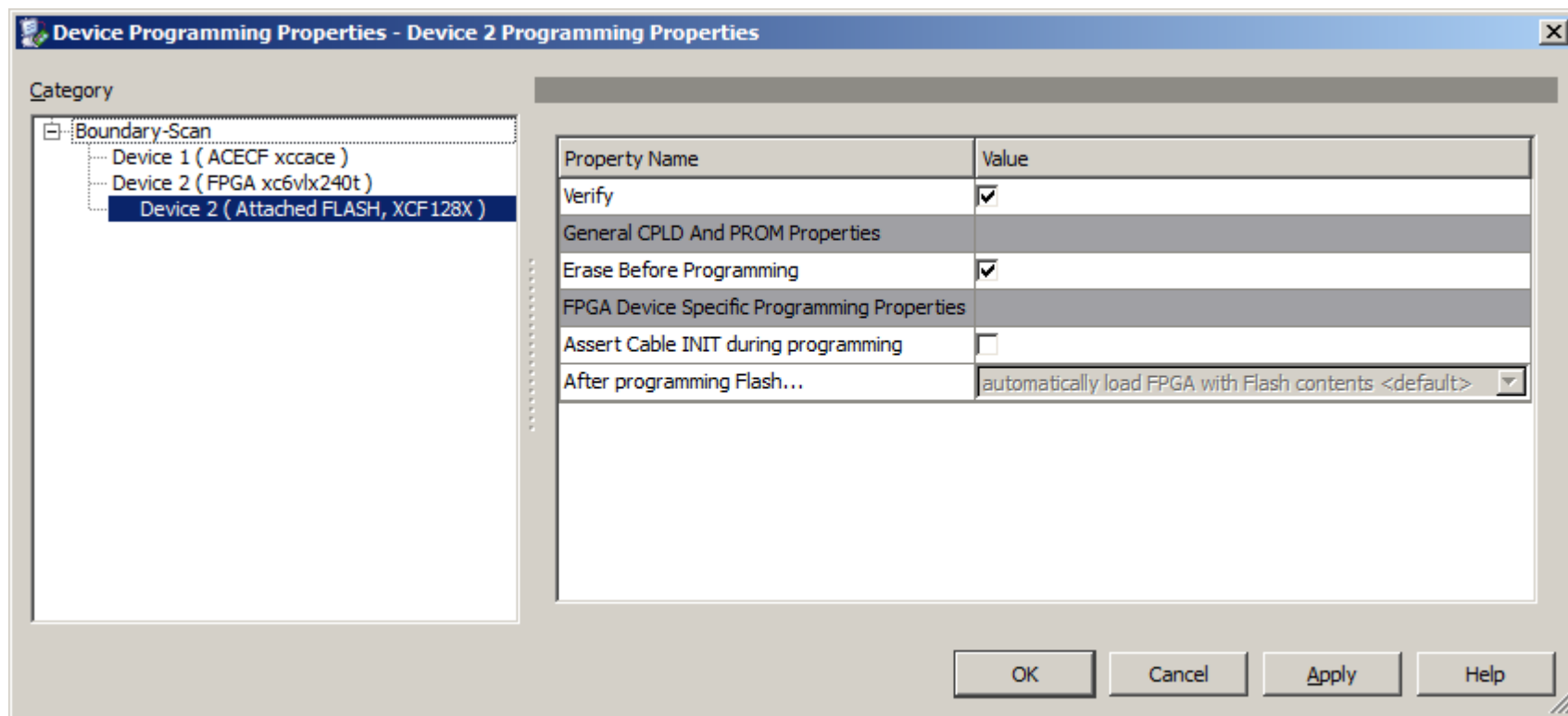
- Right click on the Flash and select Program



Note: Takes about 12 minutes

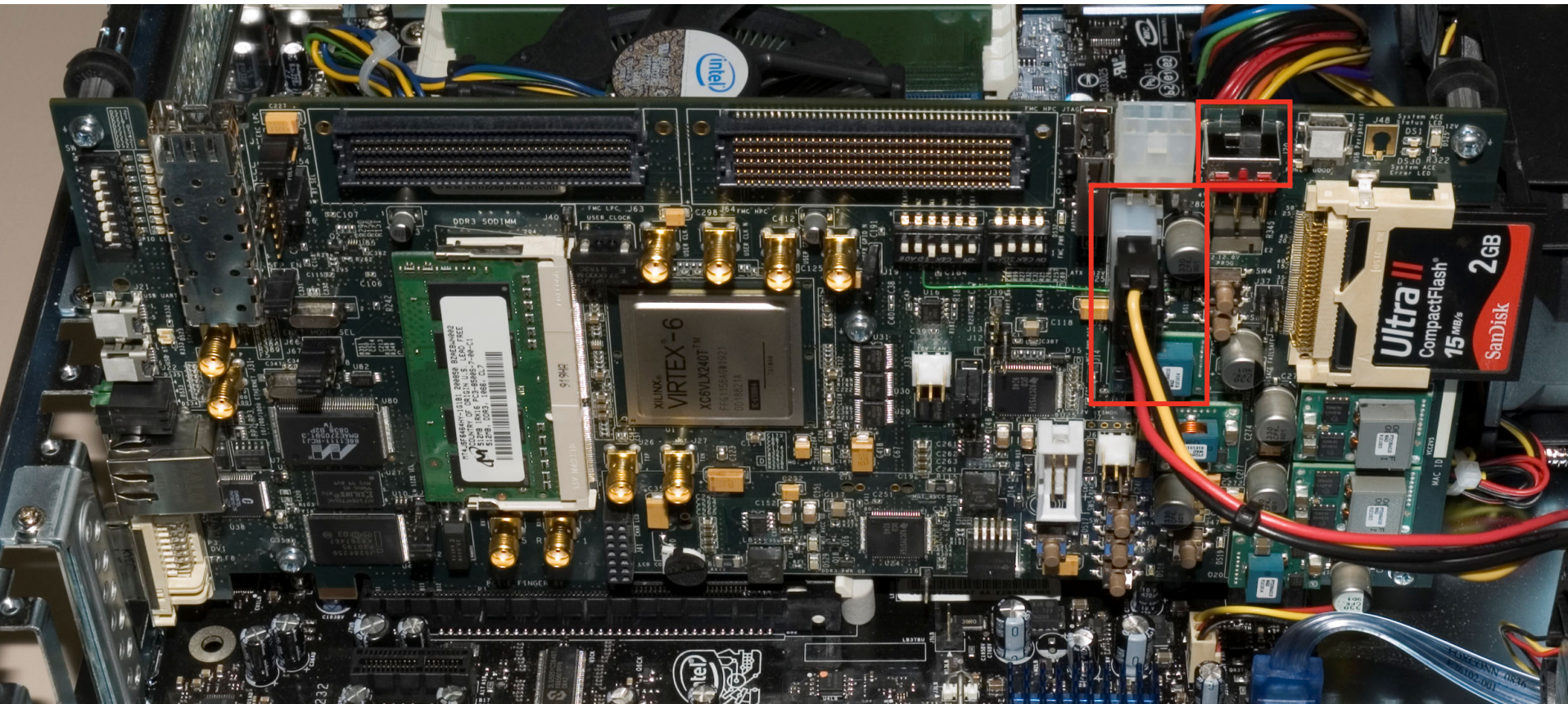
Program Platform Flash with PCIe Design

- Erase Before Programming must be selected



Hardware Setup

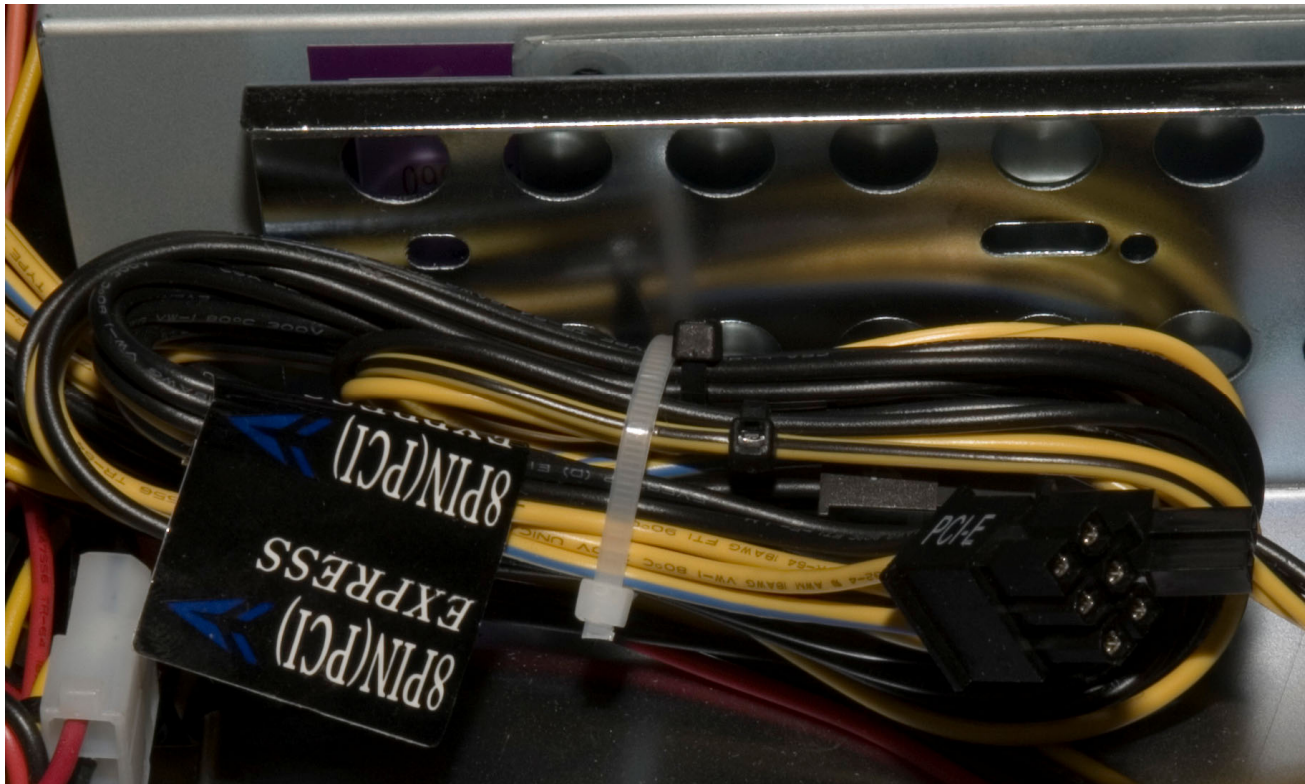
- Insert the ML605 Board into a PCIe x4 slot (x16 shown)
 - Connect PC power to J25, turn on Power Switch



Note: Presentation applies to the ML605

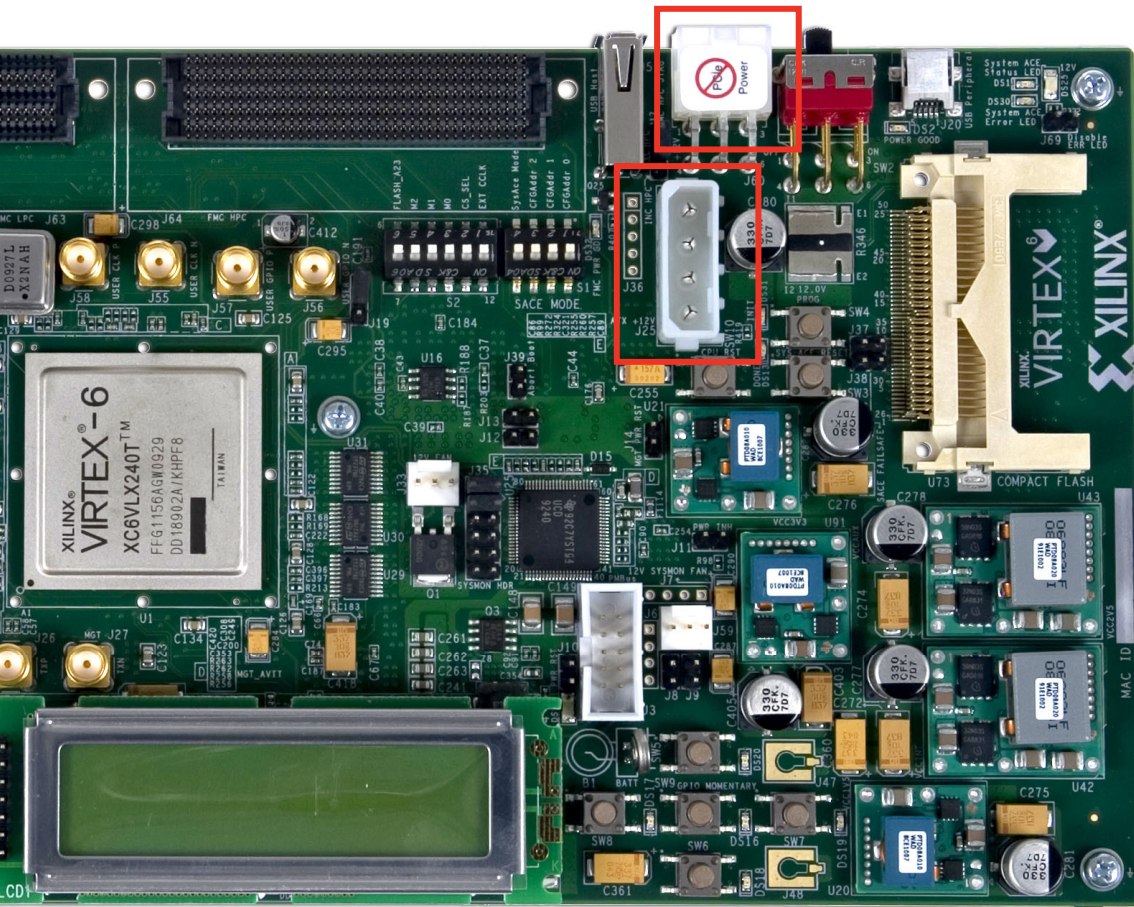
Hardware Setup

- Do *not* use the PCIe connector from the PC power supply



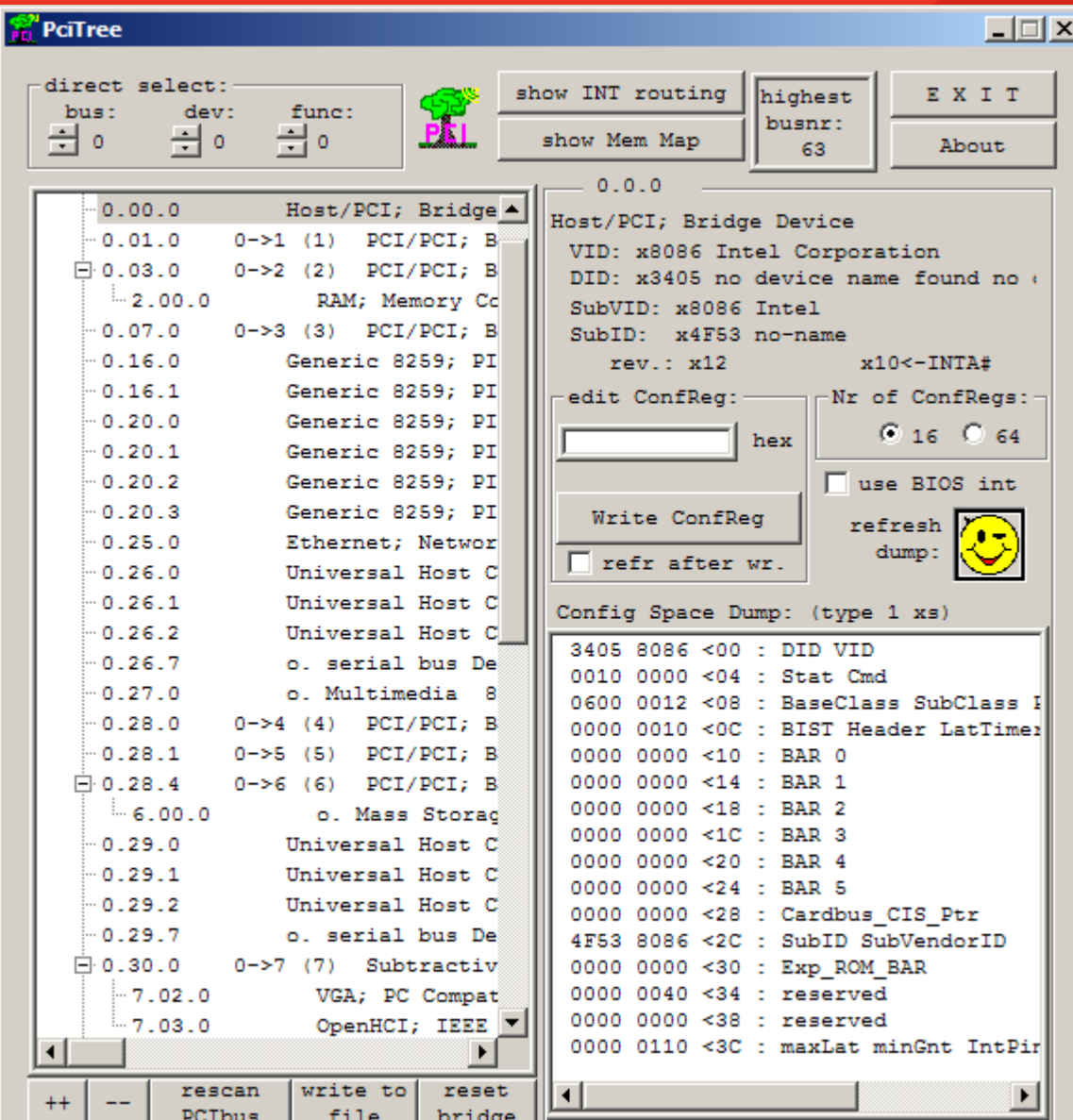
Hardware Setup

- Do not connect both the ML605 power brick connector (J60) and the four pin ATX power connector at the same time



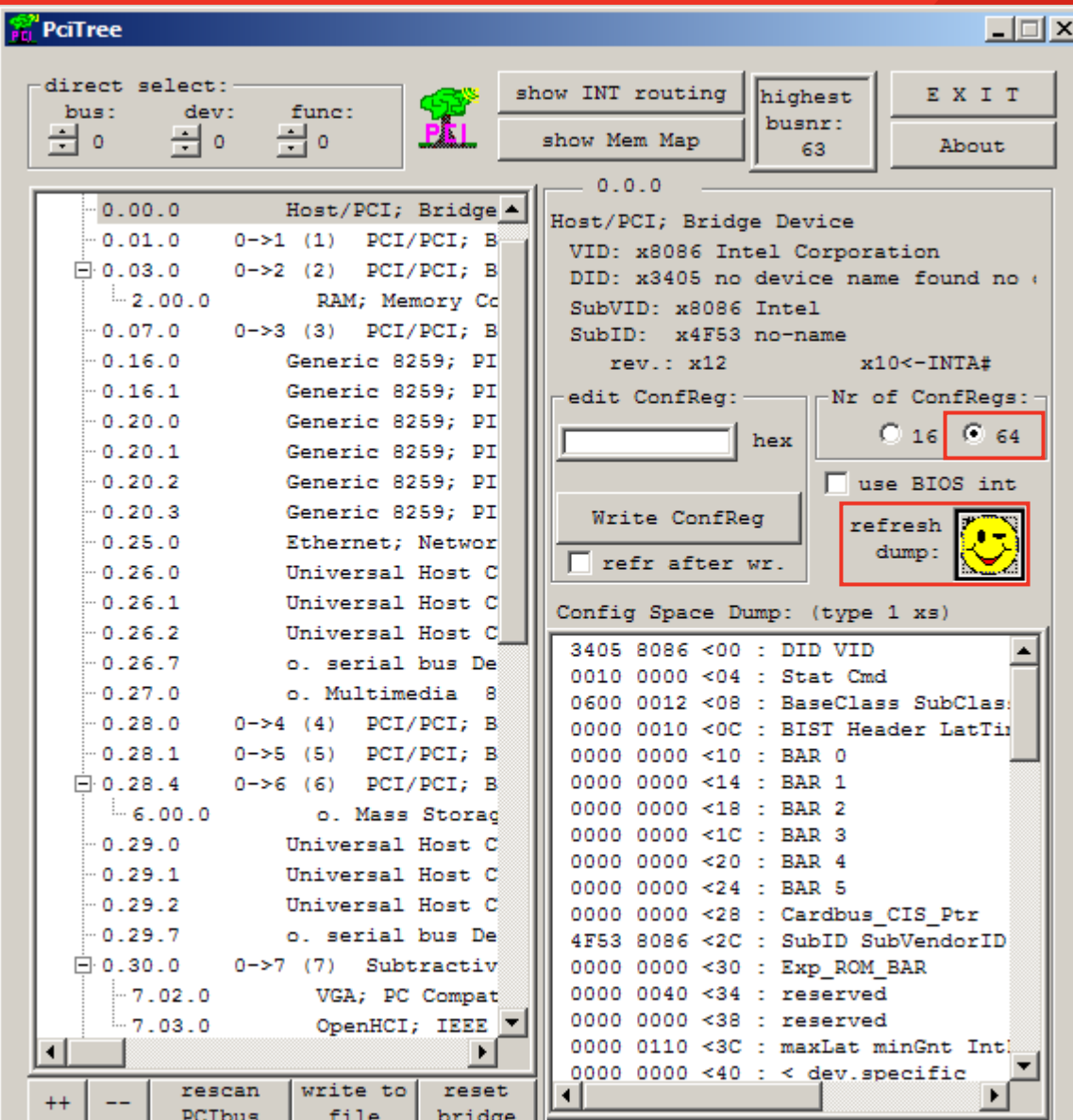
Note: Presentation applies to the ML605

Running the PCIe x4 Gen2 Design



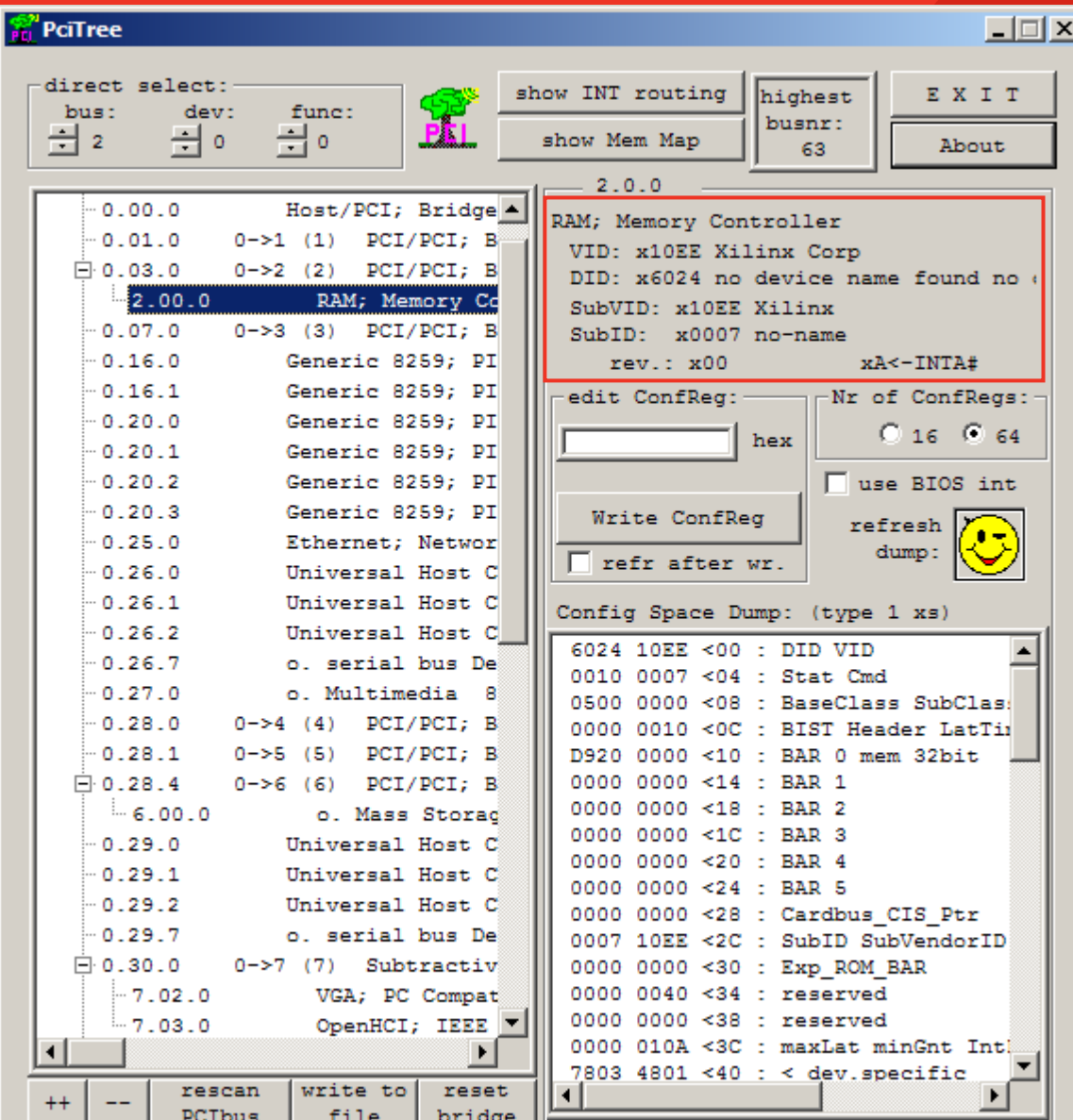
- Power on the PC
- Start PciTree

Running the PCIe x4 Gen2 Design



- Set Number of Configuration Registers to 64
- Click on Refresh dump

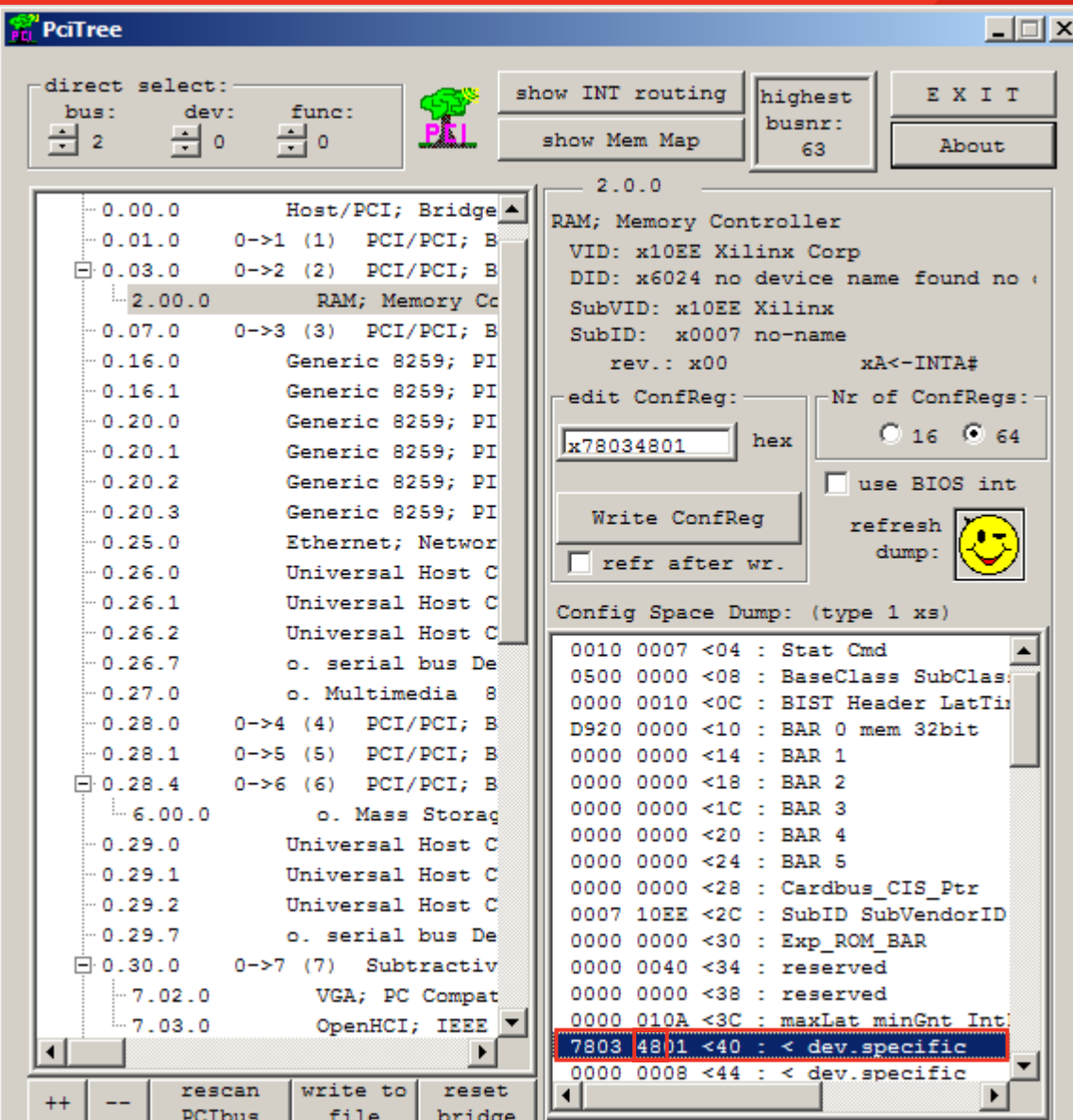
Running the PCIe x4 Gen2 Design



Locate the Xilinx Device

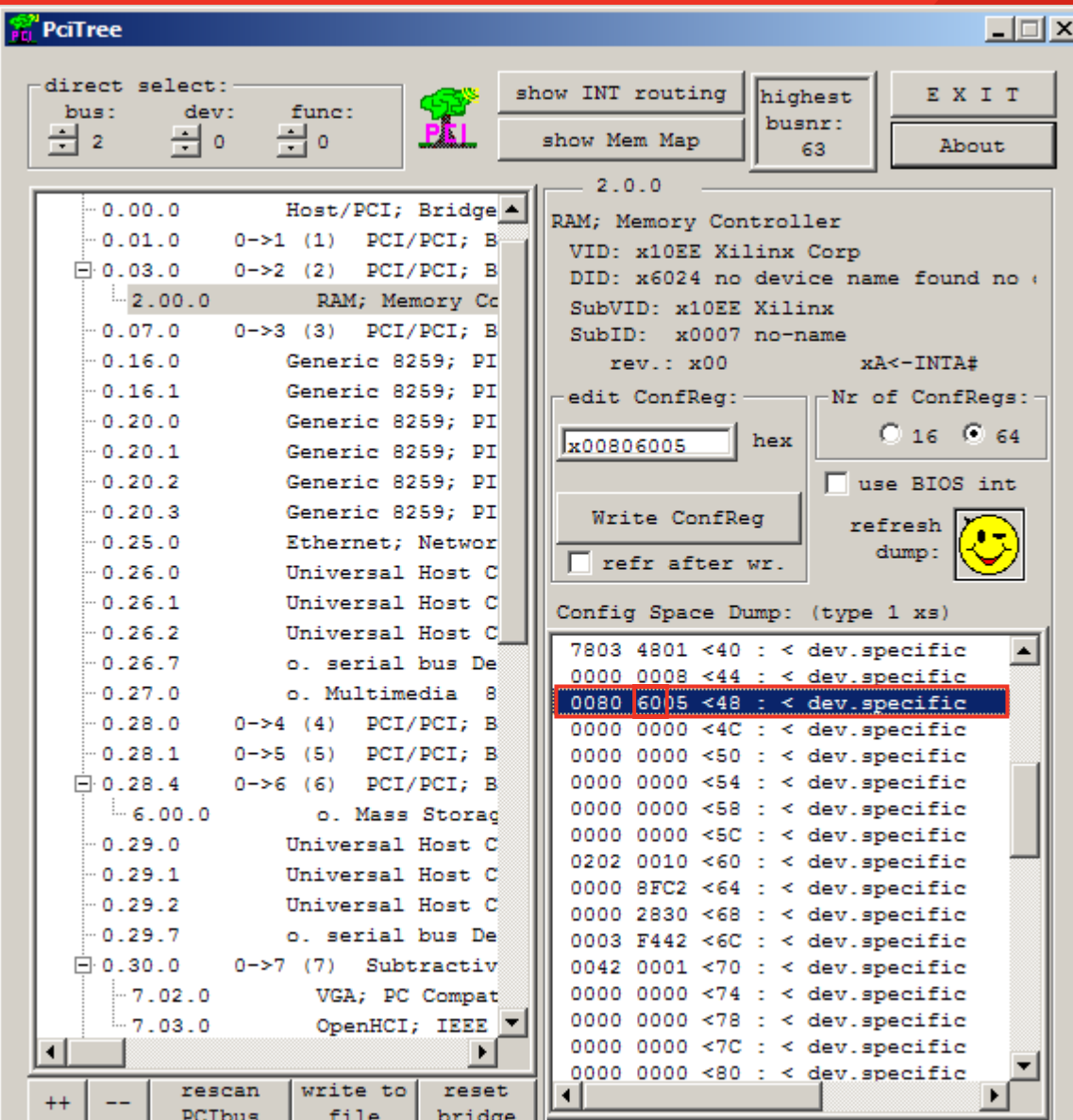
- Vendor ID is **0x10EE**
- The x4 Gen2 configuration will have a Device ID of **0x6024**

Running the PCIe x4 Gen2 Design



- Navigate the linked list in configuration space to locate the PCIe Capabilities Structure
 - See [UG517](#) for details
- With the Xilinx device selected, select Register 0x40
 - Register 0x40 points to the next structure
 - 0x48 is the address of the next structure

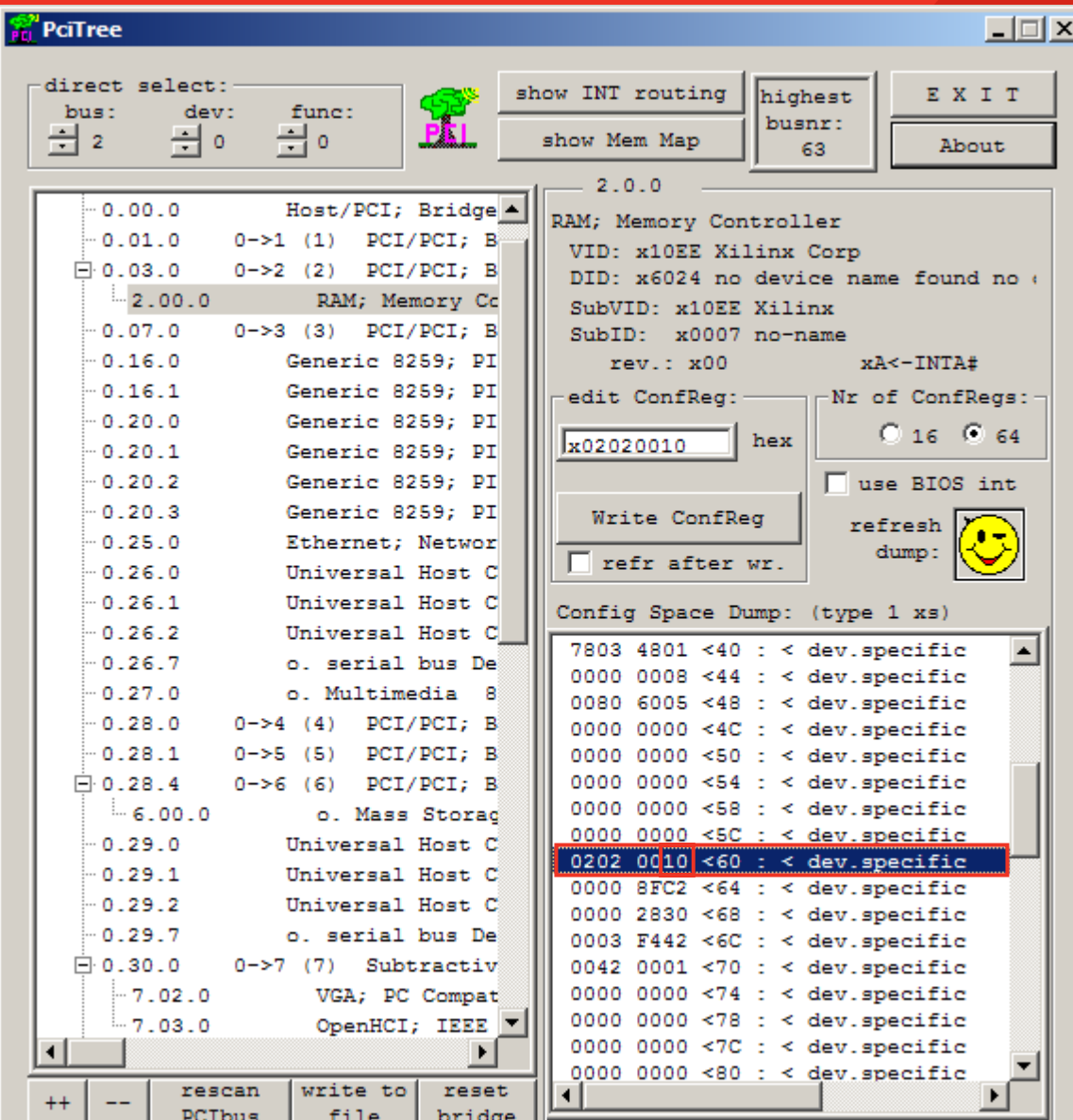
Running the PCIe x4 Gen2 Design



■ Select Register 0x48

- Register 0x48 points to the next structure
- 0x60 is the address of the next structure

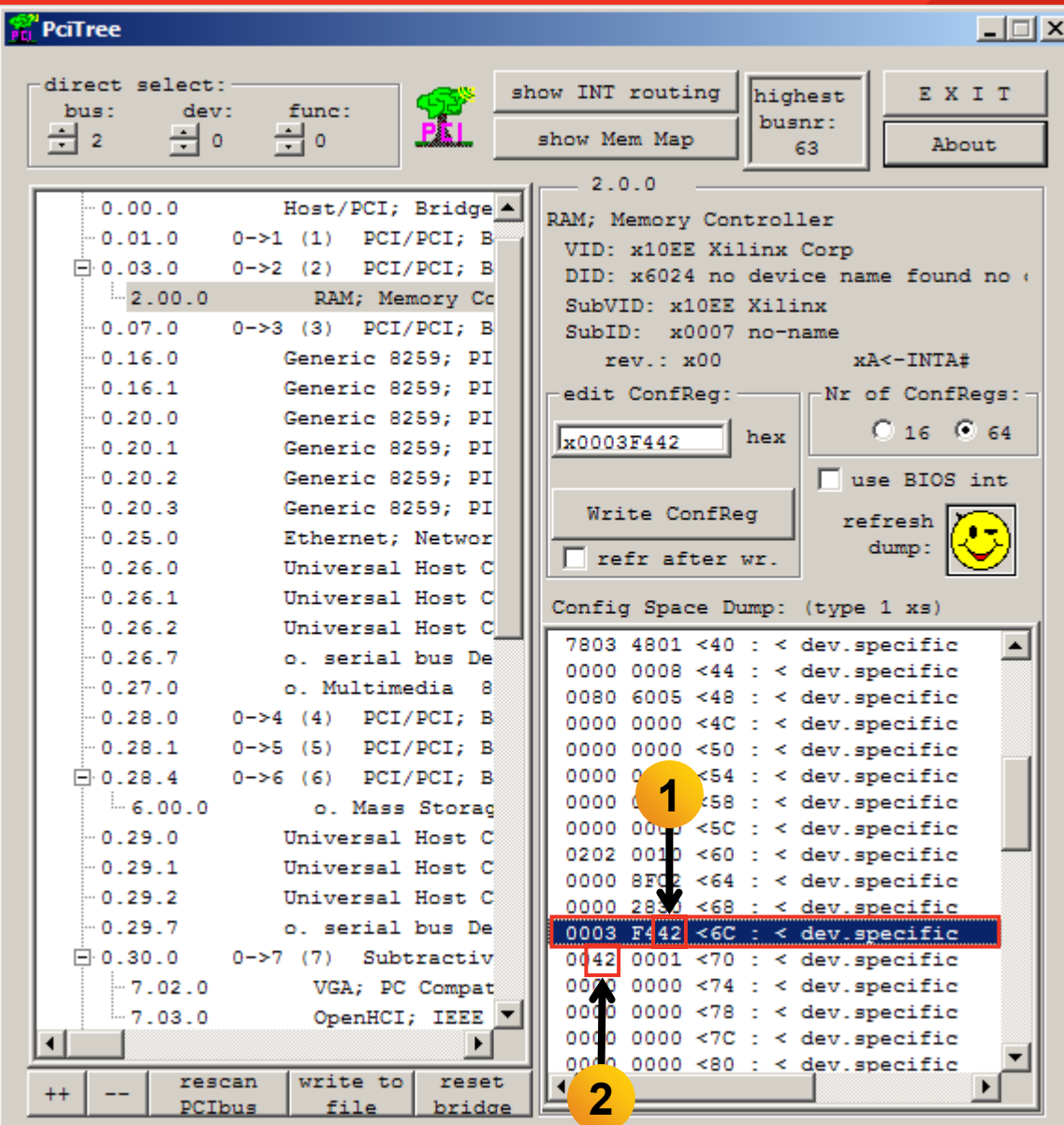
Running the PCIe x4 Gen2 Design



Register 0x60

- 0x60 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure

Running the PCIe x4 Gen2 Design



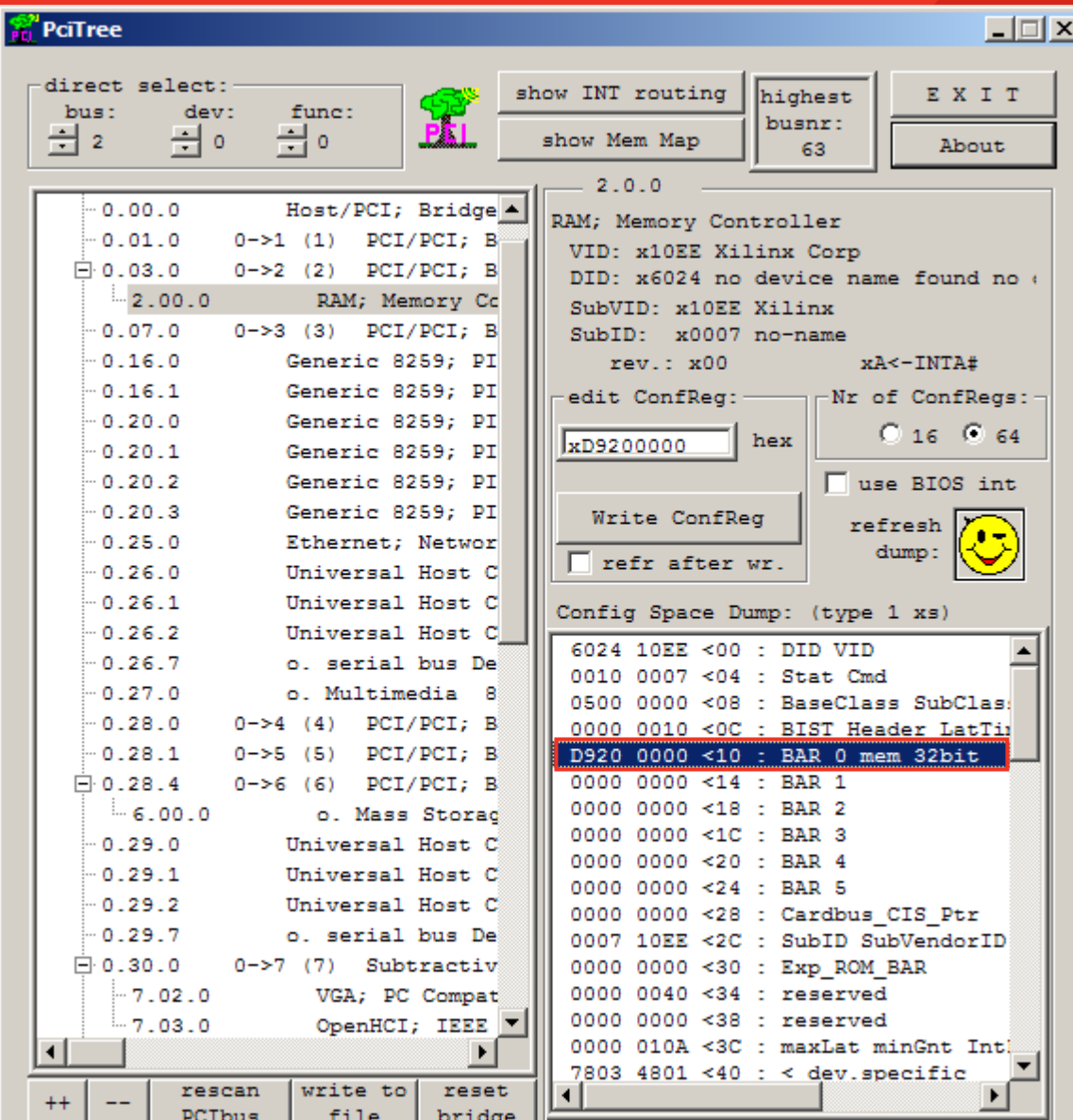
■ Register 0x6C

- Link Capabilities Register
- Indicates the maximum number of lanes and speed (Gen1, Gen2) for device
- The value 0x42 shows this is an x4 Gen2 device (1)

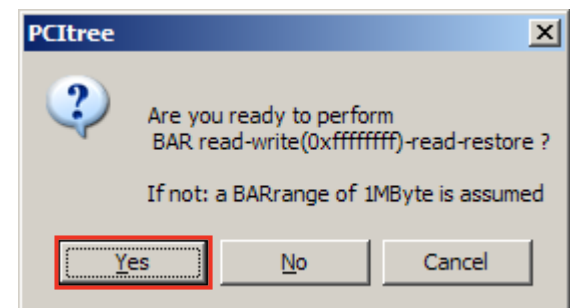
■ Link Status Register

- 0x70
- Shows the current link status
- This design, in a Gen2 chassis, trained to x4 Gen2 (2)

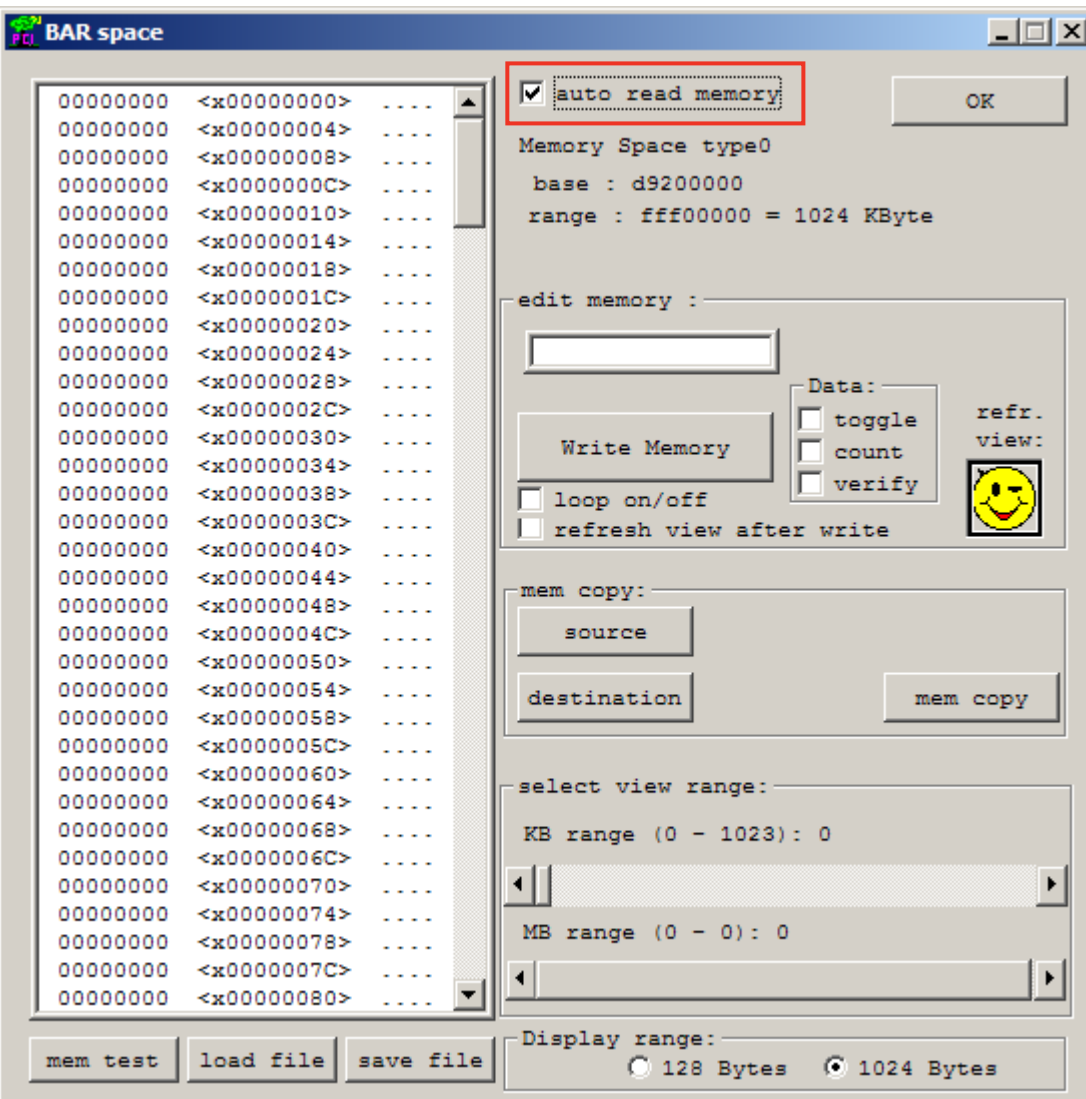
Running the PCIe x4 Gen2 Design



- Double-click on BAR 0
 - BAR 0 Address is machine dependent
- Click Yes on the Dialog box seen below

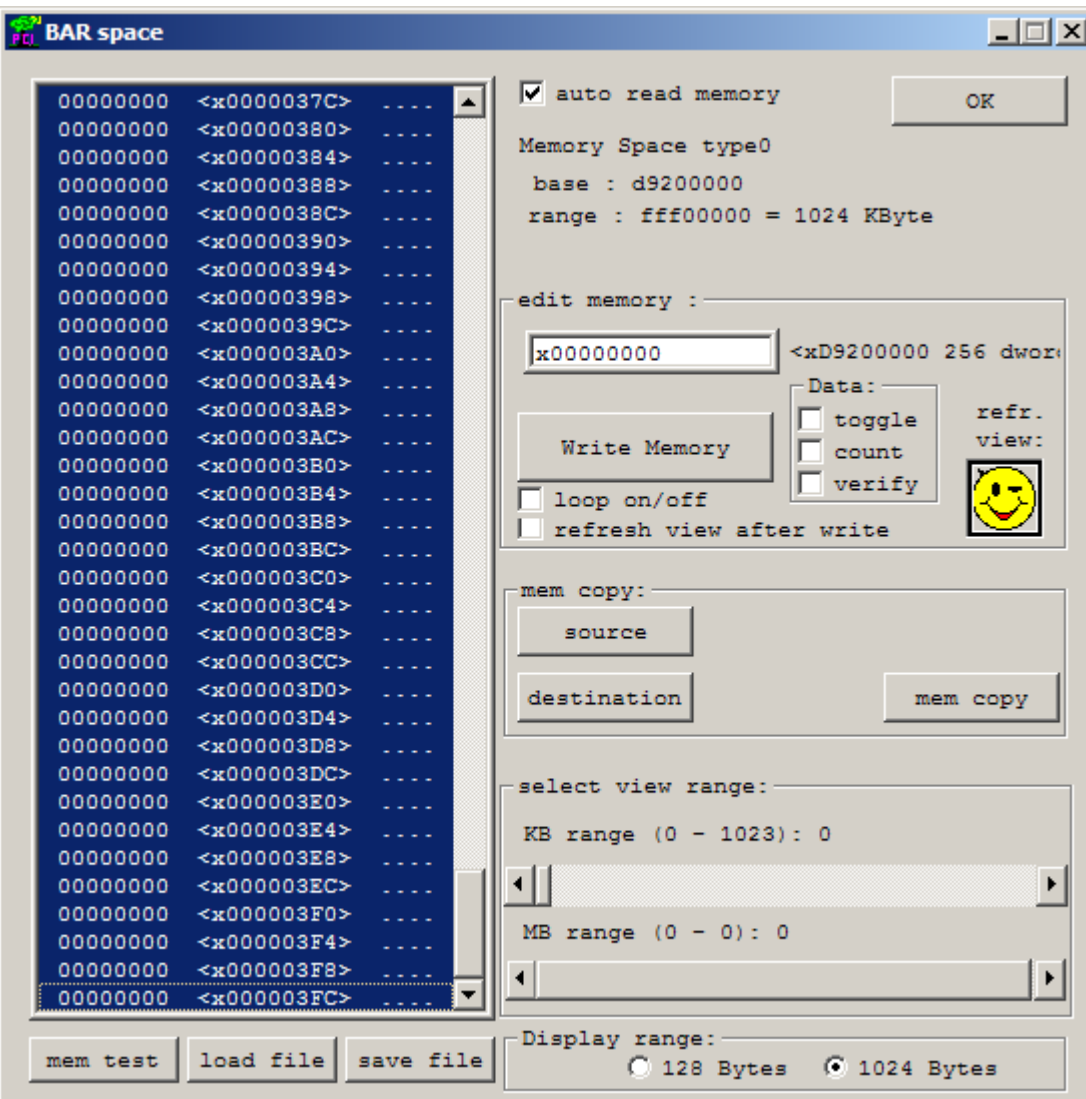


Running the PCIe x4 Gen2 Design



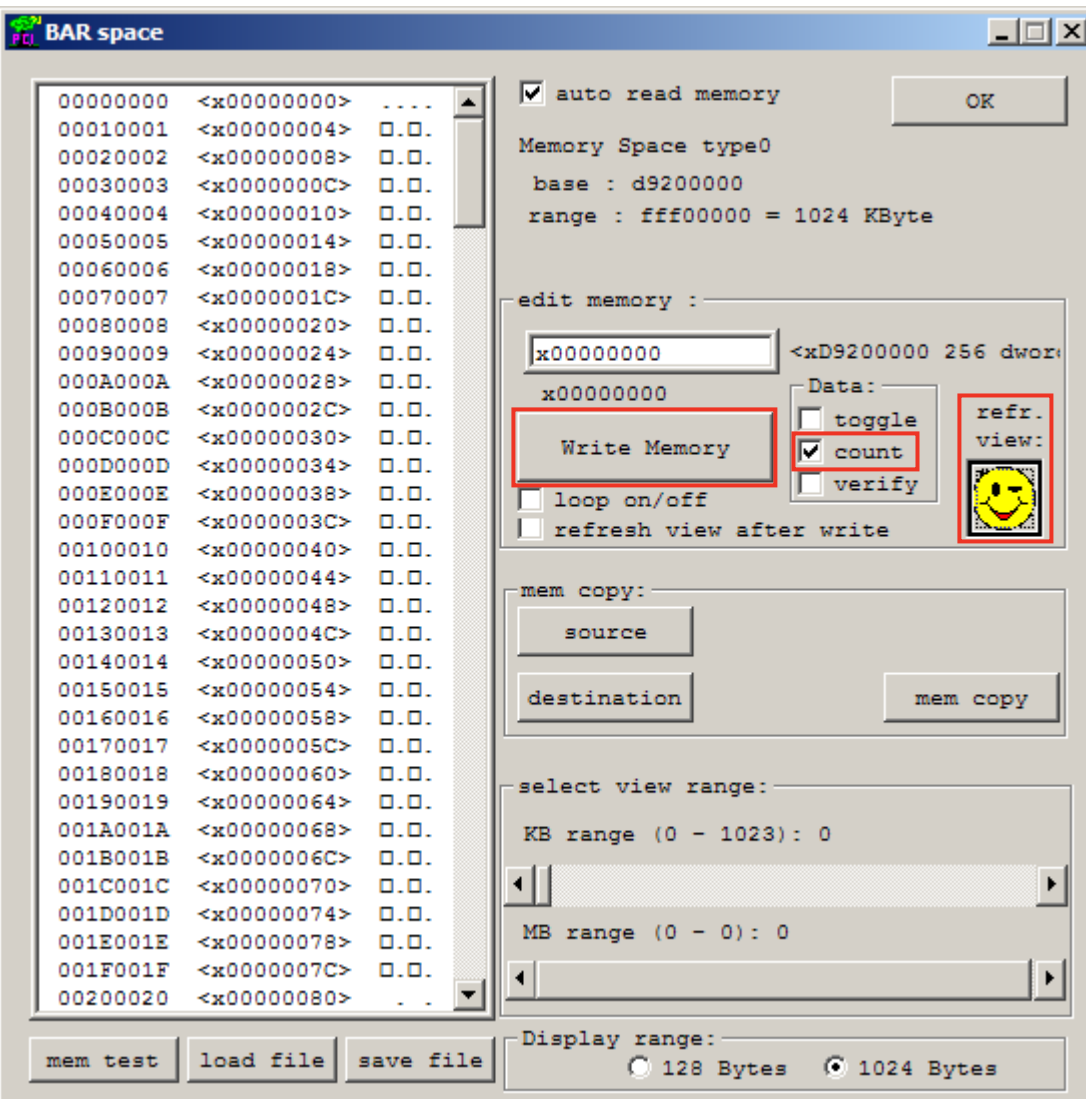
- Select auto read memory

Running the PCIe x4 Gen2 Design



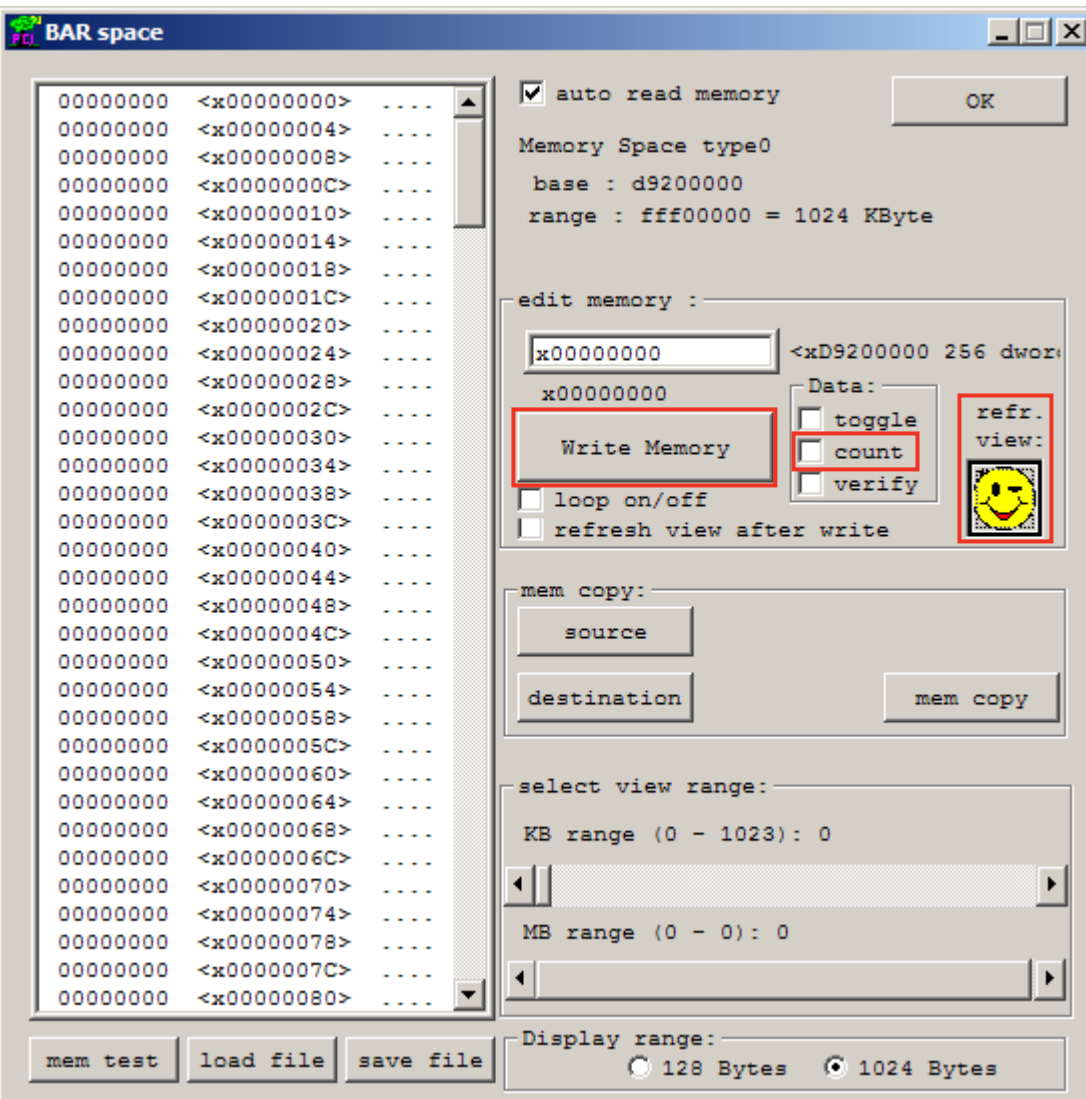
- Click on the first memory location
 - Type <Shift-End> to select 1024 Bytes

Running the PCIe x4 Gen2 Design



- **Write Memory**
 - Select count
 - Click Write Memory
 - Click refr view
- **View results – counting up to FF**

Running the PCIe x4 Gen2 Design



- **Restore Memory**
 - Deselect count
 - Click Write Memory
 - Click refr view
- **Memory is reset to zeros**

Virtex-6 PCIe x4 Gen2 Capability

- **ML605 Supports PCIe Gen1 and Gen2 Capability**
 - x4, x2, or x1 Gen2 lane width
 - x8 Gen2 not supported in -1 parts
- **LogiCORE PIO Example Design**
 - [RDF0009.zip](#)
- **LogiCORE Integrated Block for PCI Express**
 - See [UG517](#) for details

References

References

▪ PCIe Base Specification

- PCI SIG Web Site

<http://www.pcisig.com/home>

▪ Virtex-6 PCIe

- PCIe Product Overview

http://www.xilinx.com/products/ipcenter/V6_PCI_Express_Block.htm

- Virtex-6 FPGA Integrated Block v1.3 for PCI Express User Guide

http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ug517.pdf

- Virtex-6 FPGA Integrated Block v1.3 for PCI Express Data Sheet

http://www.xilinx.com/support/documentation/ip_documentation/v6_pcie_ds715.pdf

- IP Release Notes Guide

http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

Documentation

Documentation

- **Virtex-6**

- Virtex-6 FPGA Family

- <http://www.xilinx.com/products/virtex6/index.htm>

- **ML605 Documentation**

- Virtex-6 FPGA ML605 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Hardware User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf