ML605 GTX IBERT Design Creation

December 2009

XTP046

ML605 IBERT Overview

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  - Running the ML605 IBERT Design – Bank 114
  - Running the ML605 IBERT Design – Bank 115
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- **ML605 IBERT Design Creation**
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  - Create IBERT Design – Bank 113 (FMC_HPC)
  - Create IBERT Design – Bank 114 (PCIe)
  - Create IBERT Design – Bank 115 (PCIe)
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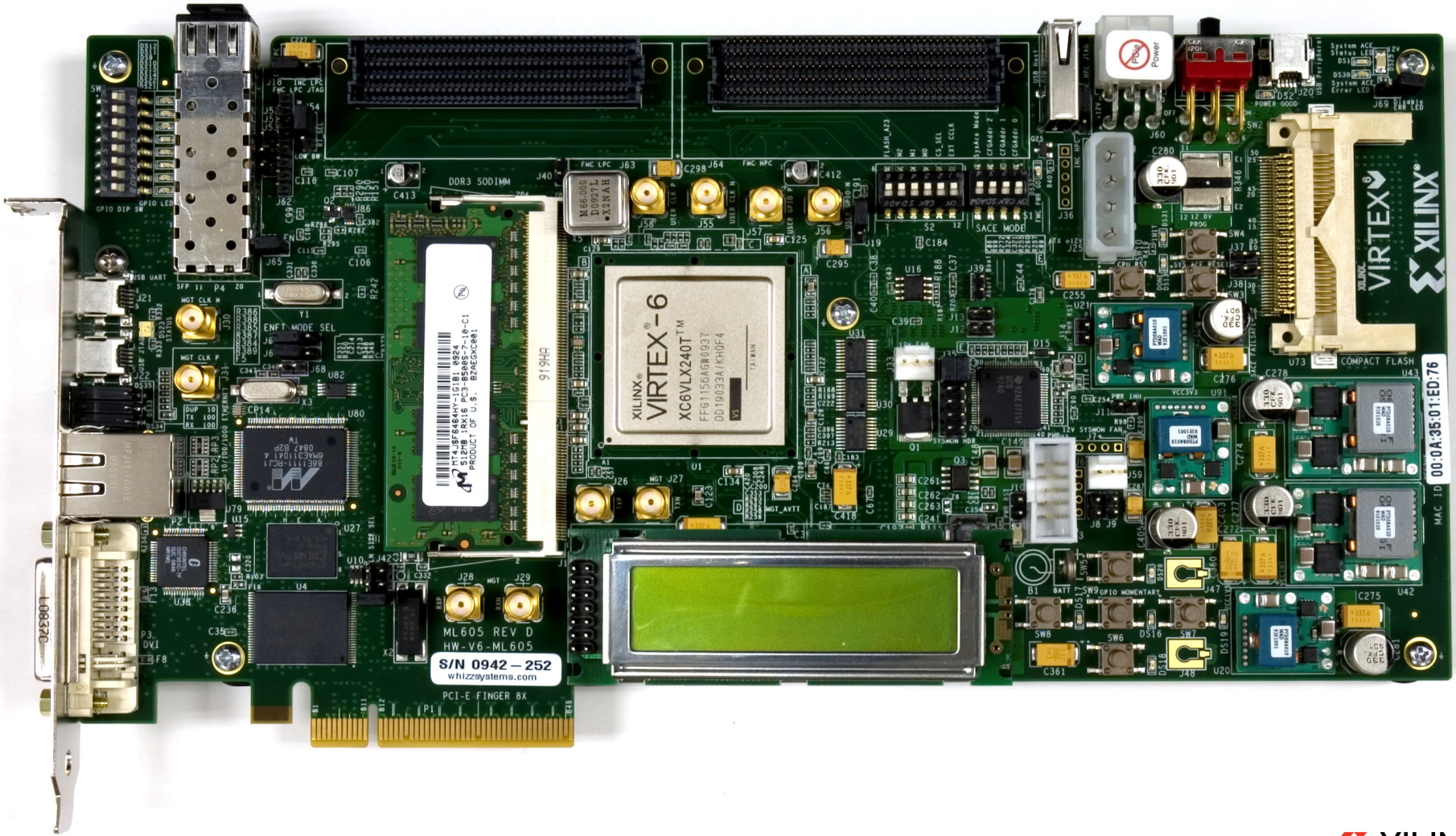
- **References**

Note: This Presentation applies to the ML605

ML605 IBERT Overview

- **Description**
  - The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Virtex-6 GTX transceivers. A graphical user interface is provided through the IBERT console window of the ChipScope Pro Analyzer
- **Reference Design IP**
  - LogiCORE IBERT Example Designs
    - SFP (1), SGMII (1), SMA (1), PCIe (8), FMC_HPC (4), FMC_LPC (1)
  - ChipScope Pro Analyzer
    - ChipScope Pro 11.4 Software and Cores User Guide (UG029)

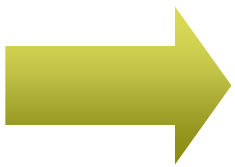
Xilinx ML605 Board

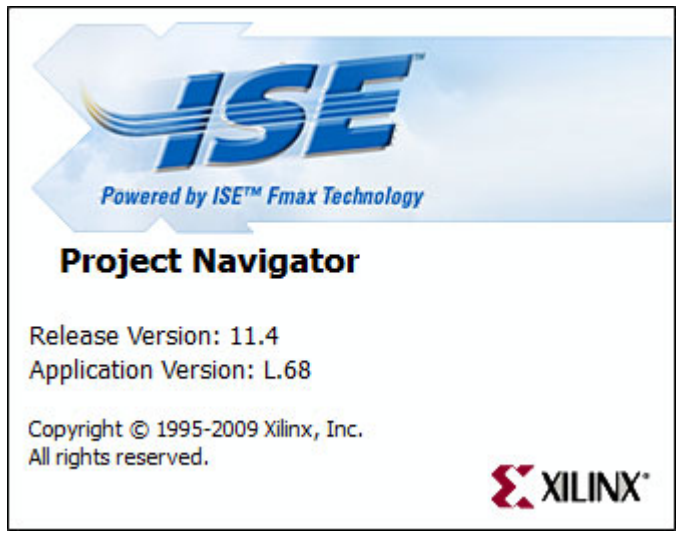


Note: Presentation applies to the ML605

Software Requirements

- **Xilinx ISE 11.4 software**





Note: Presentation applies to the SP601

ChipScope Pro Software Requirement

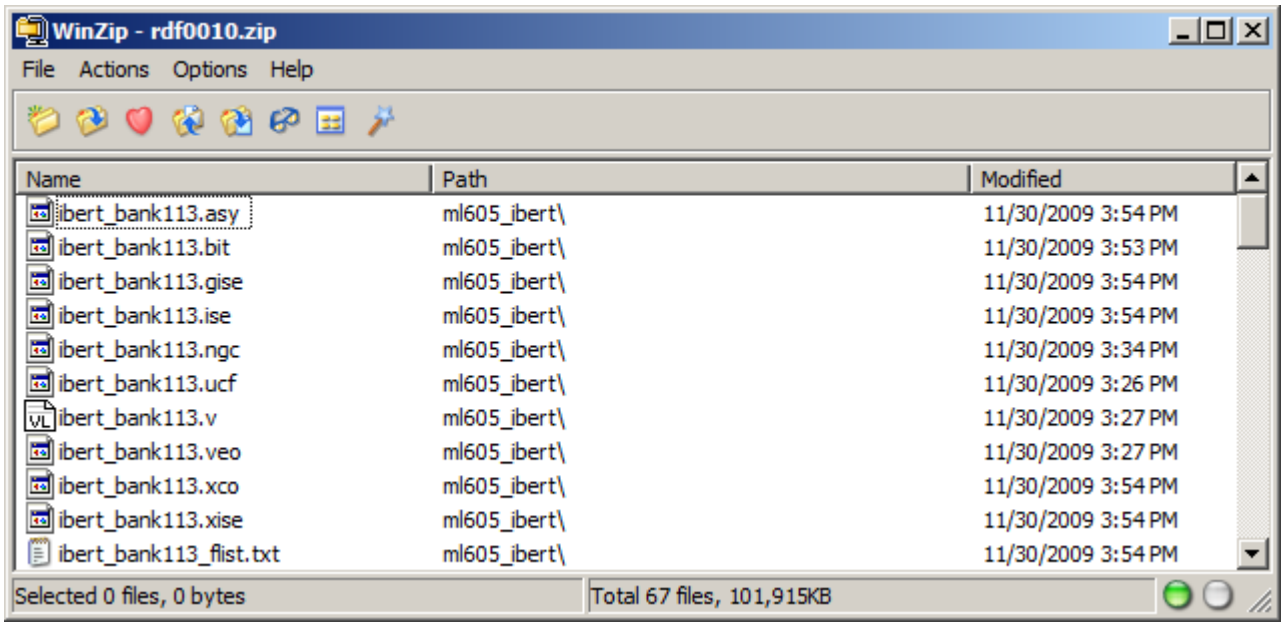
- **Xilinx ChipScope Pro 11.4 software**

Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

Setup for the ML605 IBERT Designs

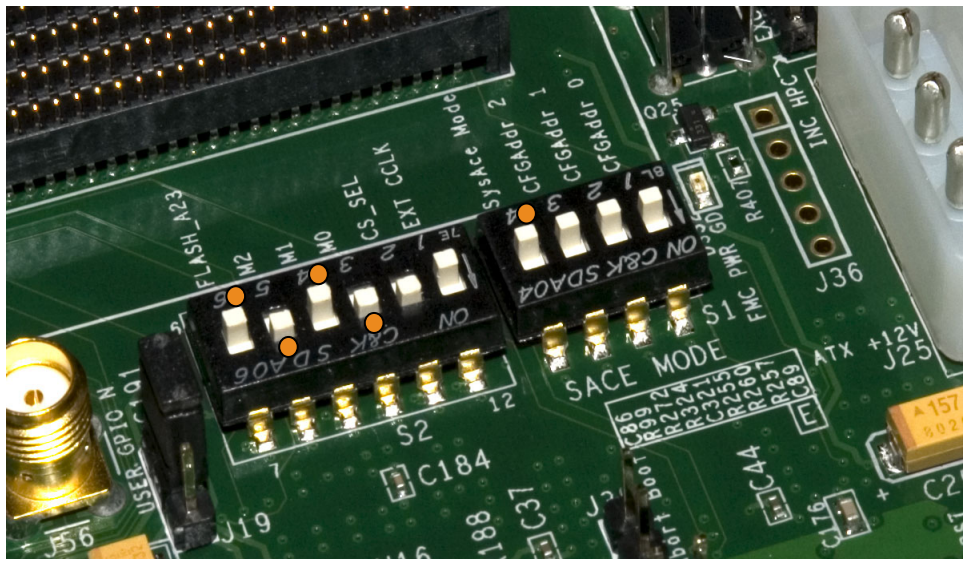
- **Unzip the rdf0010.zip file to your C:\ drive**
  - https://secure.xilinx.com/webreg/clickthrough.do?cid=139971



Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- **Set S2 to 0101XX (X = Don't care, 1 = on, Position 6 → Position 1)**
  - This selects JTAG
- **Set S1 to 0XXX (Position 4 → Position 1)**
  - This disables JTAG configuration from the Compact Flash



Note: Presentation applies to the ML605

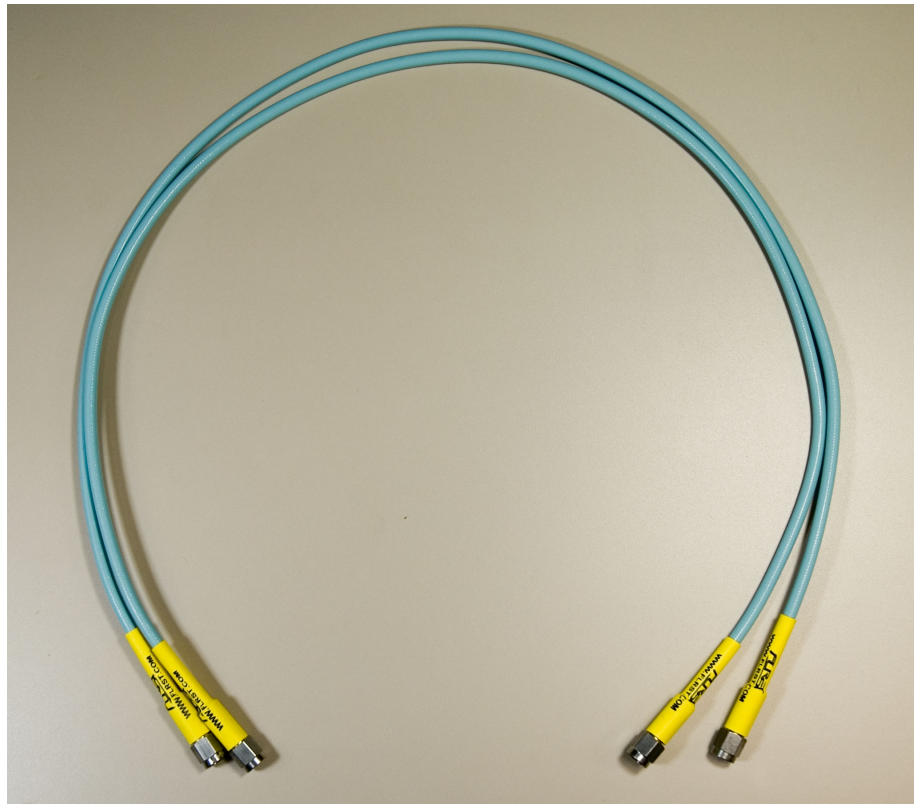
Setup for the ML605 IBERT Designs

- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board**
  - Connect this cable to your PC

Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- **SMA Cable**
  - www.flrst.com
  - P/N: ASPI-024-ASPI-S402



Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- **Using the SMA cables:**
  - Connect J28 to J26
  - Connect J29 to J27

Note: Presentation applies to the ML605

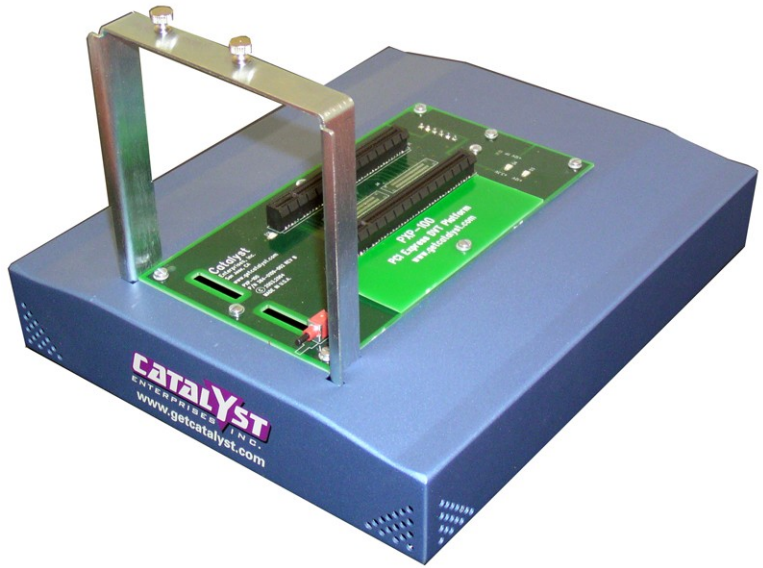
Setup for the ML605 IBERT Designs

- **Connect Optical Loopback Adapter**
  - www.molex.com
  - SFP Loopback Adapter, 3.5 db Attenuation
  - Part # 74720-0501
  - Alternatively, use an SFP transceiver with a fiber optic cable
- **Insert into the SFP Connector on the ML605 board**

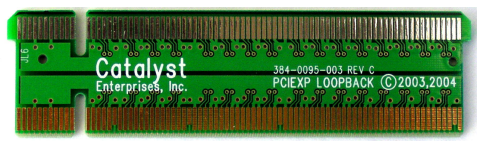
Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- **PCIe Testing Hardware:**
  - Catalyst PXP-100 DVT Platform



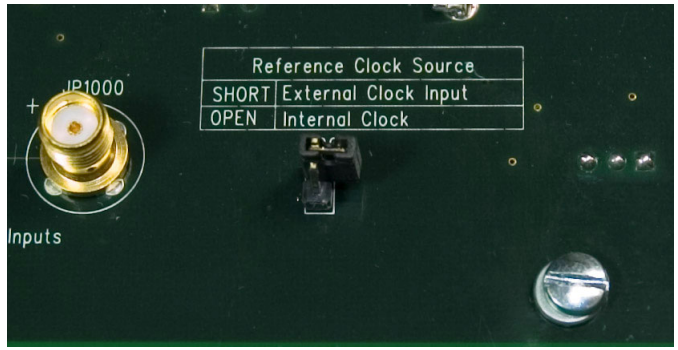
- **Catalyst PELOOP-BACK**



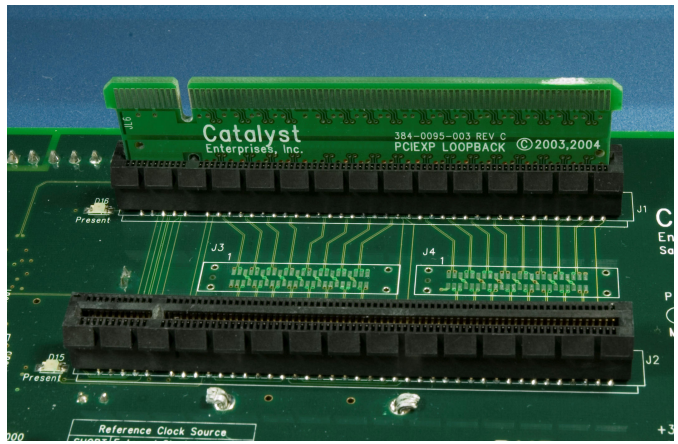
Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- On the Catalyst, set the reference clock jumper to open

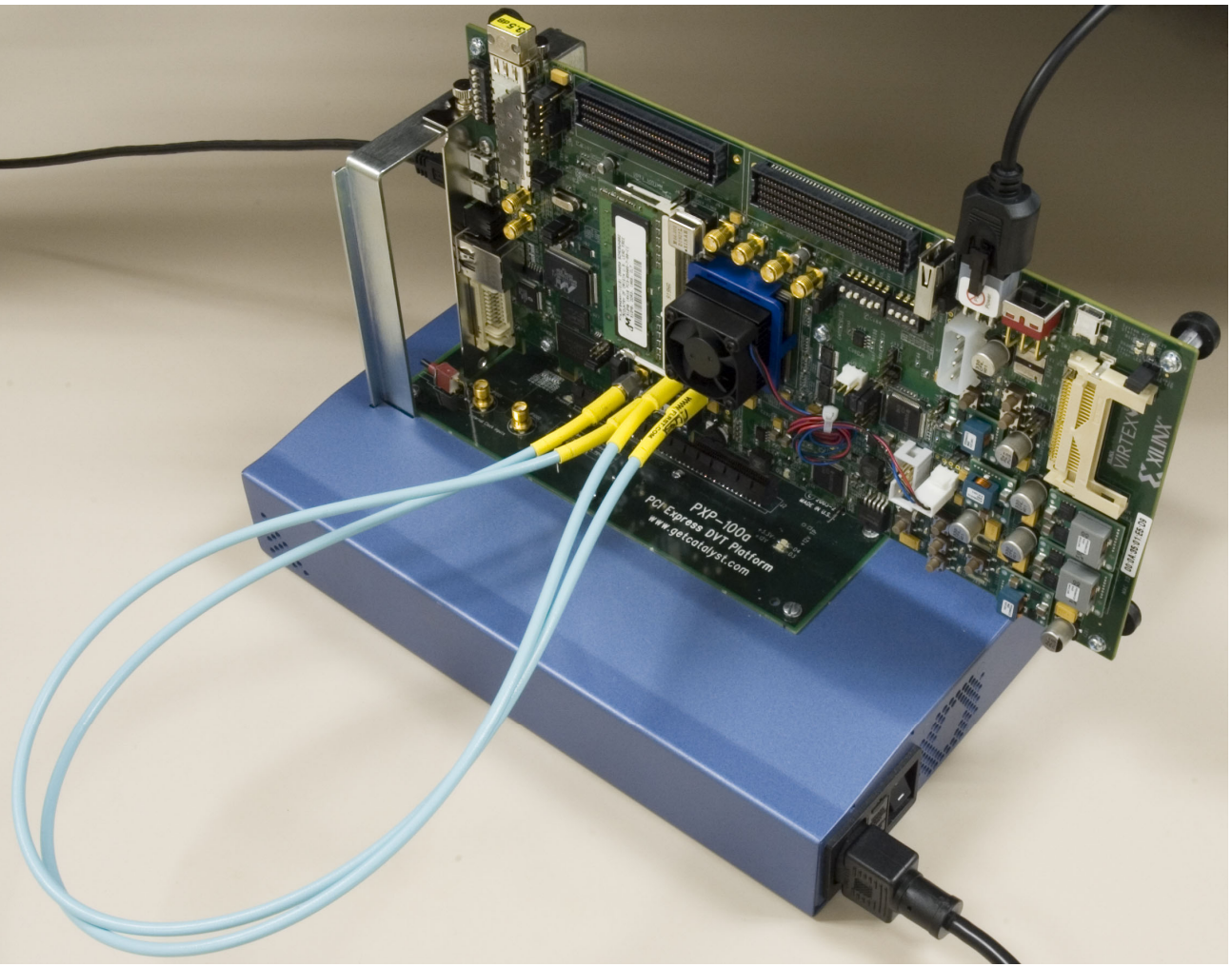


- Insert the PELOOP-BACK into one of the PCIe slots



Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

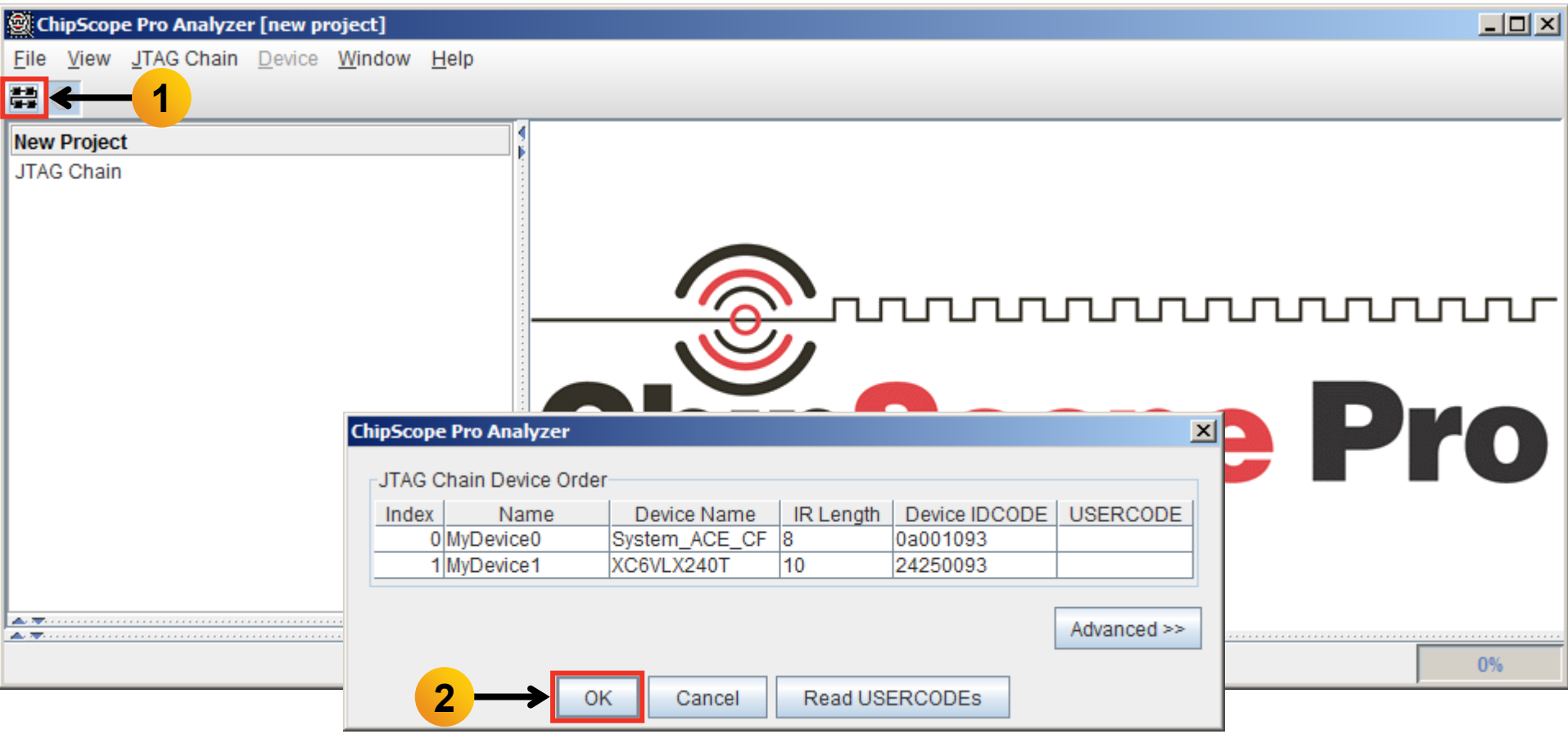


- Insert the ML605 into the other slot
- Connect the ML605 and Catalyst power
- Power up the ML605 and Catalyst

Running the ML605 IBERT Design – Bank 113

Running the ML605 IBERT Design – Bank 113

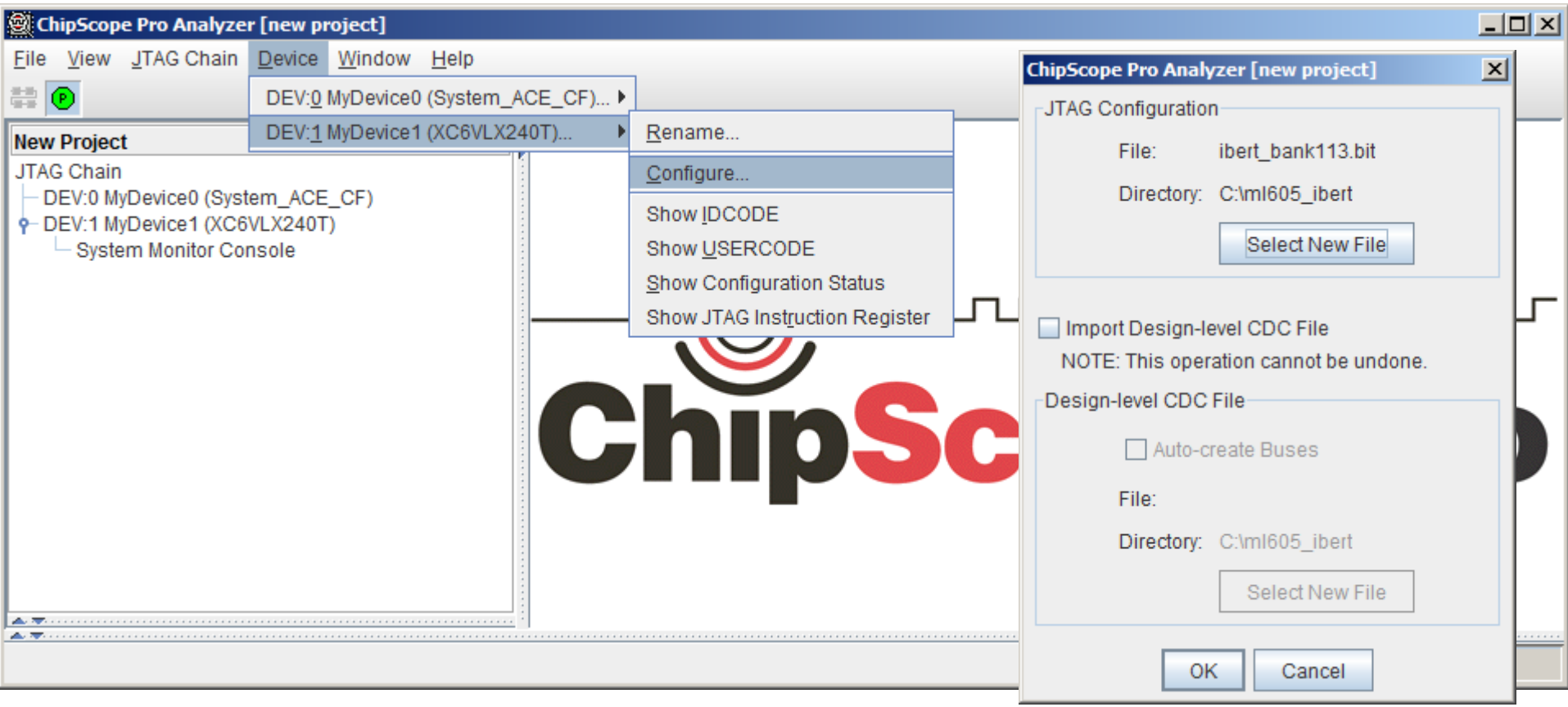
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 113

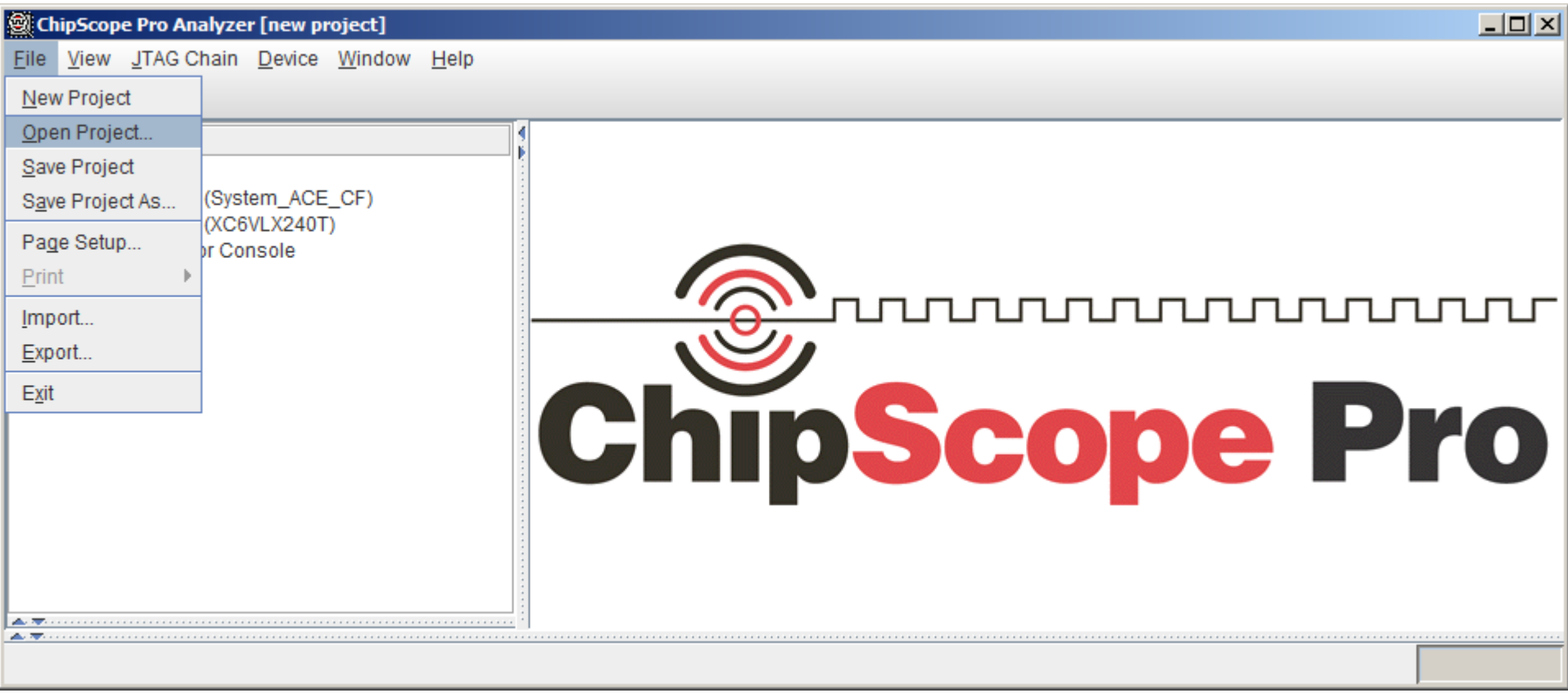
- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure…
- Select <Design Path>\ibert_bank113.bit



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 113

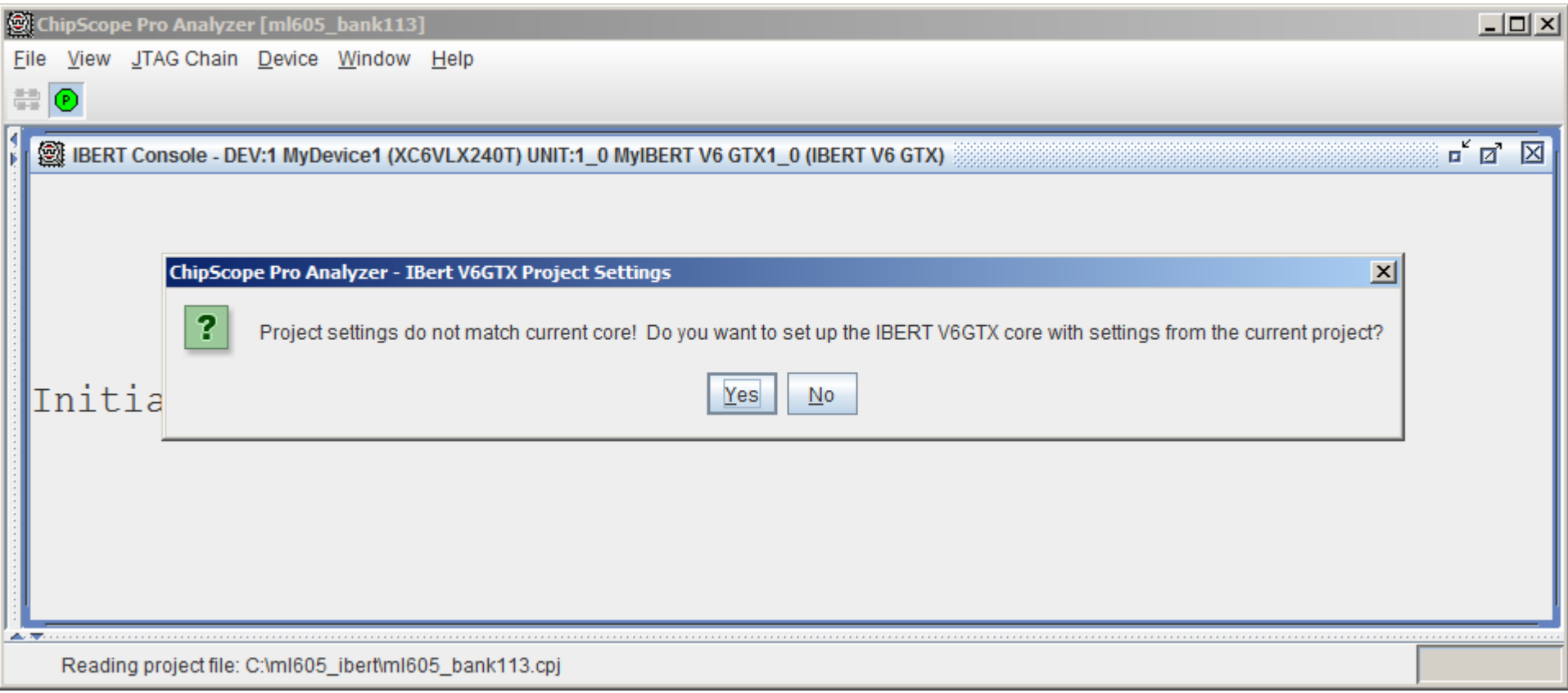
- Select File → Open Project…
- Select <Design Path>\ml605_bank113.cpj



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 113

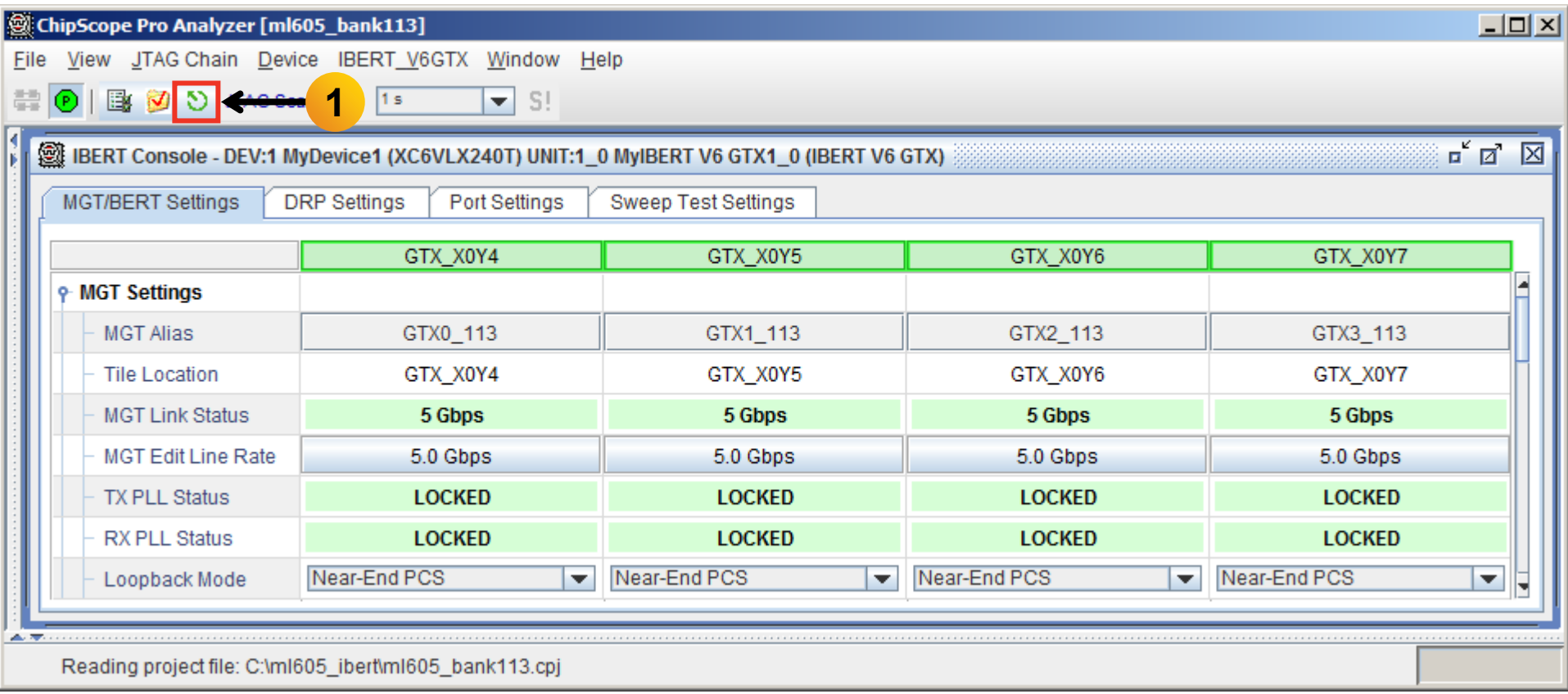
- Click Yes on this Dialog



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 113

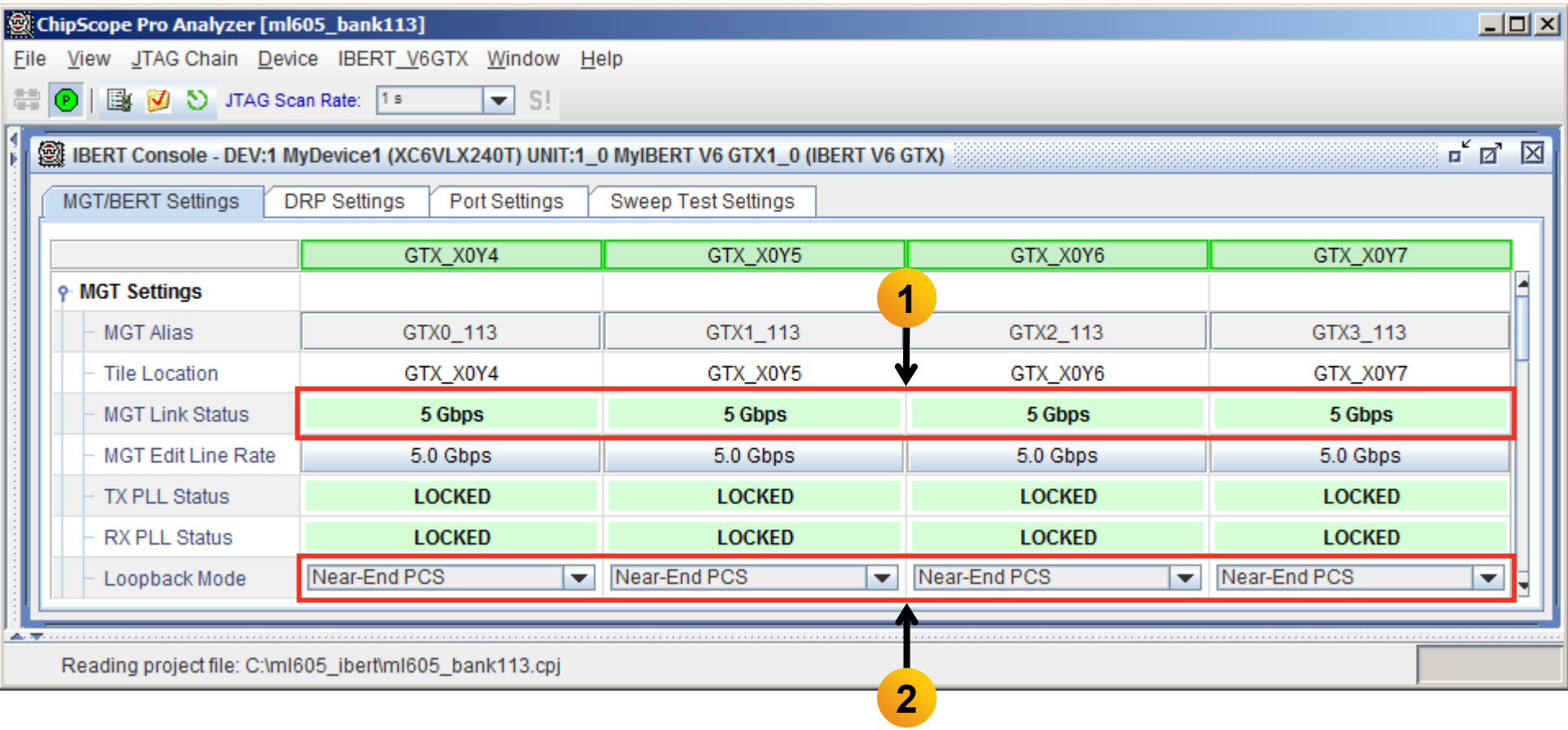
- Select the Reset All button (1)



Note: Bank 113: FMC HPC

Running the ML605 IBERT Design – Bank 113

- The line rate is 5.0 Gbps for all four GTXs (1)
- Near-End PCS is selected for all four GTXs (2)



Note: Presentation applies to the ML605

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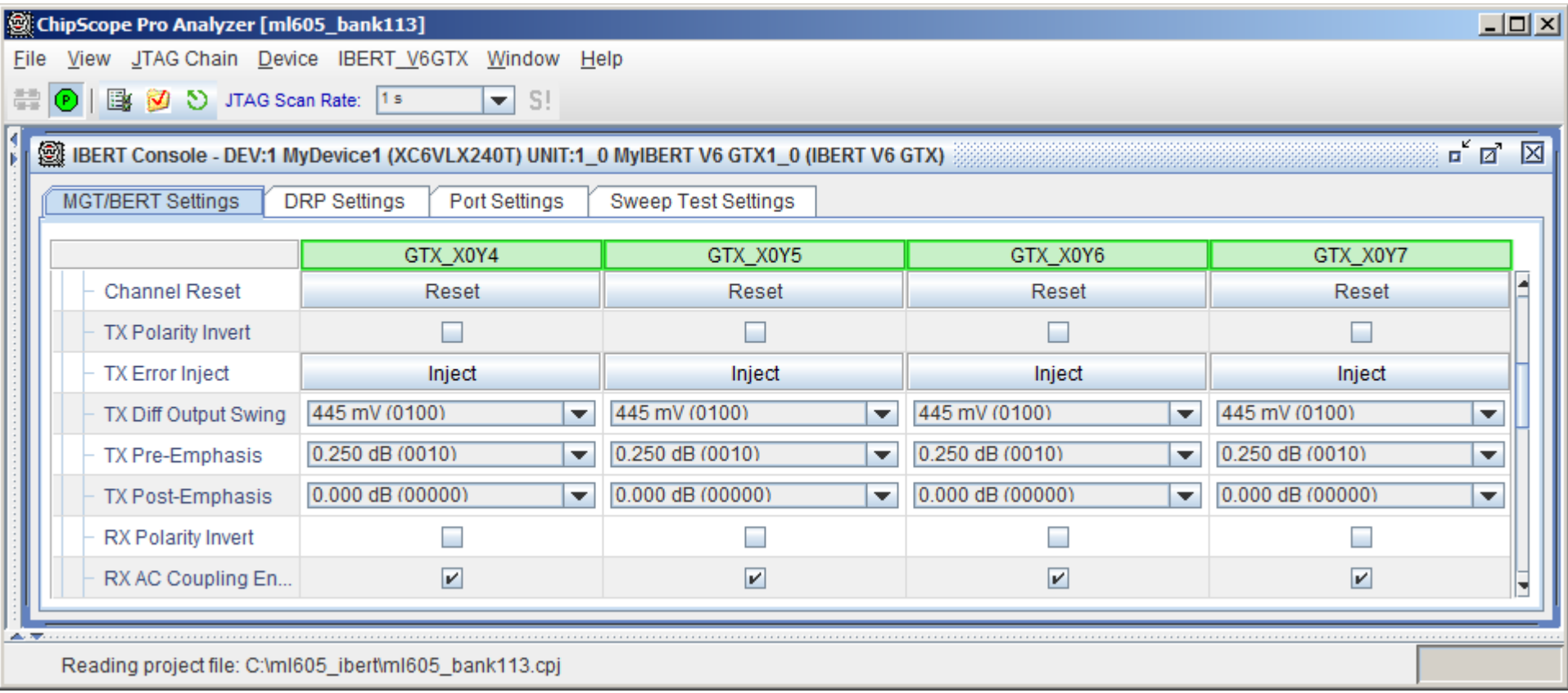
Running the ML605 IBERT Design – Bank 113

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2



Note: Presentation applies to the ML605

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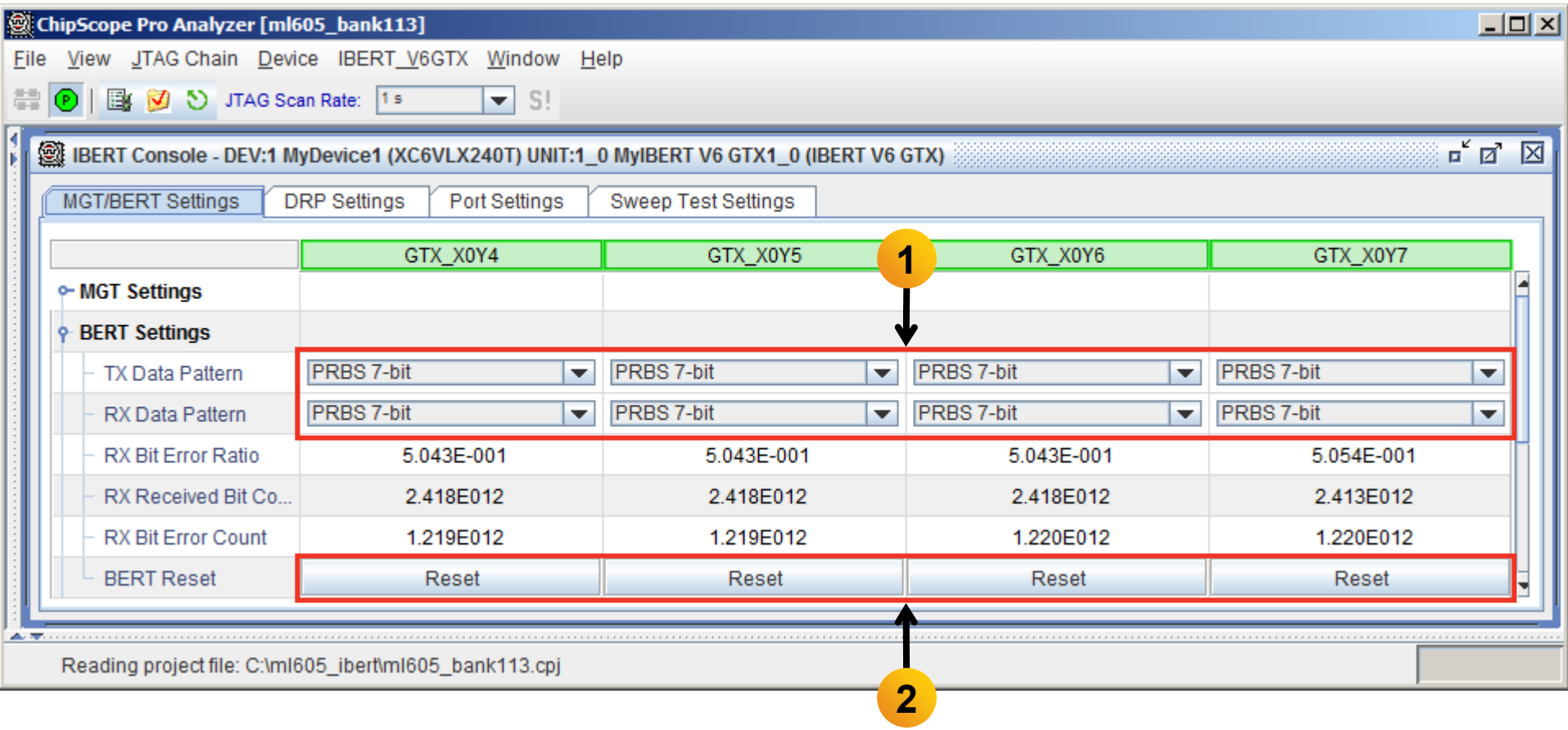
Running the ML605 IBERT Design – Bank 113

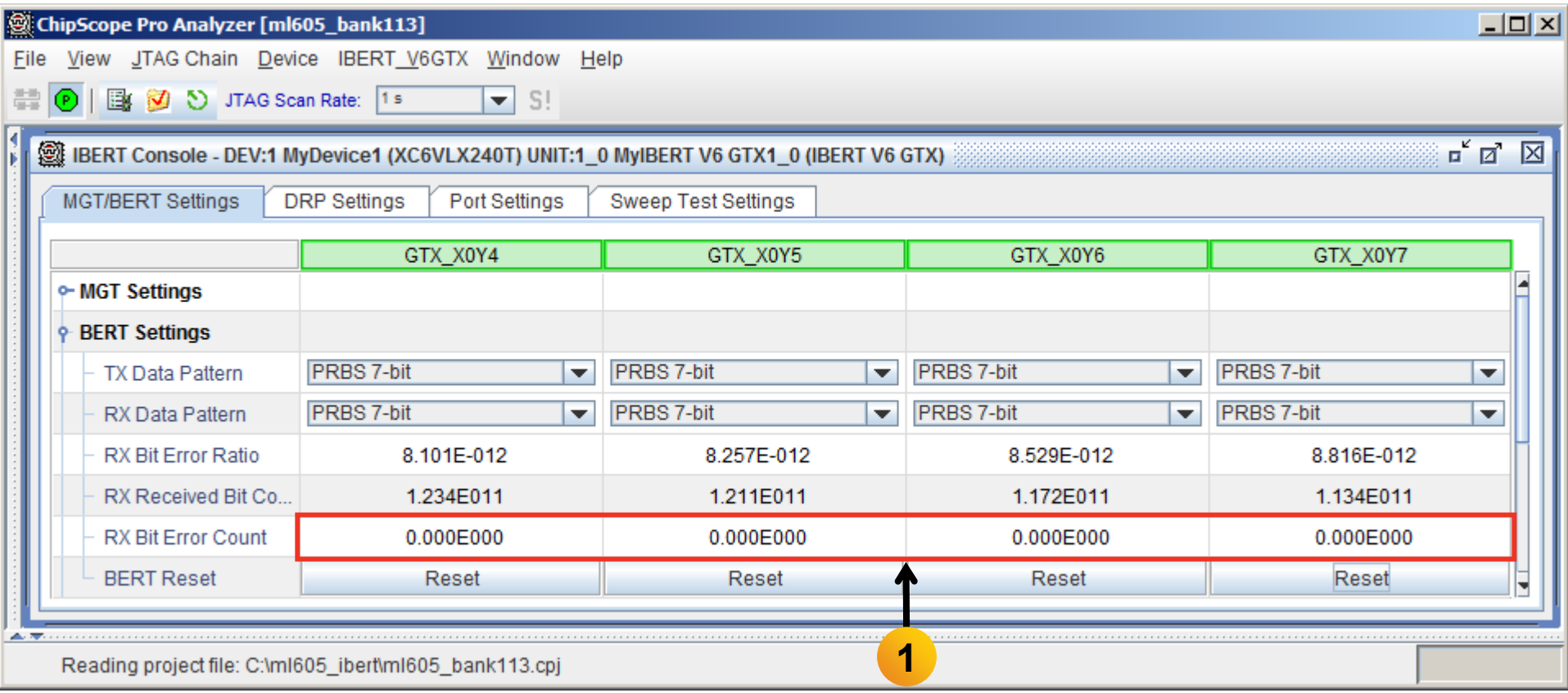
- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 113

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

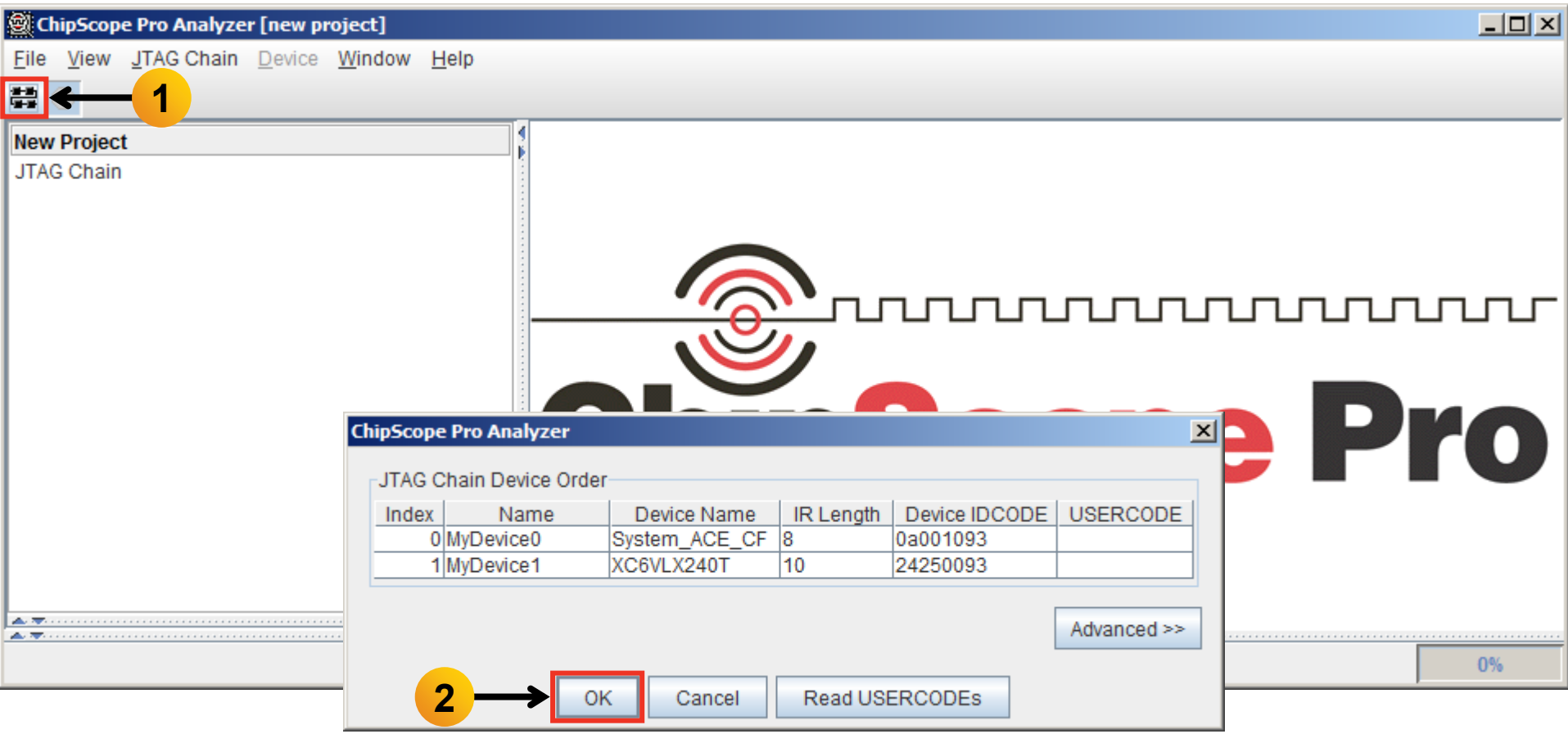


Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

Running the ML605 IBERT Design – Bank 114

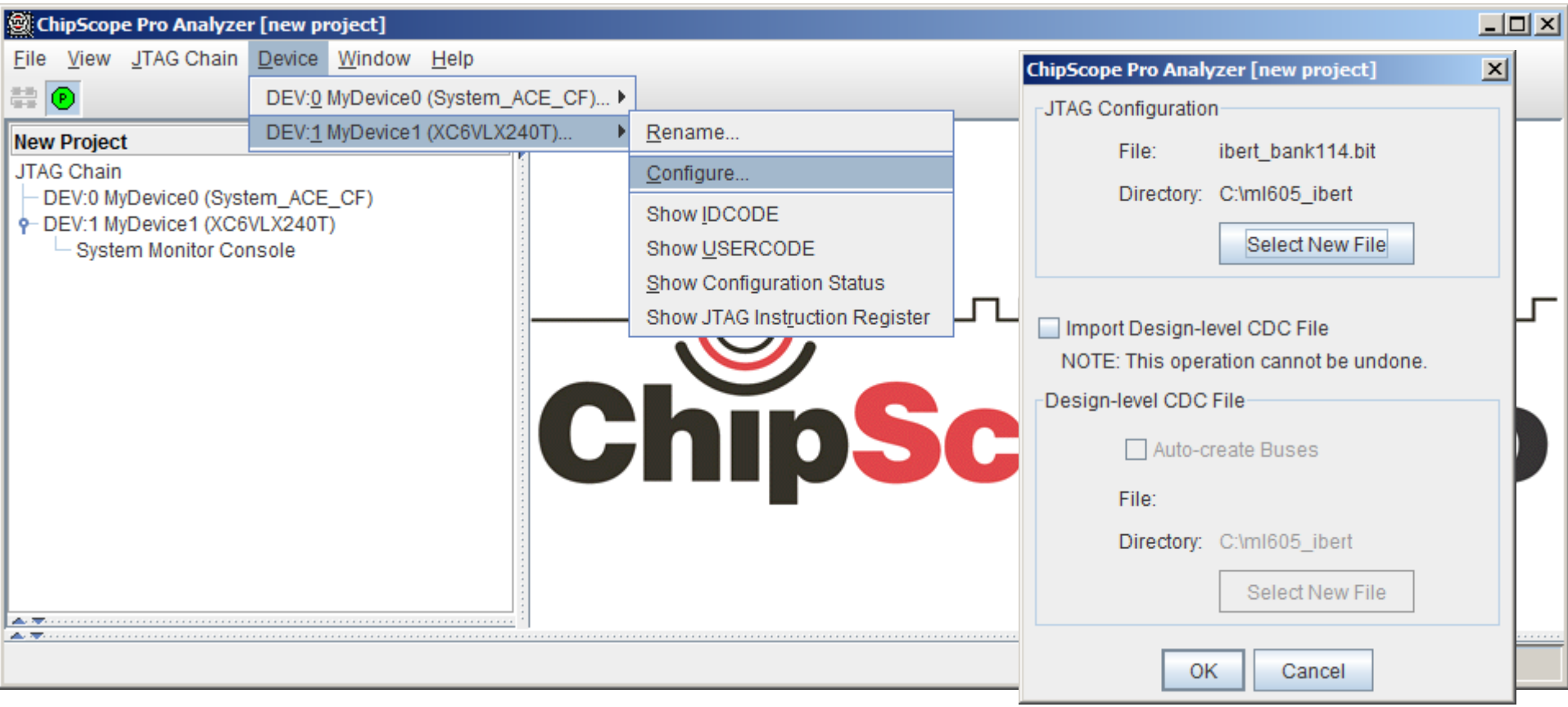
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

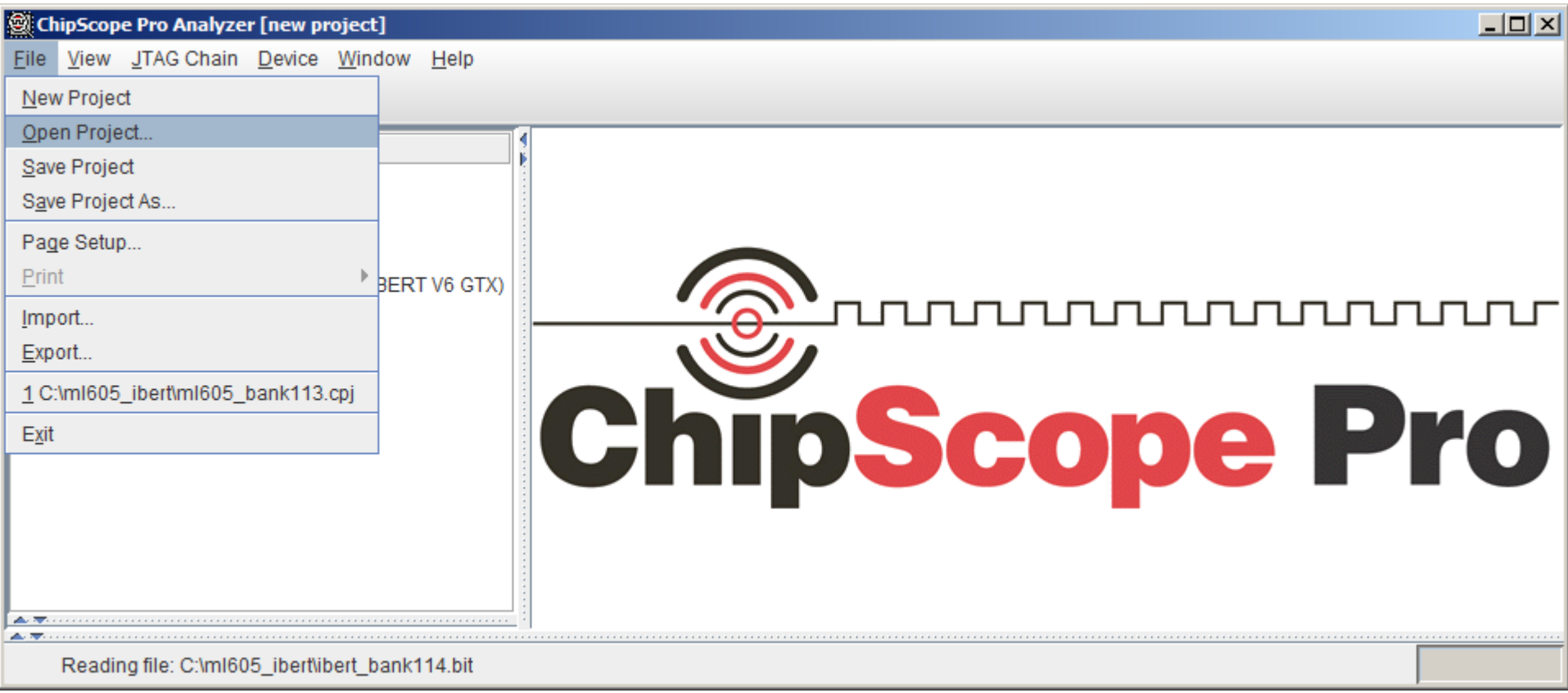
- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure…
- Select <Design Path>\ibert_bank114.bit



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

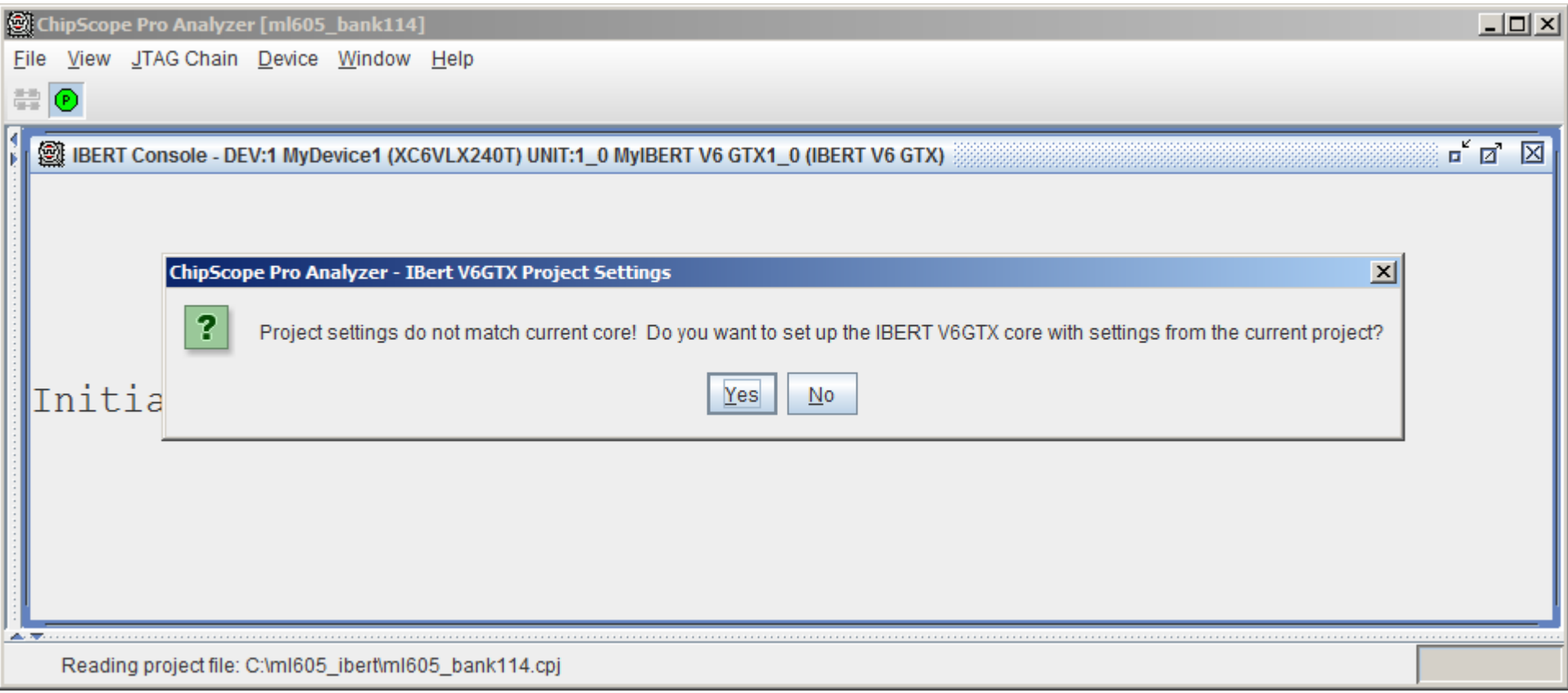
- Select File → Open Project…
- Select <Design Path>\ml605_bank114.cpj



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

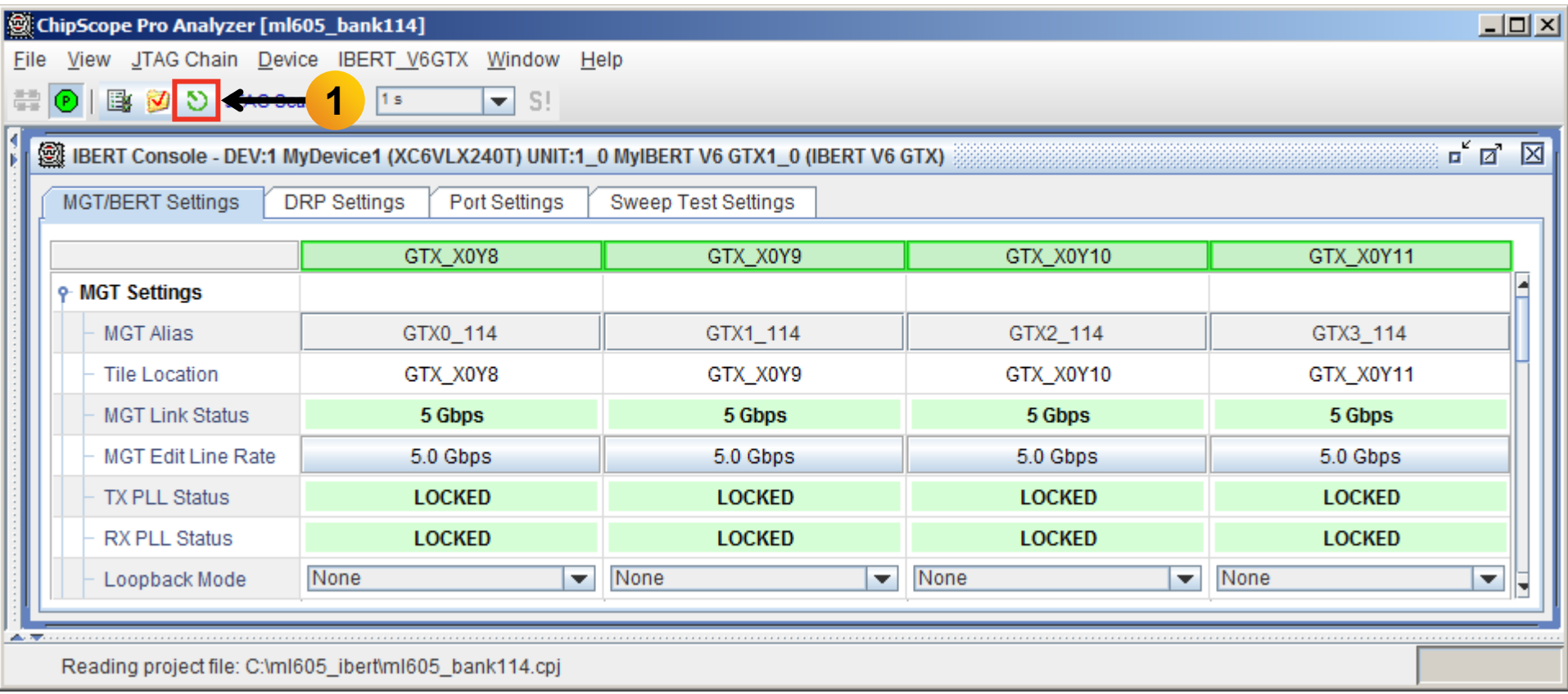
- Click Yes on this Dialog



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

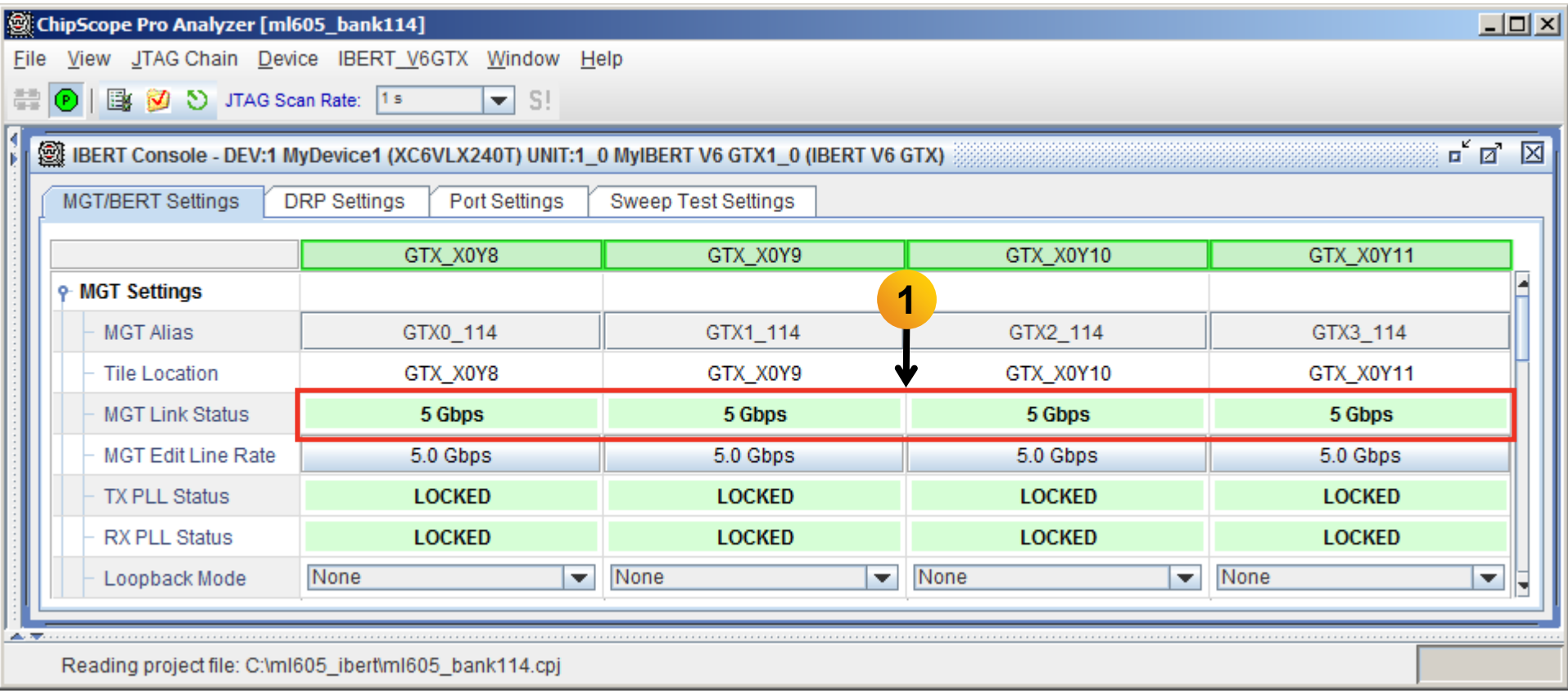
- Select the Reset All button (1)



Note: Bank 114: PCIe

Running the ML605 IBERT Design – Bank 114

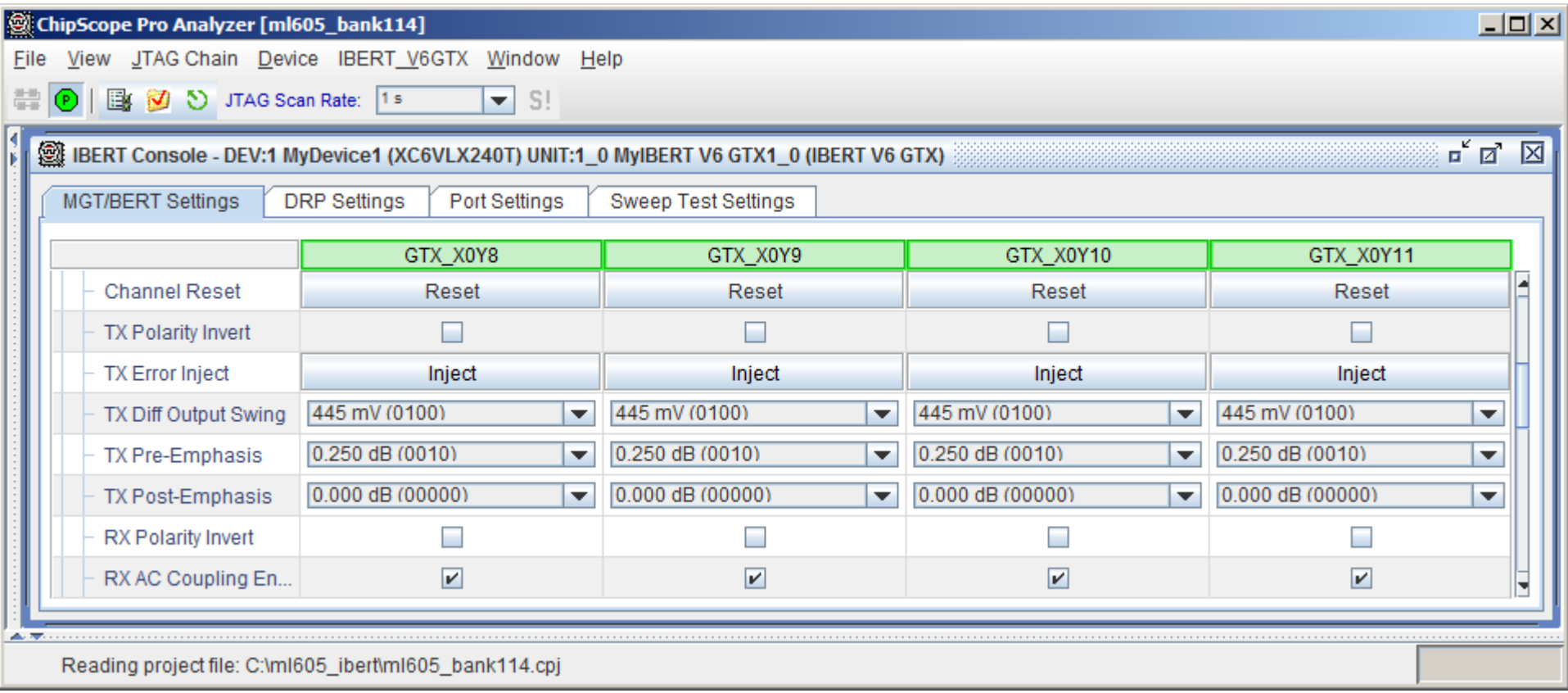
- The line rate is 5.0 Gbps for all four GTXs (1)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2



Note: Presentation applies to the ML605

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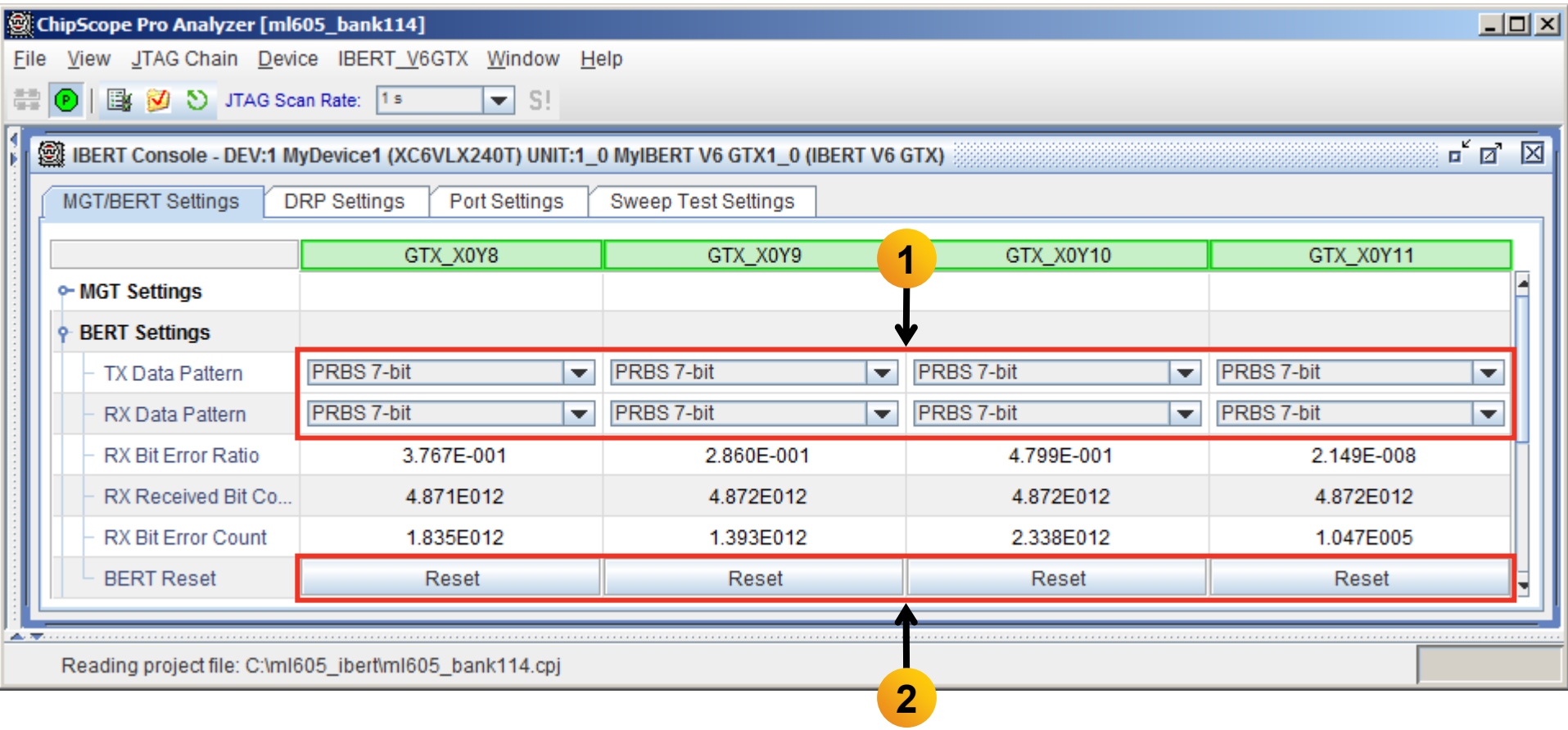
Running the ML605 IBERT Design – Bank 114

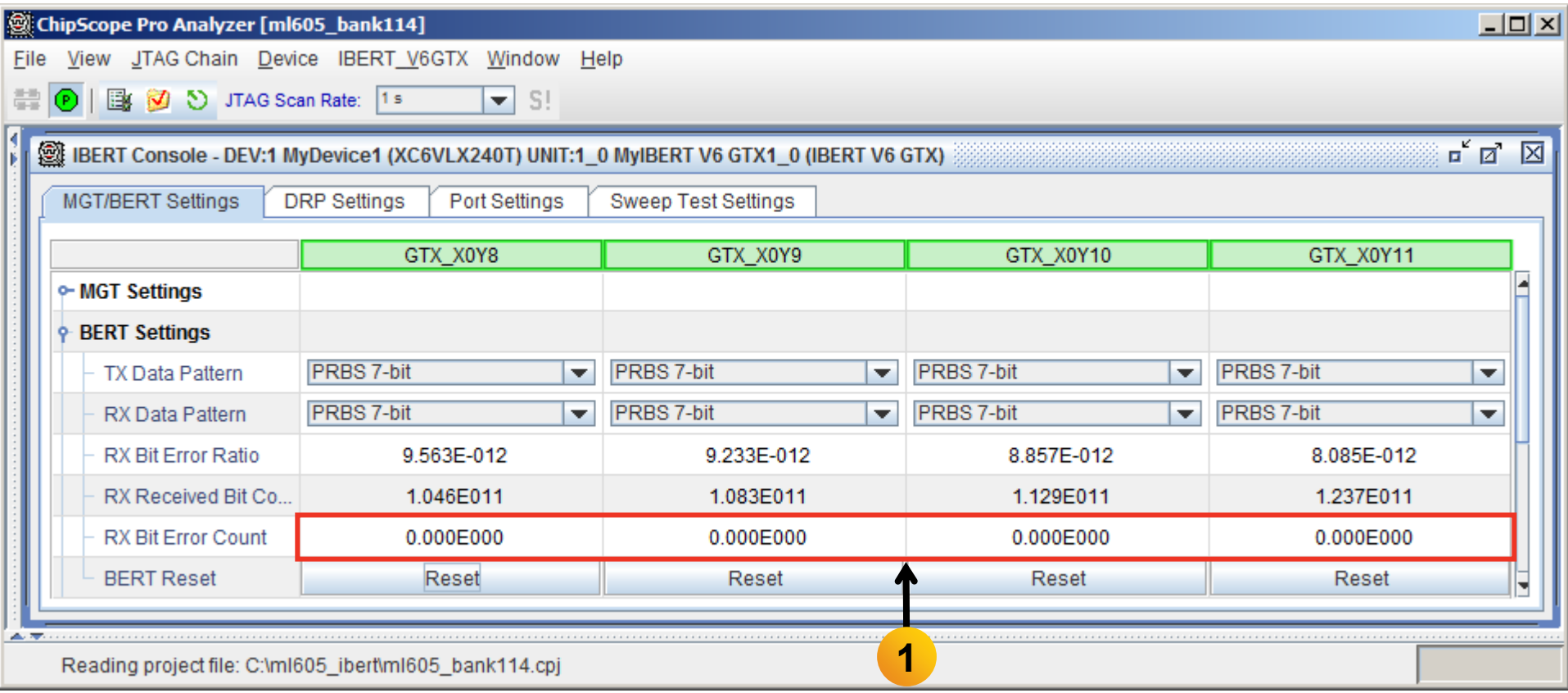
- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 114

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

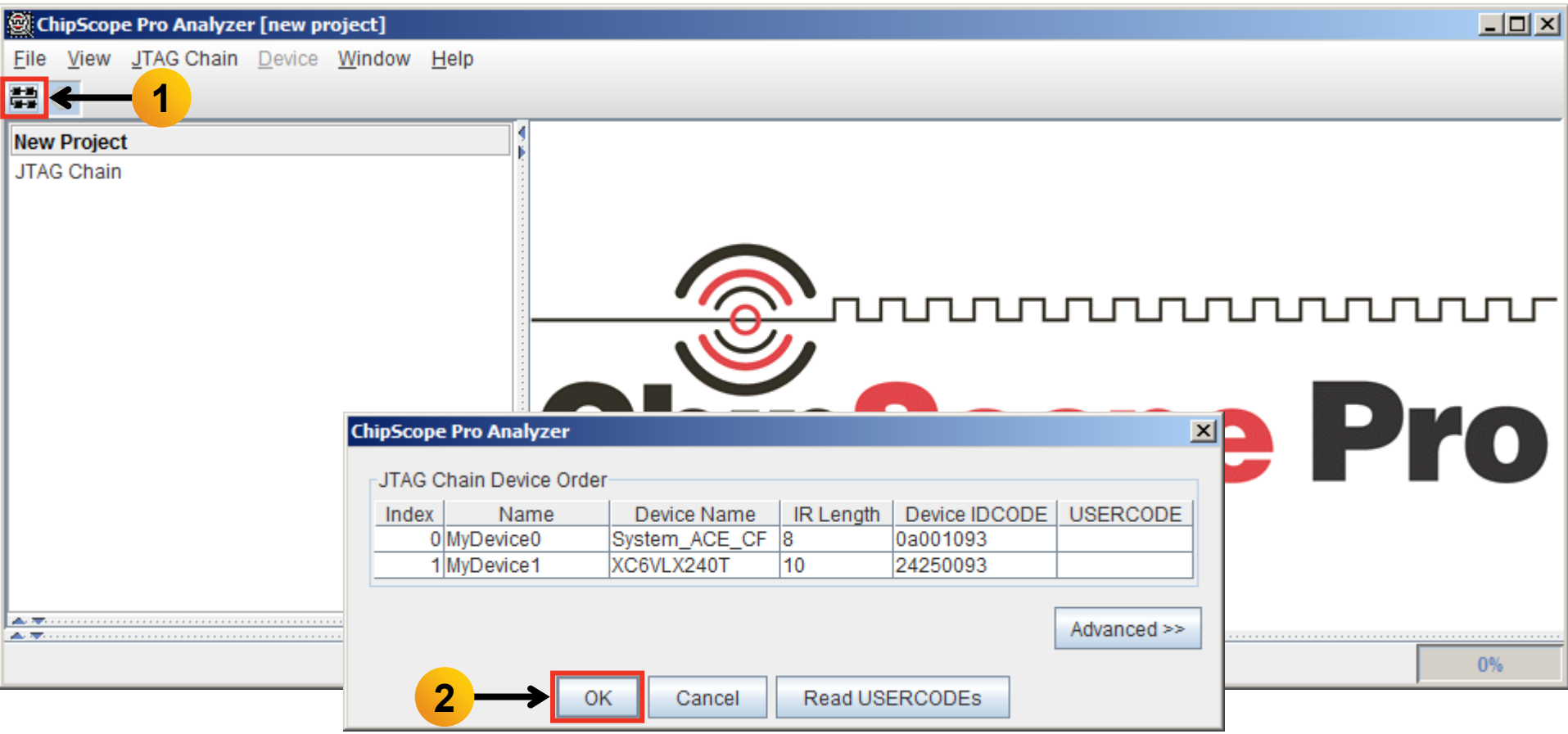


Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 115

Running the ML605 IBERT Design – Bank 115

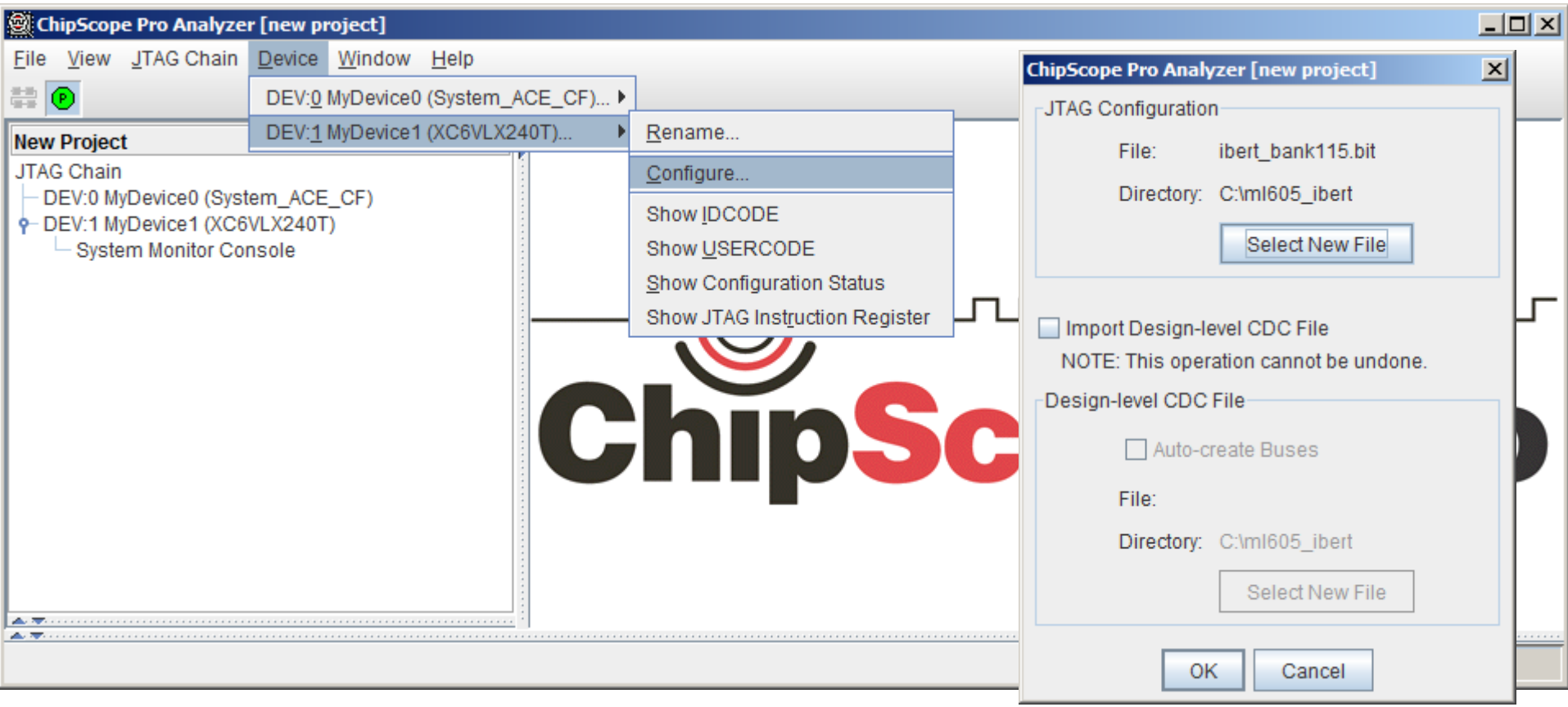
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 115

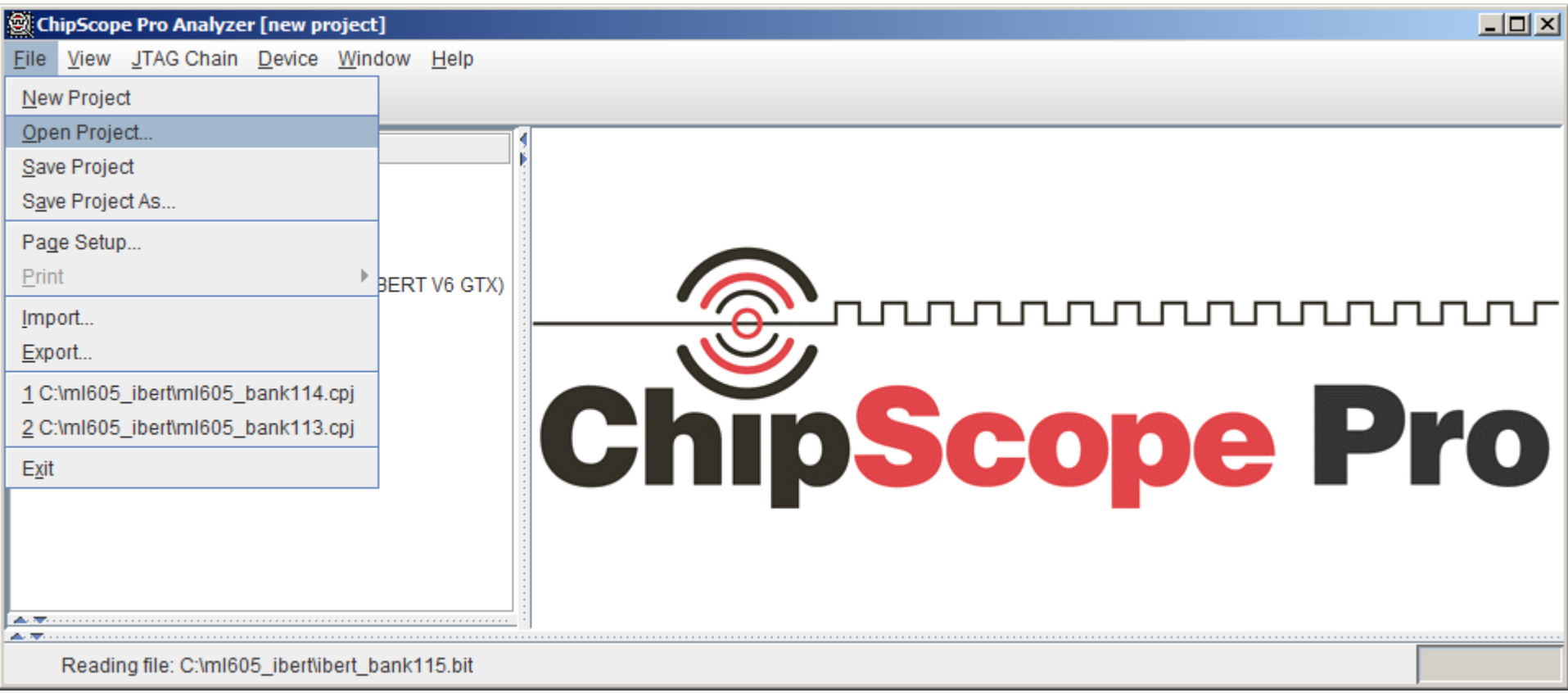
- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure…
- Select <Design Path>\ibert_bank115.bit



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 115

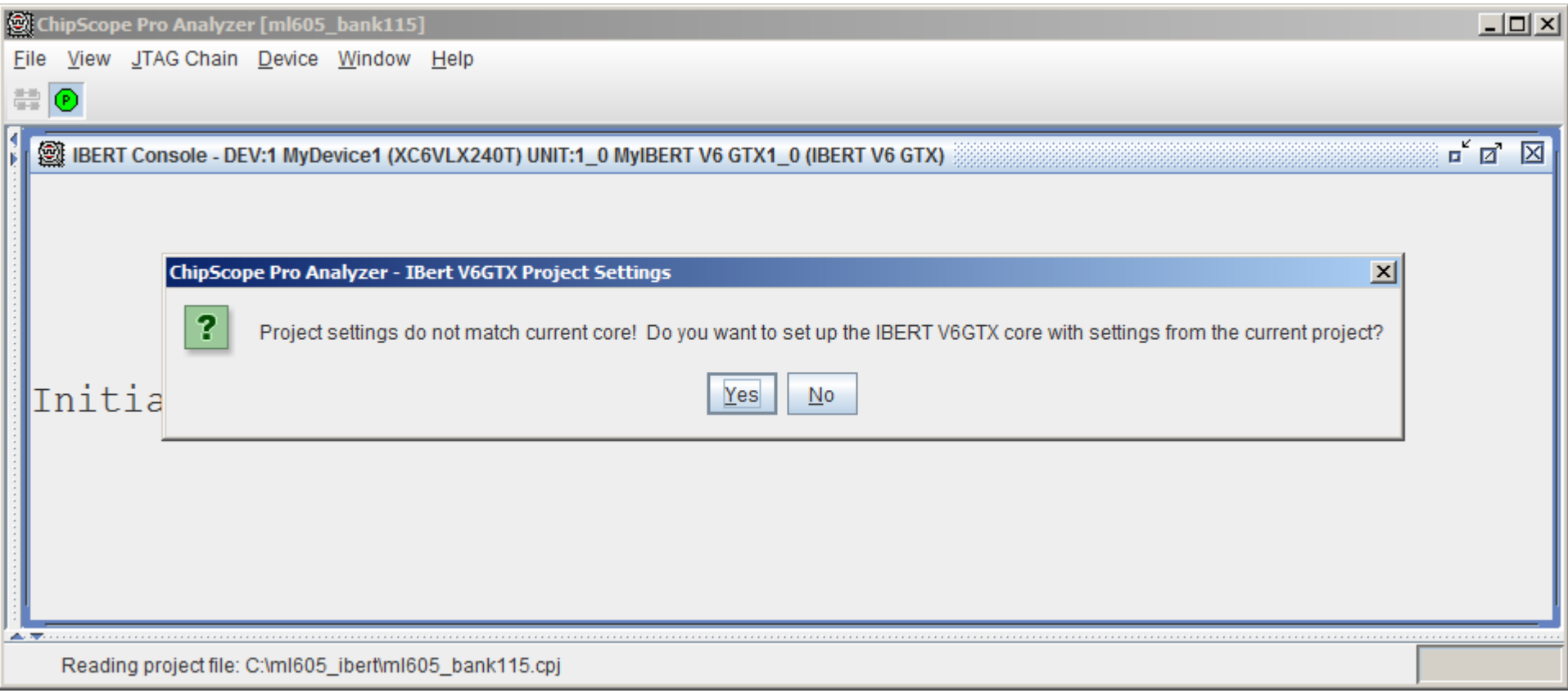
- Select File → Open Project…
- Select <Design Path>\ml605_bank115.cpj



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 115

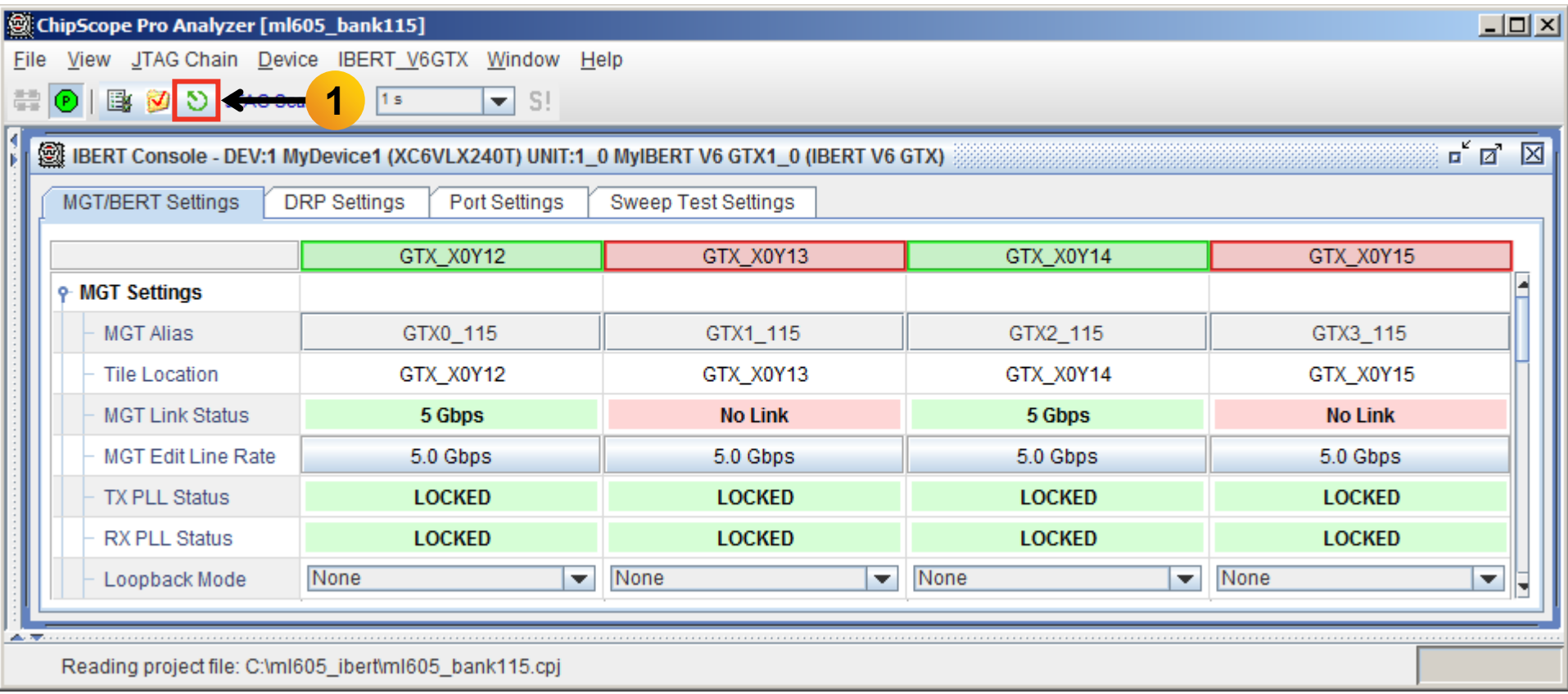
- Click Yes on this Dialog



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 115

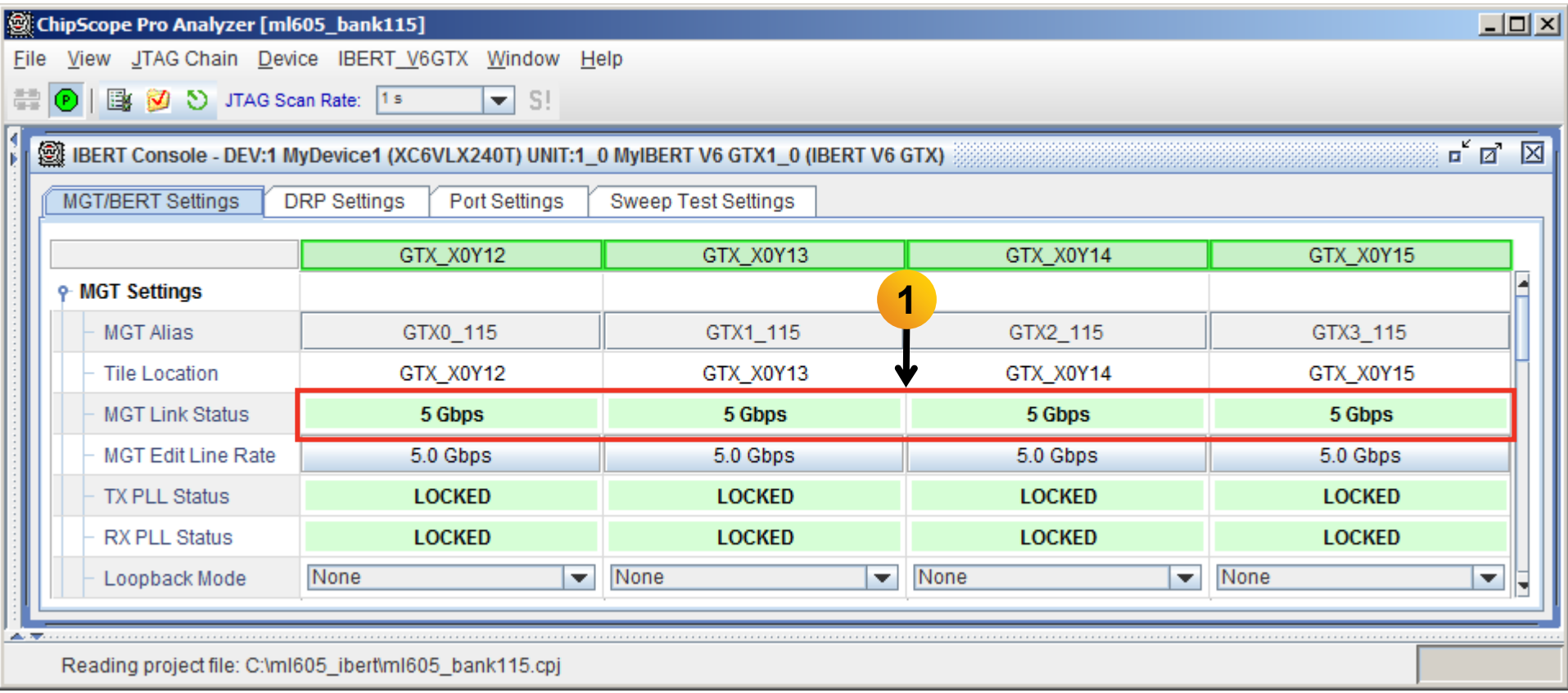
- Select the Reset All button (1)



Note: Bank 115: PCIe

Running the ML605 IBERT Design – Bank 115

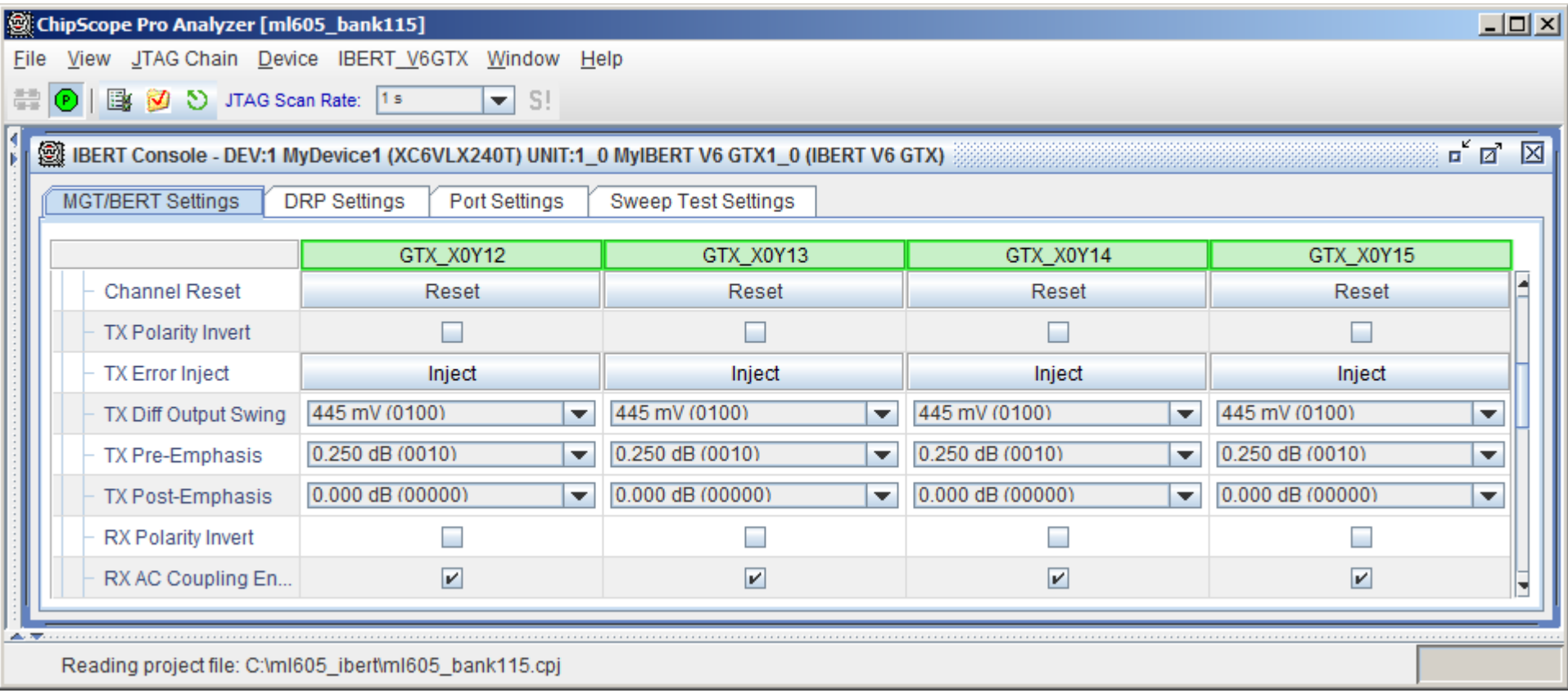
- The line rate is 5 Gbps for all four GTXs (1)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 115

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

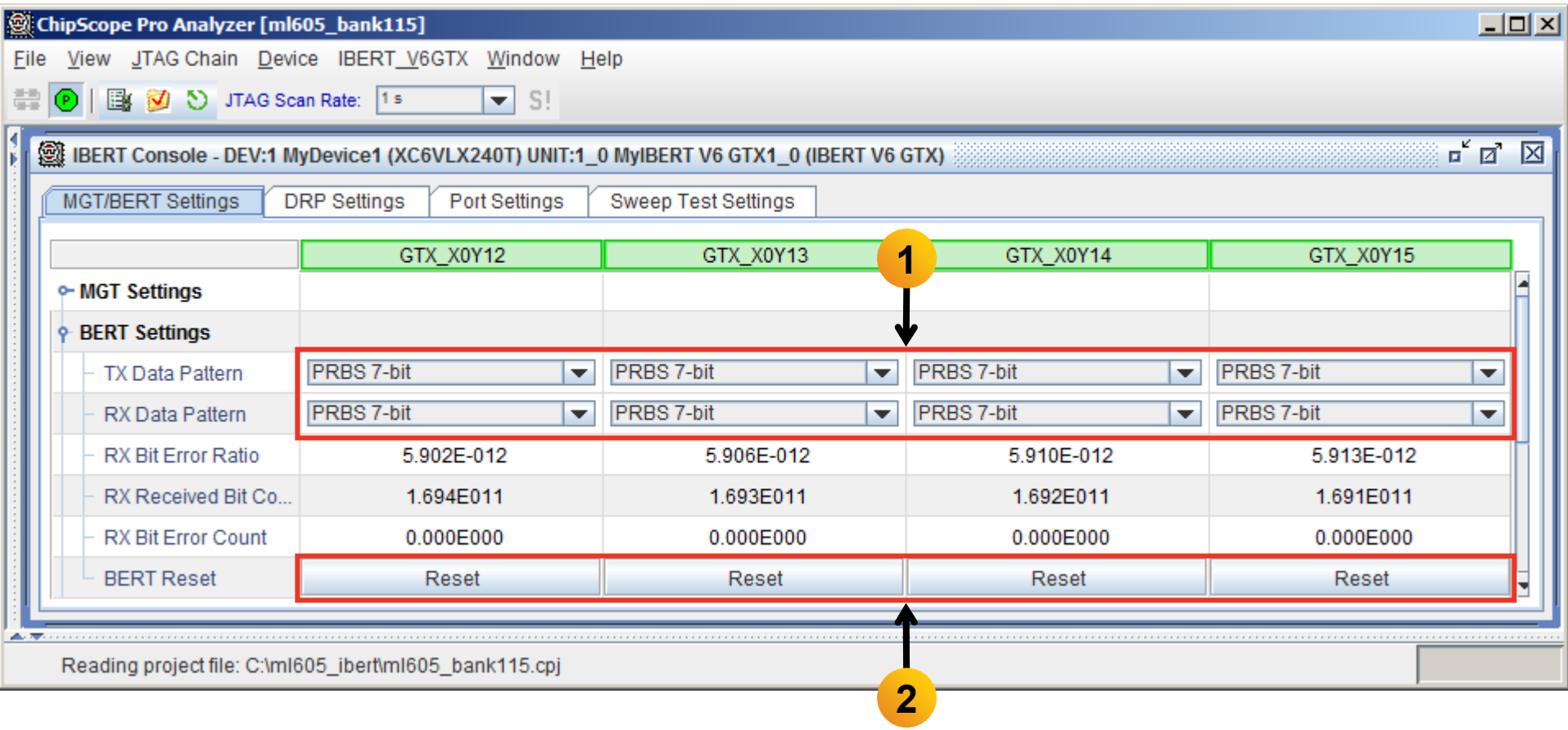


Note: Presentation applies to the ML605

XILINX®

Running the ML605 IBERT Design – Bank 115

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

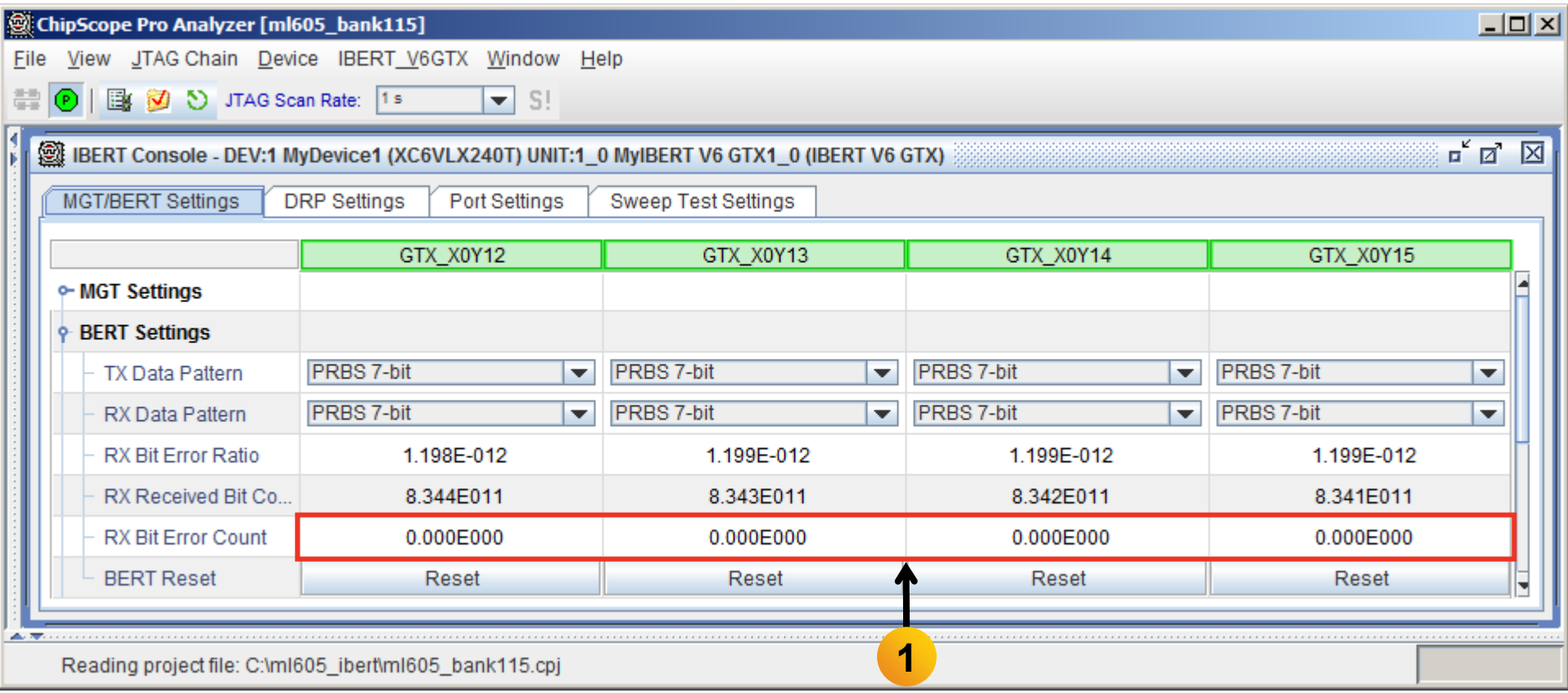


Note: Presentation applies to the ML605

XILINX®

Running the ML605 IBERT Design – Bank 115

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power



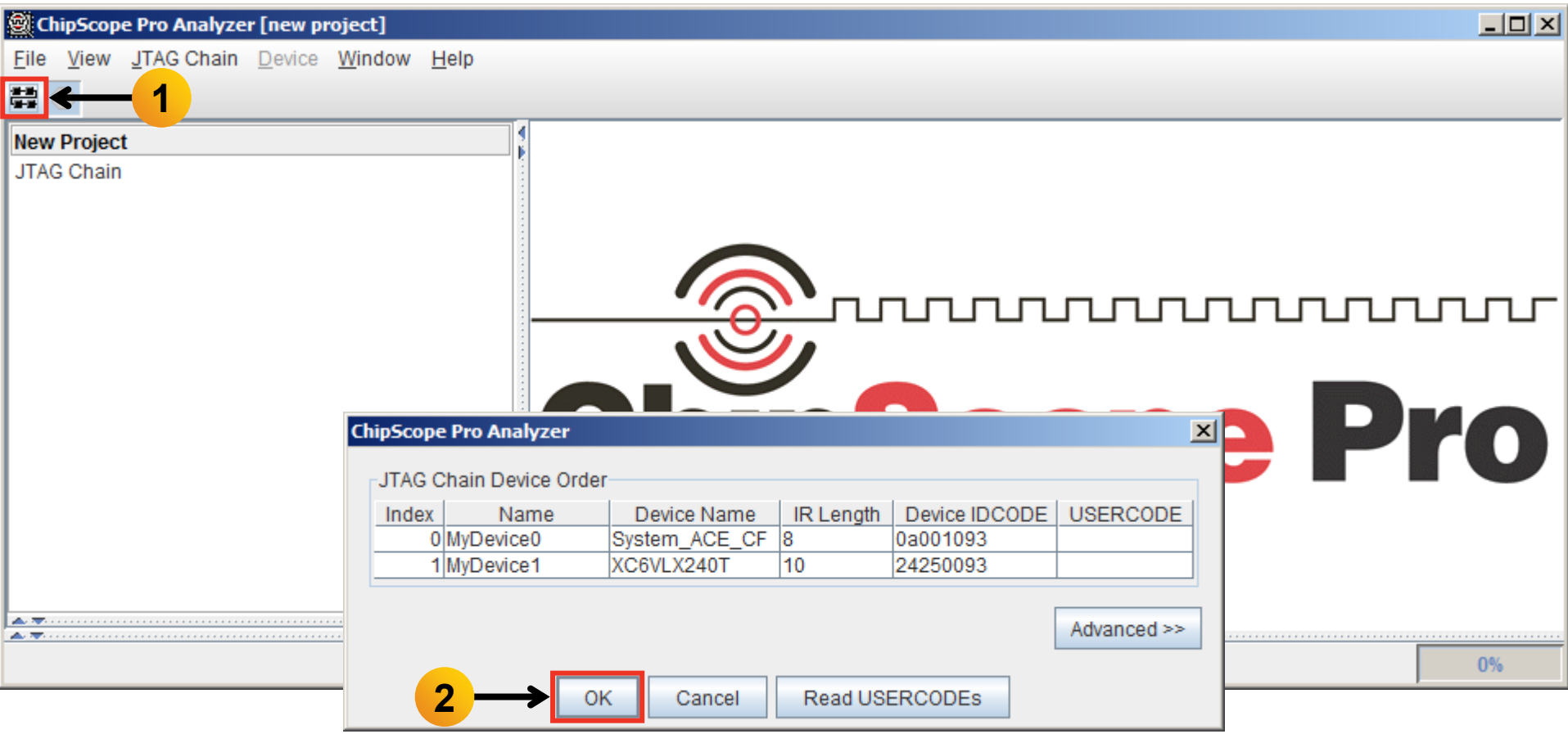
Note: Presentation applies to the ML605

XILINX®

Running the ML605 IBERT Design – Bank 116

Running the ML605 IBERT Design – Bank 116

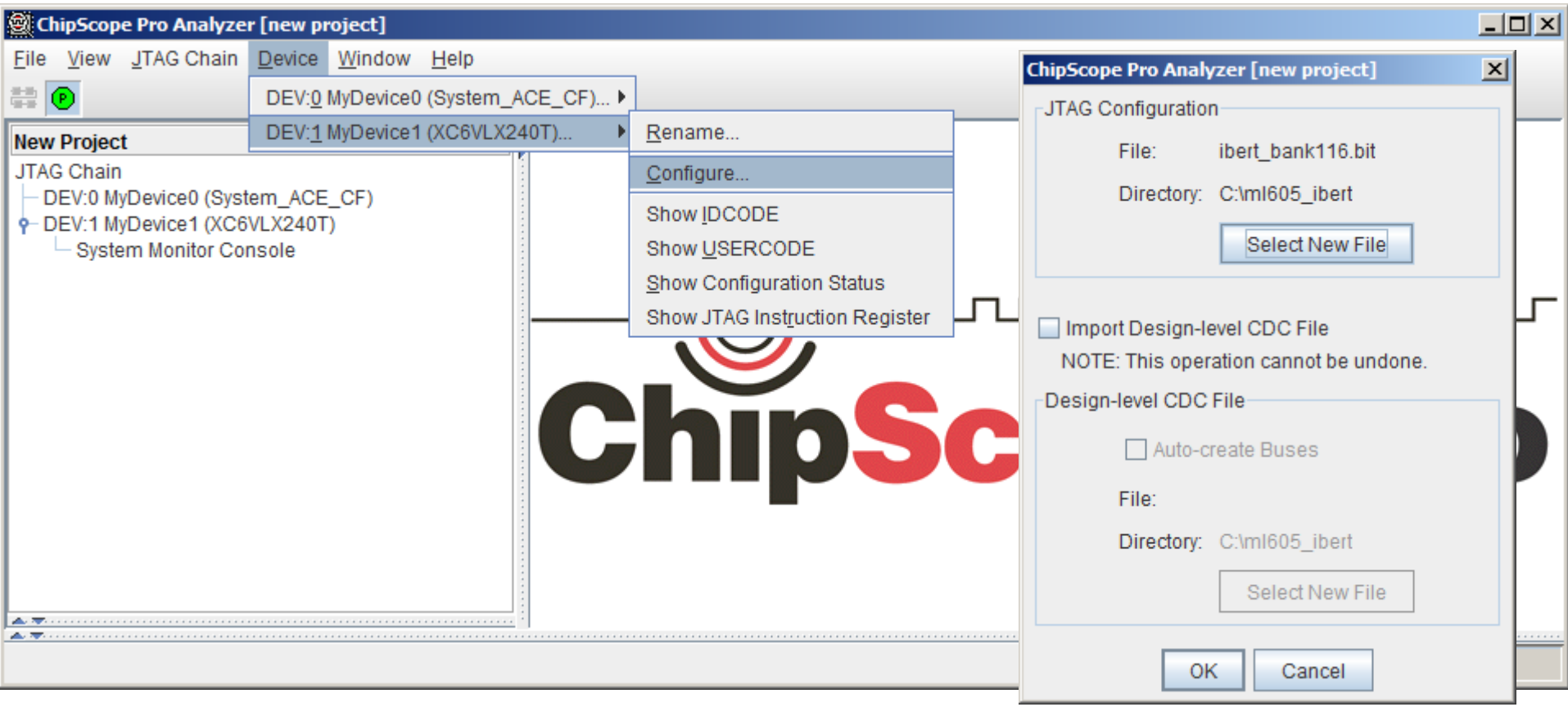
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 116

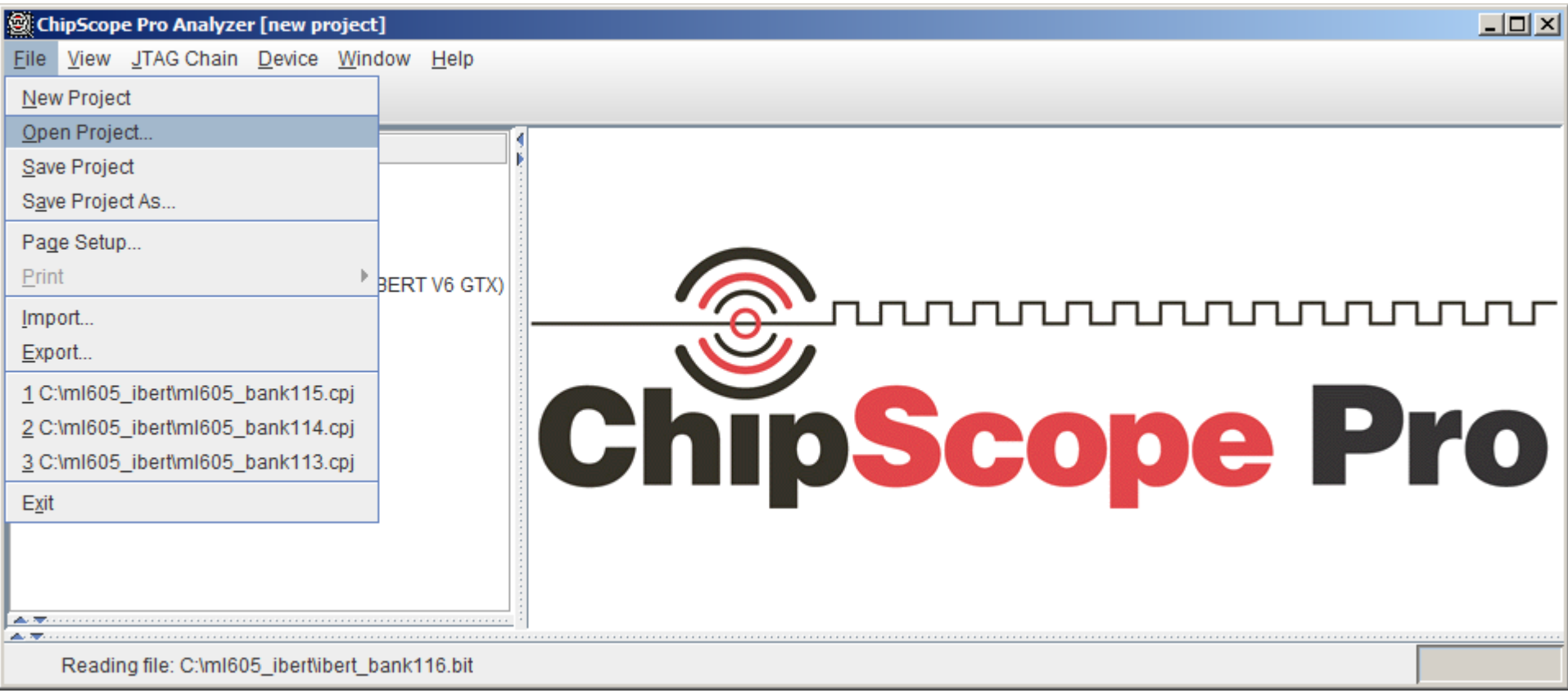
- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure…
- Select <Design Path>\ibert_bank116.bit



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 116

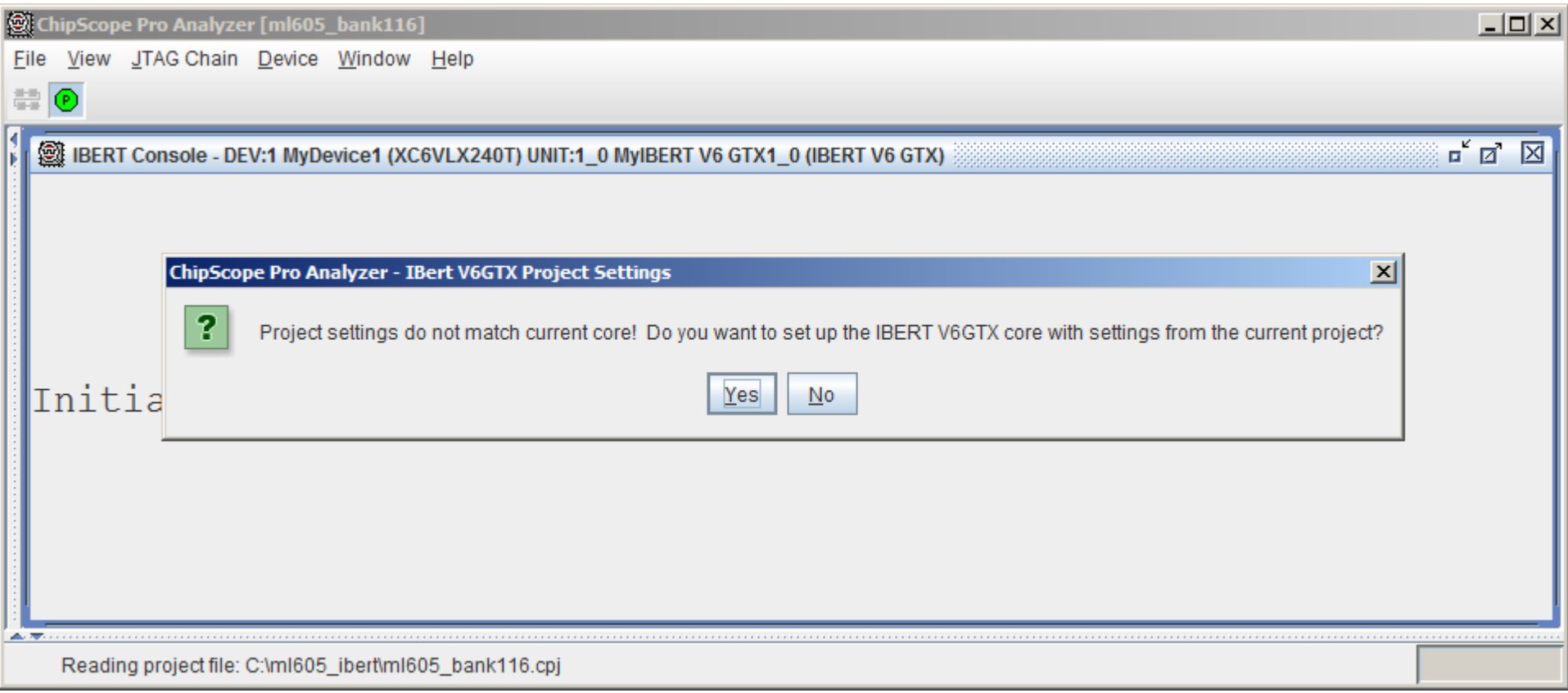
- Select File → Open Project…
- Select <Design Path>\ml605_bank116.cpj



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 116

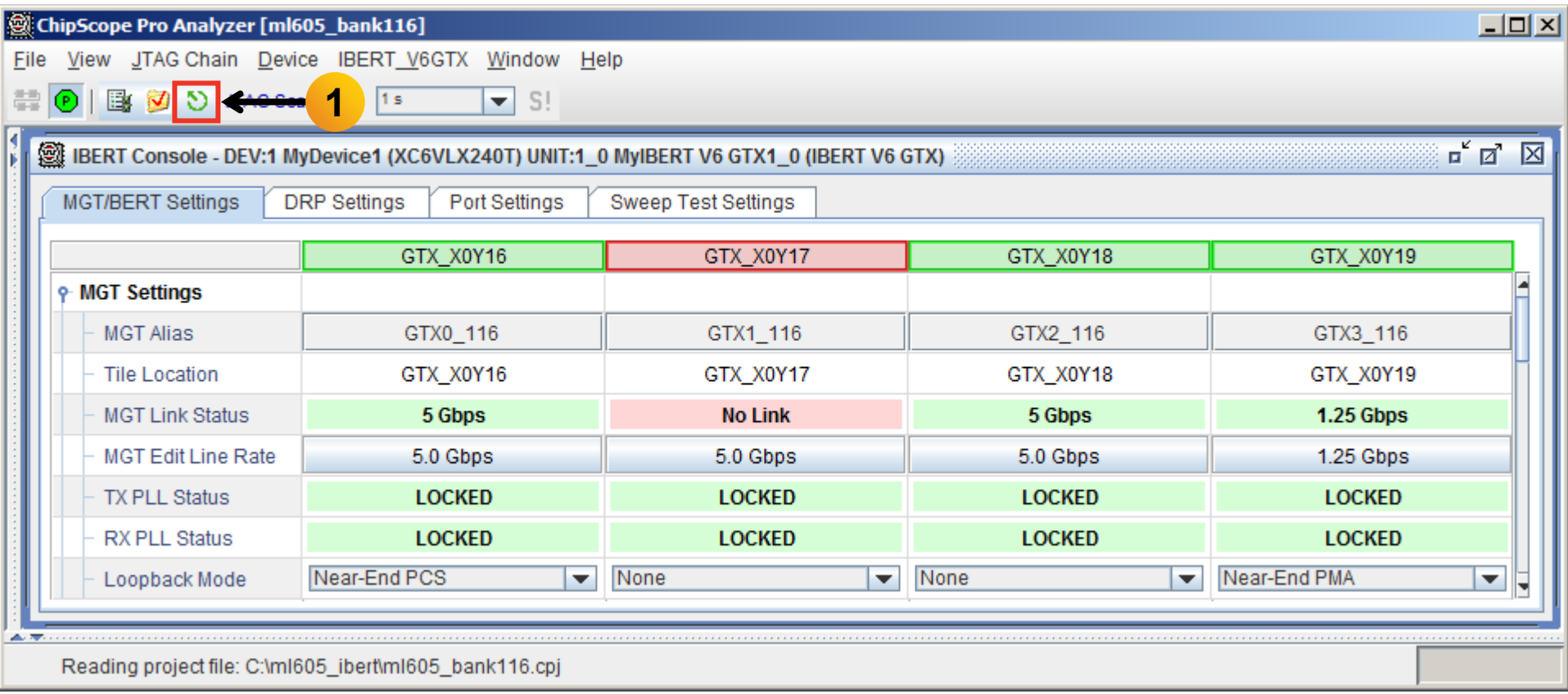
- Click Yes on this Dialog



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 116

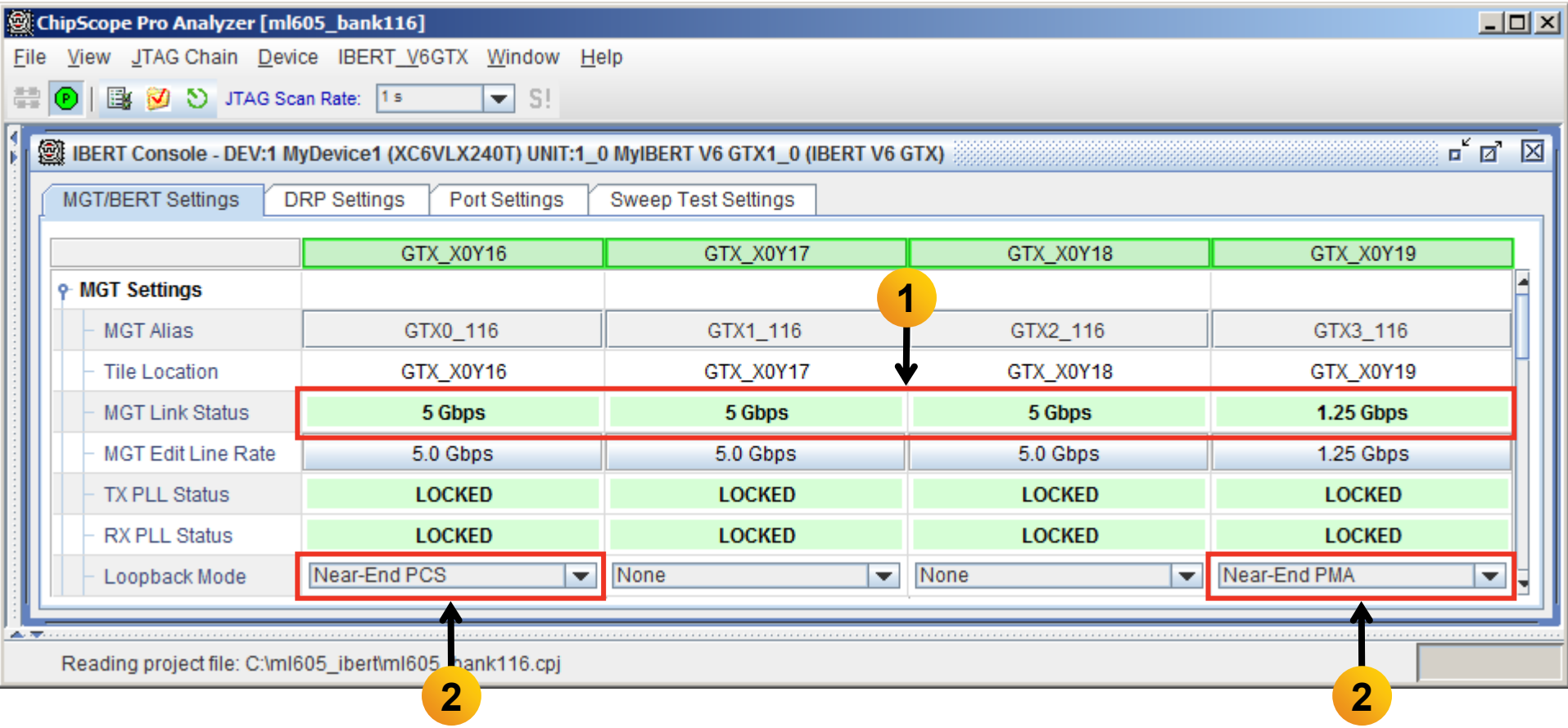
- Select the Reset All button (1)



Note: Bank 116: FMC_LPC, SFP, SMA, SGMII

Running the ML605 IBERT Design – Bank 116

- The line rates are 5.0 and 1.25 Gbps for the four GTXs (1)
- Near-End PCS and PMA is selected for FMC and SGMII (2)

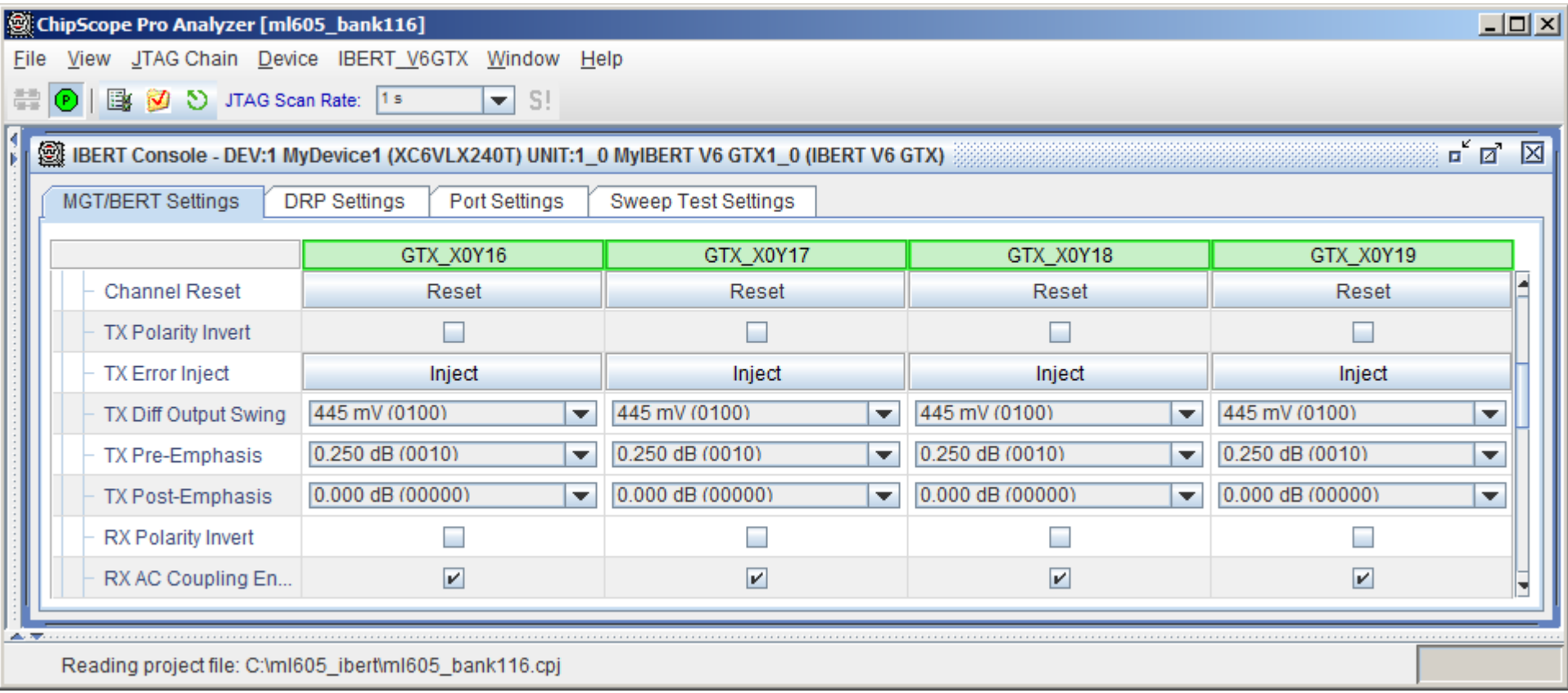


Note: Presentation applies to the ML605

XILINX®

Running the ML605 IBERT Design – Bank 116

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

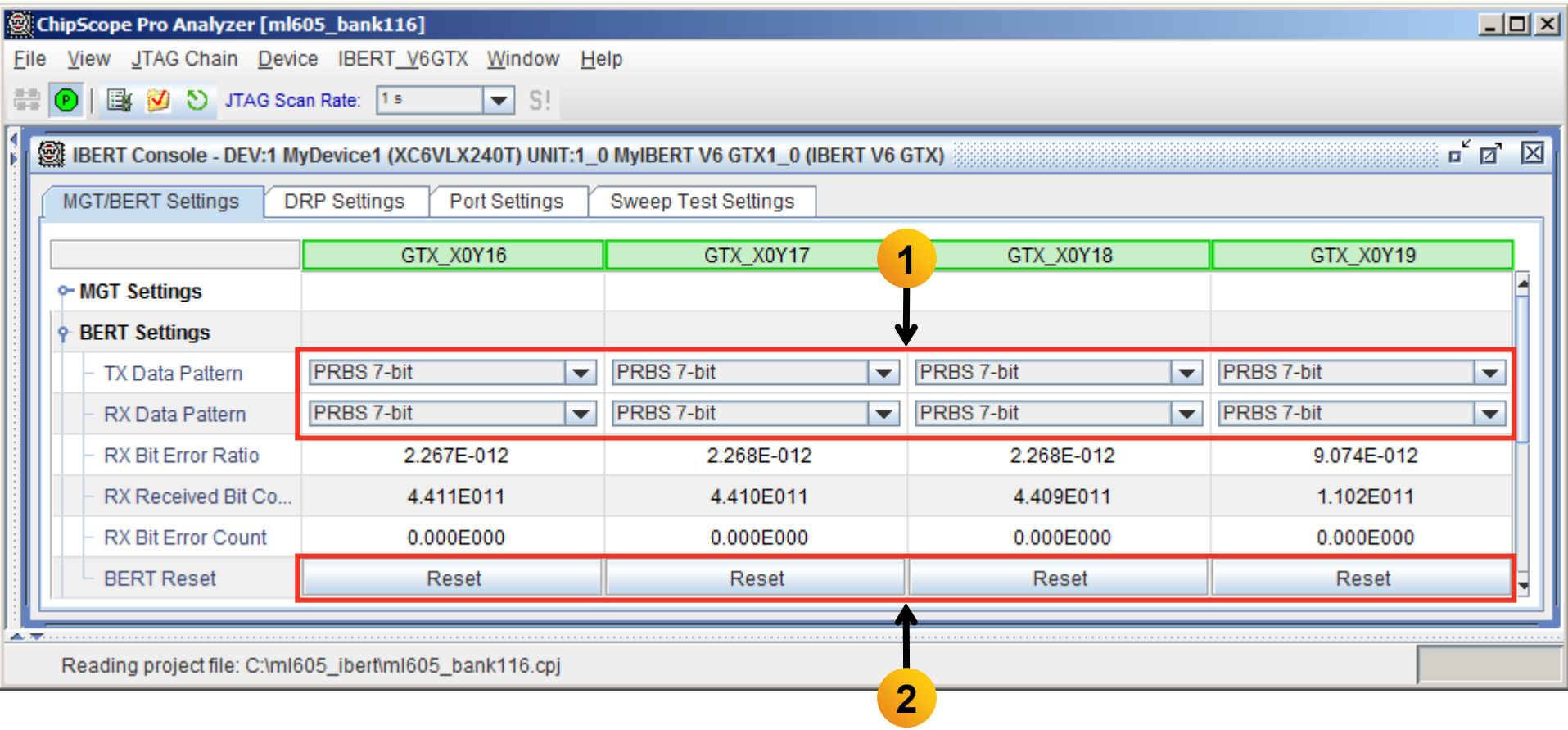


Note: Presentation applies to the ML605

XILINX®

Running the ML605 IBERT Design – Bank 116

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

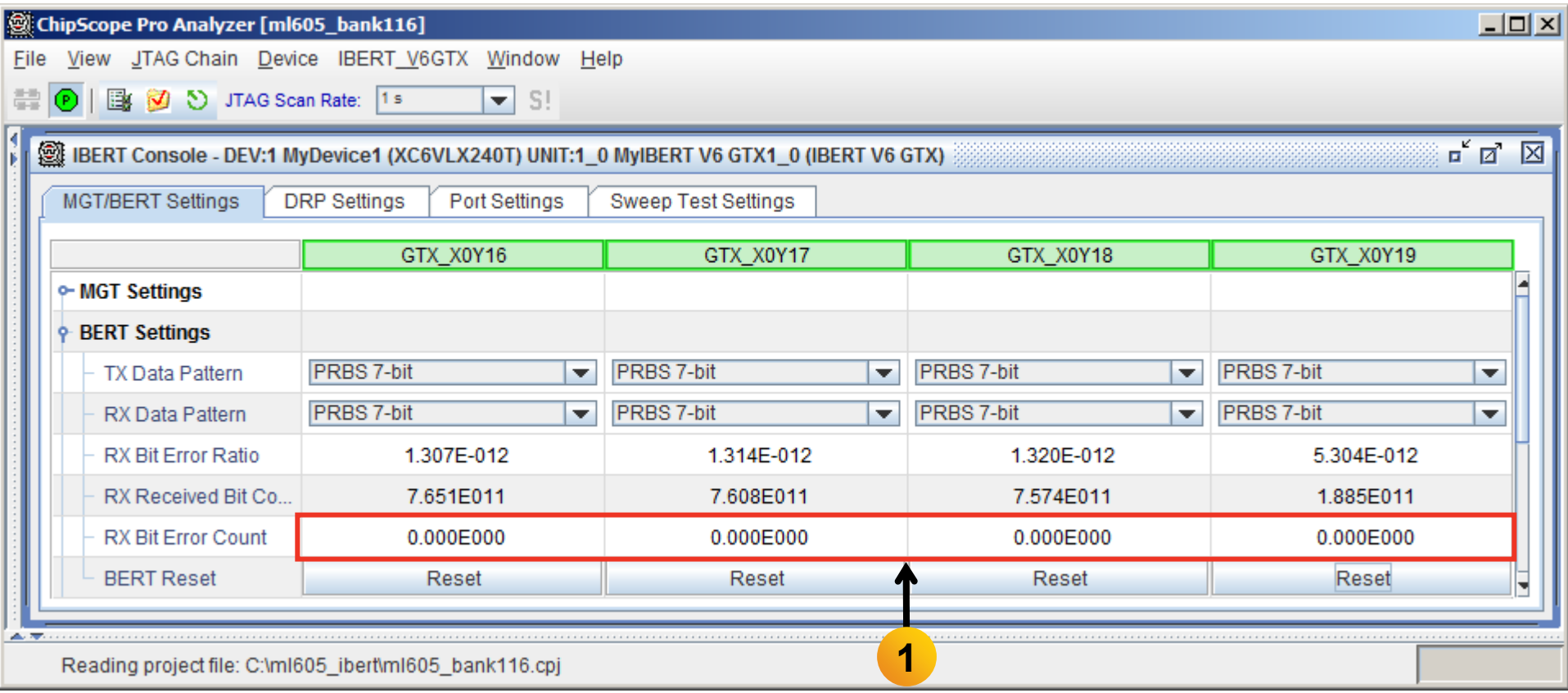


Note: Presentation applies to the ML605

XILINX®

Running the ML605 IBERT Design – Bank 116

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power



Note: Presentation applies to the ML605

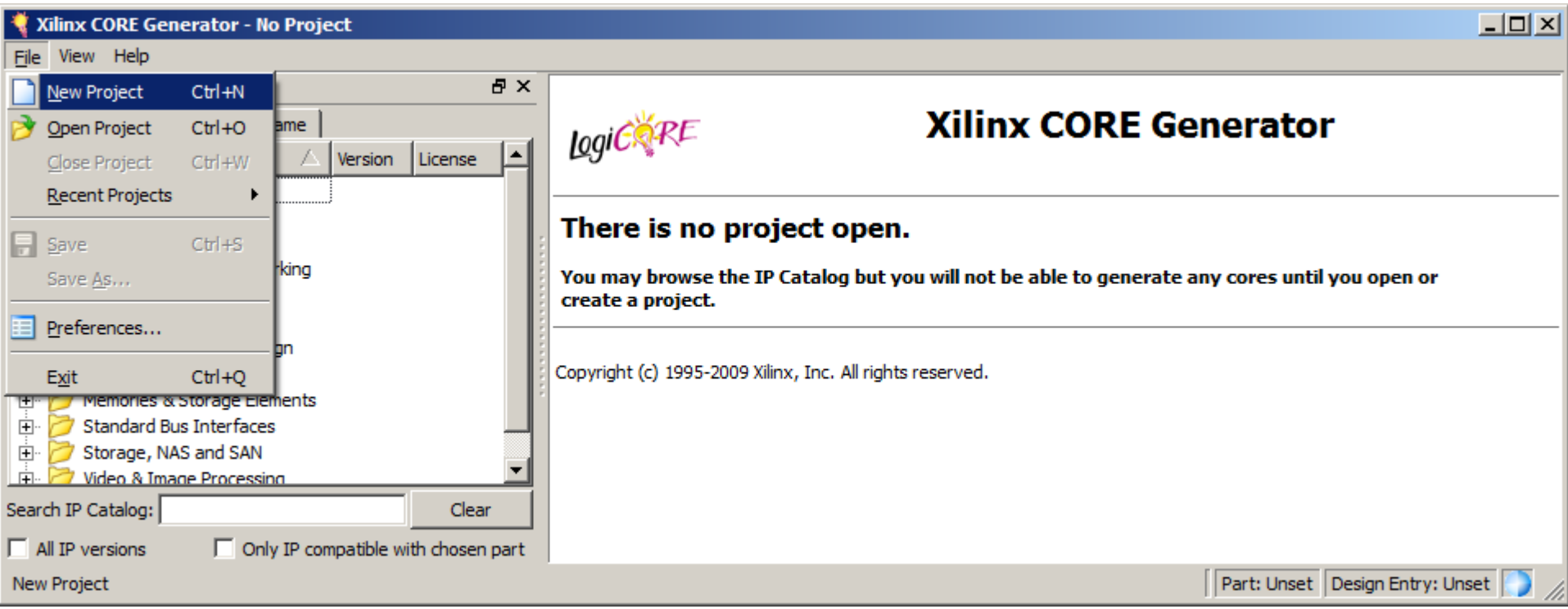
ML605 IBERT Design Creation

Create IBERT CORE Generator Project

- **Open the CORE Generator**

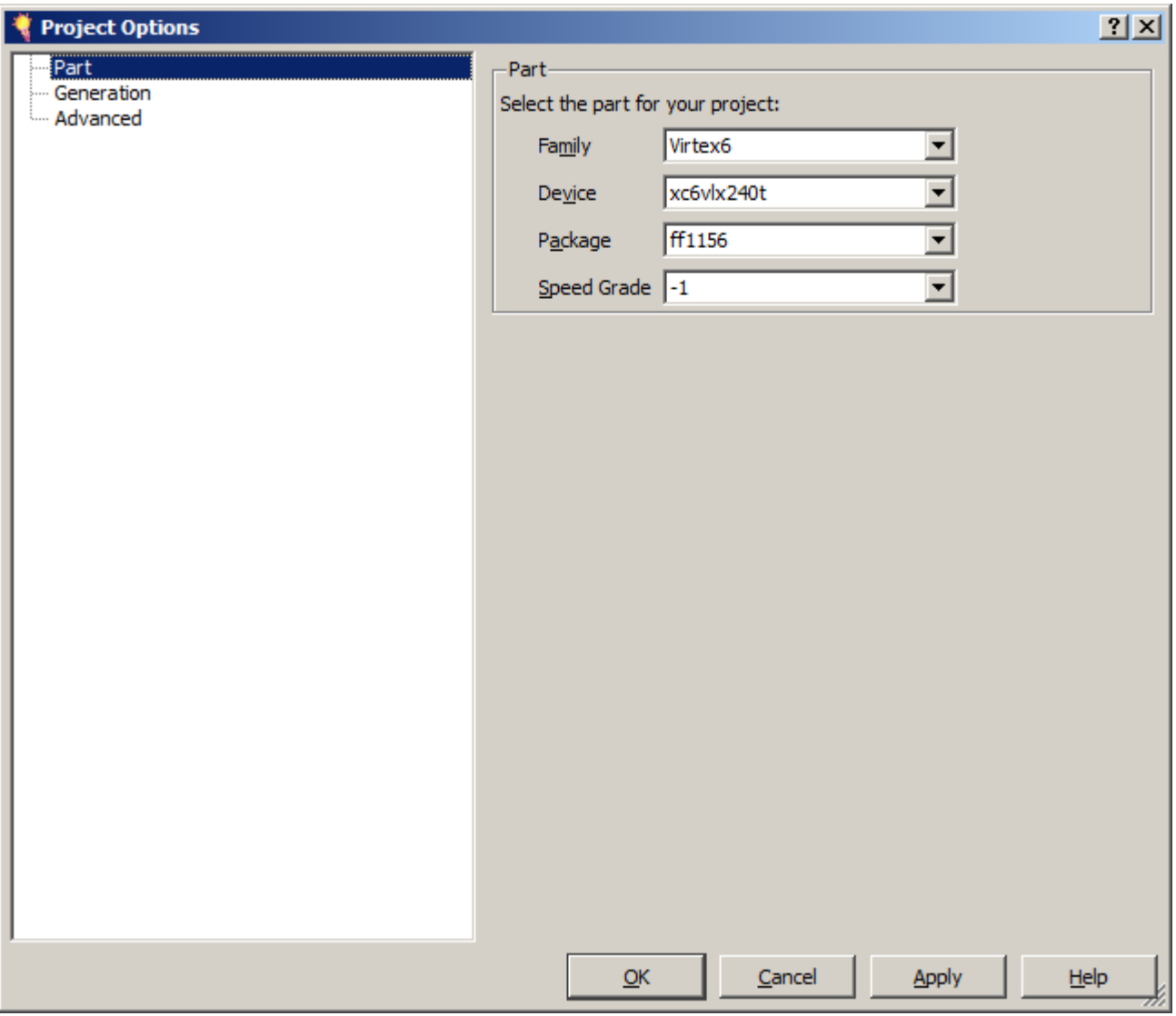
  Start → All Programs → Xilinx ISE Design Suite 11 → ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**



Note: Presentation applies to the ML605

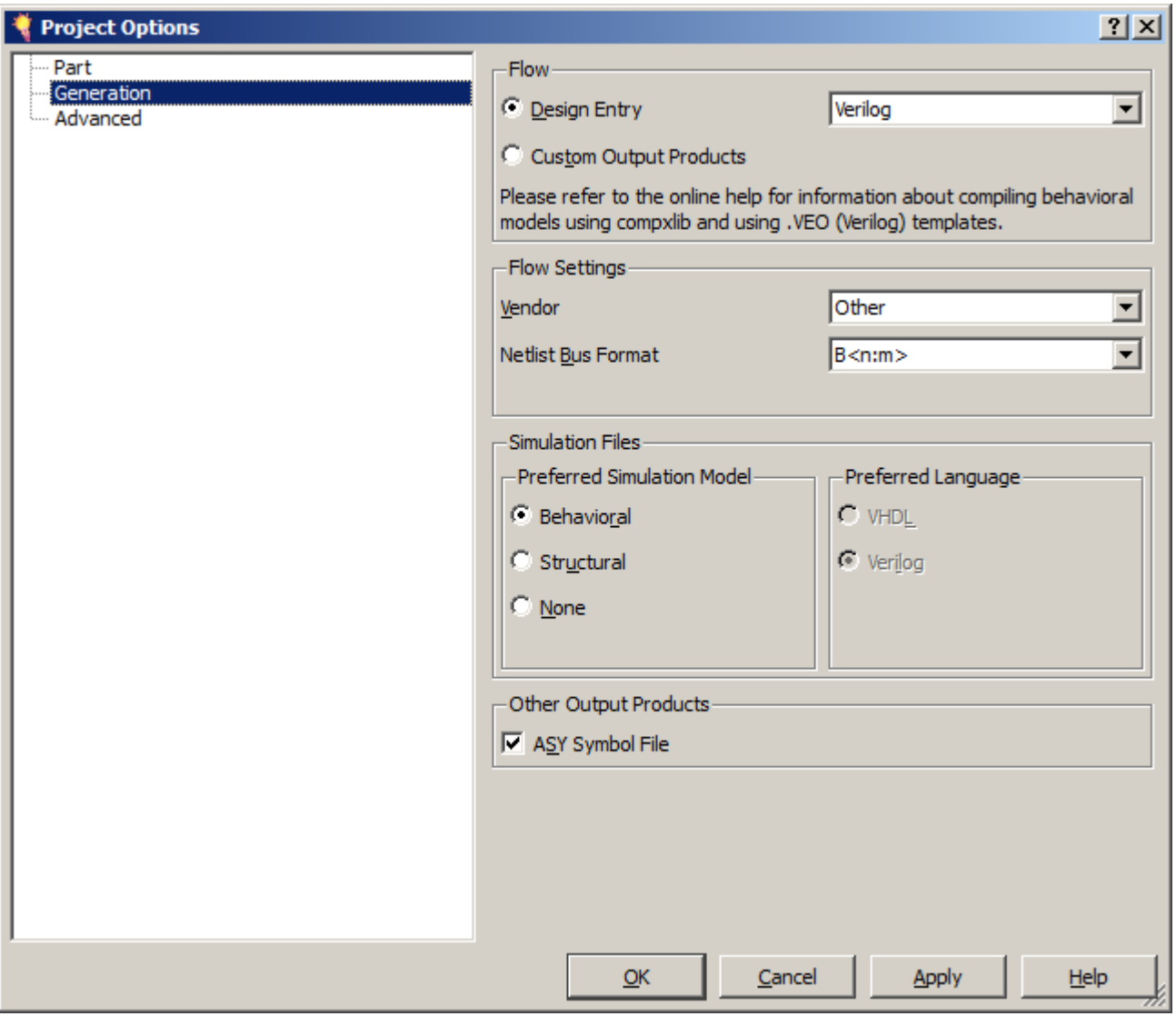
Create IBERT CORE Generator Project



- Create a project directory: ml605_ibert
- Name the project: ml605_ibert.cgp
- The Project options will appear
- Set the Part (as seen here):
  - Family: Virtex6
  - Device: xc6vlx240t
  - Package: ff1156
  - Speed Grade: -1

Note: Presentation applies to the ML605

Create IBERT CORE Generator Project



- Select Generation
- Set the Design Entry to Verilog
- Click OK

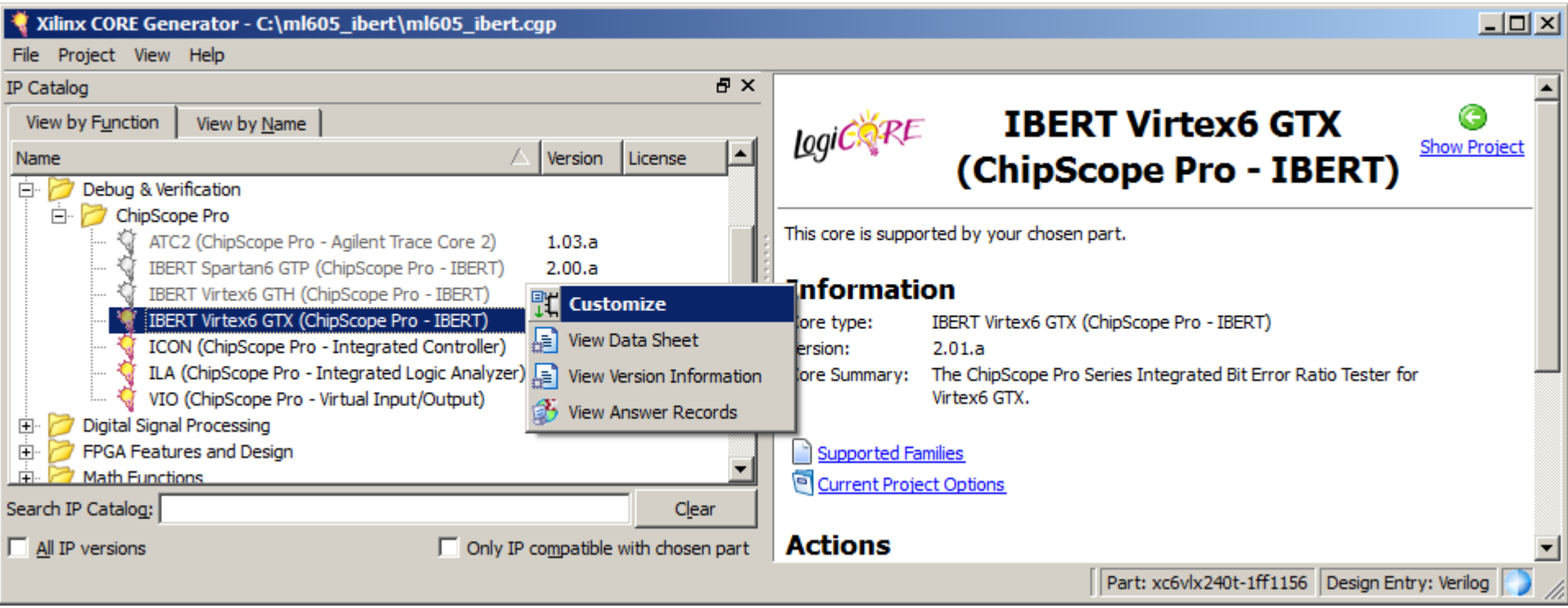
Note: Presentation applies to the ML605

XILINX®

IBERT Design Creation Bank 113

Create IBERT Design – Bank 113

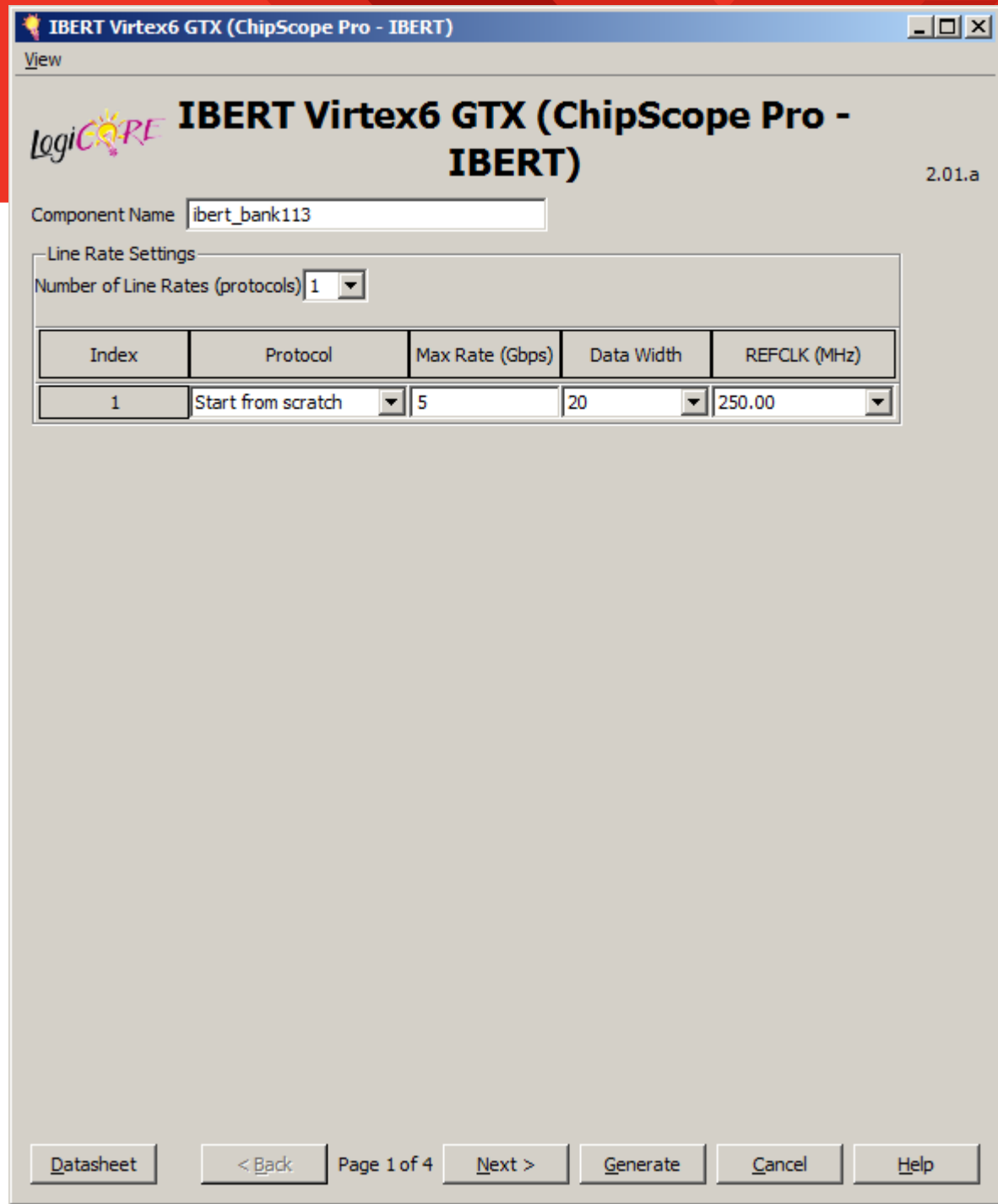
- **Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a**
  - Select **Customize**



Note: Presentation applies to the ML605

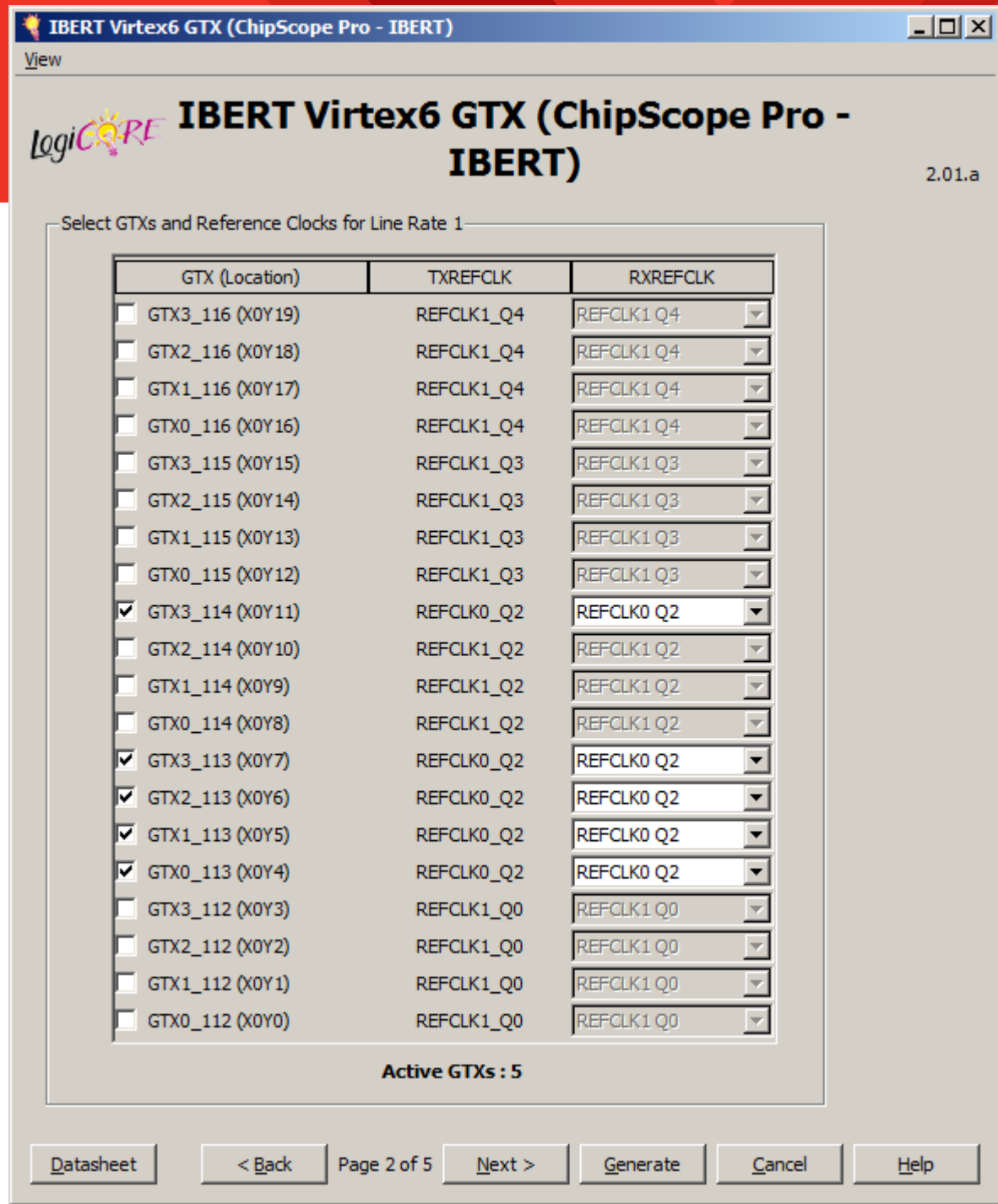
Create IBERT Design – Bank 113

- **Make the following settings:**
  - Component name: **ibert_bank113**
  - Set the number of Line Rates: **1**
  - Set the line rate to Max Rate: **5 Gbps**
- **On the ML605, Bank 113 is connected to the 250 MHz OSC**
  - Set the RefClk frequency to: **250 MHz**
- **Click Next**



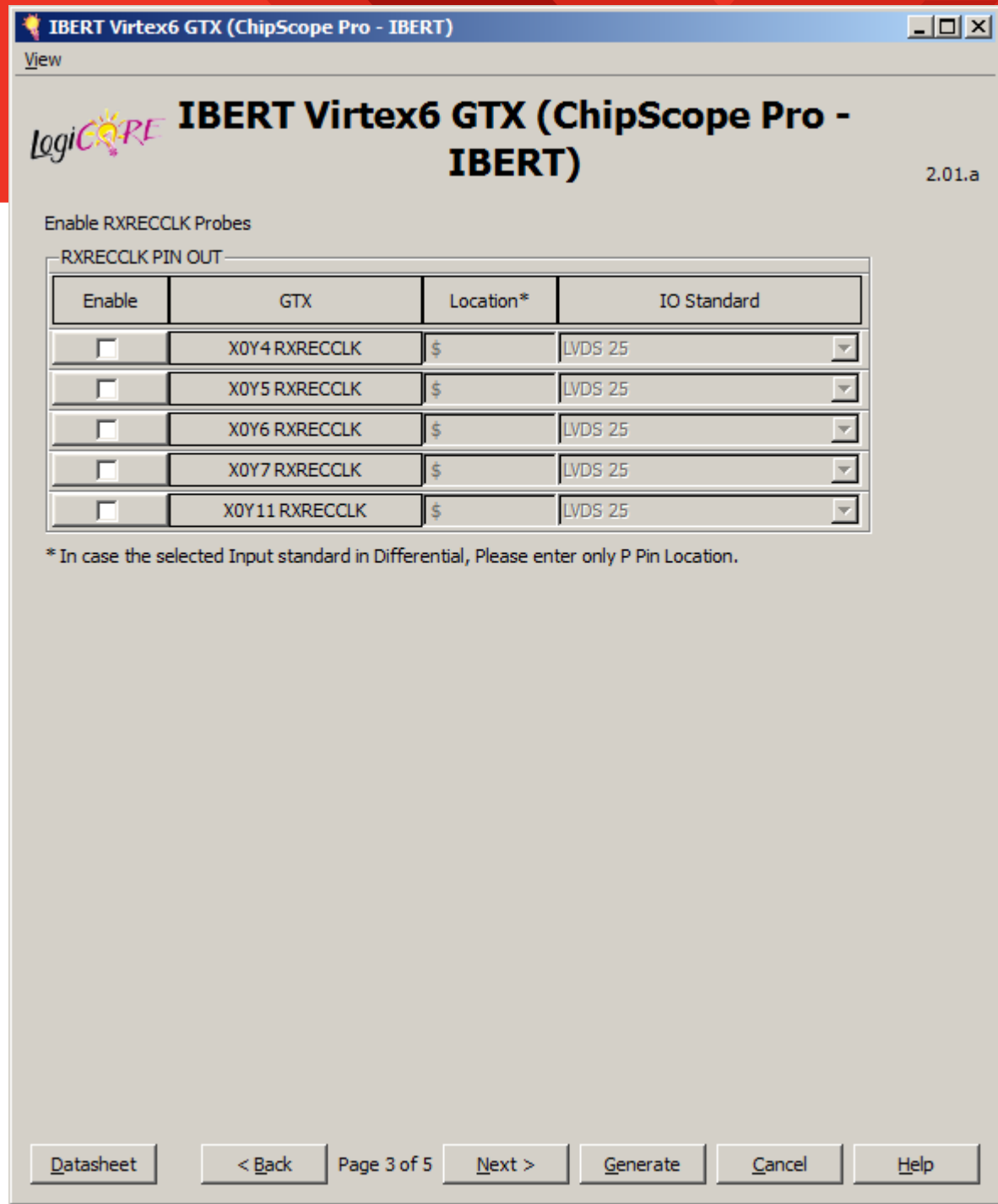
Create IBERT Design – Bank 113

- The line rate is 5 Gbps
- Select a GTX from Bank 114
  - This enables the clock used for Bank 113
- Select the four GTXs for Bank 113:
  - **X0Y7**
  - **X0Y6**
  - **X0Y5**
  - **X0Y4**
- Connect the Refclks for all GTXs to:
  - **REFCLK0 Q2**
  - This connects Bank 113 to the Bank 114 250 MHz Clock
- Click Next



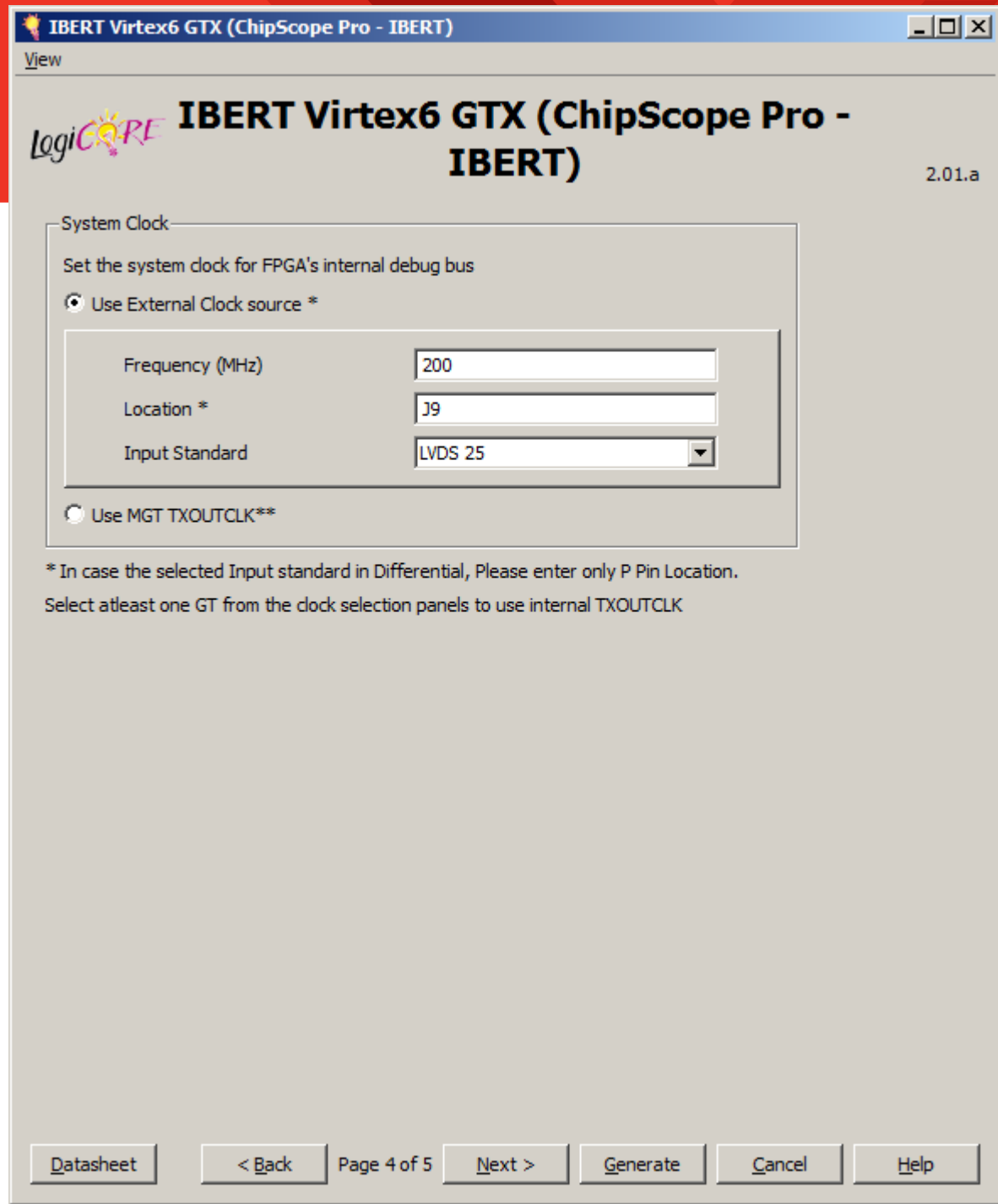
Create IBERT Design – Bank 113

- **Leave this screen as is**
  - Click Next



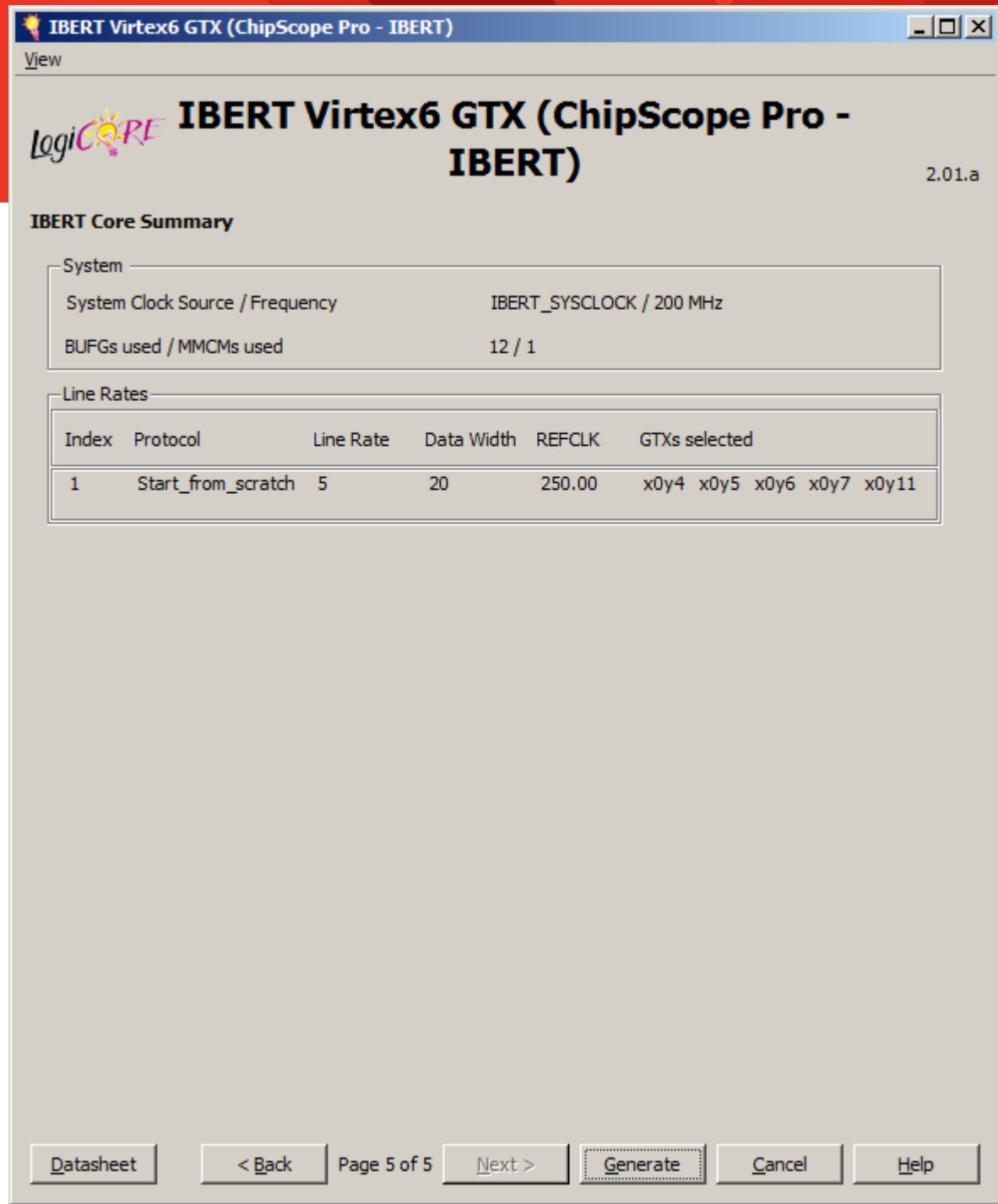
Create IBERT Design – Bank 113

- **Select the following settings:**
  - **Use External Clock source**
  - Location: **J9**
- **Click Next**



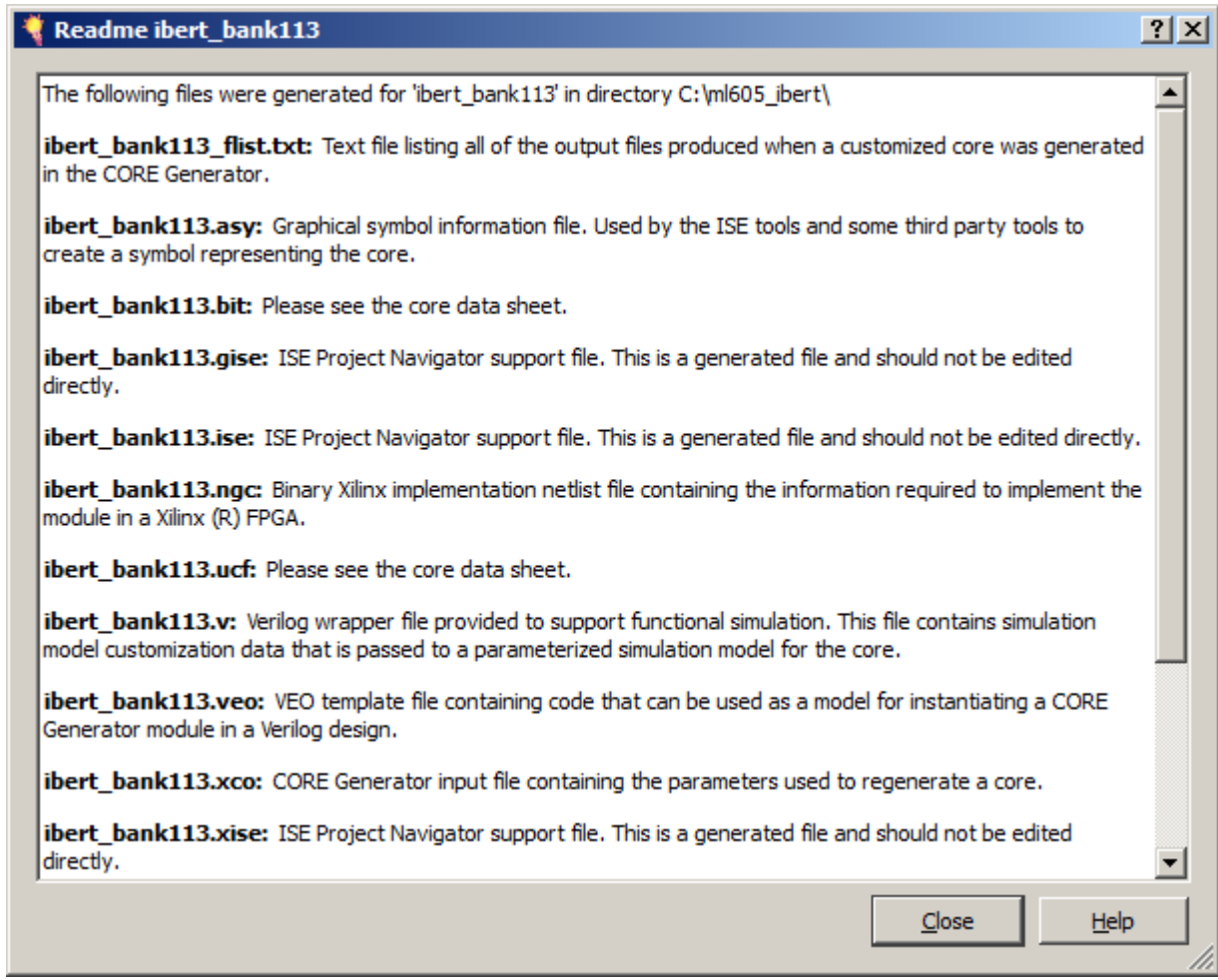
Create IBERT Design – Bank 113

- Click Generate



Create IBERT Design – Bank 113

- After the IBERT core finishes generating, click Close on the Datasheet window

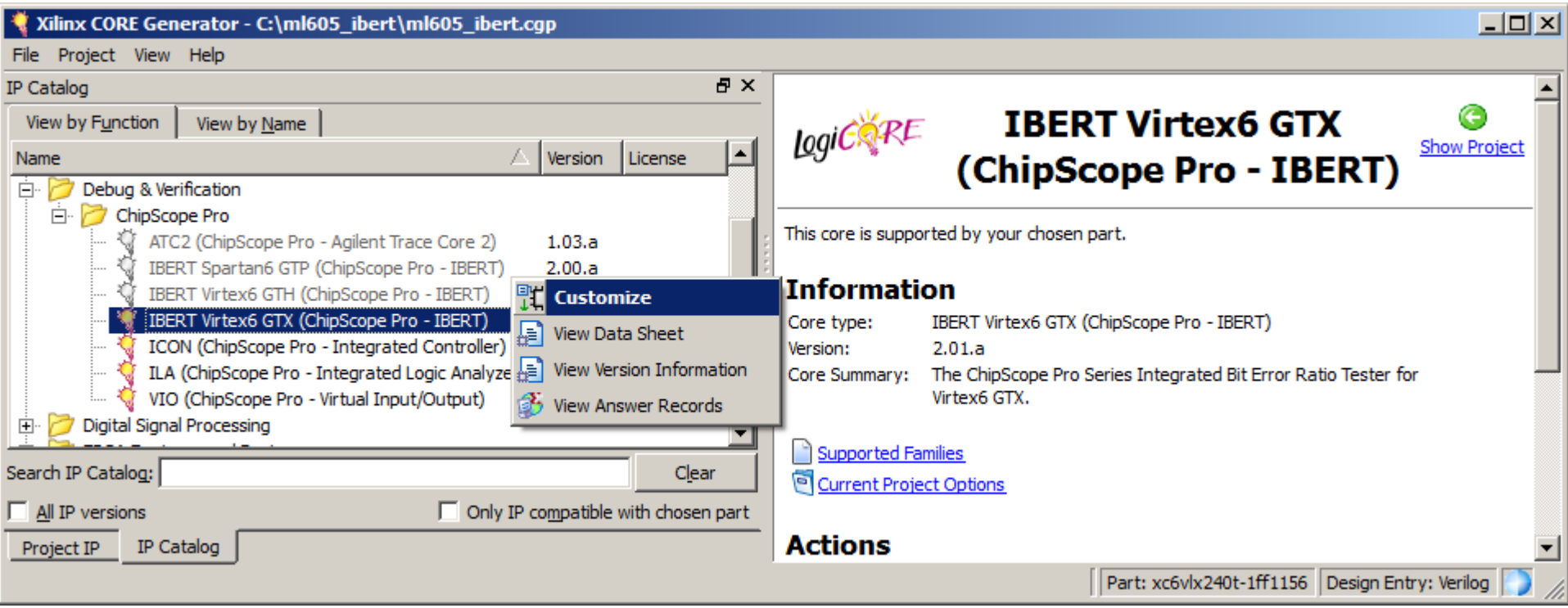


Note: Presentation applies to the ML605

IBERT Design Creation Bank 114

Create IBERT Design – Bank 114

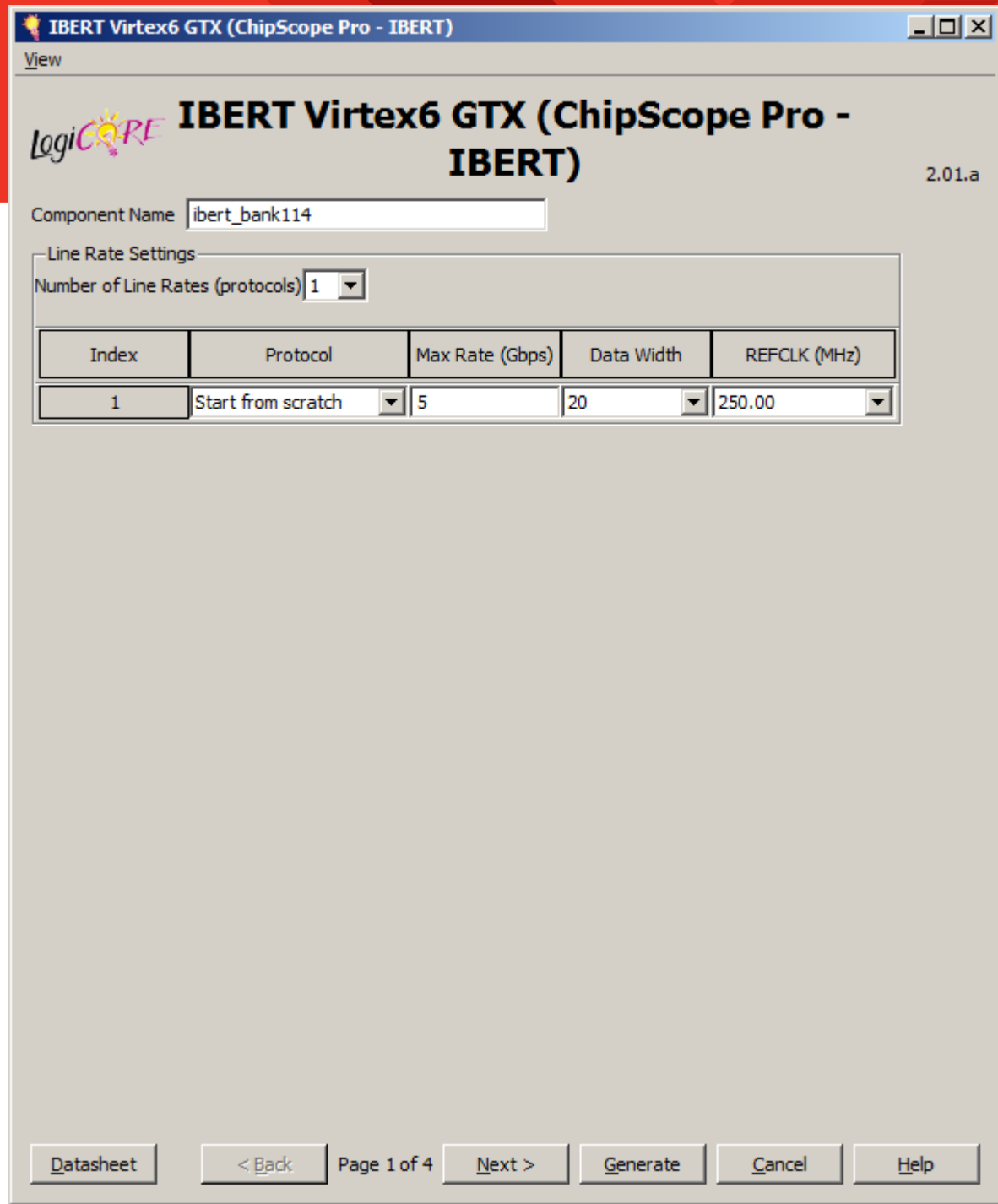
- **Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a**
  - Select **Customize**



Note: Presentation applies to the ML605

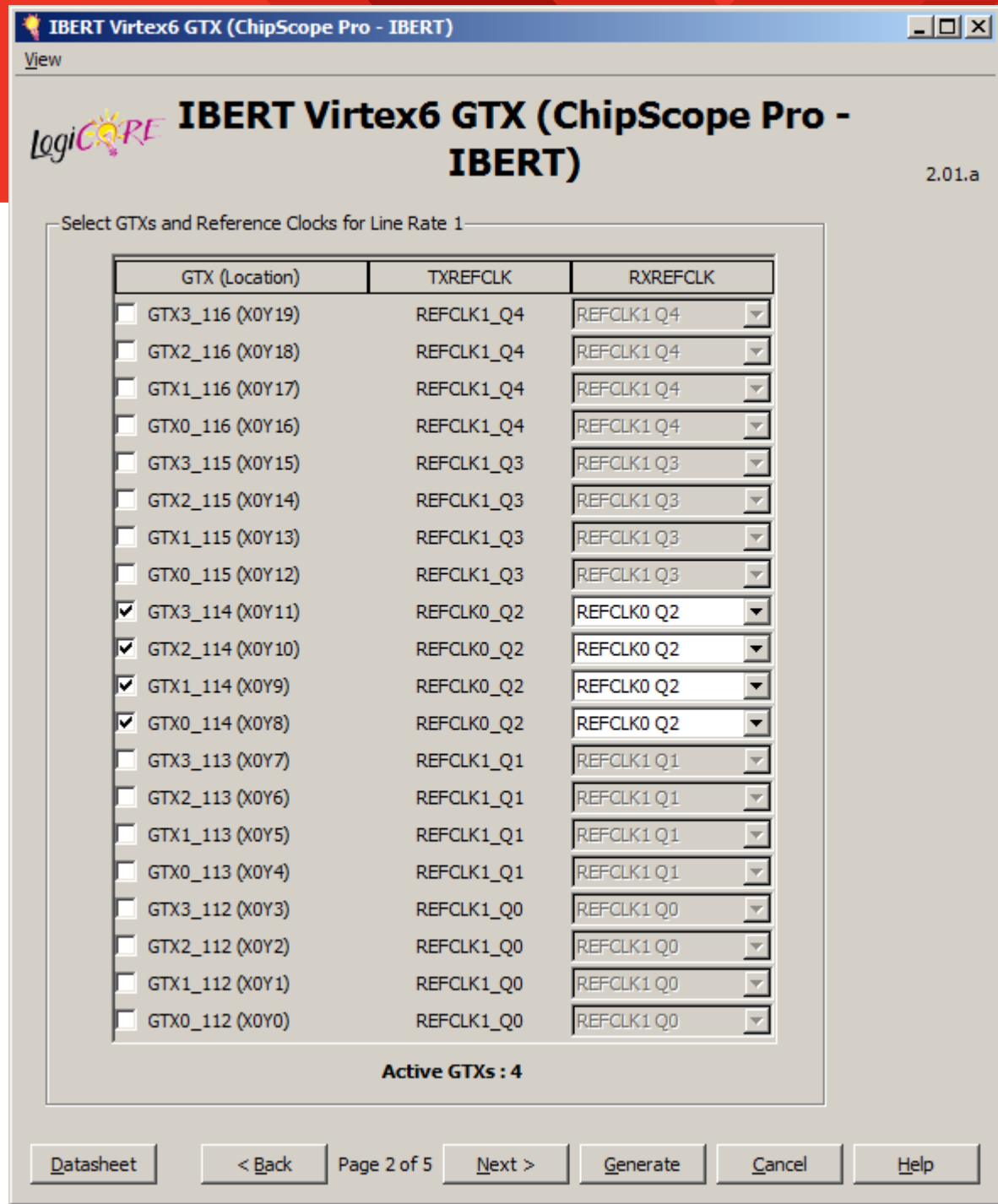
Create IBERT Design – Bank 114

- **Make the following settings:**
  - Component name: **ibert_bank114**
  - Set the number of Line Rates: **1**
  - Set the line rate to Max Rate: **5 Gbps**
- **On the ML605, Bank 114 is connected to the 250 MHz OSC**
  - Set the RefClk frequency to: **250 MHz**
- **Click Next**



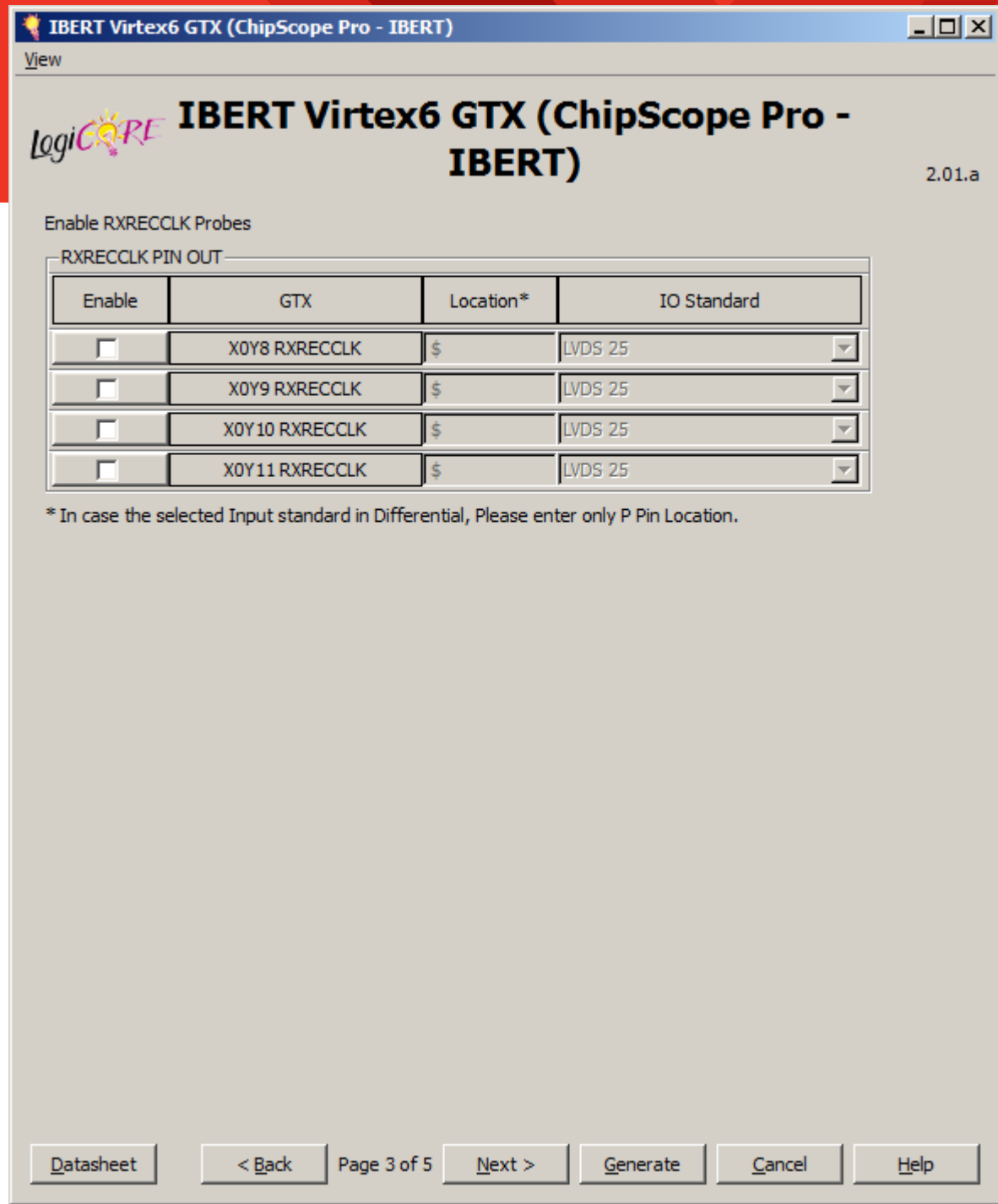
Create IBERT Design – Bank 114

- The line rate is 5 Gbps
- Select the four GTXs for Bank 114:
  - X0Y11
  - X0Y10
  - X0Y9
  - X0Y8
- Connect the Refclks to:
  - REFCLK0 Q2
- Click Next



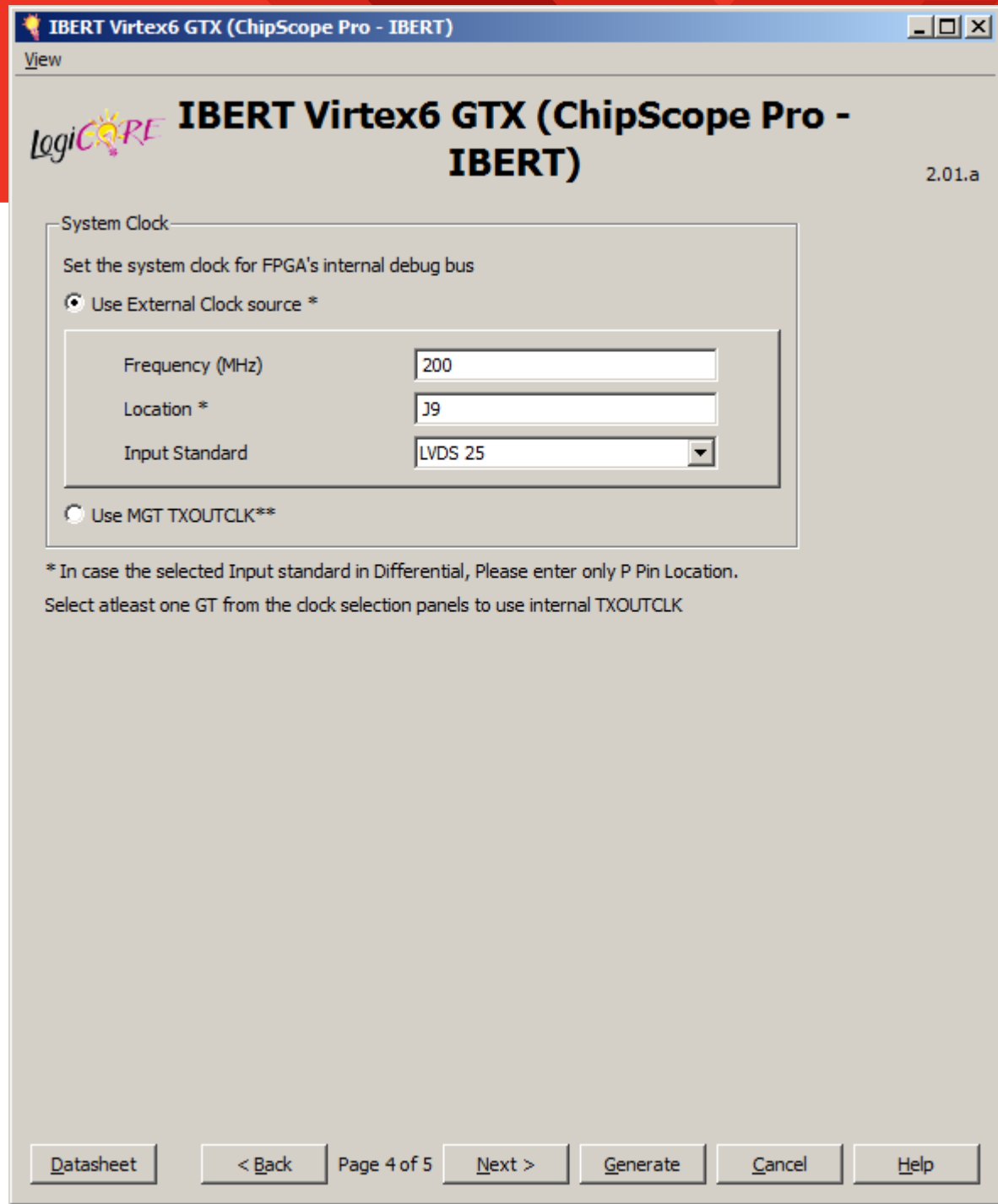
Create IBERT Design – Bank 114

- **Leave this screen as is**
  - Click Next



Create IBERT Design – Bank 114

- **Select the following settings:**
  - **Use External Clock source**
  - Location: **J9**
- **Click Next**

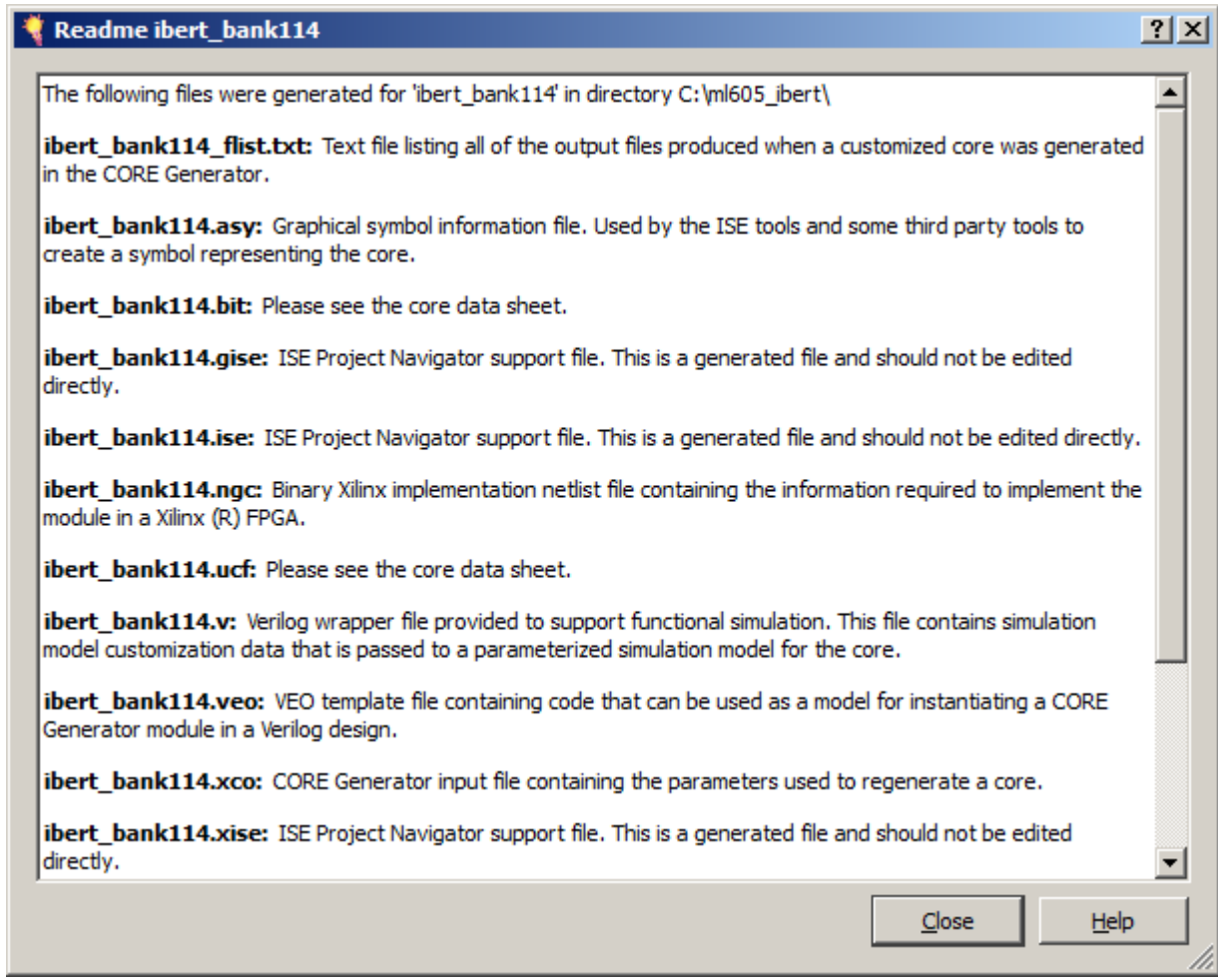


Create IBERT Design – Bank 114

- Click Generate

Create IBERT Design – Bank 114

- After the IBERT core finishes generating, click Close on the Datasheet window

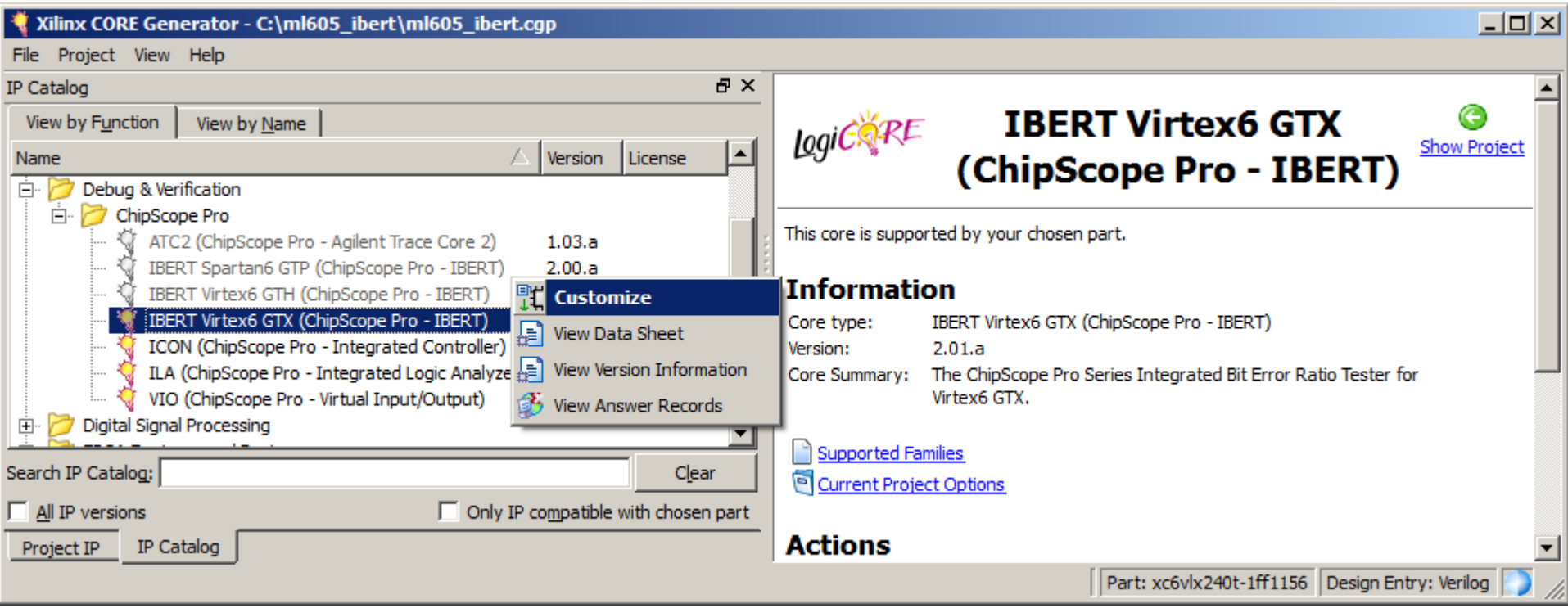


Note: Presentation applies to the ML605

IBERT Design Creation Bank 115

Create IBERT Design – Bank 115

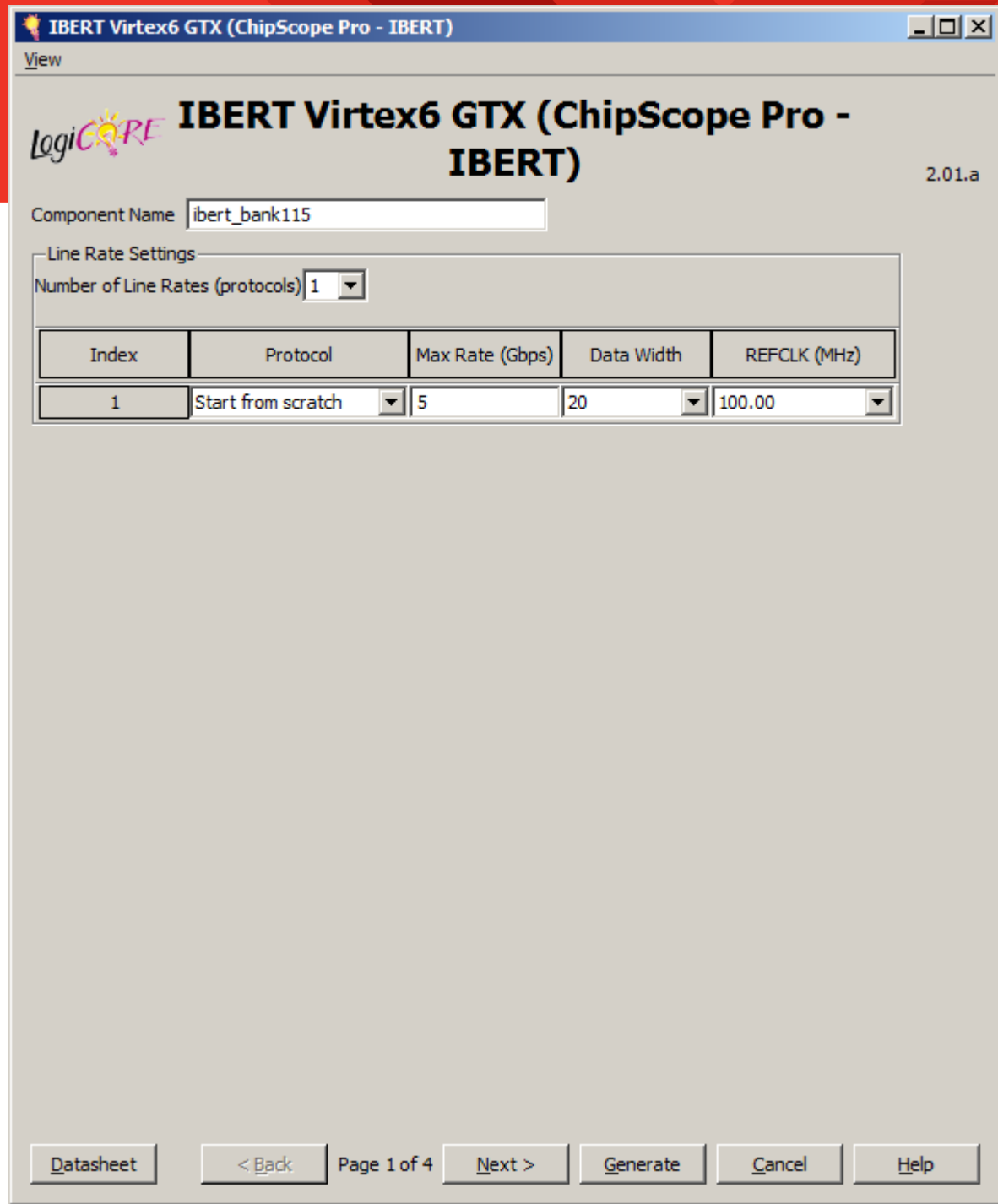
- **Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a**
  - Select **Customize**



Note: Presentation applies to the ML605

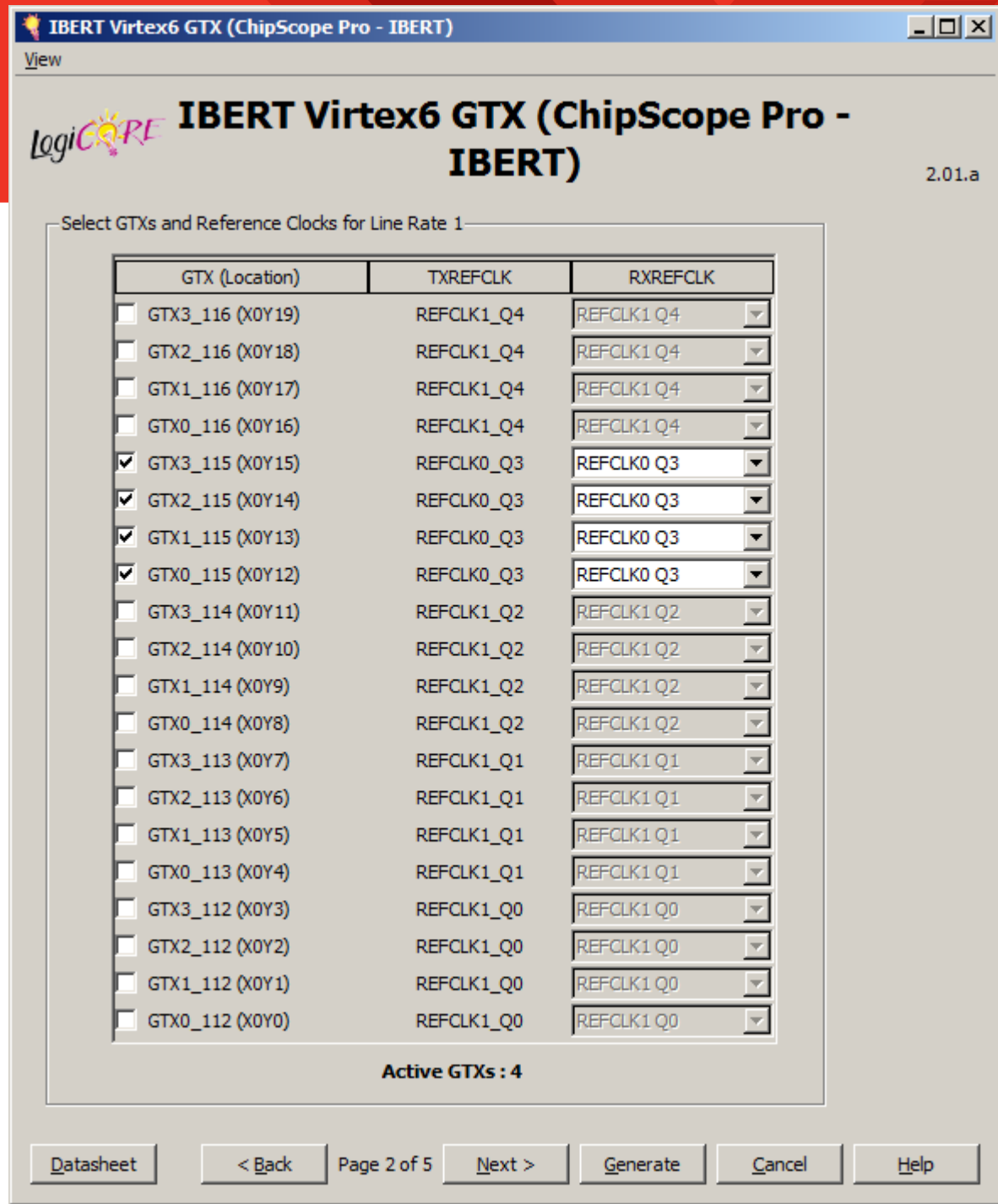
Create IBERT Design – Bank 115

- **Make the following settings:**
  - Component name: **ibert_bank115**
  - Set the number of Line Rates: **1**
  - Set the line rate to:
  - Max Rate: **5 Gbps**
- **On the ML605, Bank 115 is connected to the 100 MHz OSC**
  - Set the RefClk frequency to: **100 MHz**
- **Click Next**



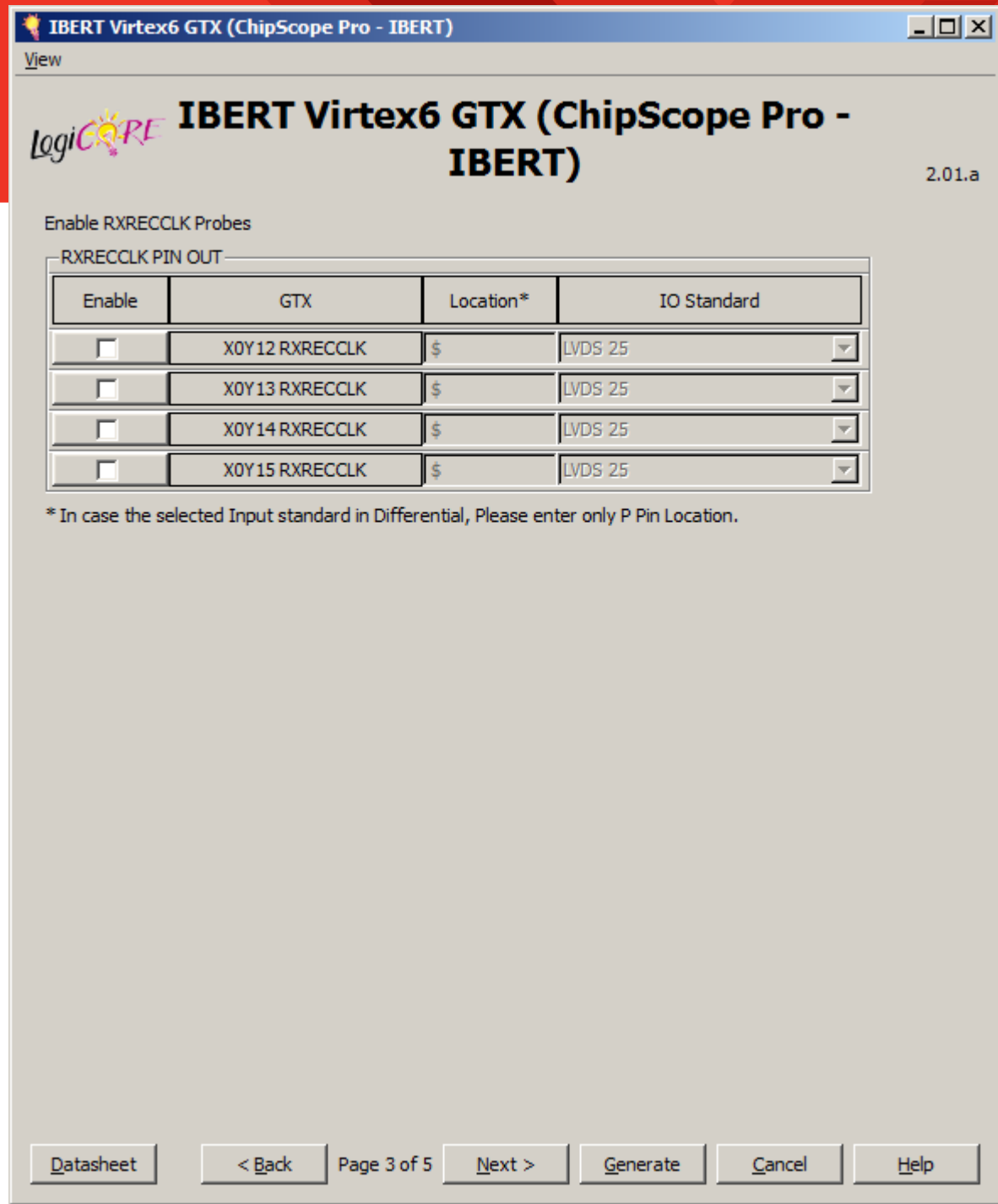
Create IBERT Design – Bank 115

- The rate is 5 Gbps
- Select the four GTXs for Bank 115:
  - X0Y15
  - X0Y14
  - X0Y13
  - X0Y12
- Connect the Refclks to:
  - REFCLK0 Q3
- Click Next



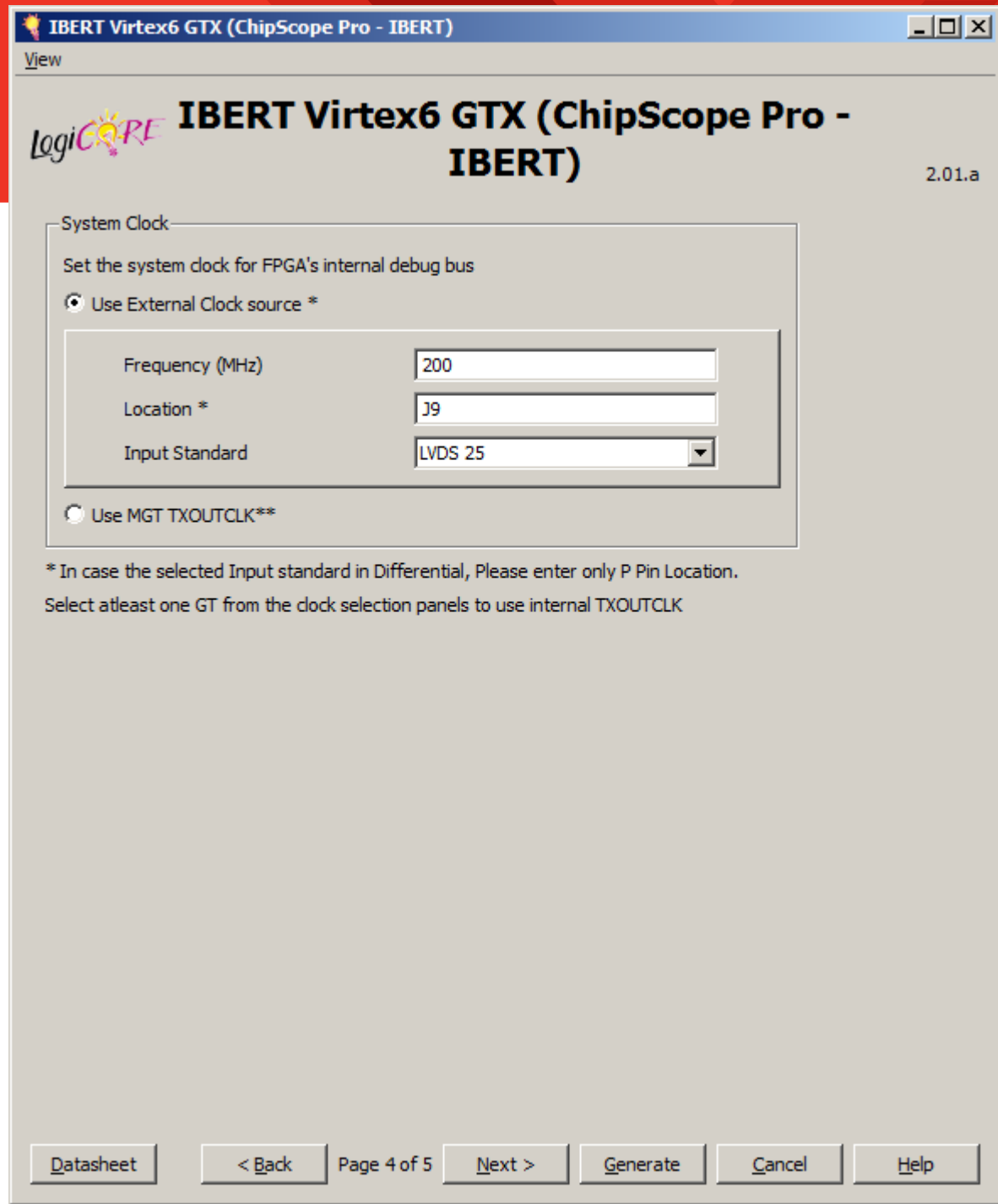
Create IBERT Design – Bank 115

- **Leave this screen as is**
  - Click Next



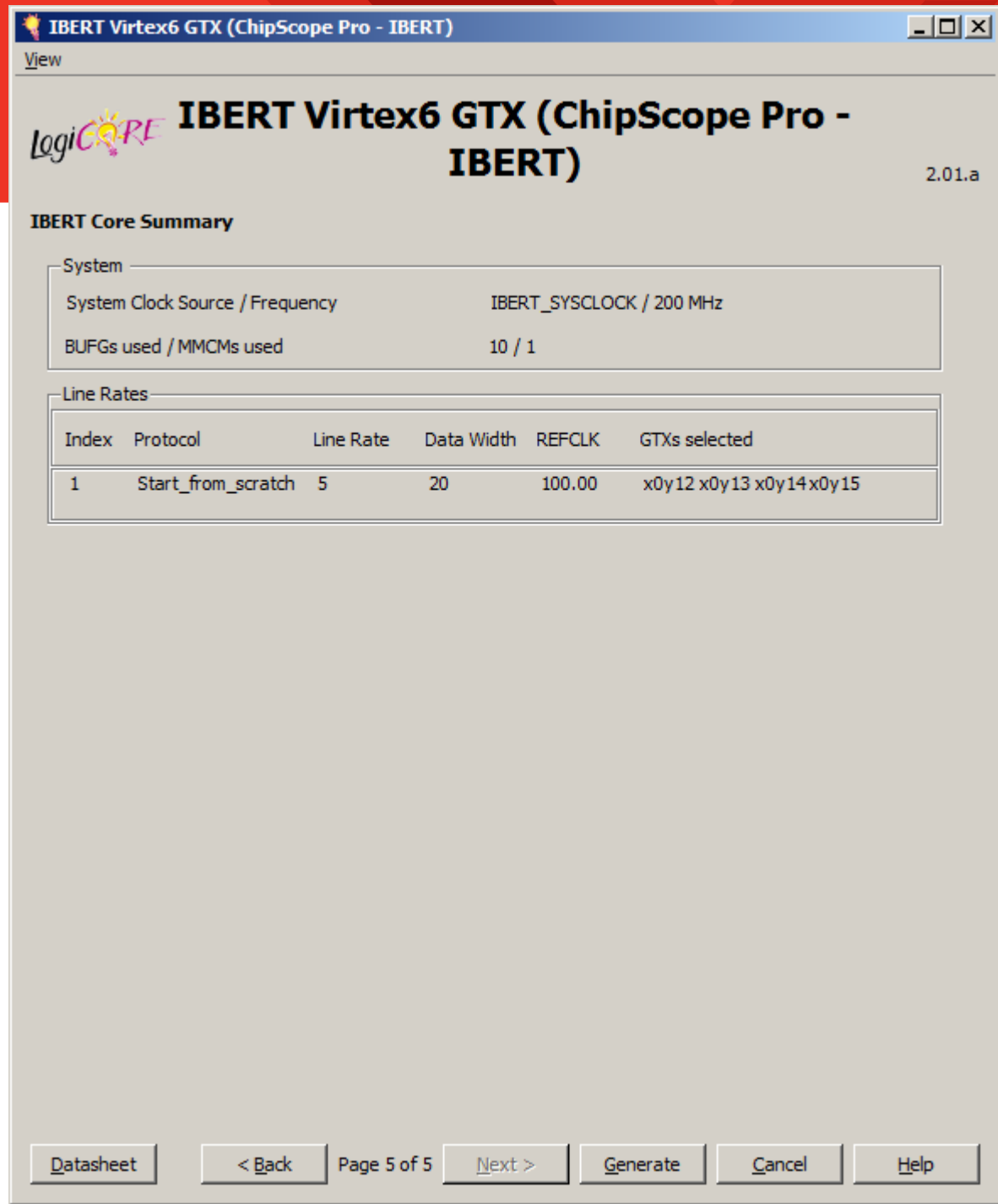
Create IBERT Design – Bank 115

- **Select the following settings:**
  - **Use External Clock source**
  - Location: **J9**
- **Click Next**



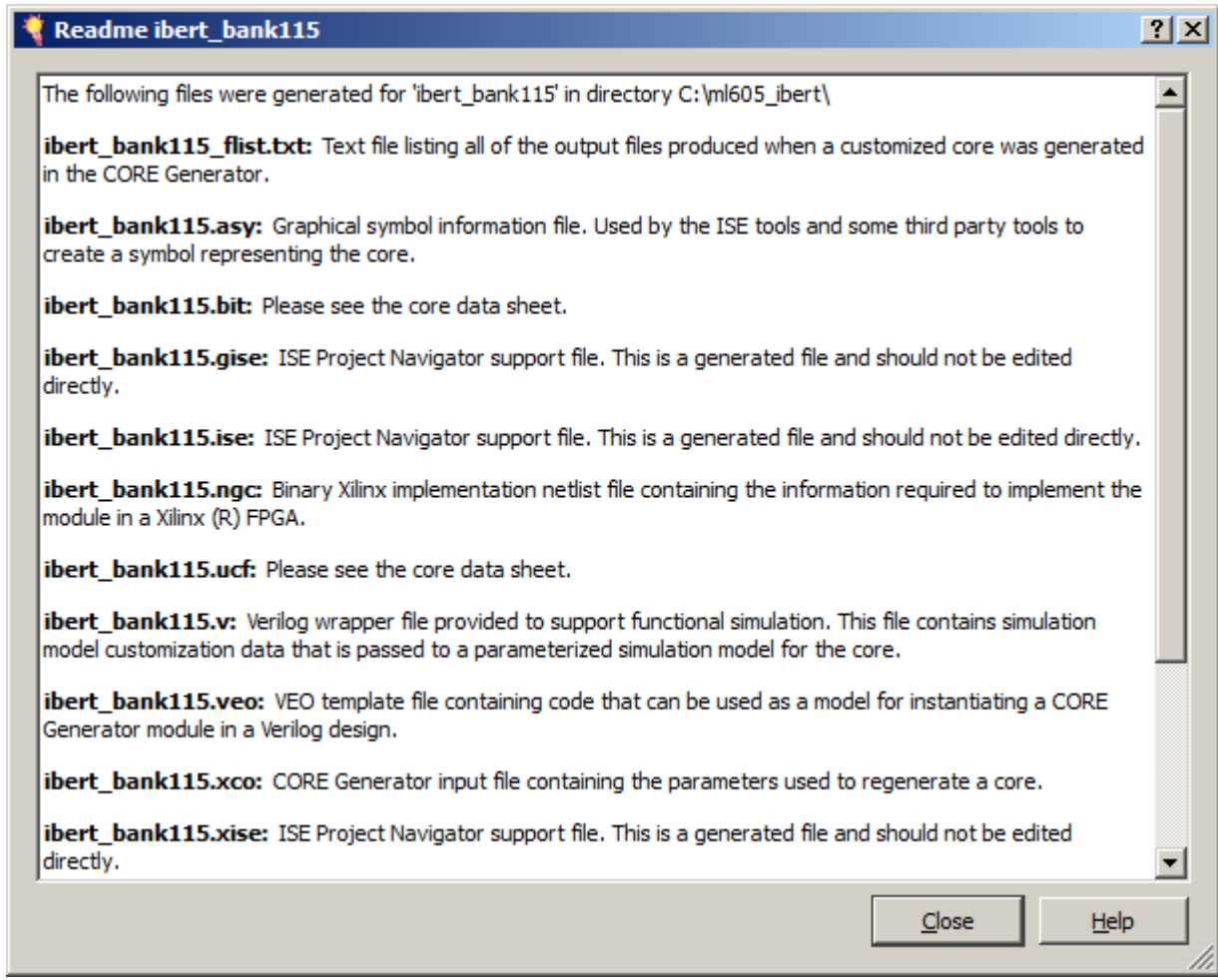
Create IBERT Design – Bank 115

- Click Generate



Create IBERT Design – Bank 115

- After the IBERT core finishes generating, click Close on the Datasheet window

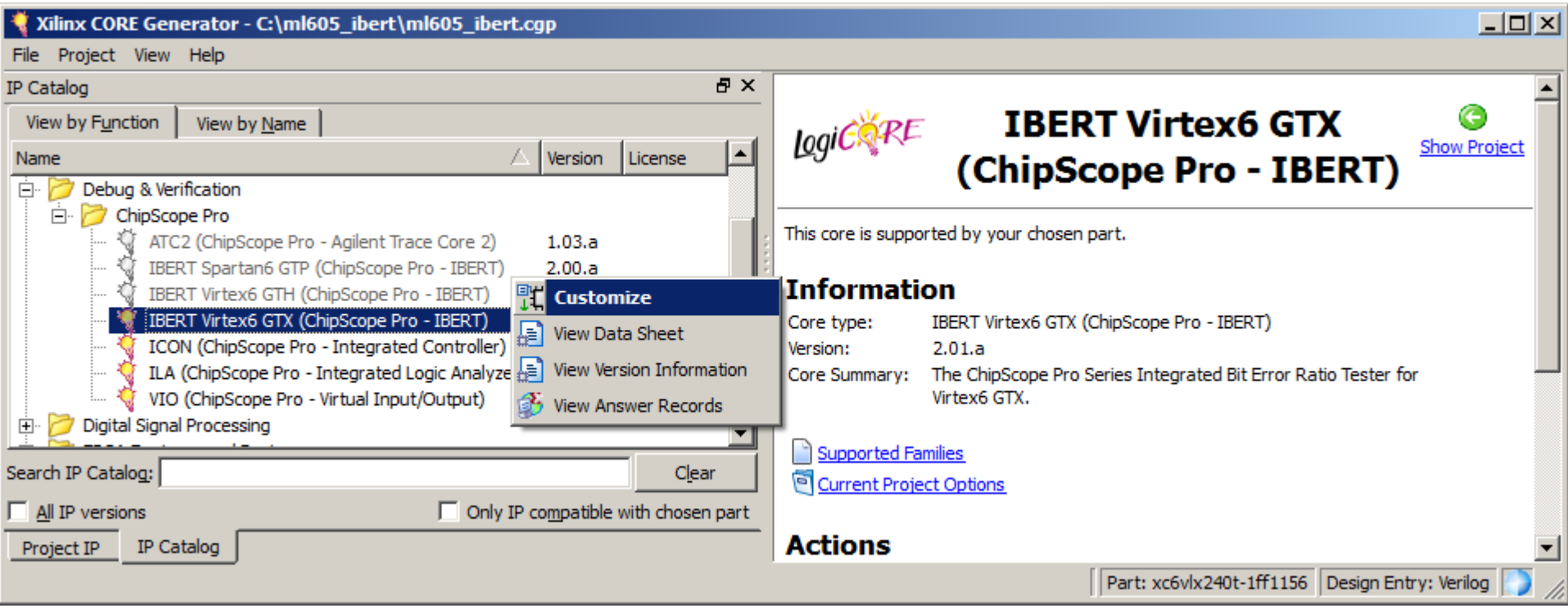


Note: Presentation applies to the ML605

IBERT Design Creation Bank 116

Create IBERT Design – Bank 116

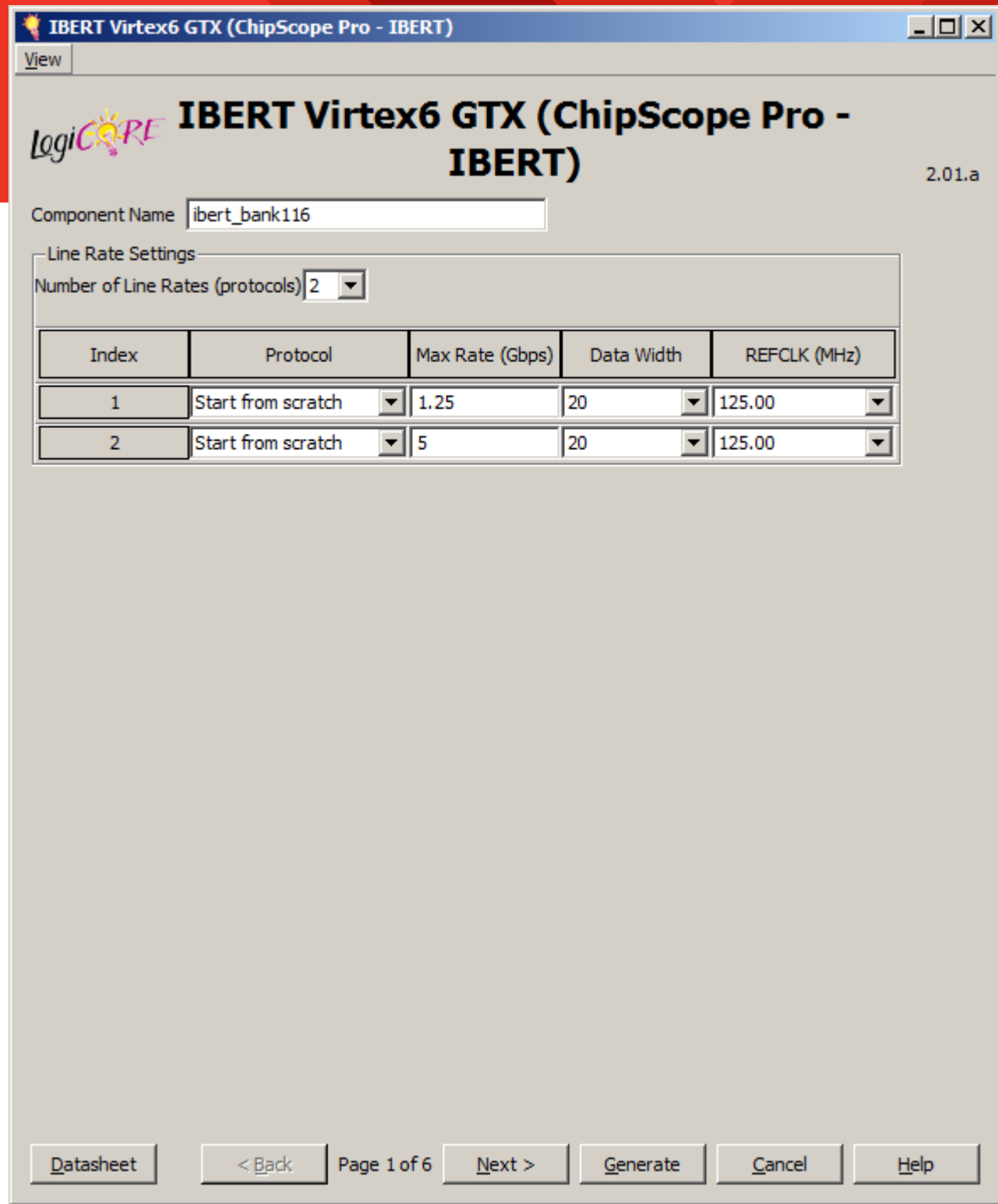
- **Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a**
  - Select **Customize**



Note: Presentation applies to the ML605

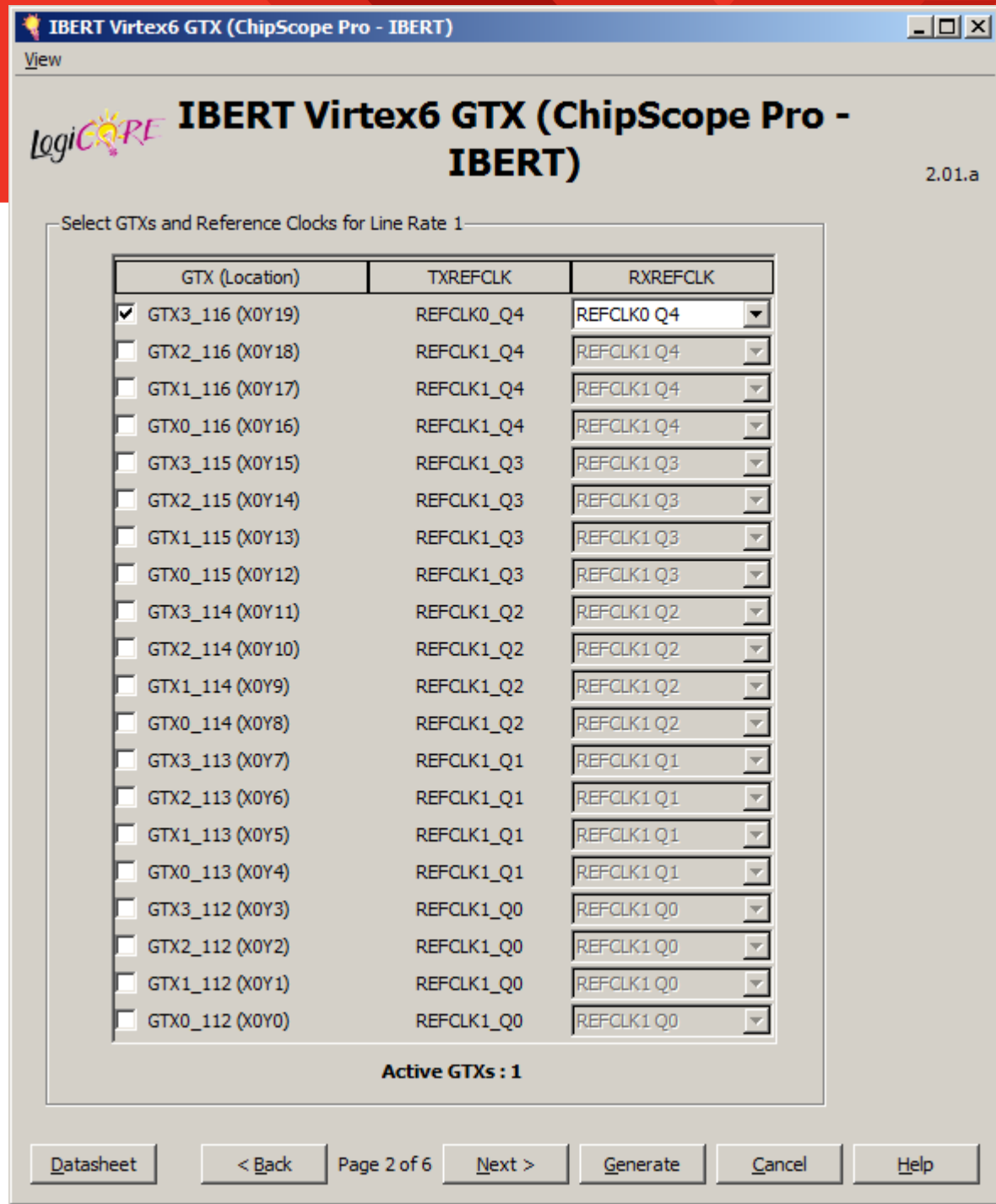
Create IBERT Design – Bank 116

- **Make the following settings:**
  - Component name: **ibert_bank116**
  - Set the number of Line Rates: 2
  - Set the first line rate to: Max Rate: 1.25 Gbps
  - Set the second line rate to: Max Rate: 5 Gbps
  - Set both RefClk frequencies to: **125 MHz**
- **Click Next**



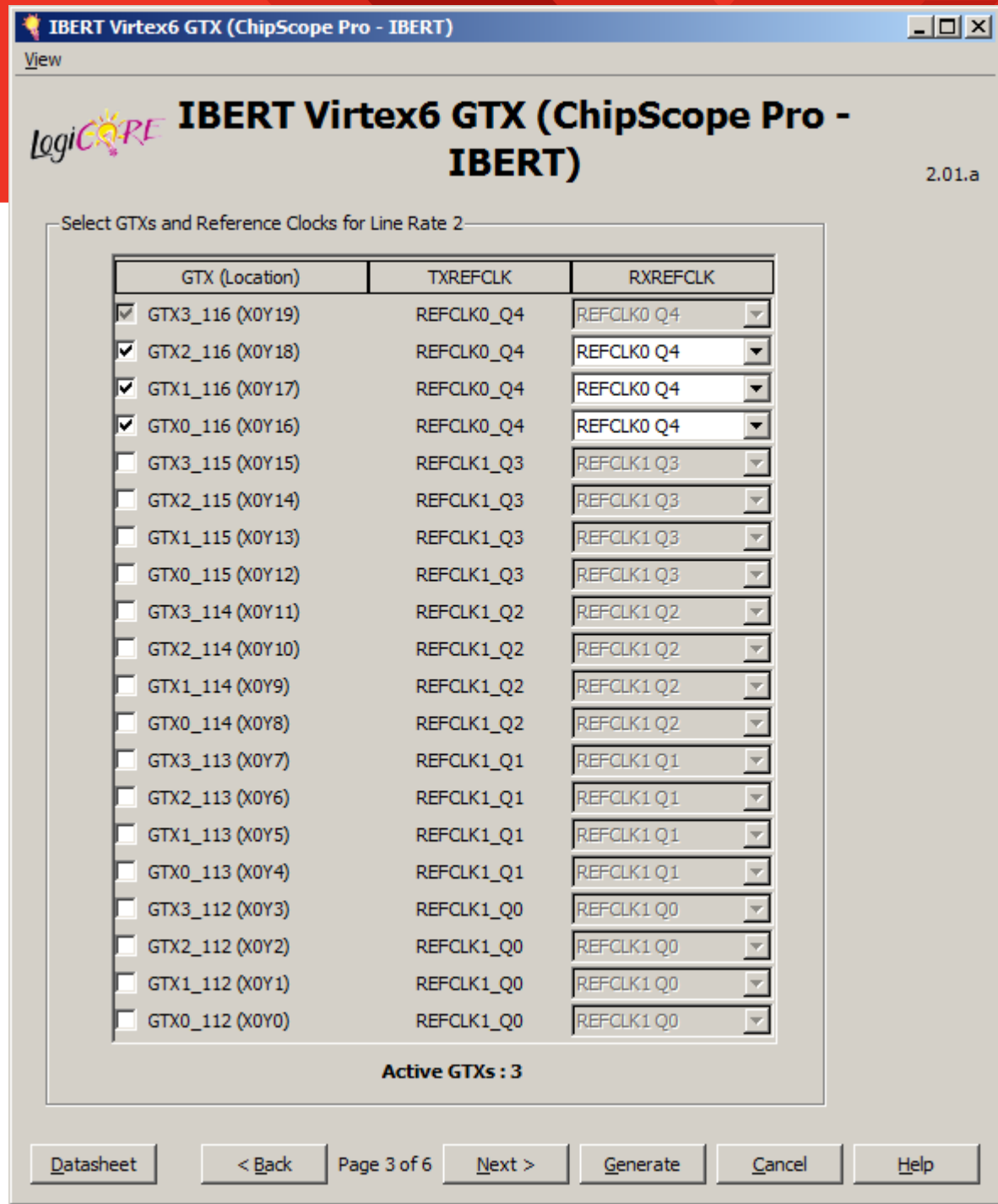
Create IBERT Design – Bank 116

- The first line rate is 1.25 Gbps
- Select the first GTX for Bank 116:
  - X0Y19
- Connect the Refclk to:
  - REFCLK0 Q4
  - This connects Bank 116 to the 125 MHz SGMII OSC
- Click Next



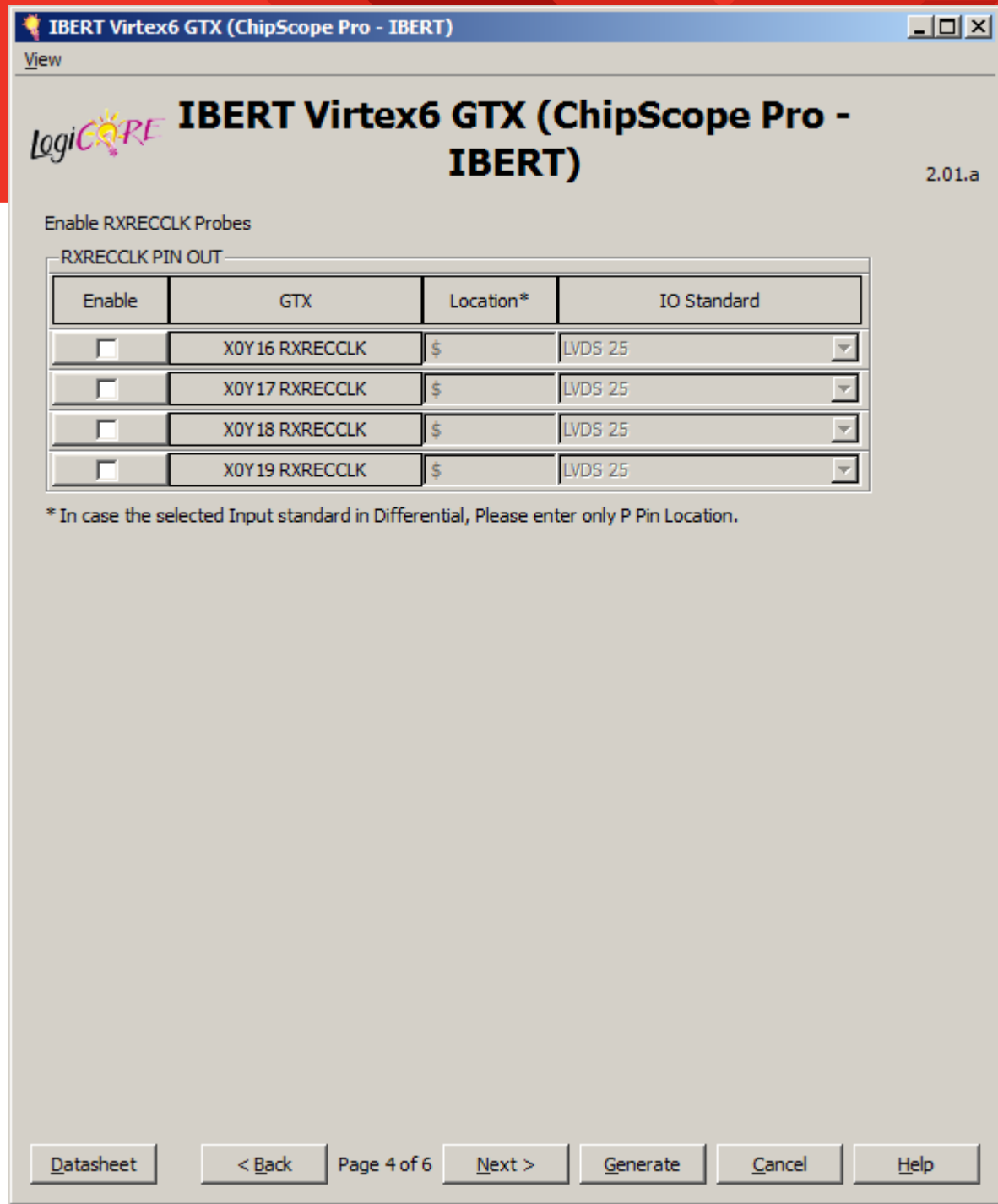
Create IBERT Design – Bank 116

- The second line rate is 5 Gbps
- Select the second and third GTXs for Bank 116:
  - X0Y18
  - X0Y17
  - X0Y16
- Connect the Refclks to:
  - REFCLK0 Q4
- Click Next



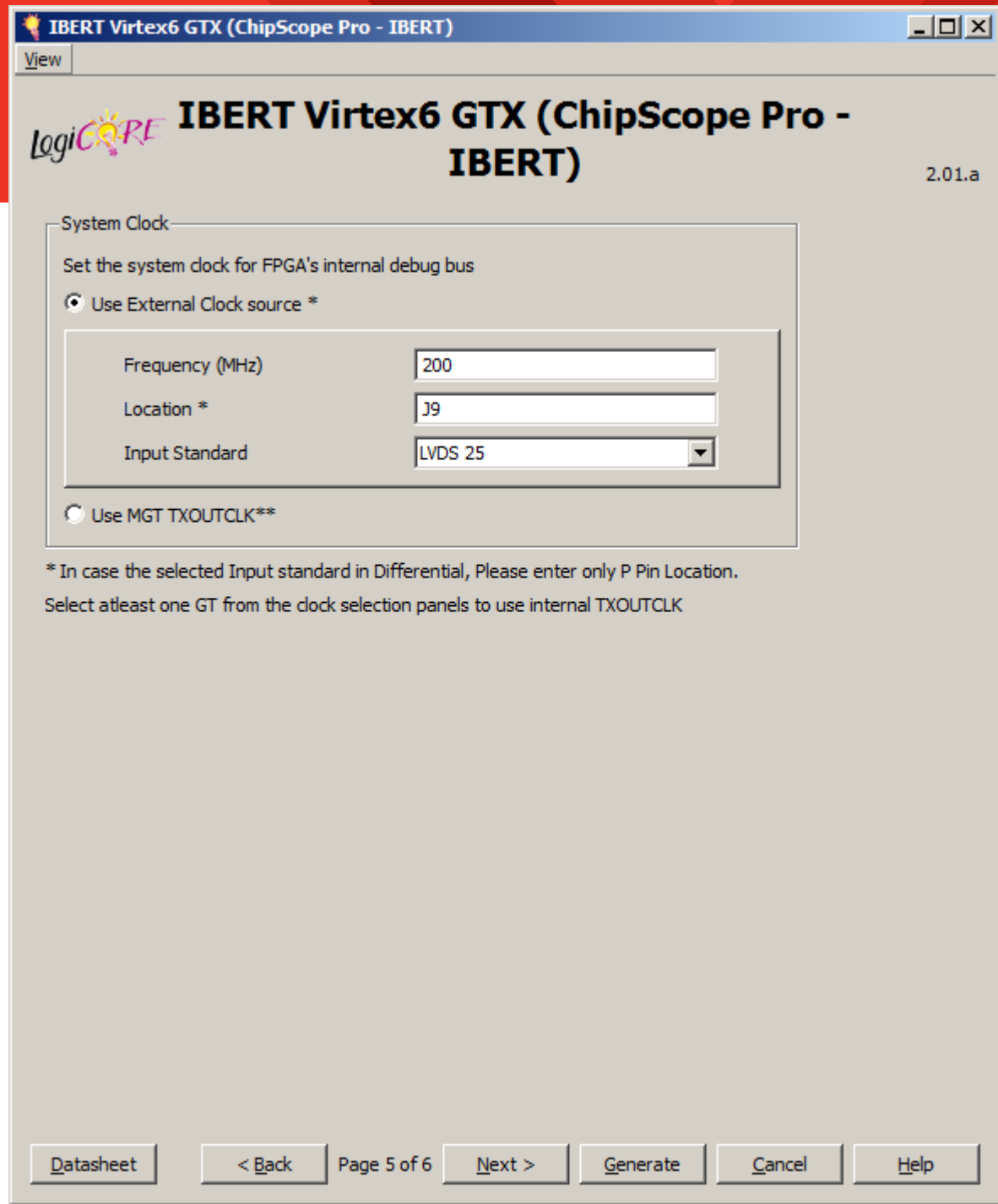
Create IBERT Design – Bank 116

- **Leave this screen as is**
  - Click Next



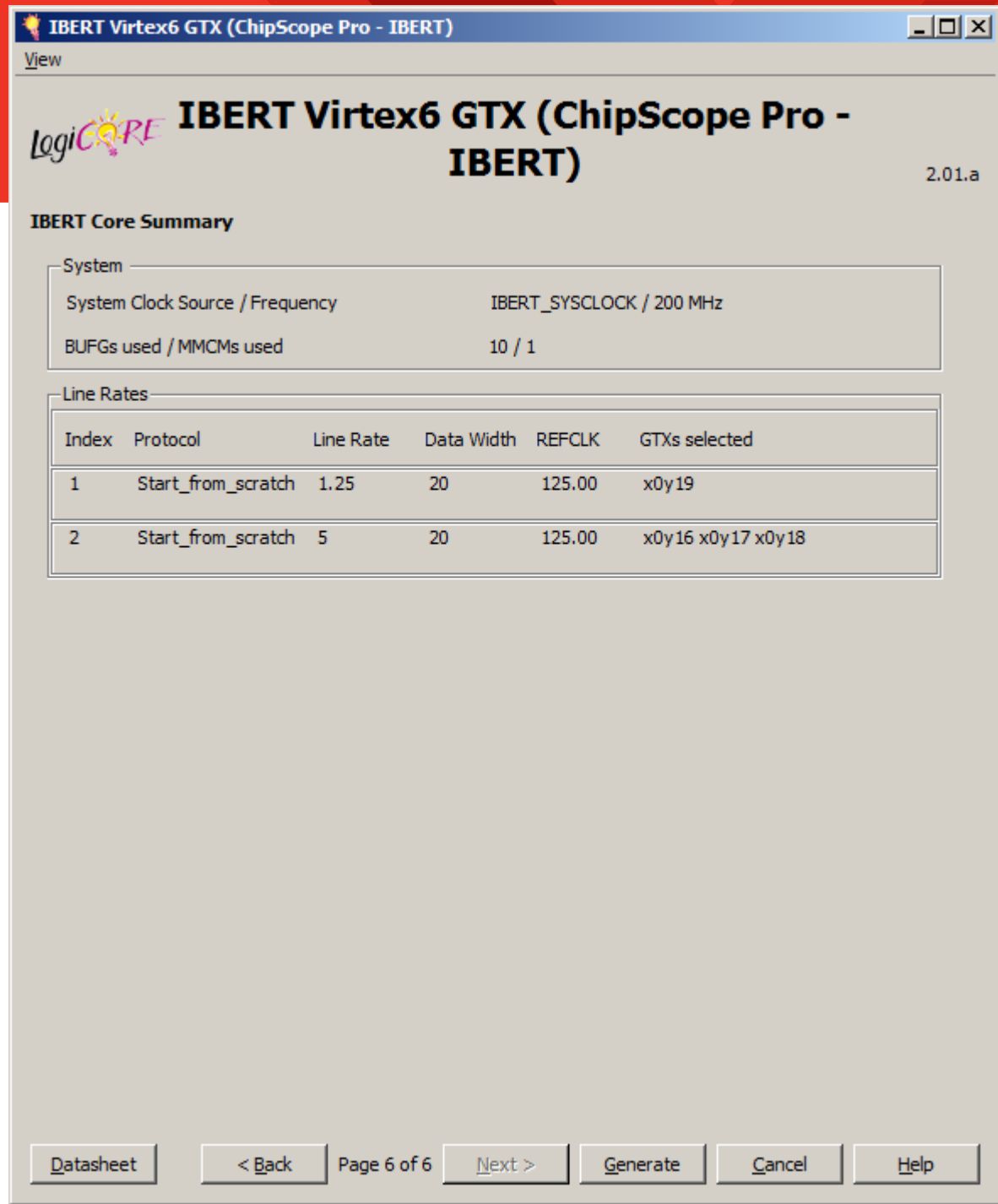
Create IBERT Design – Bank 116

- **Select the following settings:**
  - **Use External Clock source**
  - Location: **J9**
- **Click Next**



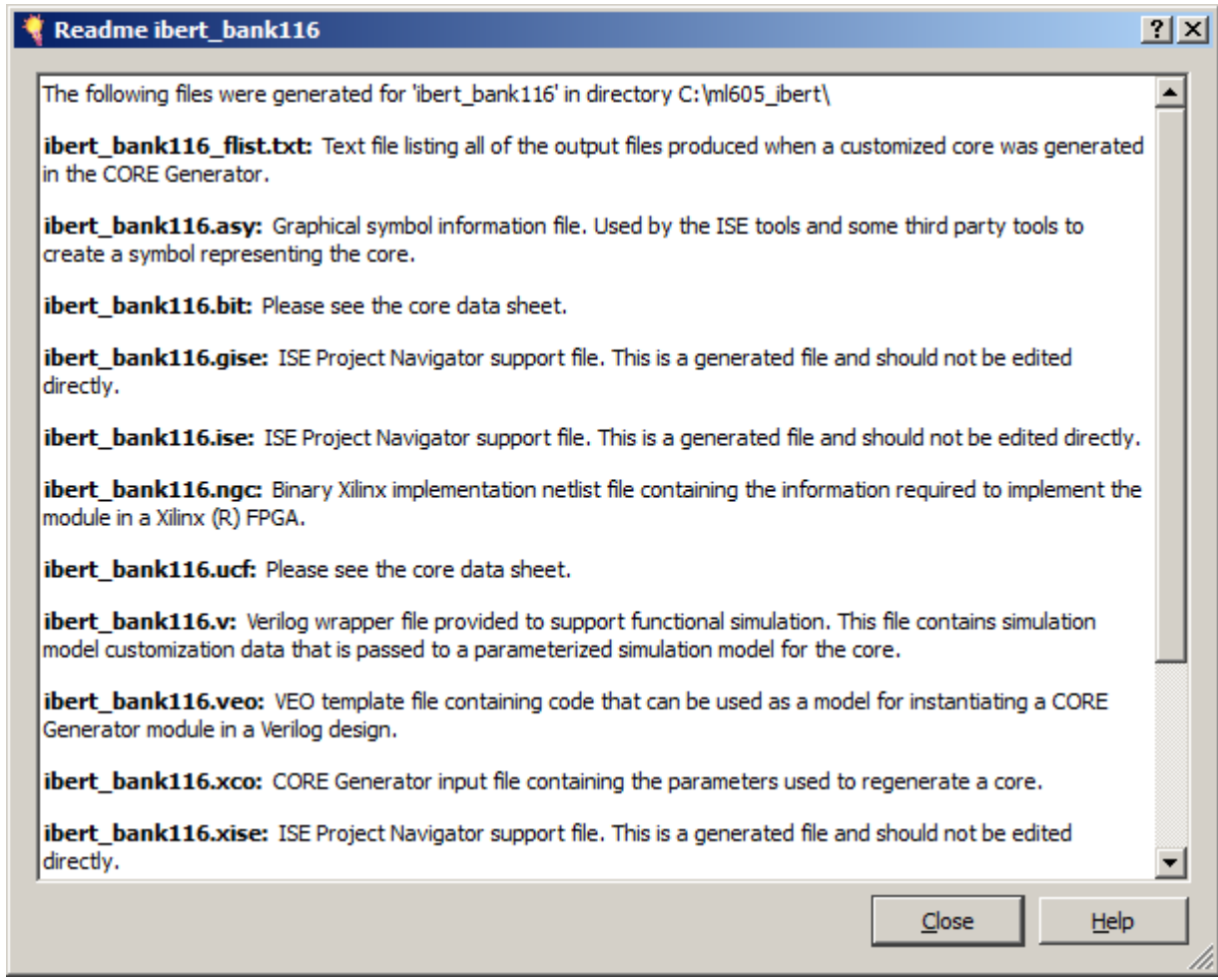
Create IBERT Design – Bank 116

- Click Generate



Create IBERT Design – Bank 116

- After the IBERT core finishes generating, click Close on the Datasheet window



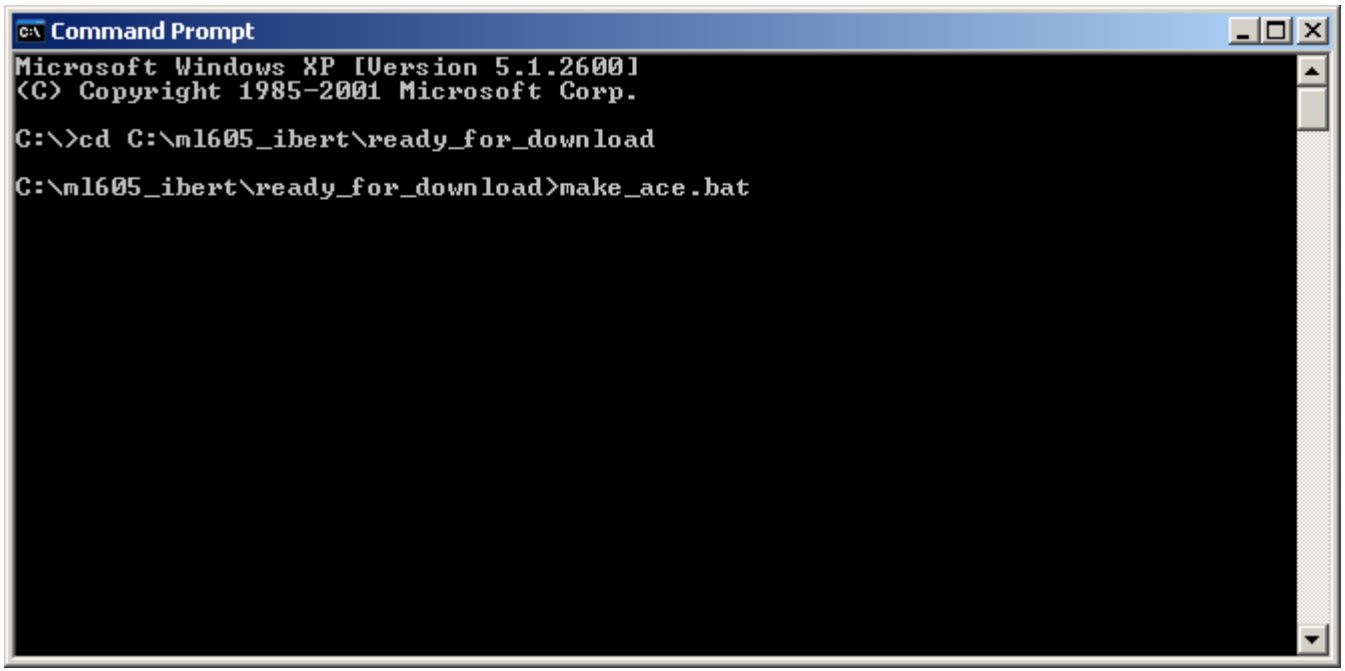
Note: Presentation applies to the ML605

Generate IBERT ACE Files (Optional)

- **Type these commands in a windows command shell:**

  cd C:\ml605_ibert\ready_for_download

  make_ace.bat



Note: Presentation applies to the ML605

References

References

- **ChipScope Pro**
  - ChipScope Pro 11.1 ChipScope Pro Software and Cores User Guide
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/chipscope_pro_sw_cores_ug029.pdf

Documentation

Documentation

- **Virtex-6**
  - Virtex-6 FPGA Family
    http://www.xilinx.com/products/virtex6/index.htm
- **ML605 Documentation**
  - Virtex-6 FPGA ML605 Evaluation Kit
    http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm
  - ML605 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf
  - ML605 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf