

ML605 GTX IBERT Design Creation

December 2009

ML605 IBERT Overview

- **Xilinx ML605 Board**
- **Software Requirements**
- **Setup for the ML605 IBERT Designs**
 - Running the ML605 IBERT Design – Bank 113
 - Running the ML605 IBERT Design – Bank 114
 - Running the ML605 IBERT Design – Bank 115
 - Running the ML605 IBERT Design – Bank 116
- **ML605 IBERT Design Creation**
 - Create IBERT CORE Generator Project
 - Create IBERT Design – Bank 113 (FMC_HPC)
 - Create IBERT Design – Bank 114 (PCIe)
 - Create IBERT Design – Bank 115 (PCIe)
 - Create IBERT Design – Bank 116 (FMC_LPC, SFP, SMA, SGMII)
- **References**

ML605 IBERT Overview

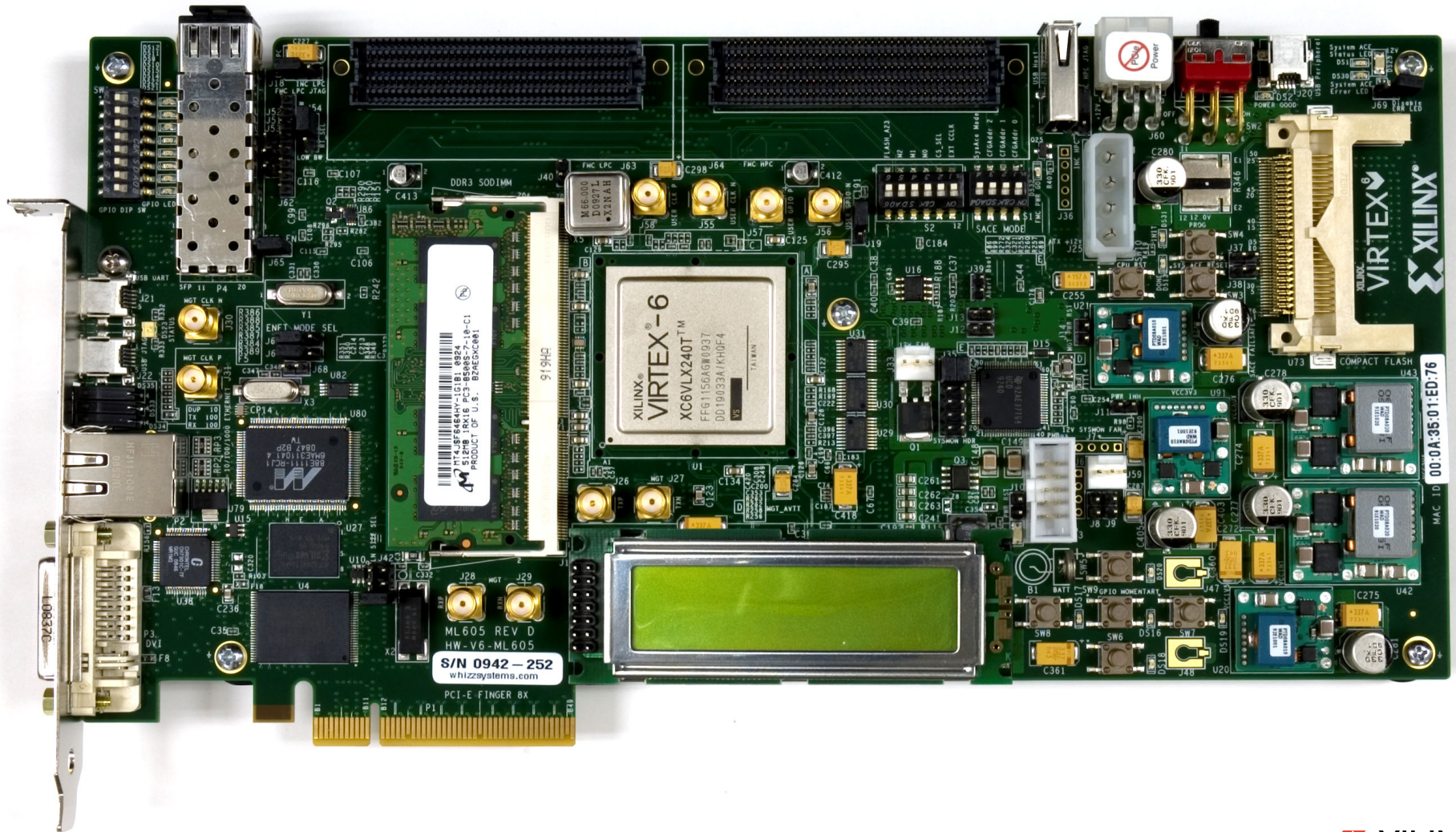
▪ Description

- The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Virtex-6 GTX transceivers. A graphical user interface is provided through the IBERT console window of the ChipScope Pro Analyzer

▪ Reference Design IP

- LogiCORE IBERT Example Designs
 - SFP (1), SGMII (1), SMA (1), PCIe (8), FMC_HPC (4), FMC_LPC (1)
- ChipScope Pro Analyzer
 - ChipScope Pro 11.4 Software and Cores User Guide (UG029)

Xilinx ML605 Board



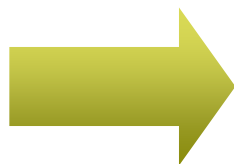
Software Requirements

- Xilinx ISE 11.4 software



ChipScope Pro Software Requirement

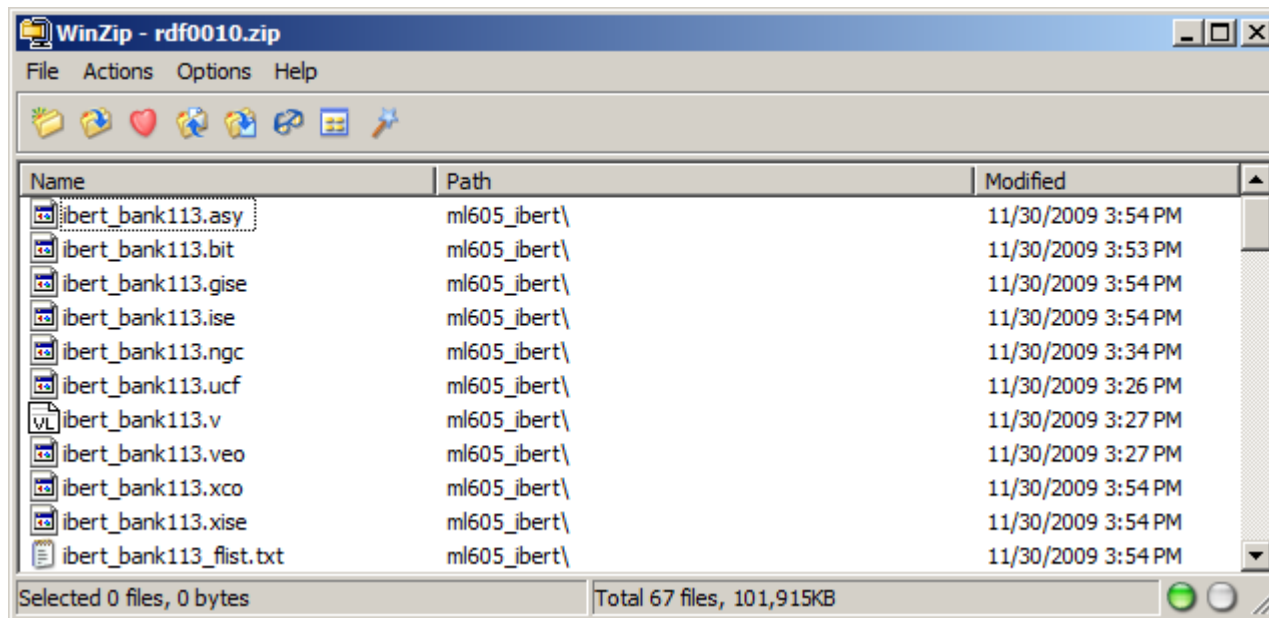
- Xilinx ChipScope Pro 11.4 software



Setup for the ML605 IBERT Designs

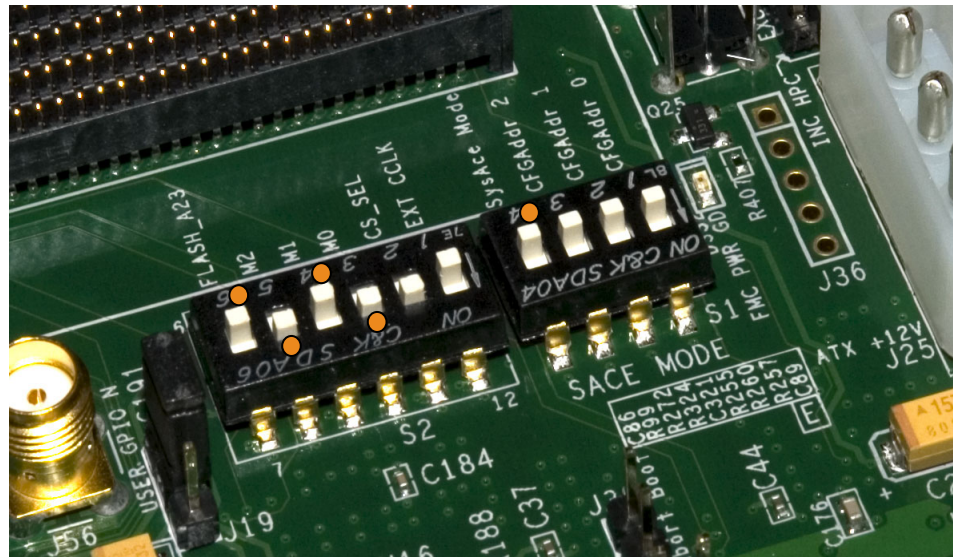
Setup for the ML605 IBERT Designs

- Unzip the rdf0010.zip file to your C:\ drive
 - <https://secure.xilinx.com/webreg/clickthrough.do?cid=139971>



Setup for the ML605 IBERT Designs

- **Set S2 to 0101XX (X = Don't care, 1 = on, Position 6 → Position 1)**
 - This selects JTAG
- **Set S1 to 0XXX (Position 4 → Position 1)**
 - This disables JTAG configuration from the Compact Flash



Setup for the ML605 IBERT Designs

- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board**
 - Connect this cable to your PC



Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- **SMA Cable**

- www.flrst.com
- P/N: ASPI-024-ASPI-S402



Setup for the ML605 IBERT Designs

■ Using the SMA cables:

- Connect J28 to J26
- Connect J29 to J27



Note: Presentation applies to the ML605

Setup for the ML605 IBERT Designs

- **Connect Optical Loopback Adapter**

- www.molex.com
- SFP Loopback Adapter, 3.5 db Attenuation
- Part # [74720-0501](#)
- Alternatively, use an SFP transceiver with a fiber optic cable

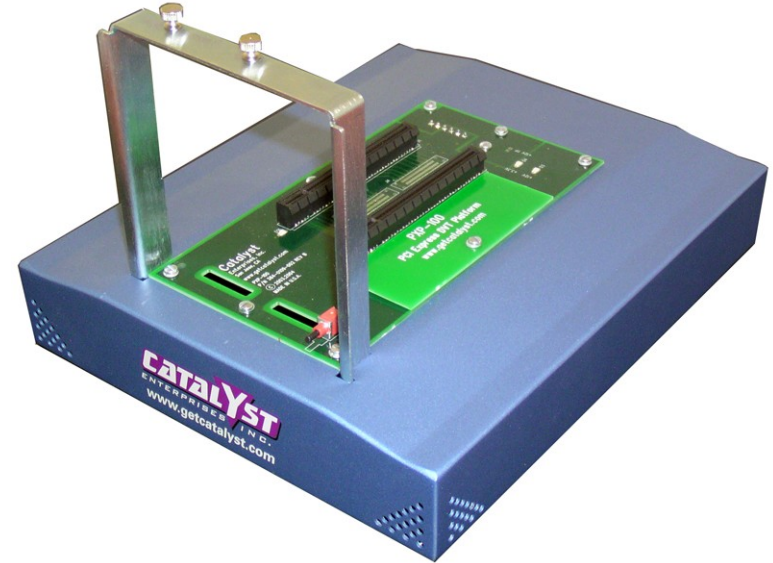
- **Insert into the SFP Connector on the ML605 board**



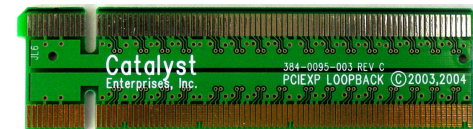
Setup for the ML605 IBERT Designs

- **PCIe Testing Hardware:**

- Catalyst [PXP-100 DVT](#) Platform

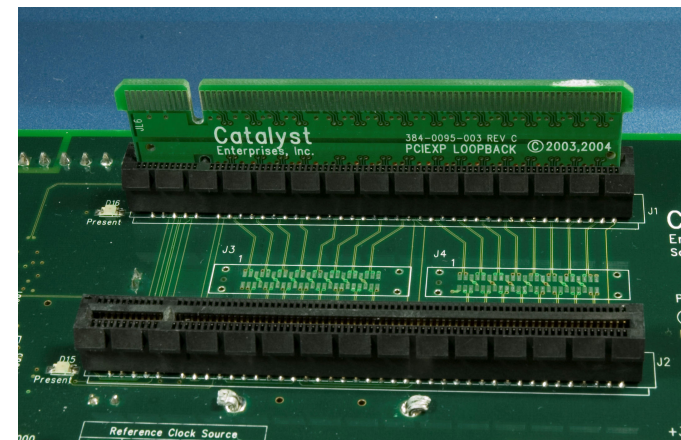
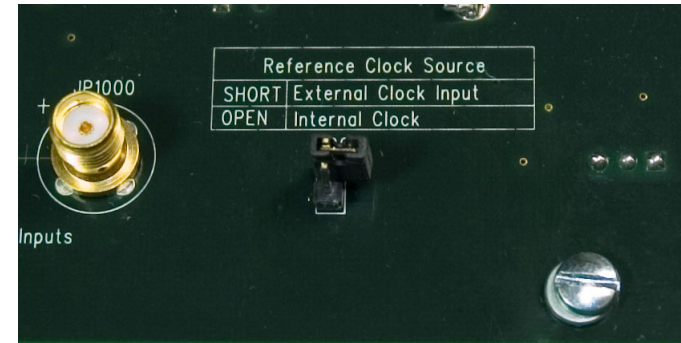


- **Catalyst [PELOOP-BACK](#)**

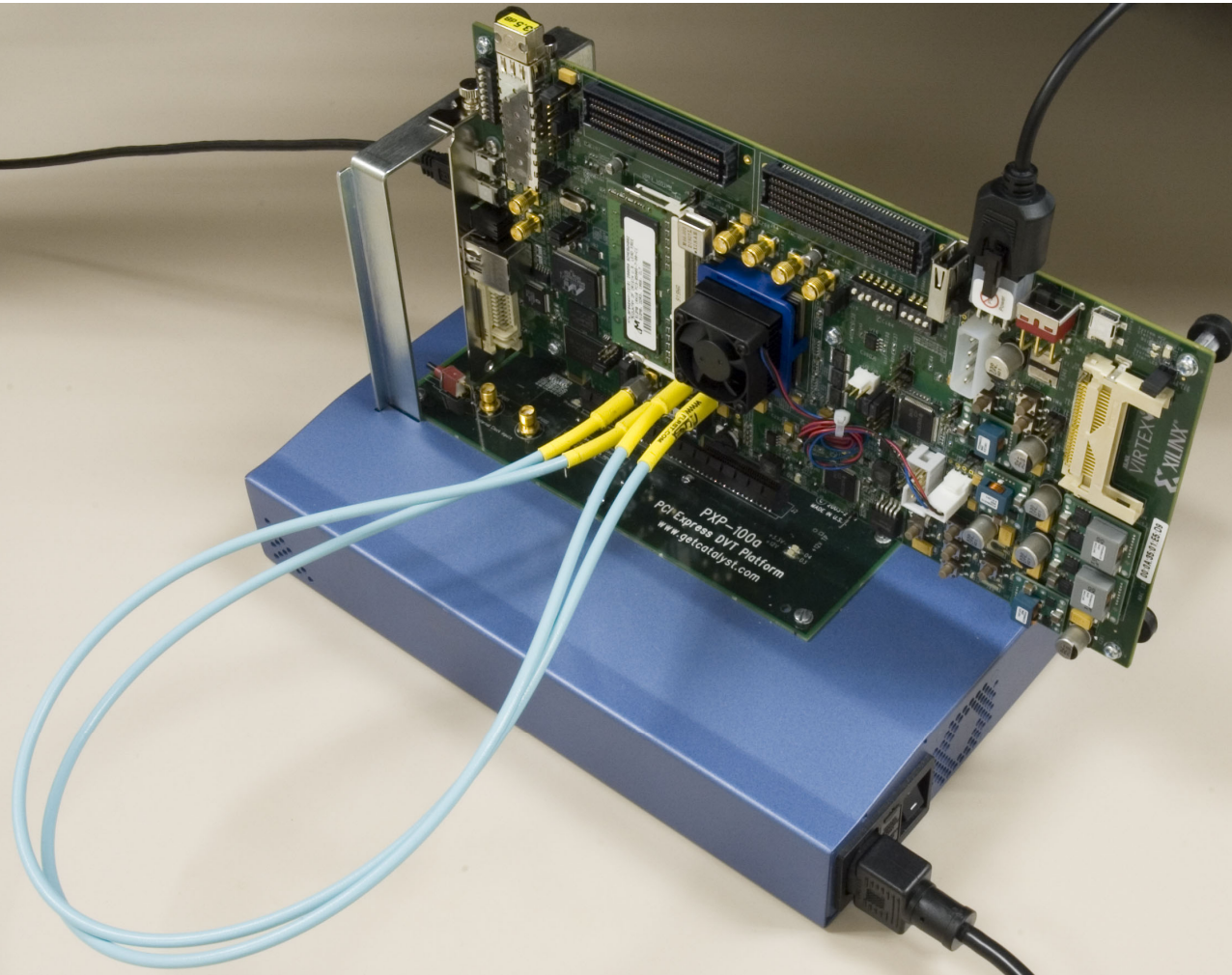


Setup for the ML605 IBERT Designs

- On the Catalyst, set the reference clock jumper to open
- Insert the PELOOP-BACK into one of the PCIe slots



Setup for the ML605 IBERT Designs

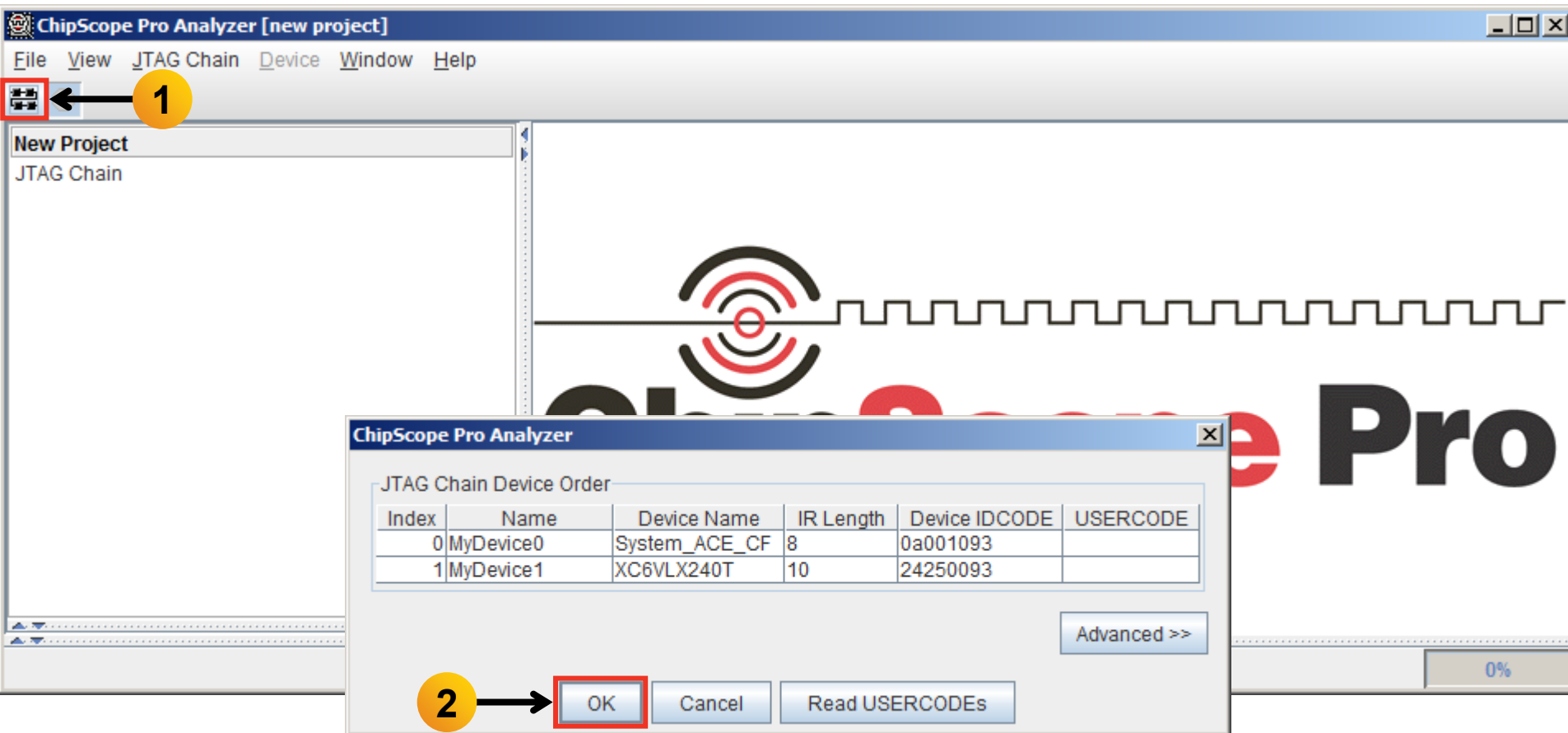


- Insert the ML605 into the other slot
- Connect the ML605 and Catalyst power
- Power up the ML605 and Catalyst

Running the ML605 IBERT Design – Bank 113

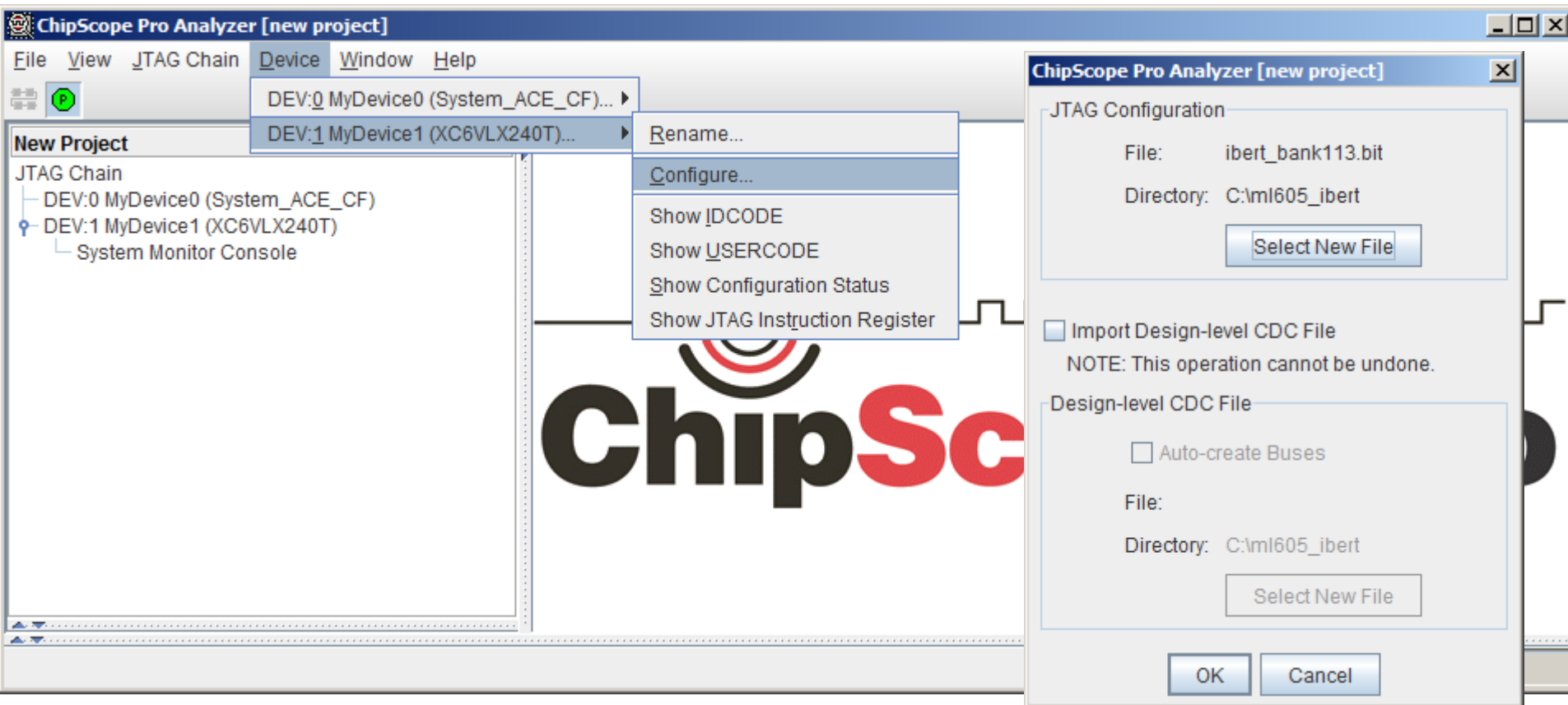
Running the ML605 IBERT Design – Bank 113

- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Running the ML605 IBERT Design – Bank 113

- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ibert_bank113.bit



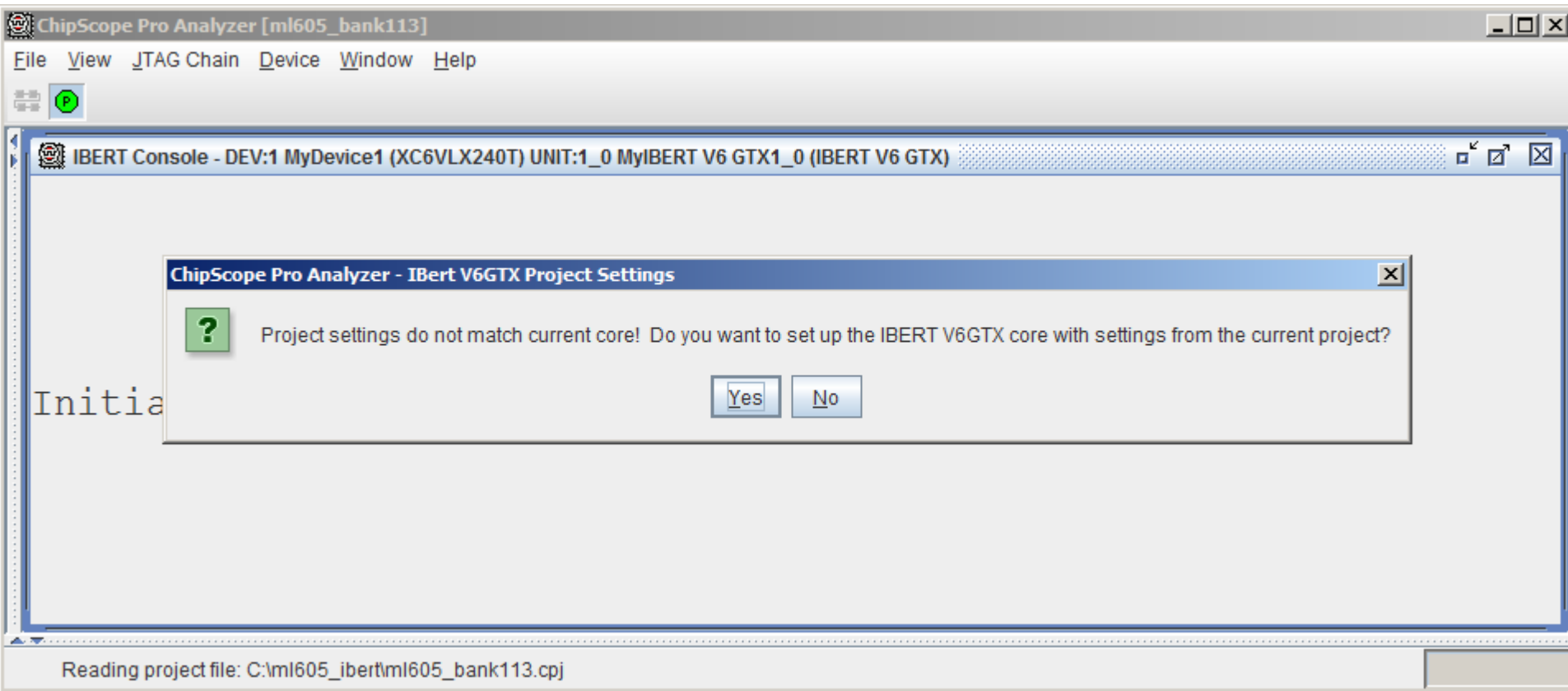
Running the ML605 IBERT Design – Bank 113

- **Select File → Open Project...**
- **Select <Design Path>\ml605_bank113.cpj**



Running the ML605 IBERT Design – Bank 113

- Click Yes on this Dialog



Running the ML605 IBERT Design – Bank 113

- Select the Reset All button (1)

The screenshot shows the ChipScope Pro Analyzer interface with the IBERT Console window open. The 'MGT/BERT Settings' tab is selected, displaying a table of settings for four GTX ports. A red box and arrow labeled '1' point to the 'Reset All' button in the top toolbar.

	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Settings				
– MGT Alias	GTX0_113	GTX1_113	GTX2_113	GTX3_113
– Tile Location	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
– MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps
– MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
– TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
– RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
– Loopback Mode	Near-End PCS	Near-End PCS	Near-End PCS	Near-End PCS

Reading project file: C:\ml605_ibert\ml605_bank113.cpj

Note: Bank 113: FMC HPC

Running the ML605 IBERT Design – Bank 113

- The line rate is 5.0 Gbps for all four GTXs (1)
- Near-End PCS is selected for all four GTXs (2)

ChipScope Pro Analyzer [ml605_bank113]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Settings				
MGT Alias	GTX0_113	GTX1_113	GTX2_113	GTX3_113
Tile Location	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps
MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	Near-End PCS	Near-End PCS	Near-End PCS	Near-End PCS

Reading project file: C:\ml605_ibert\ml605_bank113.cpj

Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 113

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

ChipScope Pro Analyzer [ml605_bank113]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
Channel Reset	Reset	Reset	Reset	Reset
TX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
TX Error Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	445 mV (0100)	445 mV (0100)	445 mV (0100)	445 mV (0100)
TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)
TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)
RX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
RX AC Coupling En...	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Reading project file: C:\ml605_ibert\ml605_bank113.cpj

Running the ML605 IBERT Design – Bank 113

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

ChipScope Pro Analyzer [ml605_bank113]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	5.043E-001	5.043E-001	5.043E-001	5.054E-001
RX Received Bit Co...	2.418E012	2.418E012	2.418E012	2.413E012
RX Bit Error Count	1.219E012	1.219E012	1.220E012	1.220E012
BERT Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ml605_ibert\ml605_bank113.cpj

Running the ML605 IBERT Design – Bank 113

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

ChipScope Pro Analyzer [ml605_bank113]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y4	GTX_X0Y5	GTX_X0Y6	GTX_X0Y7
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	8.101E-012	8.257E-012	8.529E-012	8.816E-012
RX Received Bit Co...	1.234E011	1.211E011	1.172E011	1.134E011
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset

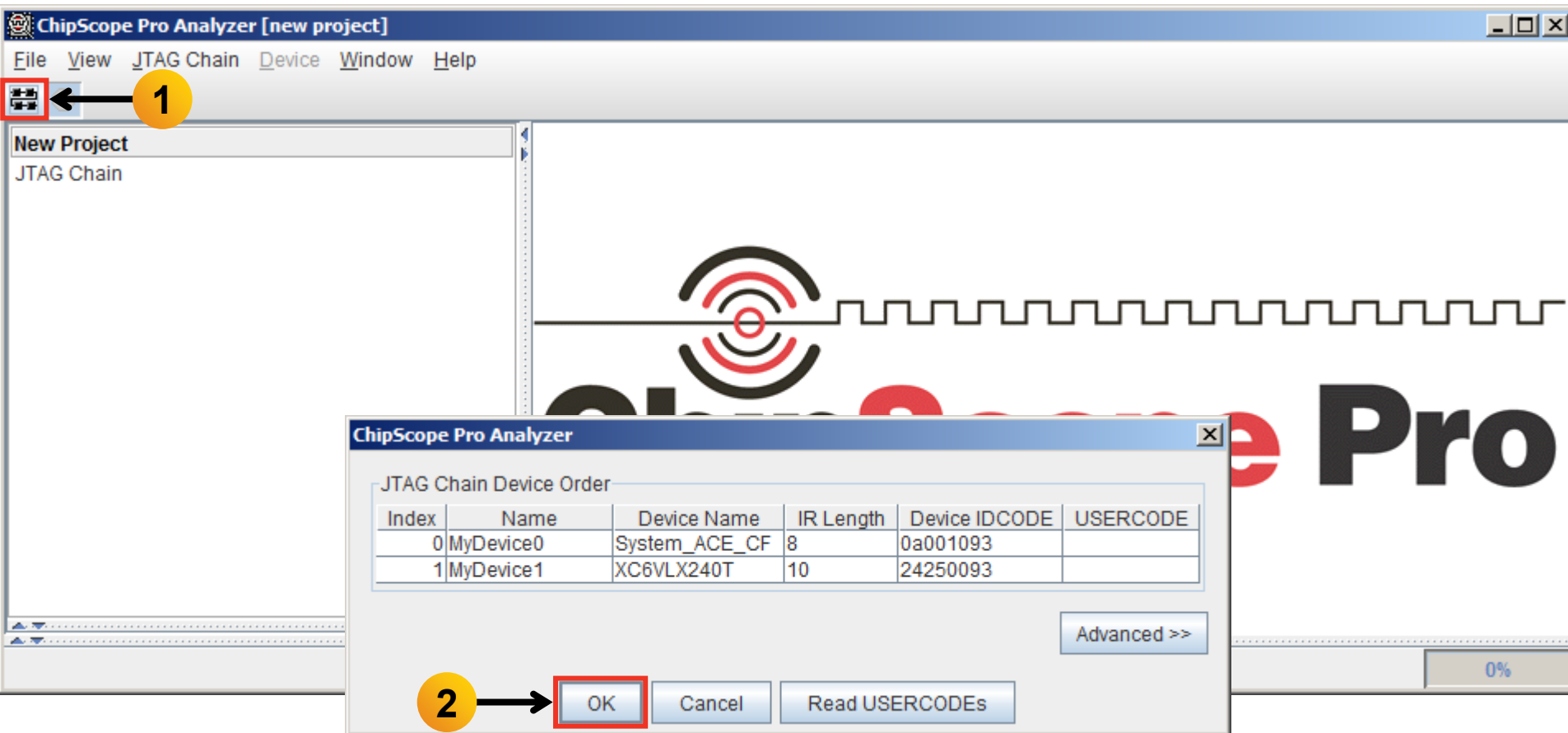
Reading project file: C:\ml605_ibert\ml605_bank113.cpj

1

Running the ML605 IBERT Design – Bank 114

Running the ML605 IBERT Design – Bank 114

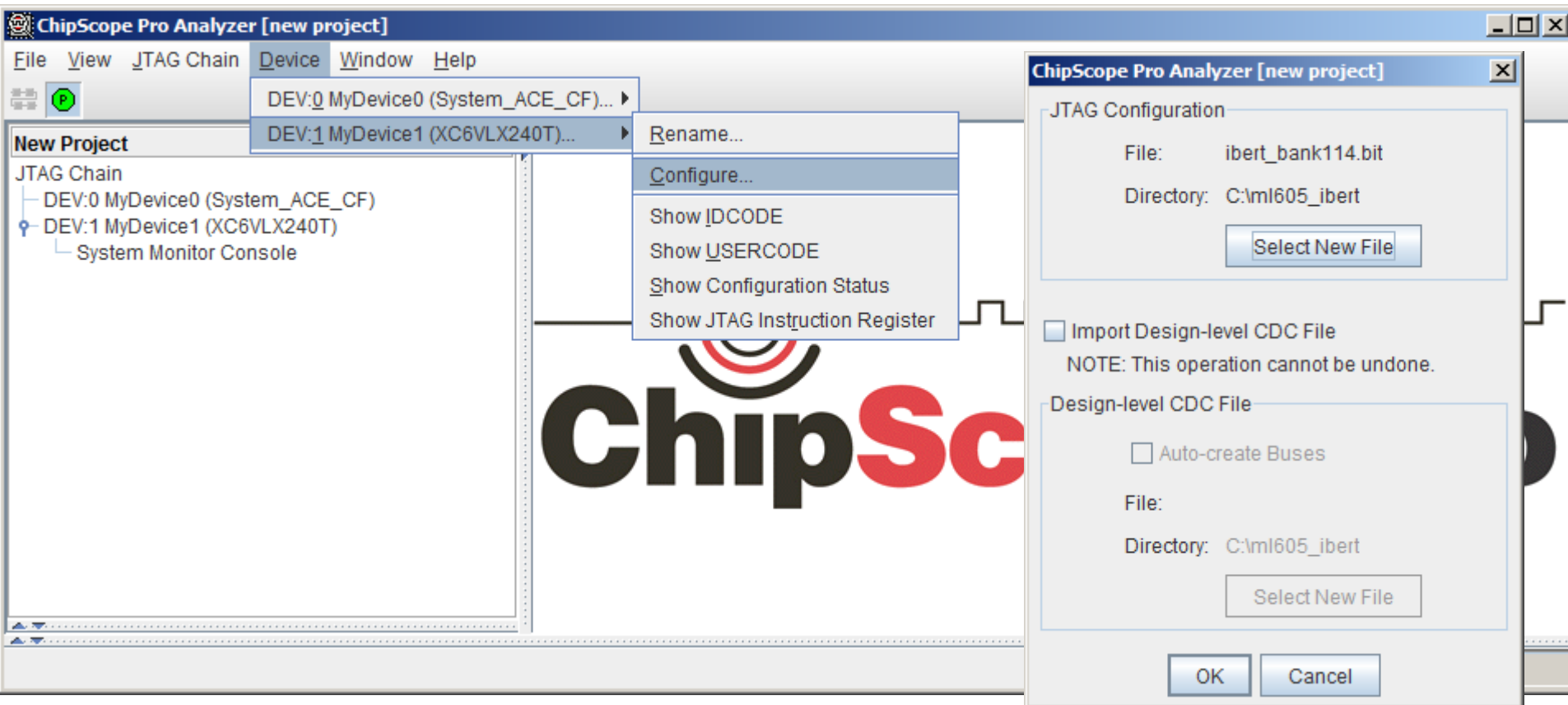
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the ML605

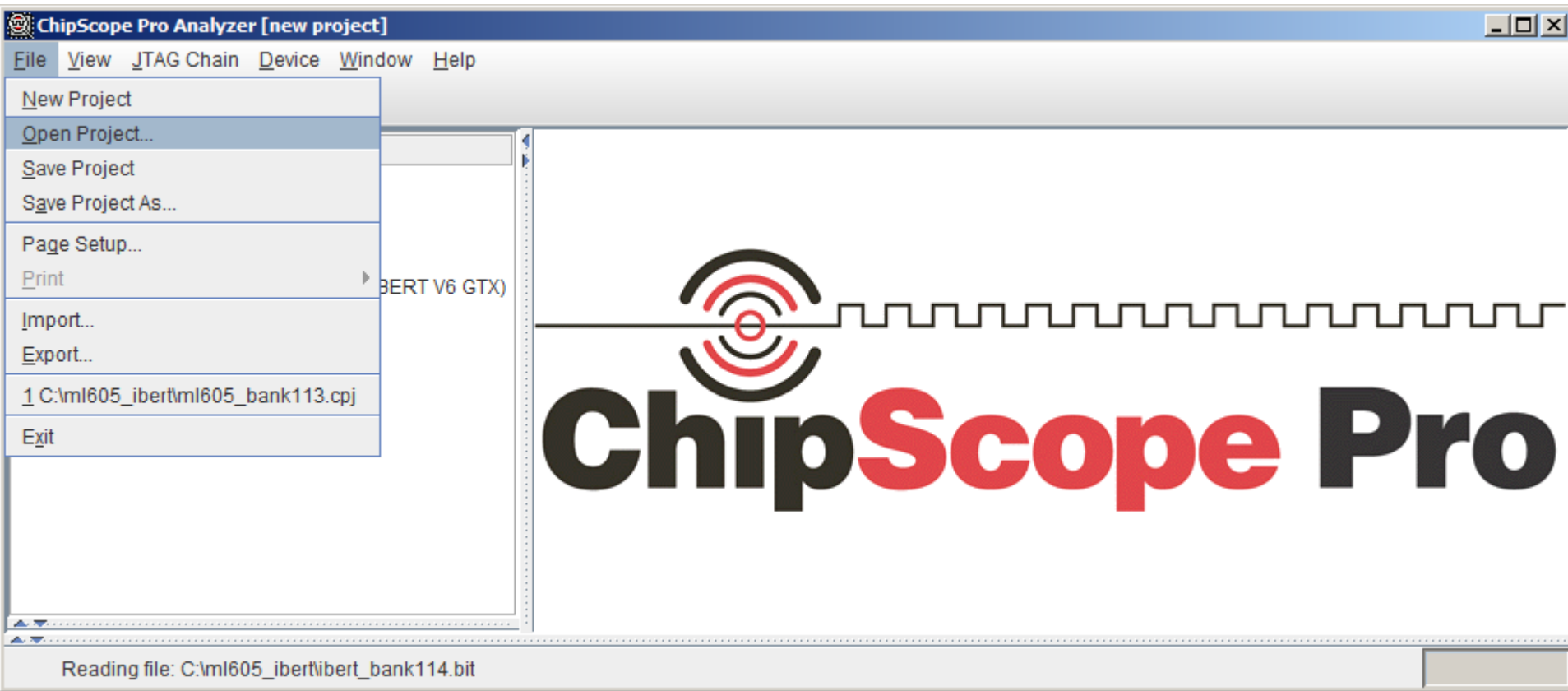
Running the ML605 IBERT Design – Bank 114

- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ibert_bank114.bit



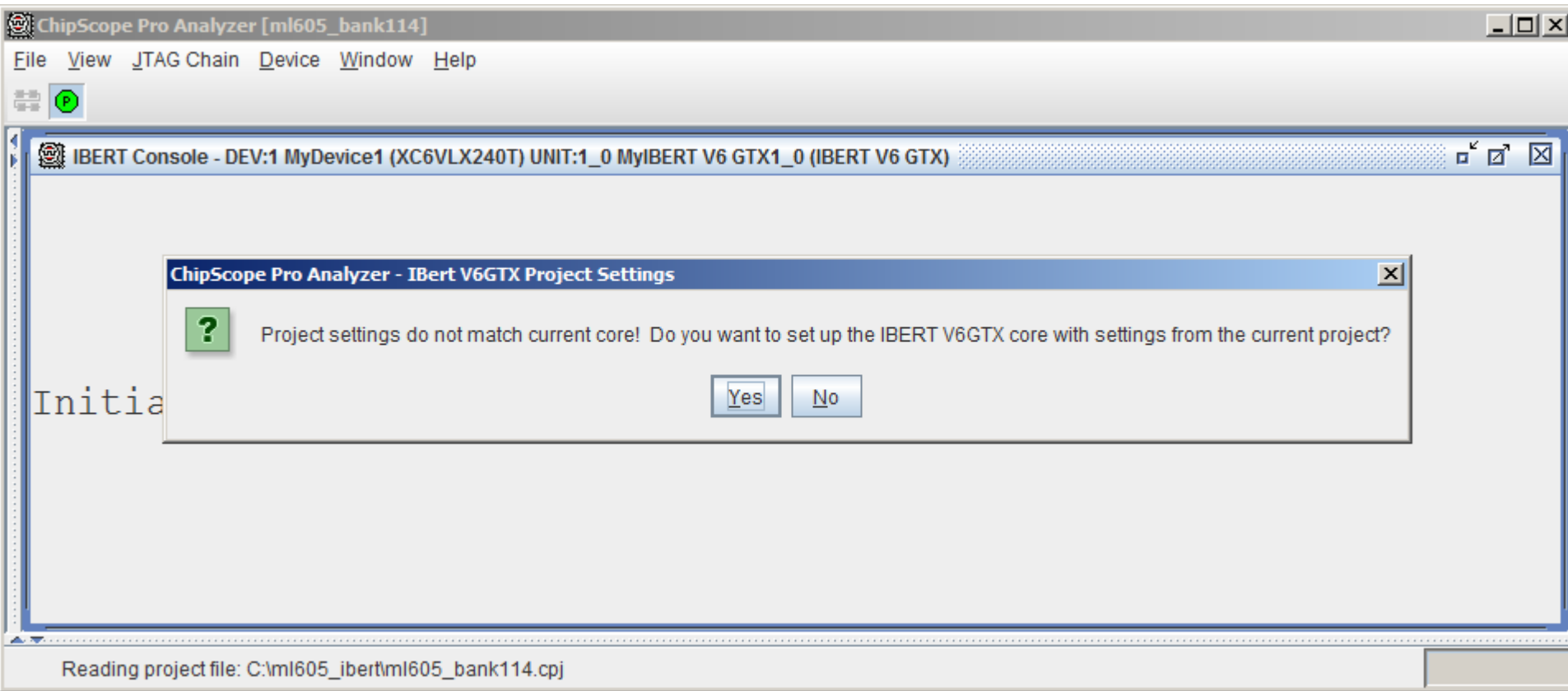
Running the ML605 IBERT Design – Bank 114

- Select File → Open Project...
- Select <Design Path>\ml605_bank114.cpj



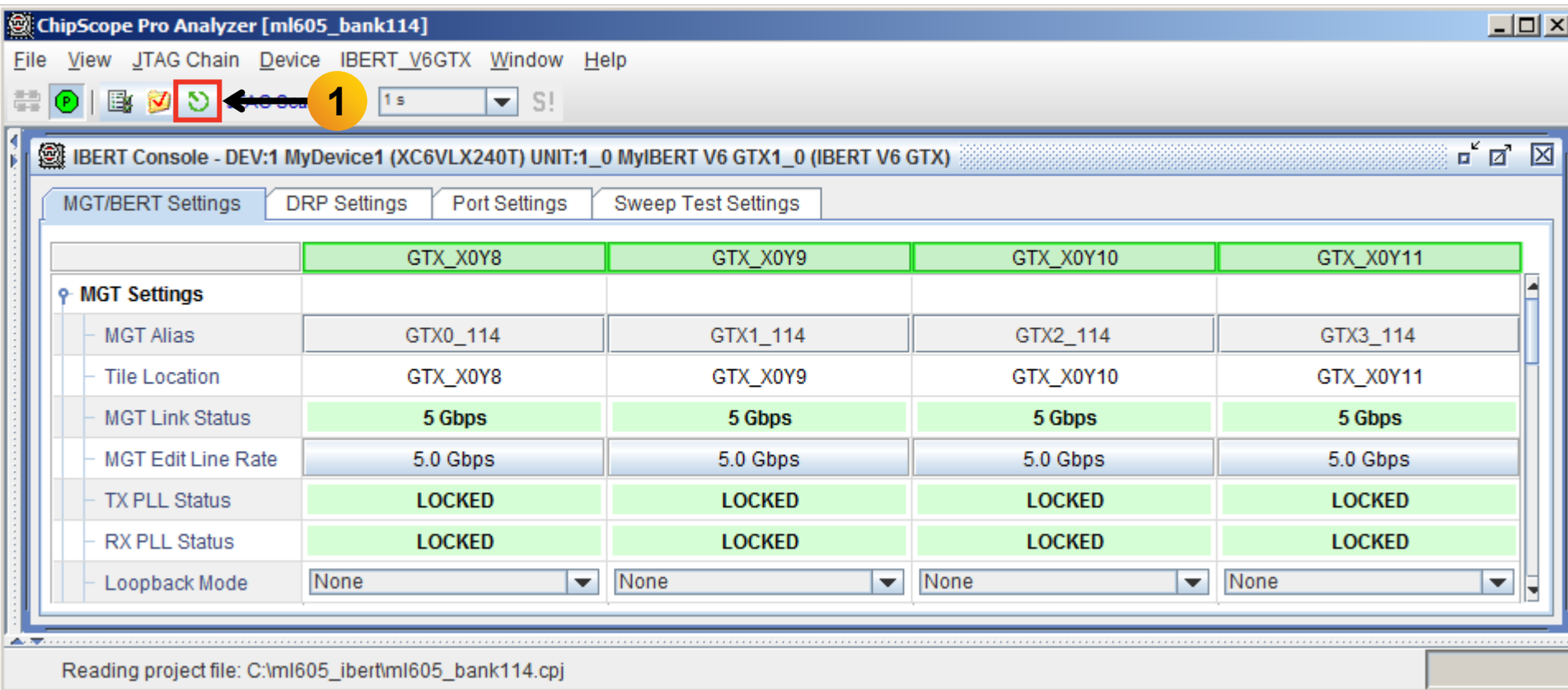
Running the ML605 IBERT Design – Bank 114

- Click Yes on this Dialog



Running the ML605 IBERT Design – Bank 114

- Select the Reset All button (1)



ChipScope Pro Analyzer [ml605_bank114]

File View JTAG Chain Device IBERT_V6GTX Window Help

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

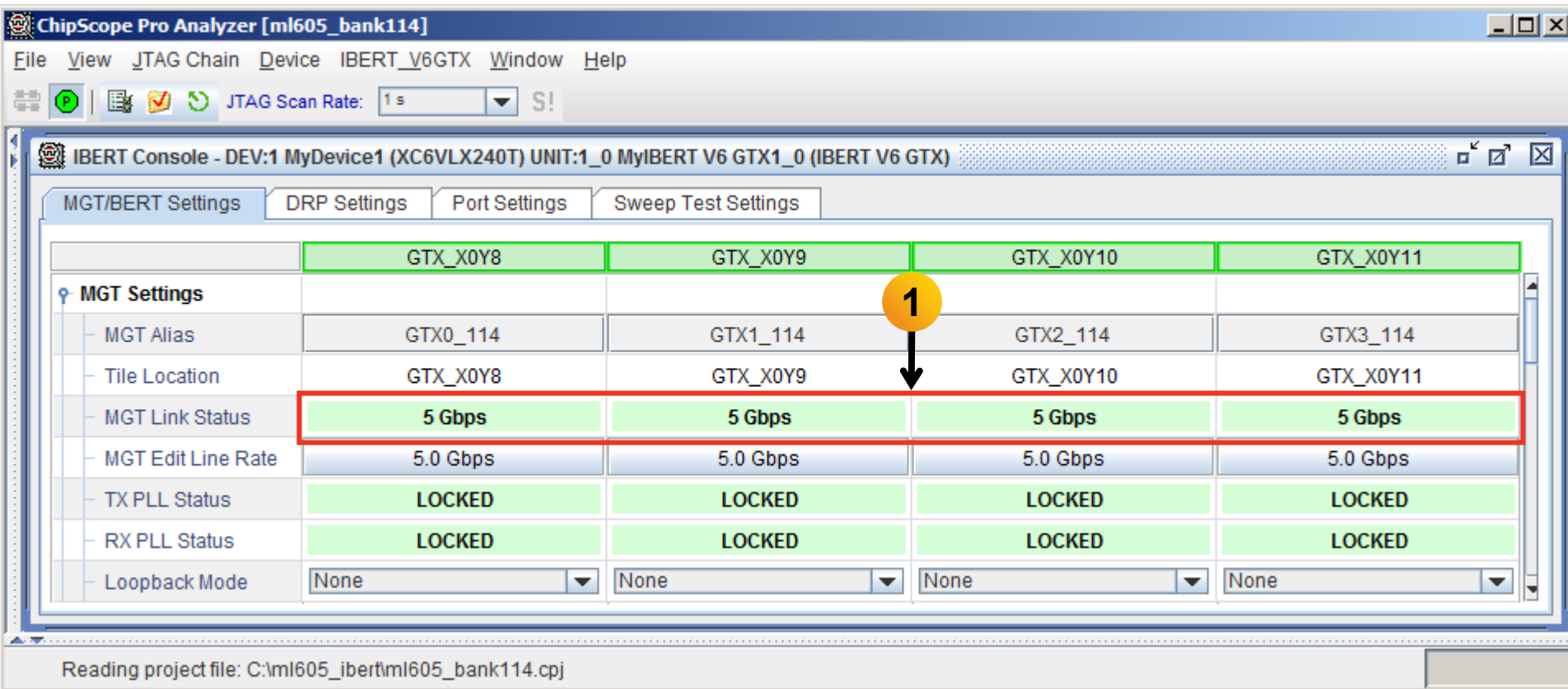
	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
MGT Settings				
– MGT Alias	GTX0_114	GTX1_114	GTX2_114	GTX3_114
– Tile Location	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
– MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps
– MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
– TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
– RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
– Loopback Mode	None	None	None	None

Reading project file: C:\ml605_ibert\ml605_bank114.cpj

Note: Bank 114: PCIe

Running the ML605 IBERT Design – Bank 114

- The line rate is 5.0 Gbps for all four GTXs (1)



ChipScope Pro Analyzer [ml605_bank114]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | **DRP Settings** | Port Settings | Sweep Test Settings

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
MGT Settings				
MGT Alias	GTX0_114	GTX1_114	GTX2_114	GTX3_114
Tile Location	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps
MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	None	None	None	None

Reading project file: C:\ml605_ibert\ml605_bank114.cpj

Running the ML605 IBERT Design – Bank 114

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

ChipScope Pro Analyzer [ml605_bank114]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/IBERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
Channel Reset	Reset	Reset	Reset	Reset
TX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
TX Error Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	445 mV (0100)	445 mV (0100)	445 mV (0100)	445 mV (0100)
TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)
TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)
RX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
RX AC Coupling En...	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Reading project file: C:\ml605_ibert\ml605_bank114.cpj

Running the ML605 IBERT Design – Bank 114

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

ChipScope Pro Analyzer [ml605_bank114]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	3.767E-001	2.860E-001	4.799E-001	2.149E-008
RX Received Bit Co...	4.871E012	4.872E012	4.872E012	4.872E012
RX Bit Error Count	1.835E012	1.393E012	2.338E012	1.047E005
BERT Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ml605_ibert\ml605_bank114.cpj

Running the ML605 IBERT Design – Bank 114

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

The screenshot shows the ChipScope Pro Analyzer window titled "ChipScope Pro Analyzer [ml605_bank114]". The "IBERT Console" tab is active, displaying settings for "DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)". The "MGT/BERT Settings" tab is selected, showing a table of settings for four GTX channels: GTX_X0Y8, GTX_X0Y9, GTX_X0Y10, and GTX_X0Y11. The "RX Bit Error Count" row is highlighted with a red box, and a yellow circle with the number 1 is placed below it, with an arrow pointing to the "Reset" button for the first channel.

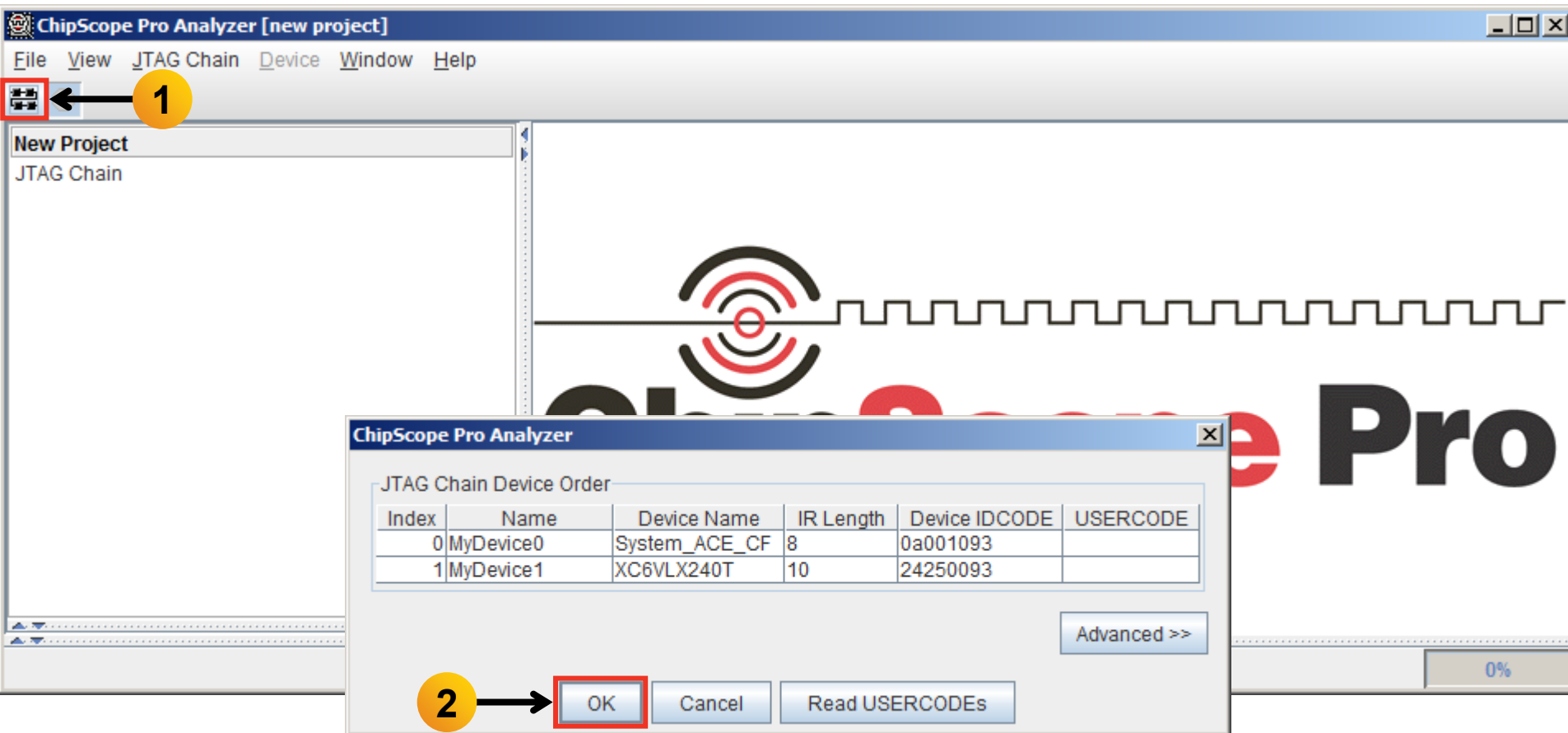
	GTX_X0Y8	GTX_X0Y9	GTX_X0Y10	GTX_X0Y11
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	9.563E-012	9.233E-012	8.857E-012	8.085E-012
RX Received Bit Co...	1.046E011	1.083E011	1.129E011	1.237E011
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ml605_ibert\ml605_bank114.cpj

Running the ML605 IBERT Design – Bank 115

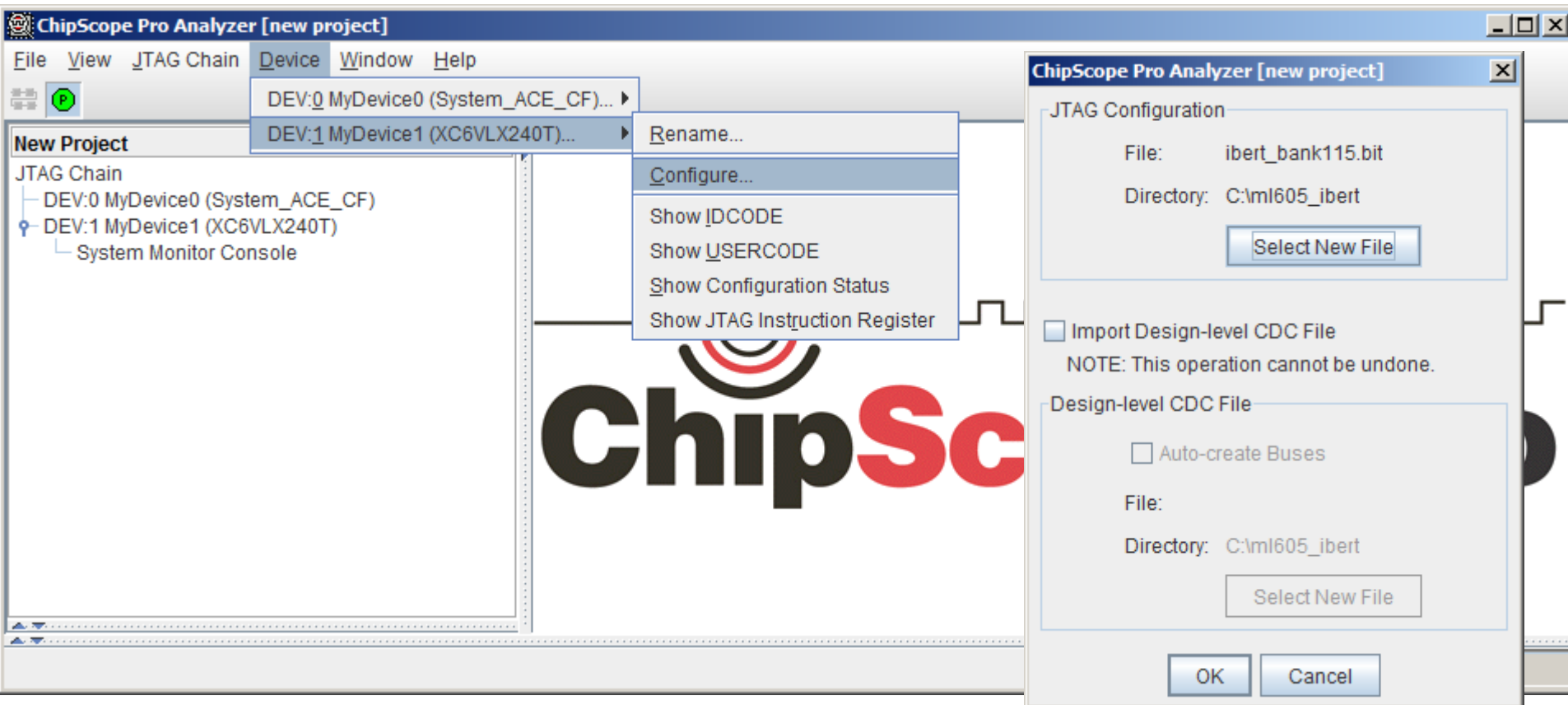
Running the ML605 IBERT Design – Bank 115

- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



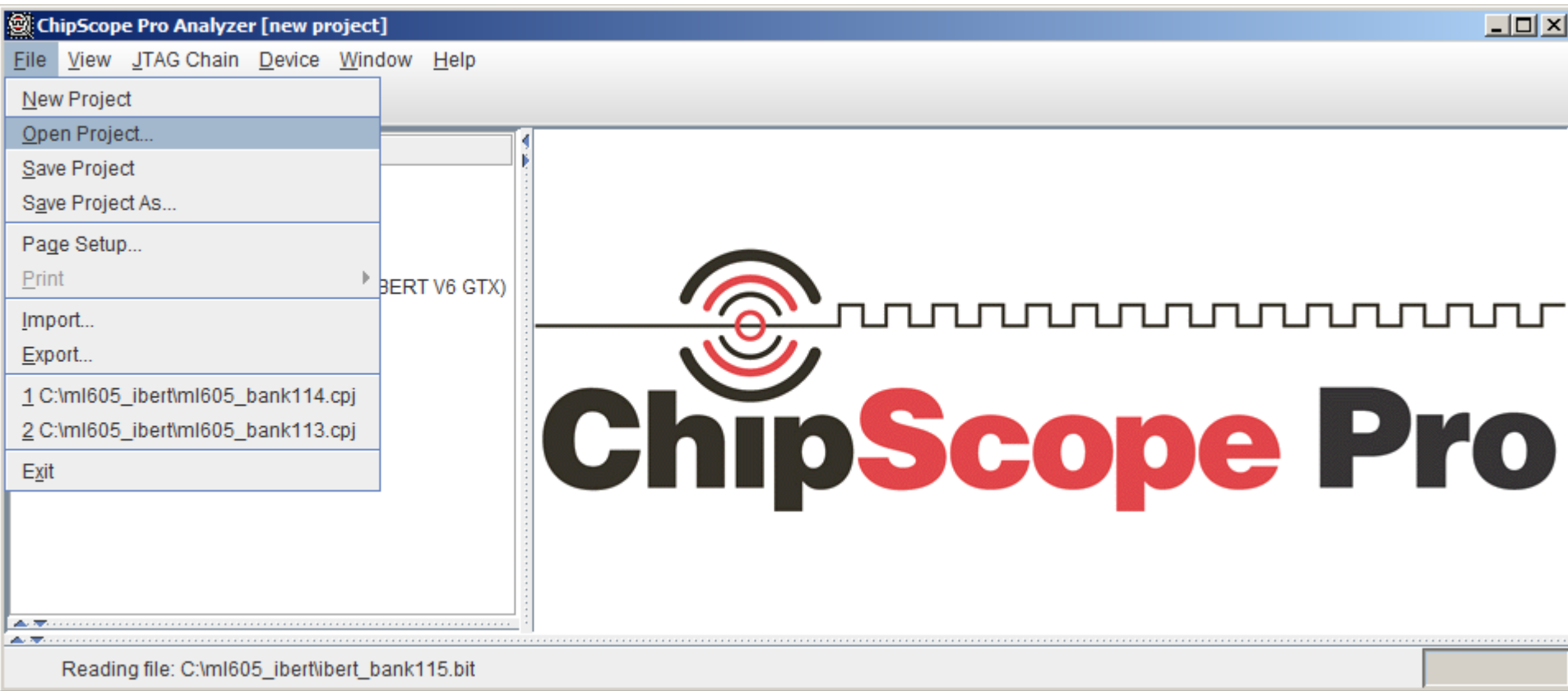
Running the ML605 IBERT Design – Bank 115

- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ibert_bank115.bit



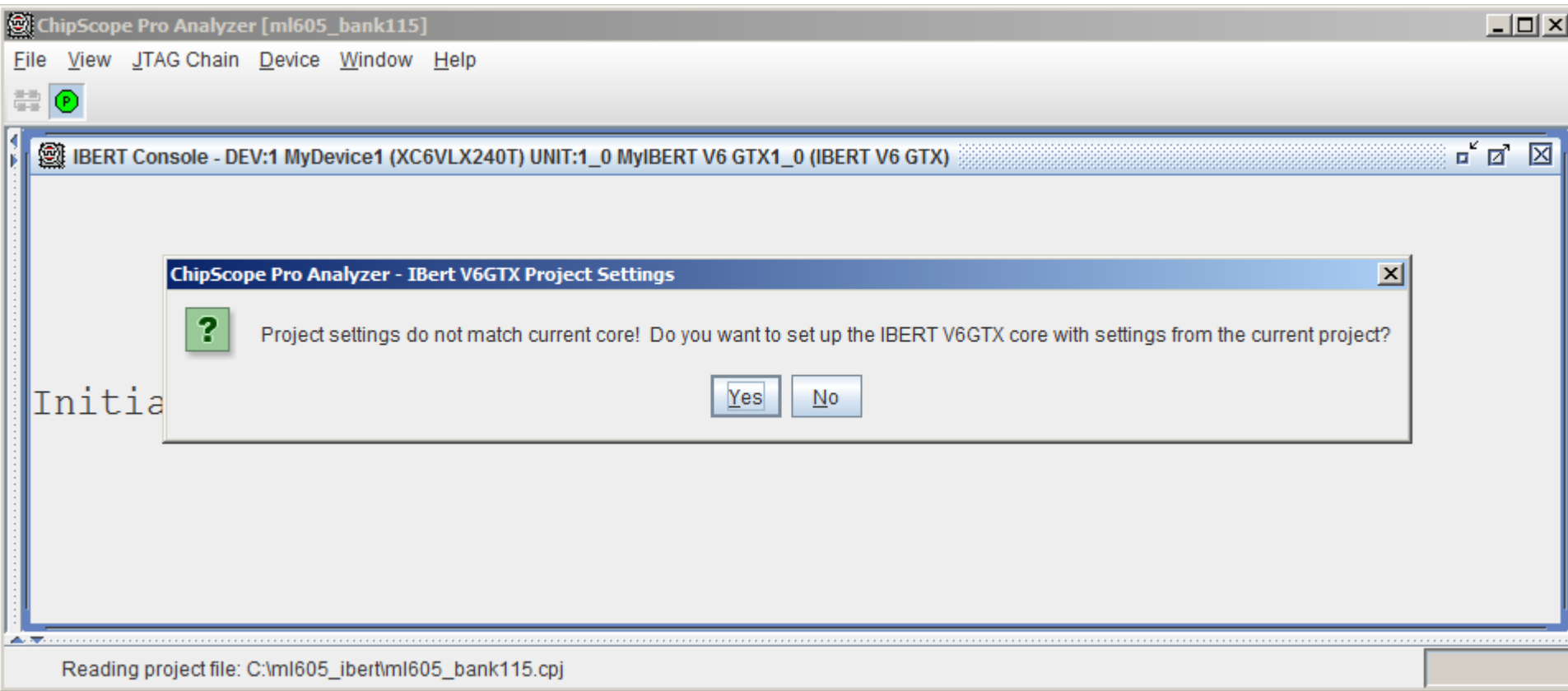
Running the ML605 IBERT Design – Bank 115

- Select File → Open Project...
- Select <Design Path>\ml605_bank115.cpj



Running the ML605 IBERT Design – Bank 115

- Click Yes on this Dialog



Running the ML605 IBERT Design – Bank 115

- Select the Reset All button (1)

ChipScope Pro Analyzer [ml605_bank115]

File View JTAG Chain Device IBERT_V6GTX Window Help

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

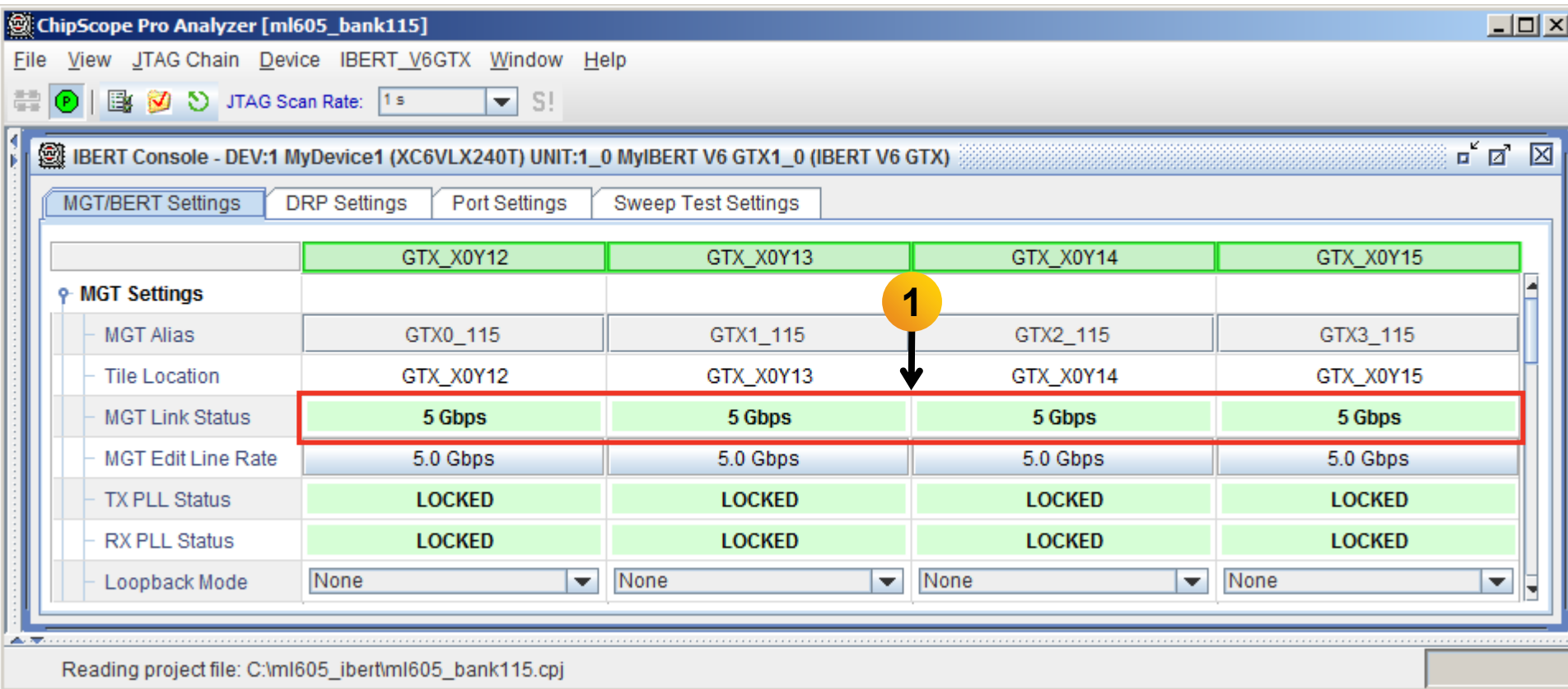
	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Settings				
MGT Alias	GTX0_115	GTX1_115	GTX2_115	GTX3_115
Tile Location	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Link Status	5 Gbps	No Link	5 Gbps	No Link
MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	None	None	None	None

Reading project file: C:\ml605_ibert\ml605_bank115.cpj

Note: Bank 115: PCIe

Running the ML605 IBERT Design – Bank 115

- The line rate is 5 Gbps for all four GTXs (1)



ChipScope Pro Analyzer [ml605_bank115]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Settings				
MGT Alias	GTX0_115	GTX1_115	GTX2_115	GTX3_115
Tile Location	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Link Status	5 Gbps	5 Gbps	5 Gbps	5 Gbps
MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	5.0 Gbps
TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	None	None	None	None

Reading project file: C:\ml605_ibert\ml605_bank115.cpj

Running the ML605 IBERT Design – Bank 115

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2

ChipScope Pro Analyzer [ml605_bank115]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/IBERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
Channel Reset	Reset	Reset	Reset	Reset
TX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
TX Error Inject	Inject	Inject	Inject	Inject
TX Diff Output Swing	445 mV (0100)	445 mV (0100)	445 mV (0100)	445 mV (0100)
TX Pre-Emphasis	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)	0.250 dB (0010)
TX Post-Emphasis	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)	0.000 dB (00000)
RX Polarity Invert	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
RX AC Coupling En...	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Reading project file: C:\ml605_ibert\ml605_bank115.cpj

Running the ML605 IBERT Design – Bank 115

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

ChipScope Pro Analyzer [ml605_bank115]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	5.902E-012	5.906E-012	5.910E-012	5.913E-012
RX Received Bit Co...	1.694E011	1.693E011	1.692E011	1.691E011
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ml605_ibert\ml605_bank115.cpj

Running the ML605 IBERT Design – Bank 115

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

ChipScope Pro Analyzer [ml605_bank115]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y12	GTX_X0Y13	GTX_X0Y14	GTX_X0Y15
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	1.198E-012	1.199E-012	1.199E-012	1.199E-012
RX Received Bit Co...	8.344E011	8.343E011	8.342E011	8.341E011
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset

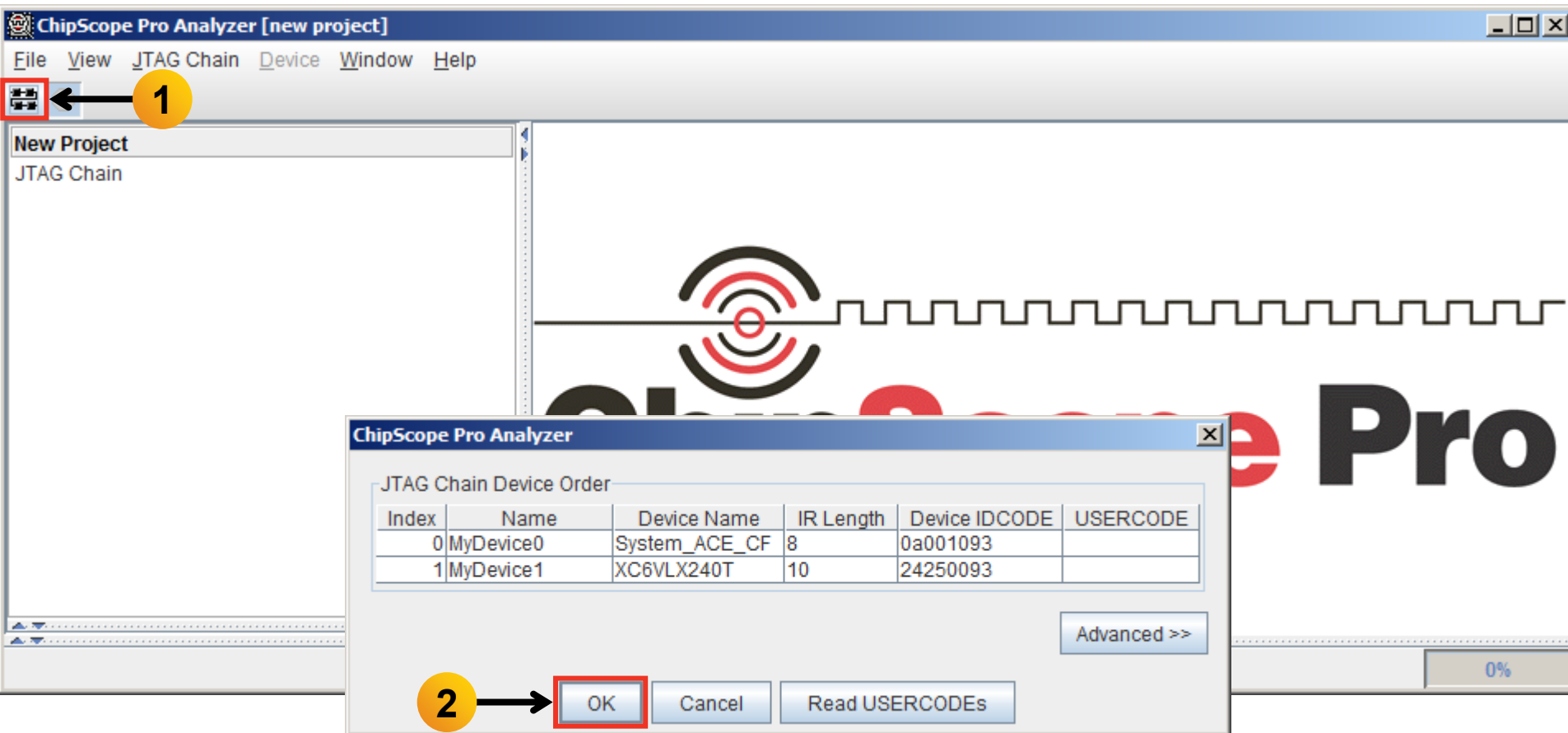
Reading project file: C:\ml605_ibert\ml605_bank115.cpj

1

Running the ML605 IBERT Design – Bank 116

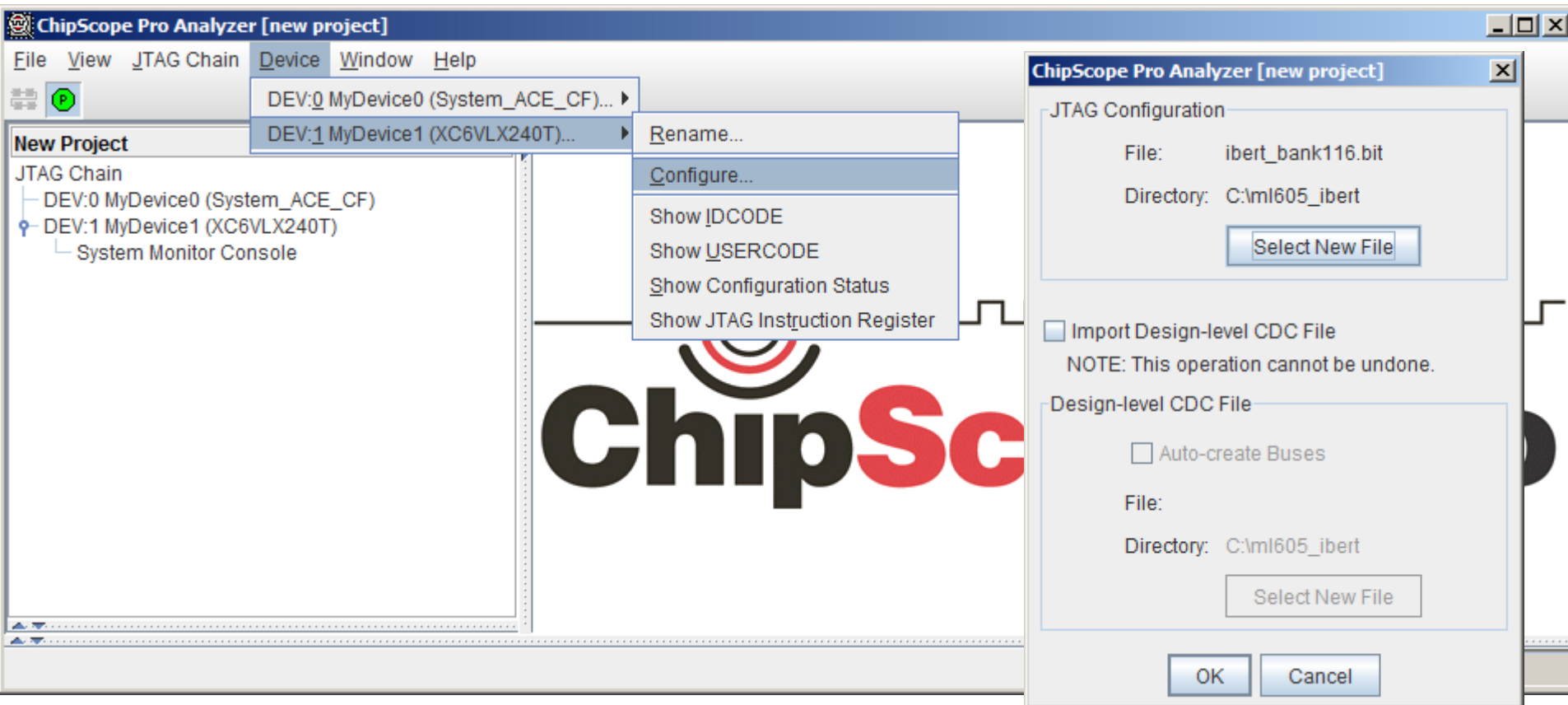
Running the ML605 IBERT Design – Bank 116

- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



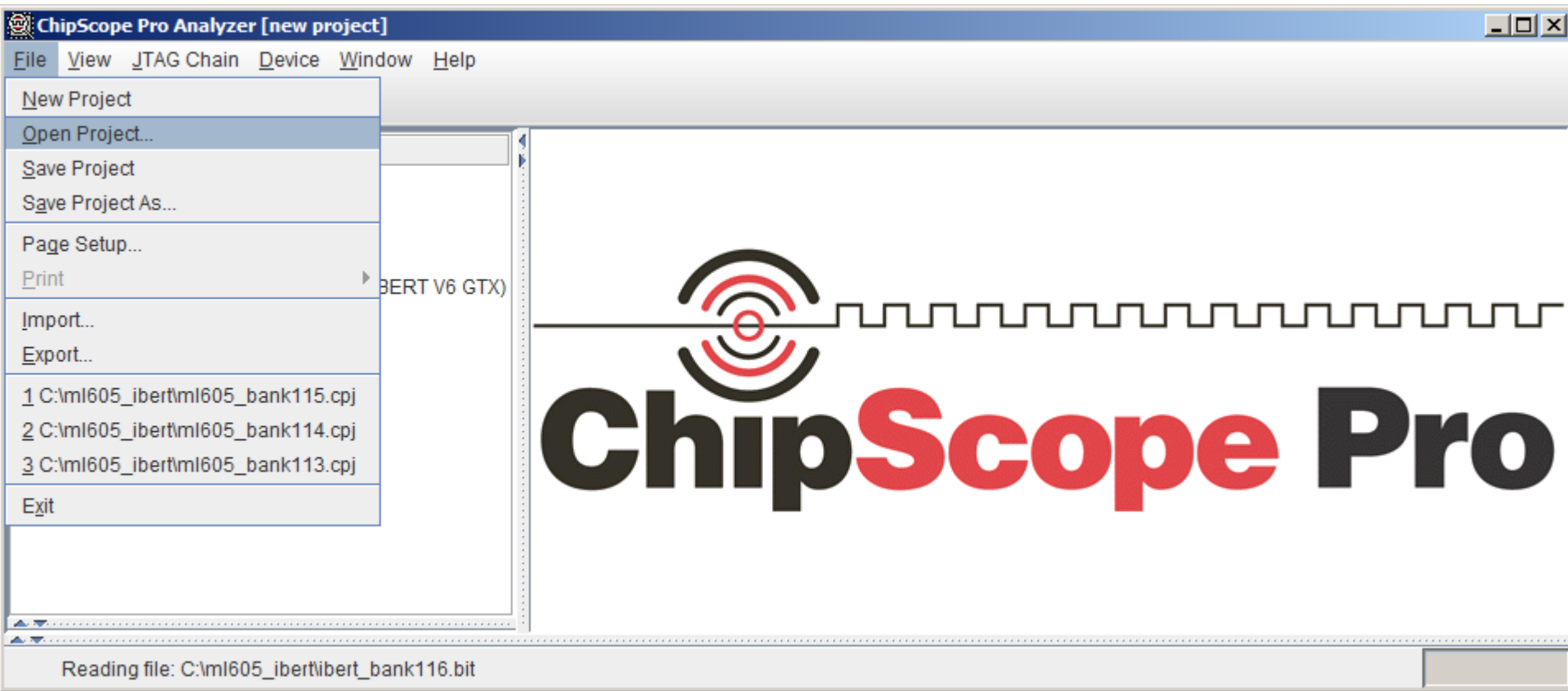
Running the ML605 IBERT Design – Bank 116

- Select Device → DEV:1 MyDevice1 (XC6VLX240T) → Configure...
- Select <Design Path>\ibert_bank116.bit



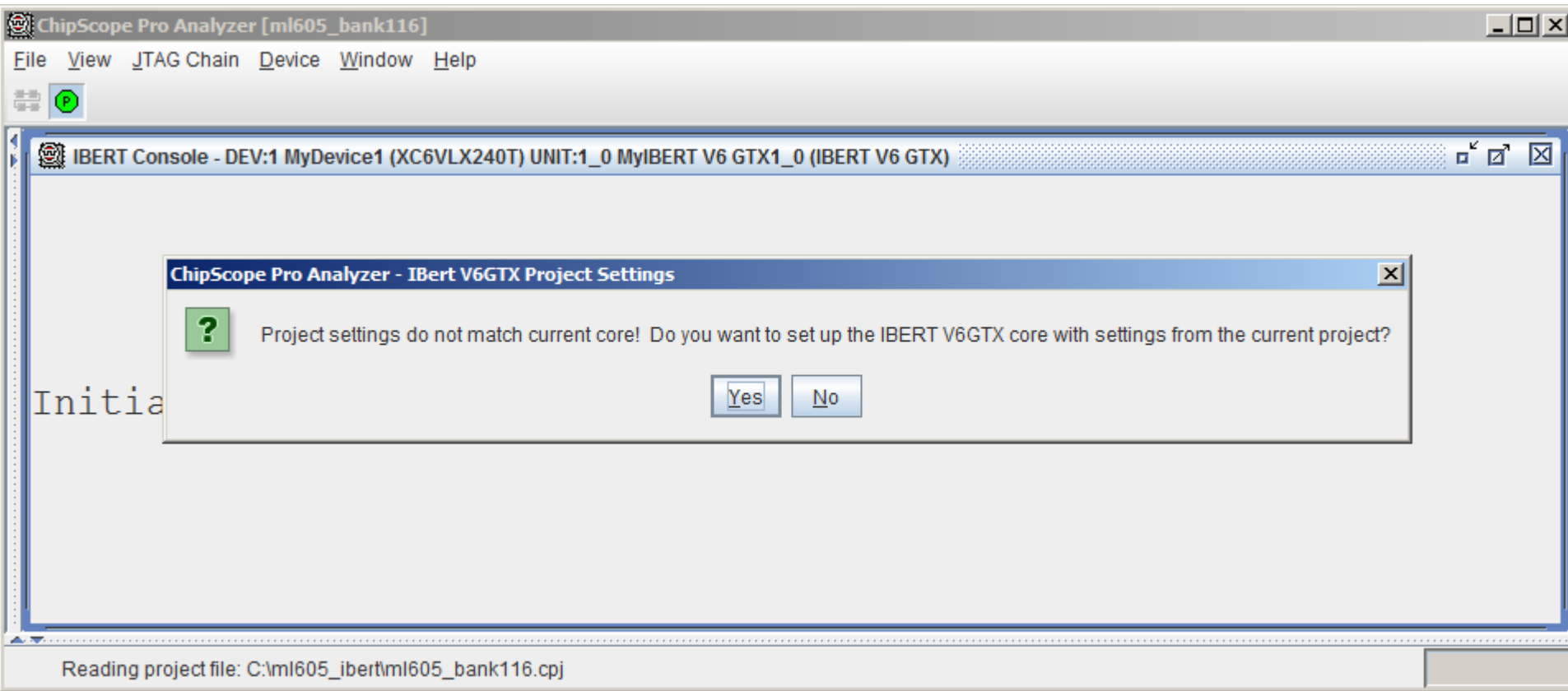
Running the ML605 IBERT Design – Bank 116

- Select File → Open Project...
- Select <Design Path>\ml605_bank116.cpj



Running the ML605 IBERT Design – Bank 116

- Click Yes on this Dialog



Running the ML605 IBERT Design – Bank 116

- Select the Reset All button (1)

ChipScope Pro Analyzer [ml605_bank116]

File View JTAG Chain Device IBERT_V6GTX Window Help

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19
MGT Settings				
MGT Alias	GTX0_116	GTX1_116	GTX2_116	GTX3_116
Tile Location	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19
MGT Link Status	5 Gbps	No Link	5 Gbps	1.25 Gbps
MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	1.25 Gbps
TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	Near-End PCS	None	None	Near-End PMA

Reading project file: C:\ml605_ibert\ml605_bank116.cpj

Note: Bank 116: FMC_LPC, SFP, SMA, SGMII

Running the ML605 IBERT Design – Bank 116

- The line rates are 5.0 and 1.25 Gbps for the four GTXs (1)
- Near-End PCS and PMA is selected for FMC and SGMII (2)

ChipScope Pro Analyzer [ml605_bank116]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

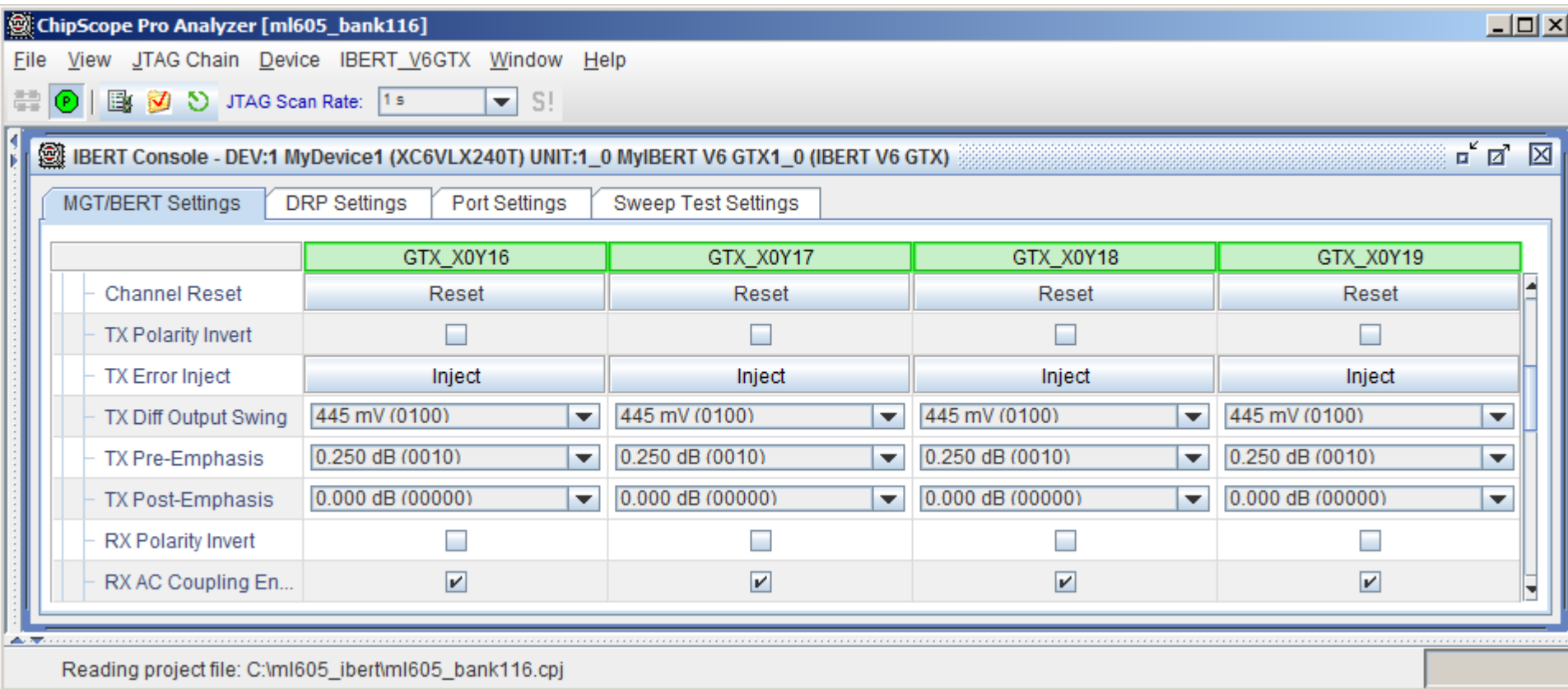
MGT/BERT Settings | DRP Settings | Port Settings | Sweep Test Settings

	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19
MGT Settings				
MGT Alias	GTX0_116	GTX1_116	GTX2_116	GTX3_116
Tile Location	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19
MGT Link Status	5 Gbps	5 Gbps	5 Gbps	1.25 Gbps
MGT Edit Line Rate	5.0 Gbps	5.0 Gbps	5.0 Gbps	1.25 Gbps
TX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
RX PLL Status	LOCKED	LOCKED	LOCKED	LOCKED
Loopback Mode	Near-End PCS	None	None	Near-End PMA

Reading project file: C:\ml605_ibert\ml605_bank116.cpj

Running the ML605 IBERT Design – Bank 116

- TX Diff Output Swing = 4
- TX Pre-Emphasis = 2



Note: Presentation applies to the ML605

Running the ML605 IBERT Design – Bank 116

- TX/RX Data Patterns are set to PRBS 7-bit (1)
- Click BERT Reset buttons (2)

ChipScope Pro Analyzer [ml605_bank116]

File View JTAG Chain Device IBERT_V6GTX Window Help

JTAG Scan Rate: 1 s S!

IBERT Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1_0 MyIBERT V6 GTX1_0 (IBERT V6 GTX)

MGT/BERT Settings DRP Settings Port Settings Sweep Test Settings

	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	2.267E-012	2.268E-012	2.268E-012	9.074E-012
RX Received Bit Co...	4.411E011	4.410E011	4.409E011	1.102E011
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ml605_ibert\ml605_bank116.cpj

Running the ML605 IBERT Design – Bank 116

- View the RX Bit Error Count (1)
- Close ChipScope Pro Analyzer and cycle ML605 board power

The screenshot shows the ChipScope Pro Analyzer window for the project 'ml605_bank116'. The IBERT Console is open, displaying the MGT/BERT Settings tab. The console shows the RX Bit Error Count for four GTX channels (GTX_X0Y16, GTX_X0Y17, GTX_X0Y18, and GTX_X0Y19). The RX Bit Error Count is 0.000E000 for all channels, which is highlighted with a red box. A yellow circle with the number 1 and an arrow points to the RX Bit Error Count row.

	GTX_X0Y16	GTX_X0Y17	GTX_X0Y18	GTX_X0Y19
MGT Settings				
BERT Settings				
TX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Data Pattern	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	1.307E-012	1.314E-012	1.320E-012	5.304E-012
RX Received Bit Co...	7.651E011	7.608E011	7.574E011	1.885E011
RX Bit Error Count	0.000E000	0.000E000	0.000E000	0.000E000
BERT Reset	Reset	Reset	Reset	Reset

Reading project file: C:\ml605_ibert\ml605_bank116.cpj

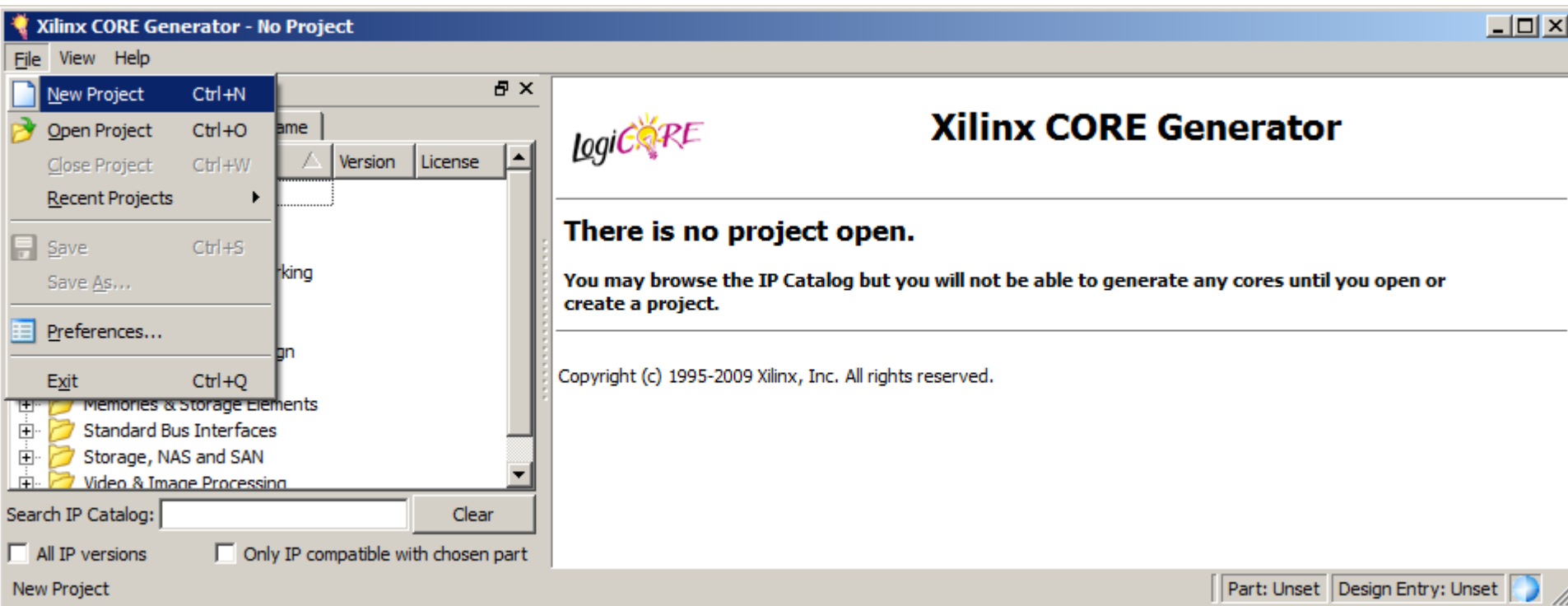
ML605 IBERT Design Creation

Create IBERT CORE Generator Project

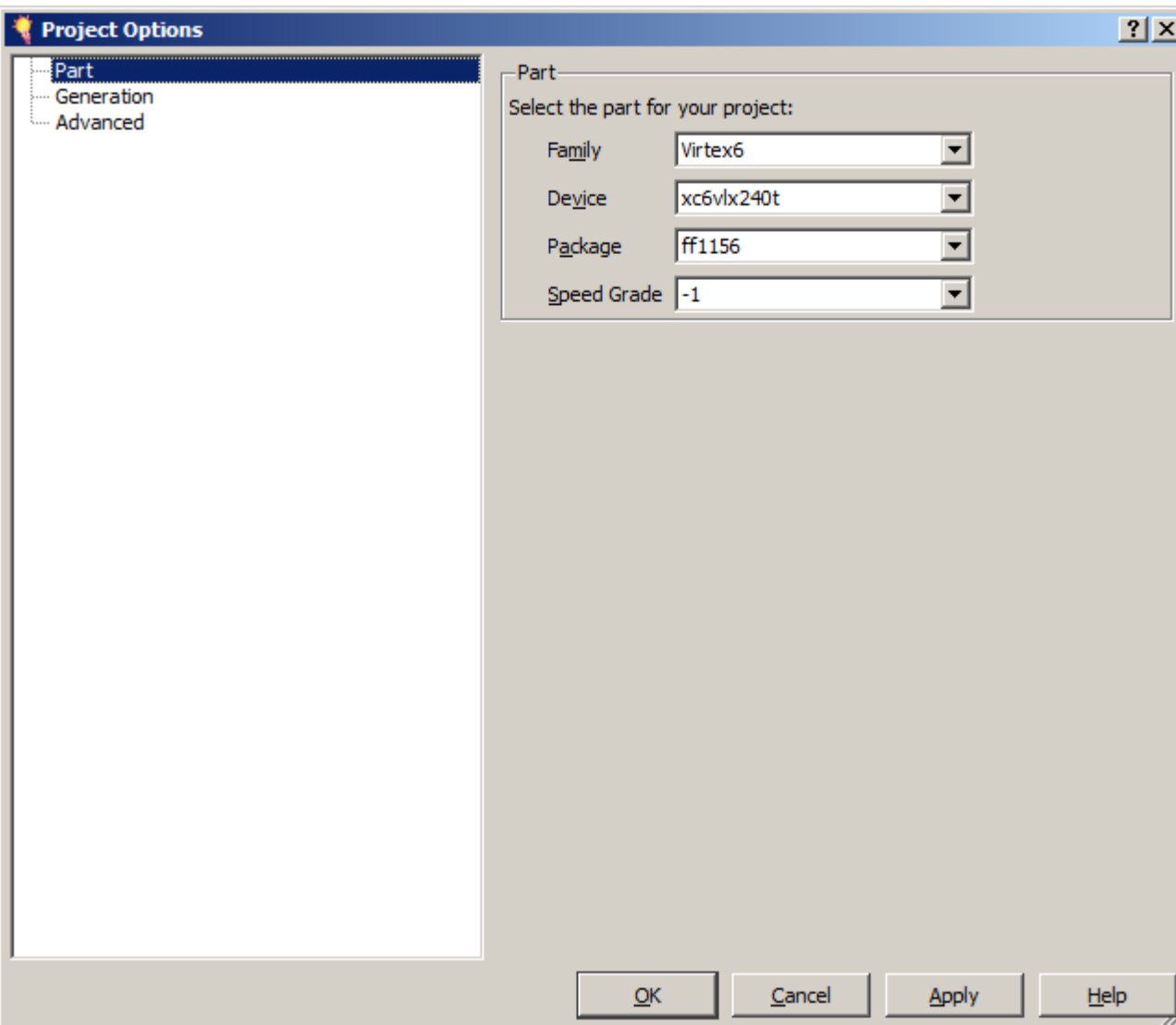
- **Open the CORE Generator**

Start → All Programs → Xilinx ISE Design Suite 11 →
ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**

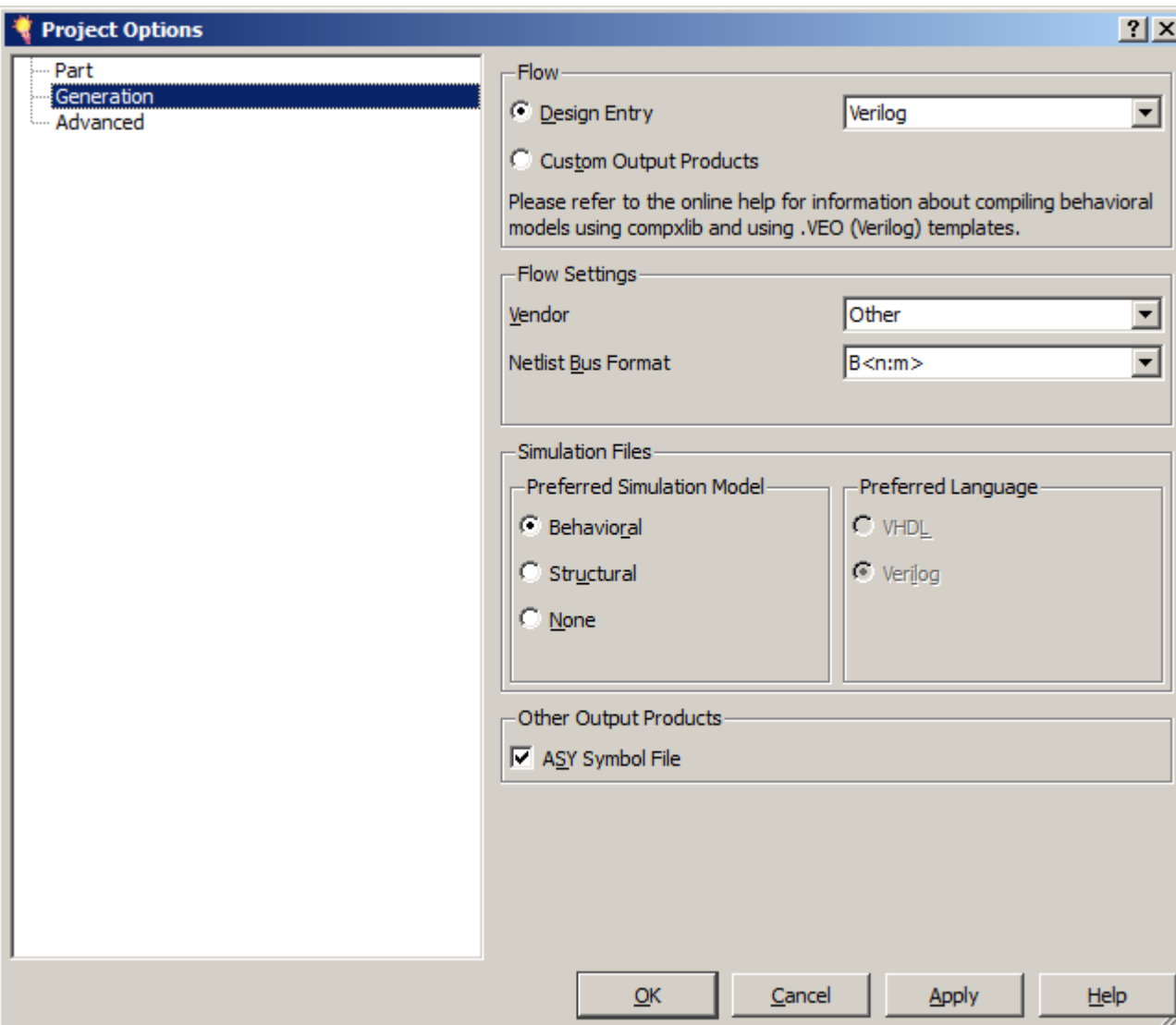


Create IBERT CORE Generator Project



- Create a project directory:
ml605_ibert
- Name the project:
ml605_ibert.cgp
- The Project options will appear
- Set the Part (as seen here):
 - Family: Virtex6
 - Device: xc6vlx240t
 - Package: ff1156
 - Speed Grade: -1

Create IBERT CORE Generator Project



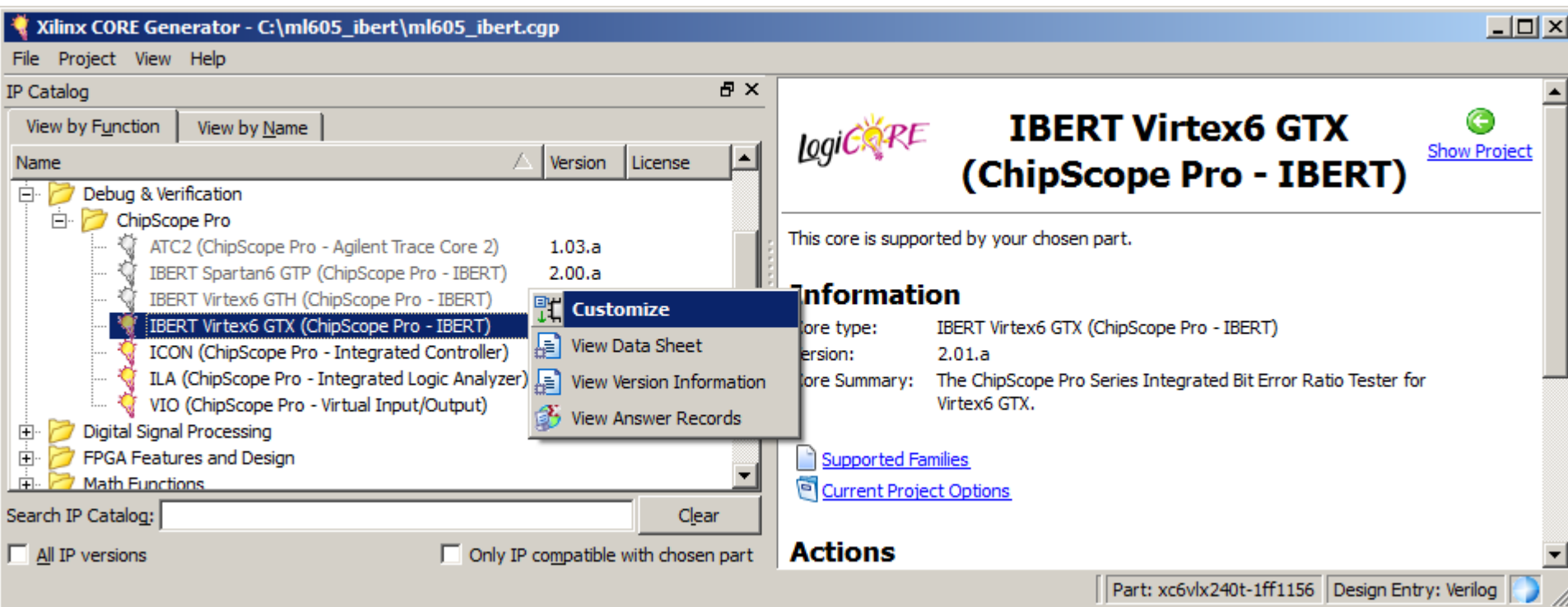
- Select Generation
- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the ML605

IBERT Design Creation Bank 113

Create IBERT Design – Bank 113

- Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a)
 - Select **Customize**



Create IBERT Design – Bank 113

- **Make the following settings:**
 - Component name:
ibert_bank113
 - Set the number of Line Rates: **1**
 - Set the line rate to Max Rate: **5 Gbps**
- **On the ML605, Bank 113 is connected to the 250 MHz OSC**
 - Set the RefClk frequency to: **250 MHz**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

Component Name

Line Rate Settings

Number of Line Rates (protocols)

Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	Start from scratch	5	20	250.00

[Datasheet](#) [< Back](#) Page 1 of 4 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 113

- The line rate is 5 Gbps
- Select a GTX from Bank 114
 - This enables the clock used for Bank 113
- Select the four GTXs for Bank 113:
 - X0Y7
 - X0Y6
 - X0Y5
 - X0Y4
- Connect the Refclks for all GTXs to:
 - REFCLK0 Q2
 - This connects Bank 113 to the Bank 114 250 MHz Clock
- Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Select GTXs and Reference Clocks for Line Rate 1

GTX (Location)	TXREFCLK	RXREFCLK
<input type="checkbox"/> GTX3_116 (X0Y19)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX3_115 (X0Y15)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX0_115 (X0Y12)	REFCLK1_Q3	REFCLK1 Q3
<input checked="" type="checkbox"/> GTX3_114 (X0Y11)	REFCLK0_Q2	REFCLK0 Q2
<input type="checkbox"/> GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2
<input checked="" type="checkbox"/> GTX3_113 (X0Y7)	REFCLK0_Q2	REFCLK0 Q2
<input checked="" type="checkbox"/> GTX2_113 (X0Y6)	REFCLK0_Q2	REFCLK0 Q2
<input checked="" type="checkbox"/> GTX1_113 (X0Y5)	REFCLK0_Q2	REFCLK0 Q2
<input checked="" type="checkbox"/> GTX0_113 (X0Y4)	REFCLK0_Q2	REFCLK0 Q2
<input type="checkbox"/> GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0

Active GTXs : 5


Datasheet < Back Page 2 of 5 Next > Generate Cancel Help

Create IBERT Design – Bank 113

- Leave this screen as is
– Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

Enable RXRECCLK Probes

RXRECCLK PIN OUT

Enable	GTX	Location*	IO Standard
<input type="checkbox"/>	X0Y4 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y5 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y6 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y7 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y11 RXRECCLK	\$	LVDS 25

* In case the selected Input standard in Differential, Please enter only P Pin Location.


[Datasheet](#) [< Back](#) Page 3 of 5 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 113

- **Select the following settings:**
 - **Use External Clock source**
 - Location: **J9**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

System Clock

Set the system clock for FPGA's internal debug bus

☒ Use External Clock source *

Frequency (MHz)	<input type="text" value="200"/>
Location *	<input type="text" value="J9"/>
Input Standard	<input type="text" value="LVDS 25"/>

☐ Use MGT TXOUTCLK**

* In case the selected Input standard in Differential, Please enter only P Pin Location.
Select atleast one GT from the clock selection panels to use internal TXOUTCLK

[Datasheet](#) [< Back](#) Page 4 of 5 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 113

- Click Generate

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

IBERT Core Summary

System

System Clock Source / Frequency	IBERT_SYSCLOCK / 200 MHz
BUFGs used / MMCMs used	12 / 1

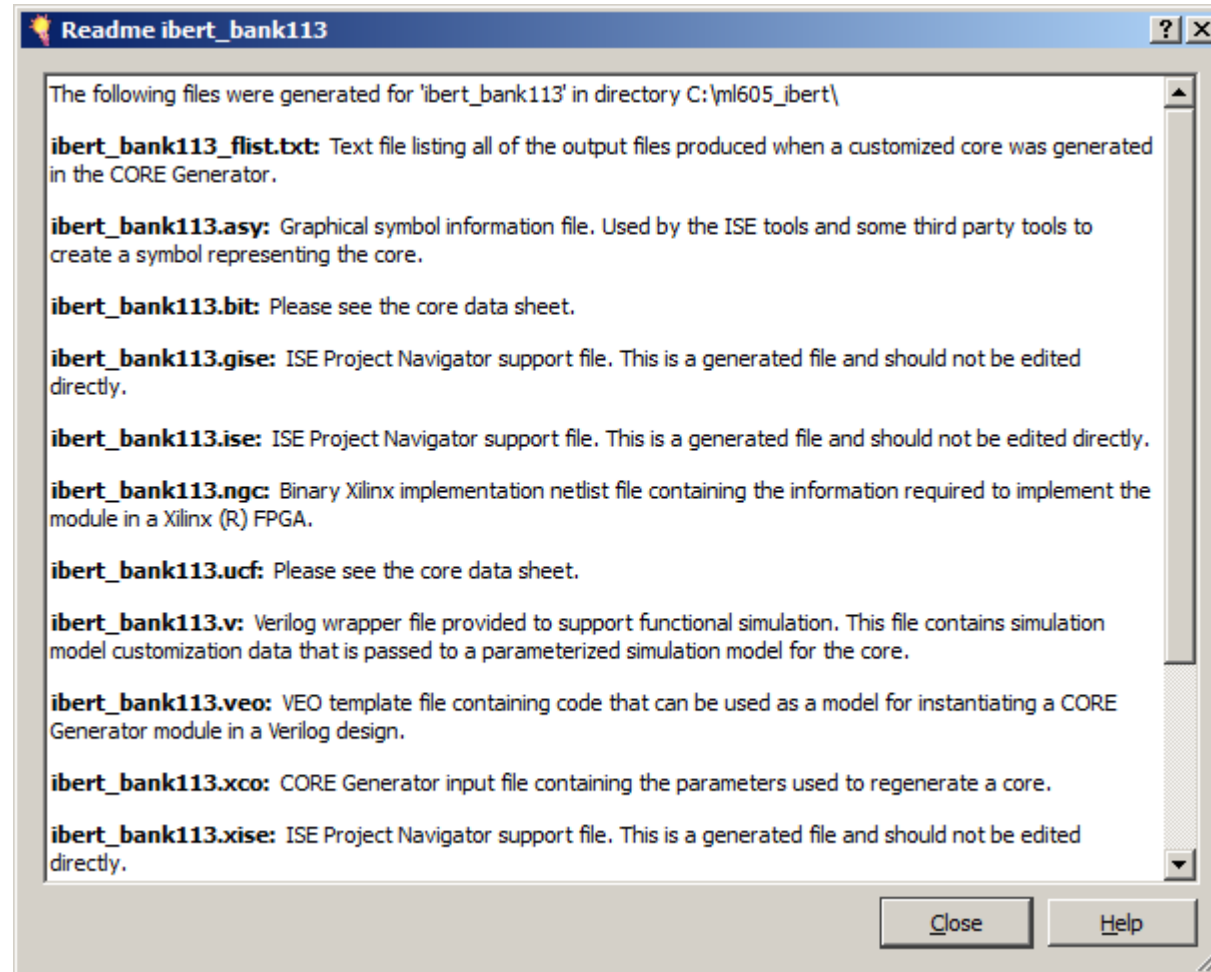
Line Rates

Index	Protocol	Line Rate	Data Width	REFCLK	GTXs selected
1	Start_from_scratch	5	20	250.00	x0y4 x0y5 x0y6 x0y7 x0y11

Datasheet < Back Page 5 of 5 Next > Generate Cancel Help

Create IBERT Design – Bank 113

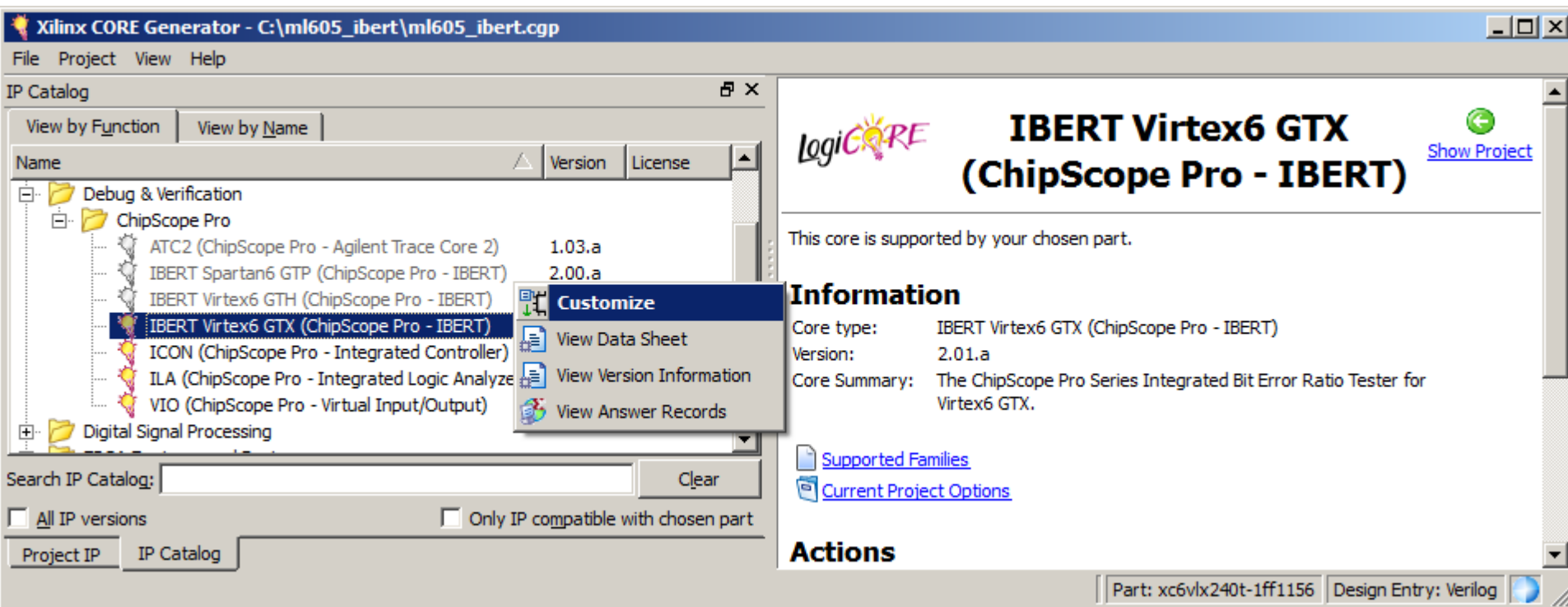
- After the IBERT core finishes generating, click Close on the Datasheet window



IBERT Design Creation Bank 114

Create IBERT Design – Bank 114

- Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a)
 - Select **Customize**



Note: Presentation applies to the ML605

Create IBERT Design – Bank 114

- **Make the following settings:**
 - Component name:
ibert_bank114
 - Set the number of Line Rates: **1**
 - Set the line rate to Max Rate: **5 Gbps**
- **On the ML605, Bank 114 is connected to the 250 MHz OSC**
 - Set the RefClk frequency to: **250 MHz**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Component Name

Line Rate Settings

Number of Line Rates (protocols)

Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	<input type="text" value="Start from scratch"/>	<input type="text" value="5"/>	<input type="text" value="20"/>	<input type="text" value="250.00"/>

[Datasheet](#) [< Back](#) Page 1 of 4 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 114

- The line rate is 5 Gbps
- Select the four GTXs for Bank 114:
 - X0Y11
 - X0Y10
 - X0Y9
 - X0Y8
- Connect the Refclks to:
 - REFCLK0 Q2
- Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Select GTXs and Reference Clocks for Line Rate 1

GTX (Location)	TXREFCLK	RXREFCLK
<input type="checkbox"/> GTX3_116 (X0Y19)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX3_115 (X0Y15)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX0_115 (X0Y12)	REFCLK1_Q3	REFCLK1 Q3
<input checked="" type="checkbox"/> GTX3_114 (X0Y11)	REFCLK0_Q2	REFCLK0 Q2
<input checked="" type="checkbox"/> GTX2_114 (X0Y10)	REFCLK0_Q2	REFCLK0 Q2
<input checked="" type="checkbox"/> GTX1_114 (X0Y9)	REFCLK0_Q2	REFCLK0 Q2
<input checked="" type="checkbox"/> GTX0_114 (X0Y8)	REFCLK0_Q2	REFCLK0 Q2
<input type="checkbox"/> GTX3_113 (X0Y7)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0

Active GTXs : 4


Datasheet < Back Page 2 of 5 Next > Generate Cancel Help

Create IBERT Design – Bank 114

- Leave this screen as is
– Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

Enable RXRECCLK Probes

RXRECCLK PIN OUT

Enable	GTX	Location*	IO Standard
<input type="checkbox"/>	X0Y8 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y9 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y10 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y11 RXRECCLK	\$	LVDS 25

* In case the selected Input standard in Differential, Please enter only P Pin Location.


[Datasheet](#) [< Back](#) Page 3 of 5 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 114

- **Select the following settings:**
 - **Use External Clock source**
 - Location: **J9**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

System Clock

Set the system clock for FPGA's internal debug bus

☒ Use External Clock source *

Frequency (MHz)	200
Location *	J9
Input Standard	LVDS 25

☐ Use MGT TXOUTCLK**

* In case the selected Input standard in Differential, Please enter only P Pin Location.
Select atleast one GT from the clock selection panels to use internal TXOUTCLK

[Datasheet](#) [< Back](#) Page 4 of 5 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 114

- Click Generate

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

IBERT Core Summary

System

System Clock Source / Frequency	IBERT_SYSCLOCK / 200 MHz
BUFGs used / MMCMs used	10 / 1

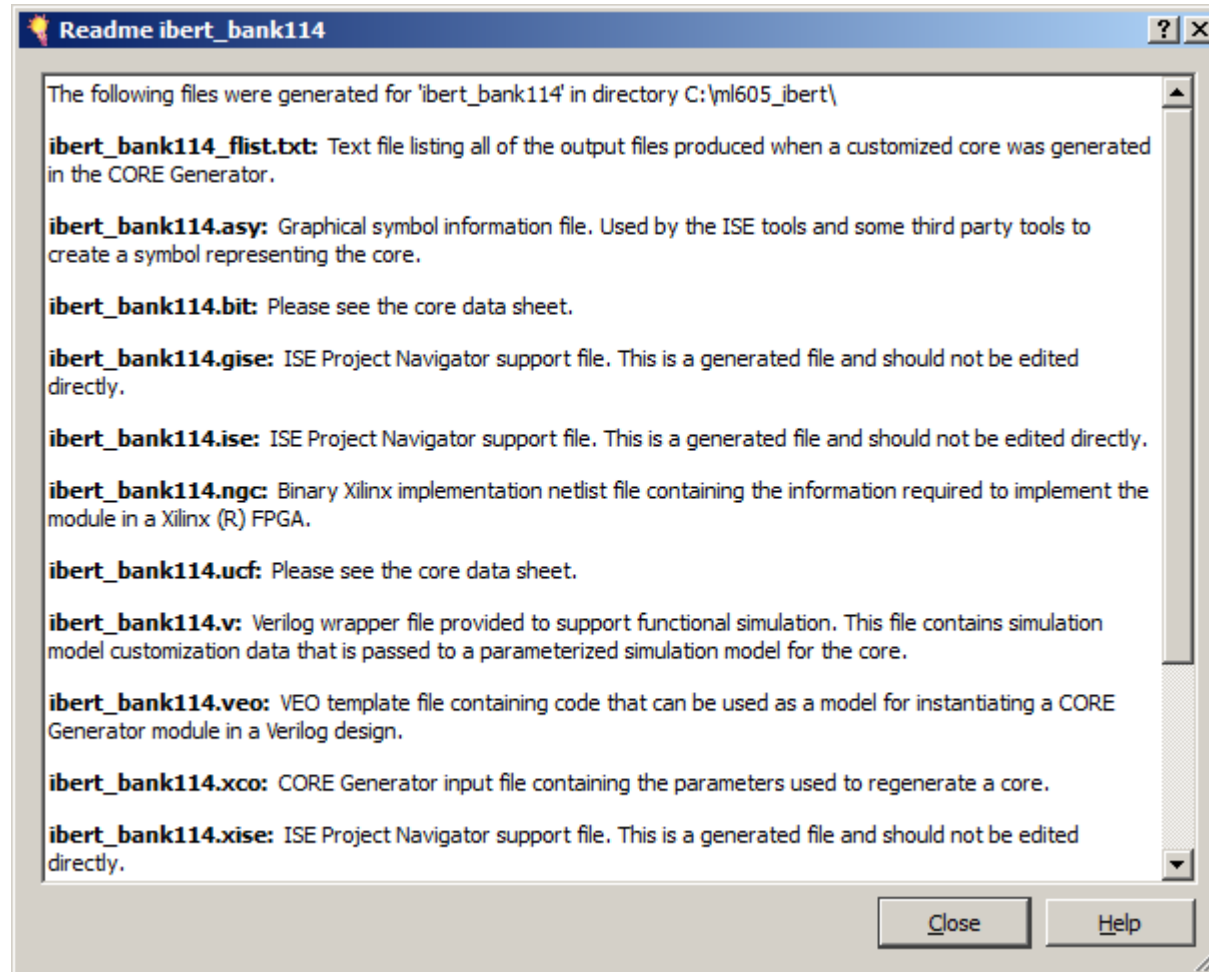
Line Rates

Index	Protocol	Line Rate	Data Width	REFCLK	GTXs selected
1	Start_from_scratch	5	20	250.00	x0y8 x0y9 x0y10 x0y11

Datasheet < Back Page 5 of 5 Next > Generate Cancel Help

Create IBERT Design – Bank 114

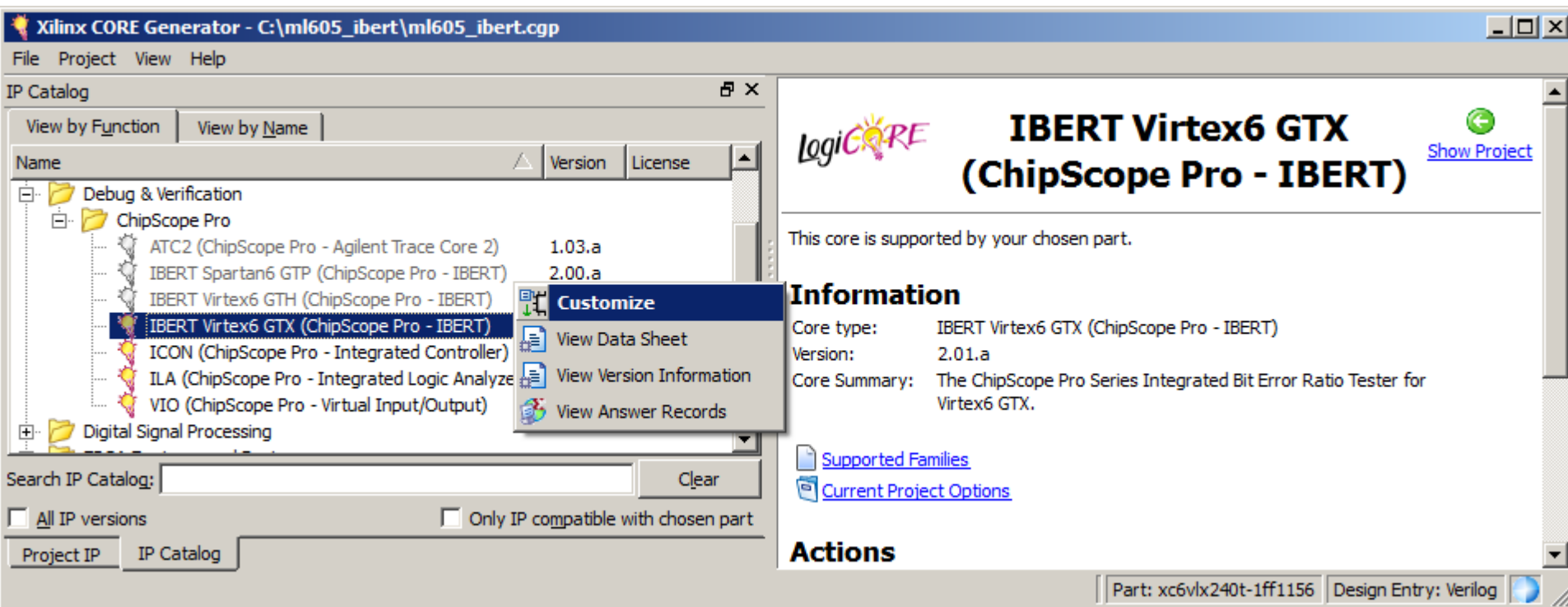
- After the IBERT core finishes generating, click Close on the Datasheet window



IBERT Design Creation Bank 115

Create IBERT Design – Bank 115

- Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a)
 - Select **Customize**



Create IBERT Design – Bank 115

- **Make the following settings:**
 - Component name: **ibert_bank115**
 - Set the number of Line Rates: **1**
 - Set the line rate to:
 - Max Rate: **5 Gbps**
- **On the ML605, Bank 115 is connected to the 100 MHz OSC**
 - Set the RefClk frequency to: **100 MHz**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

Component Name

Line Rate Settings

Number of Line Rates (protocols)

Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	Start from scratch	5	20	100.00

[Datasheet](#) [< Back](#) Page 1 of 4 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 115

- The rate is 5 Gbps
- Select the four GTXs for Bank 115:
 - X0Y15
 - X0Y14
 - X0Y13
 - X0Y12
- Connect the Refclks to:
 - REFCLK0 Q3
- Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Select GTXs and Reference Clocks for Line Rate 1

GTX (Location)	TXREFCLK	RXREFCLK
<input type="checkbox"/> GTX3_116 (X0Y19)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
<input checked="" type="checkbox"/> GTX3_115 (X0Y15)	REFCLK0_Q3	REFCLK0 Q3
<input checked="" type="checkbox"/> GTX2_115 (X0Y14)	REFCLK0_Q3	REFCLK0 Q3
<input checked="" type="checkbox"/> GTX1_115 (X0Y13)	REFCLK0_Q3	REFCLK0 Q3
<input checked="" type="checkbox"/> GTX0_115 (X0Y12)	REFCLK0_Q3	REFCLK0 Q3
<input type="checkbox"/> GTX3_114 (X0Y11)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX3_113 (X0Y7)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0

Active GTXs : 4


Datasheet < Back Page 2 of 5 Next > Generate Cancel Help

Create IBERT Design – Bank 115

- Leave this screen as is
– Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

Enable RXRECCLK Probes

RXRECCLK PIN OUT

Enable	GTX	Location*	IO Standard
<input type="checkbox"/>	X0Y12 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y13 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y14 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y15 RXRECCLK	\$	LVDS 25

* In case the selected Input standard in Differential, Please enter only P Pin Location.


[Datasheet](#) [< Back](#) Page 3 of 5 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 115

- **Select the following settings:**
 - **Use External Clock source**
 - Location: **J9**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

System Clock

Set the system clock for FPGA's internal debug bus

☒ Use External Clock source *

Frequency (MHz)	<input type="text" value="200"/>
Location *	<input type="text" value="J9"/>
Input Standard	<input type="text" value="LVDS 25"/>

☐ Use MGT TXOUTCLK**

* In case the selected Input standard in Differential, Please enter only P Pin Location.
Select atleast one GT from the clock selection panels to use internal TXOUTCLK

[Datasheet](#) [< Back](#) Page 4 of 5 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 115

- Click Generate

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

IBERT Core Summary

System

System Clock Source / Frequency	IBERT_SYSCLOCK / 200 MHz
BUFGs used / MMCMs used	10 / 1

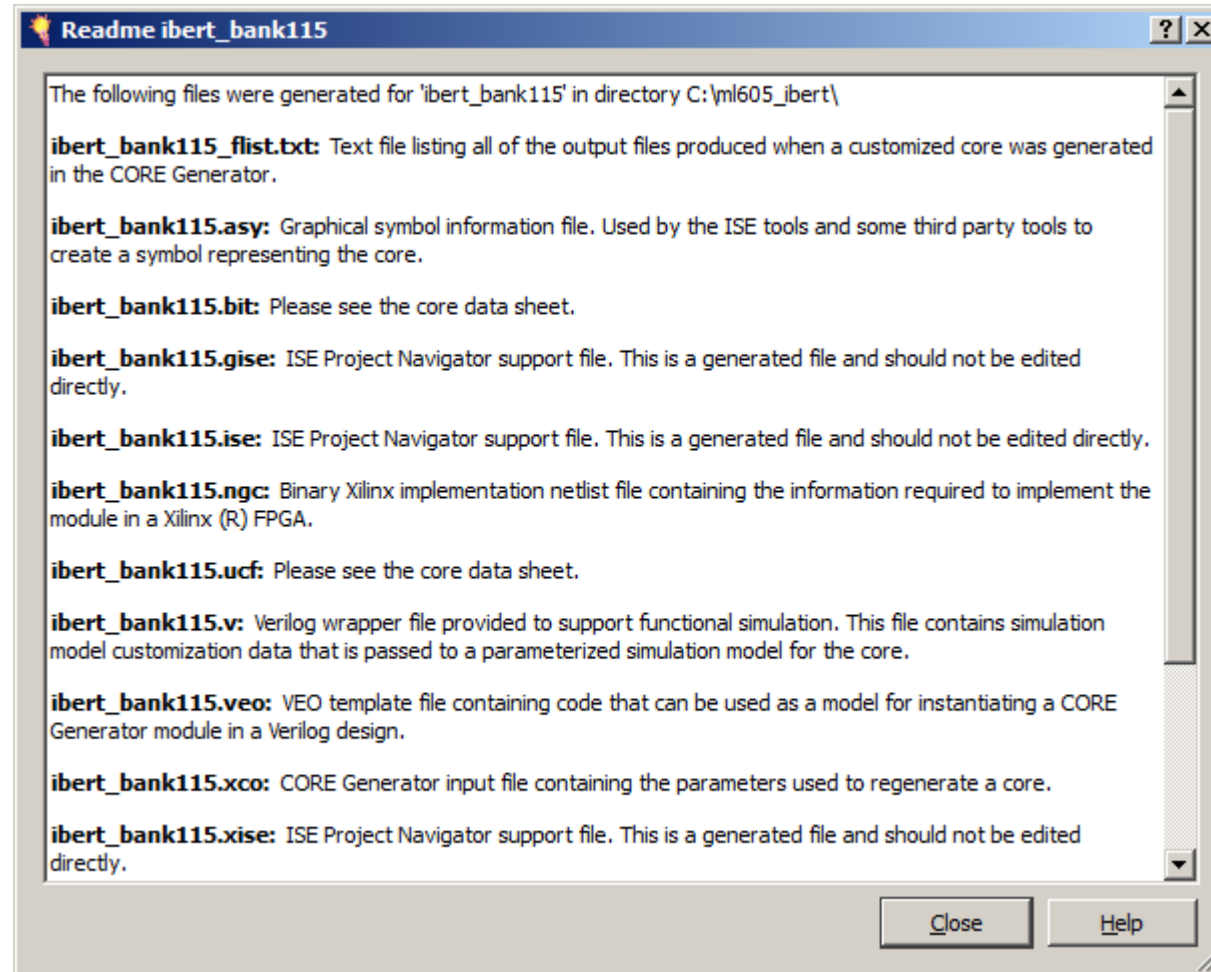
Line Rates

Index	Protocol	Line Rate	Data Width	REFCLK	GTXs selected
1	Start_from_scratch	5	20	100.00	x0y12 x0y13 x0y14 x0y15

Datasheet < Back Page 5 of 5 Next > Generate Cancel Help

Create IBERT Design – Bank 115

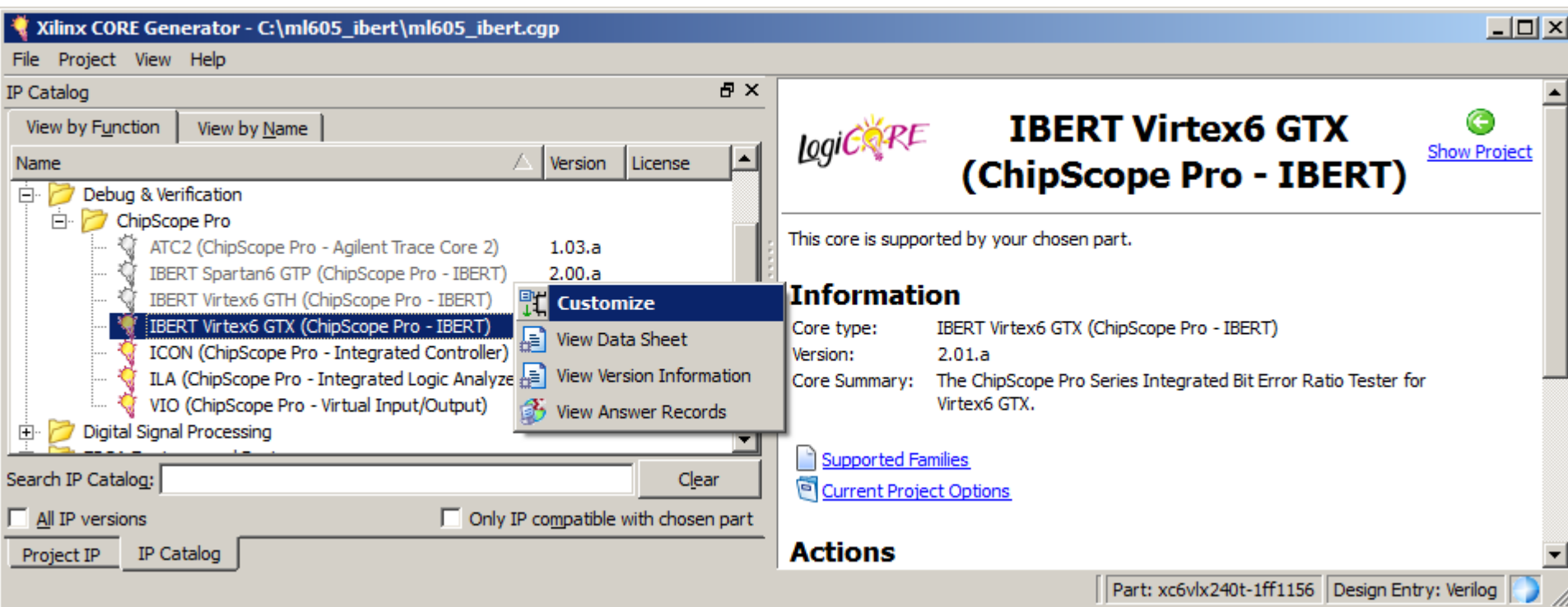
- After the IBERT core finishes generating, click Close on the Datasheet window



IBERT Design Creation Bank 116

Create IBERT Design – Bank 116

- Right click on the IBERT Virtex6 GTX (ChipScope Pro - IBERT, Version 2.01a)
 - Select **Customize**



Create IBERT Design – Bank 116

▪ Make the following settings:

- Component name:
ibert_bank116
- Set the number of Line Rates: 2
- Set the first line rate to:
Max Rate: 1.25 Gbps
- Set the second line rate to:
Max Rate: 5 Gbps
- Set both RefClk frequencies to: **125 MHz**

▪ Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Component Name

Line Rate Settings

Number of Line Rates (protocols)

Index	Protocol	Max Rate (Gbps)	Data Width	REFCLK (MHz)
1	Start from scratch	1.25	20	125.00
2	Start from scratch	5	20	125.00

[Datasheet](#) [< Back](#) Page 1 of 6 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 116

- The first line rate is 1.25 Gbps
- Select the first GTX for Bank 116:
 - X0Y19
- Connect the Refclk to:
 - REFCLK0 Q4
 - This connects Bank 116 to the 125 MHz SGMII OSC
- Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Select GTXs and Reference Clocks for Line Rate 1

GTX (Location)	TXREFCLK	RXREFCLK
<input checked="" type="checkbox"/> GTX3_116 (X0Y19)	REFCLK0_Q4	REFCLK0 Q4
<input type="checkbox"/> GTX2_116 (X0Y18)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX1_116 (X0Y17)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX0_116 (X0Y16)	REFCLK1_Q4	REFCLK1 Q4
<input type="checkbox"/> GTX3_115 (X0Y15)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX0_115 (X0Y12)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX3_114 (X0Y11)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX3_113 (X0Y7)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0

Active GTXs : 1

Datasheet < Back Page 2 of 6 Next > Generate Cancel Help

Create IBERT Design – Bank 116

- The second line rate is 5 Gbps
- Select the second and third GTXs for Bank 116:
 - X0Y18
 - X0Y17
 - X0Y16
- Connect the Refclks to:
 - REFCLK0 Q4
- Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE IBERT Virtex6 GTX (ChipScope Pro - IBERT) 2.01.a

Select GTXs and Reference Clocks for Line Rate 2

GTX (Location)	TXREFCLK	RXREFCLK
<input checked="" type="checkbox"/> GTX3_116 (X0Y19)	REFCLK0_Q4	REFCLK0 Q4
<input checked="" type="checkbox"/> GTX2_116 (X0Y18)	REFCLK0_Q4	REFCLK0 Q4
<input checked="" type="checkbox"/> GTX1_116 (X0Y17)	REFCLK0_Q4	REFCLK0 Q4
<input checked="" type="checkbox"/> GTX0_116 (X0Y16)	REFCLK0_Q4	REFCLK0 Q4
<input type="checkbox"/> GTX3_115 (X0Y15)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX2_115 (X0Y14)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX1_115 (X0Y13)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX0_115 (X0Y12)	REFCLK1_Q3	REFCLK1 Q3
<input type="checkbox"/> GTX3_114 (X0Y11)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX2_114 (X0Y10)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX1_114 (X0Y9)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX0_114 (X0Y8)	REFCLK1_Q2	REFCLK1 Q2
<input type="checkbox"/> GTX3_113 (X0Y7)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX2_113 (X0Y6)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX1_113 (X0Y5)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX0_113 (X0Y4)	REFCLK1_Q1	REFCLK1 Q1
<input type="checkbox"/> GTX3_112 (X0Y3)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX2_112 (X0Y2)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX1_112 (X0Y1)	REFCLK1_Q0	REFCLK1 Q0
<input type="checkbox"/> GTX0_112 (X0Y0)	REFCLK1_Q0	REFCLK1 Q0

Active GTXs : 3


Datasheet < Back Page 3 of 6 Next > Generate Cancel Help

Create IBERT Design – Bank 116

- Leave this screen as is
– Click Next

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

Enable RXRECCLK Probes

RXRECCLK PIN OUT

Enable	GTX	Location*	IO Standard
<input type="checkbox"/>	X0Y16 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y17 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y18 RXRECCLK	\$	LVDS 25
<input type="checkbox"/>	X0Y19 RXRECCLK	\$	LVDS 25

* In case the selected Input standard in Differential, Please enter only P Pin Location.

[Datasheet](#) [< Back](#) Page 4 of 6 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 116

- **Select the following settings:**
 - **Use External Clock source**
 - Location: **J9**
- **Click Next**

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

LogiCORE **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

System Clock

Set the system clock for FPGA's internal debug bus

☒ Use External Clock source *

Frequency (MHz) 200

Location * J9

Input Standard LVDS 25

☐ Use MGT TXOUTCLK**

* In case the selected Input standard in Differential, Please enter only P Pin Location.
Select atleast one GT from the clock selection panels to use internal TXOUTCLK


Datasheet < Back Page 5 of 6 Next > Generate Cancel Help

Create IBERT Design – Bank 116

- Click Generate

IBERT Virtex6 GTX (ChipScope Pro - IBERT)

View

 **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** 2.01.a

IBERT Core Summary

System

System Clock Source / Frequency	IBERT_SYSCLOCK / 200 MHz
BUFGs used / MMCMs used	10 / 1

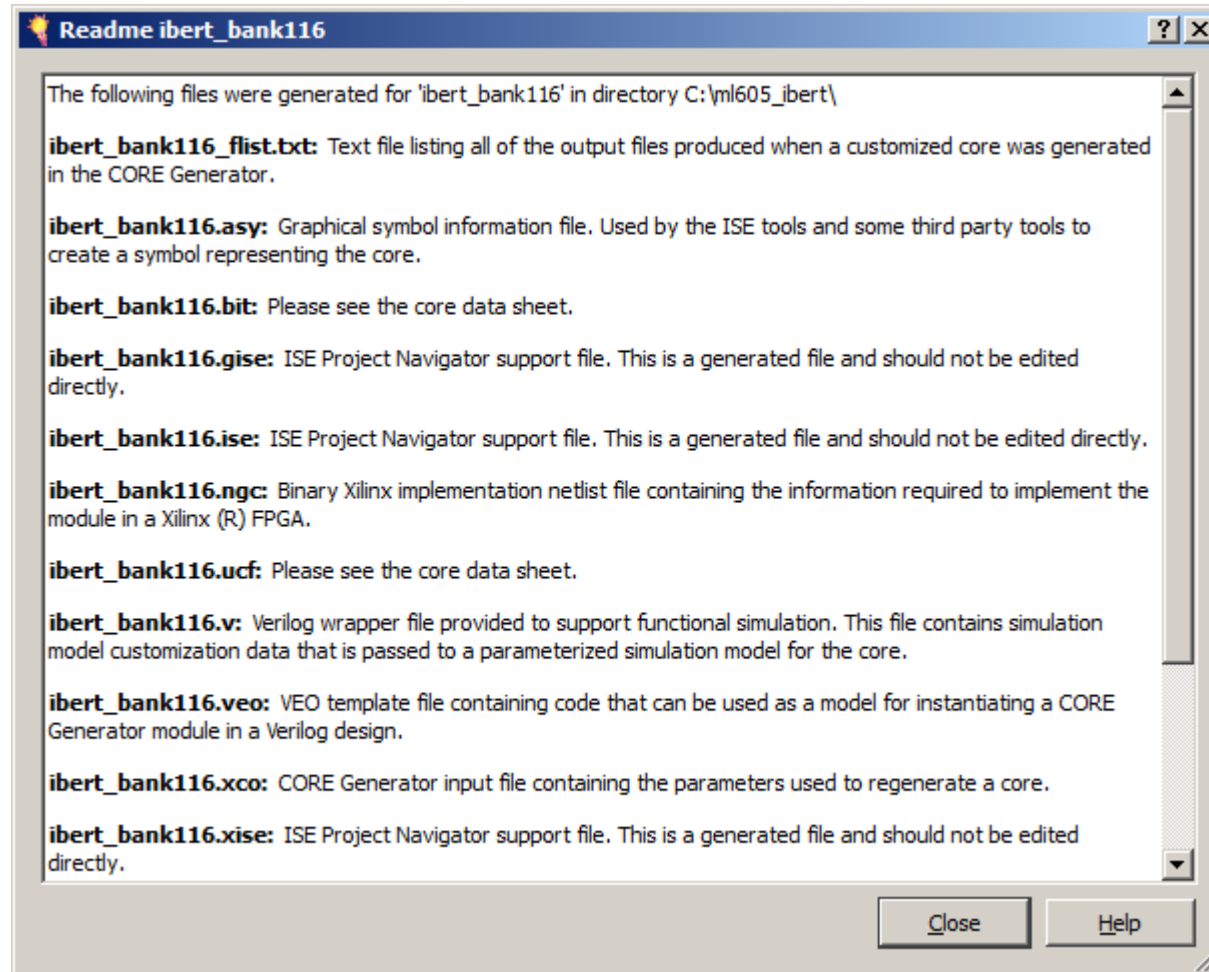
Line Rates

Index	Protocol	Line Rate	Data Width	REFCLK	GTXs selected
1	Start_from_scratch	1.25	20	125.00	x0y19
2	Start_from_scratch	5	20	125.00	x0y16 x0y17 x0y18

[Datasheet](#) [< Back](#) Page 6 of 6 [Next >](#) [Generate](#) [Cancel](#) [Help](#)

Create IBERT Design – Bank 116

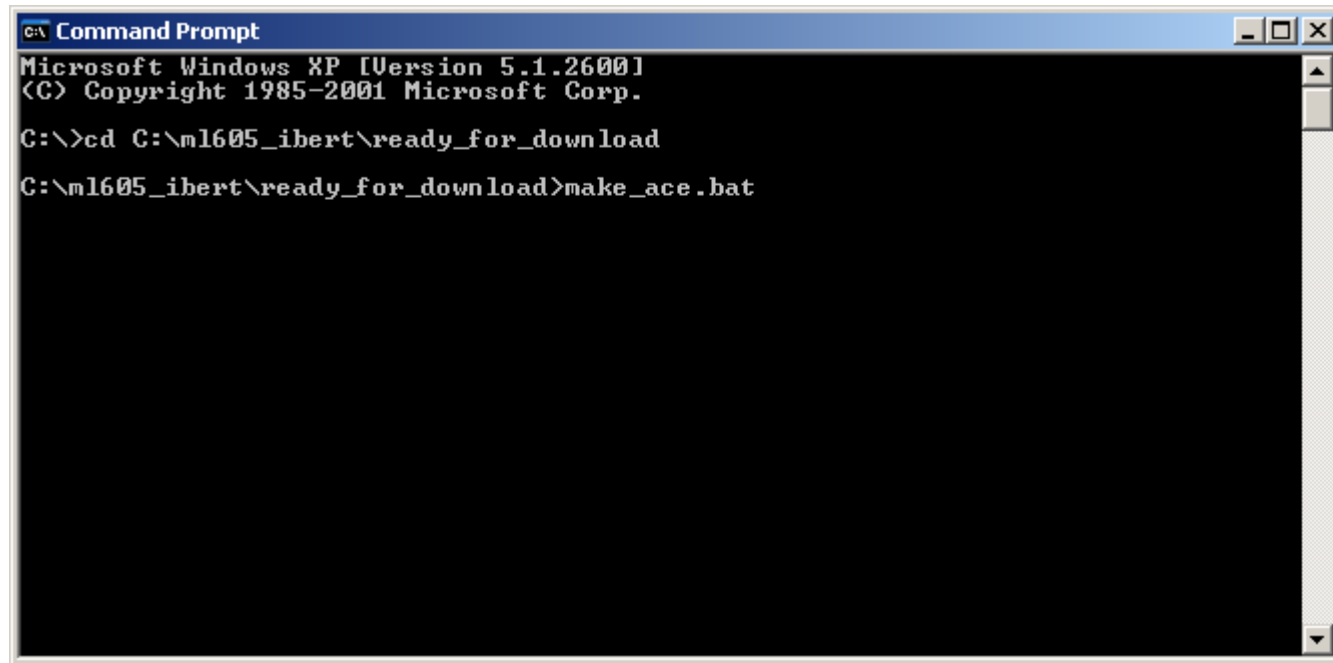
- After the IBERT core finishes generating, click Close on the Datasheet window



Generate IBERT ACE Files (Optional)

- Type these commands in a windows command shell:

```
cd C:\ml605_ibert\ready_for_download  
make_ace.bat
```



```
C:\> Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd C:\ml605_ibert\ready_for_download  
C:\ml605_ibert\ready_for_download>make_ace.bat
```


References

References

- **ChipScope Pro**

- ChipScope Pro 11.1 ChipScope Pro Software and Cores User Guide

http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/chipscope_pro_sw_cores_ug029.pdf

Documentation

Documentation

- **Virtex-6**

- Virtex-6 FPGA Family

- <http://www.xilinx.com/products/virtex6/index.htm>

- **ML605 Documentation**

- Virtex-6 FPGA ML605 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Hardware User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf