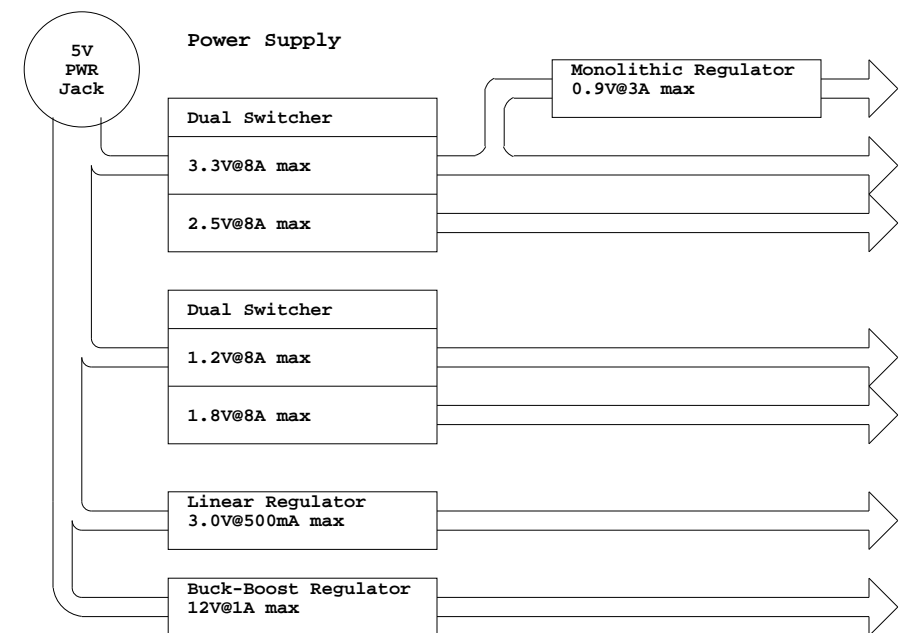
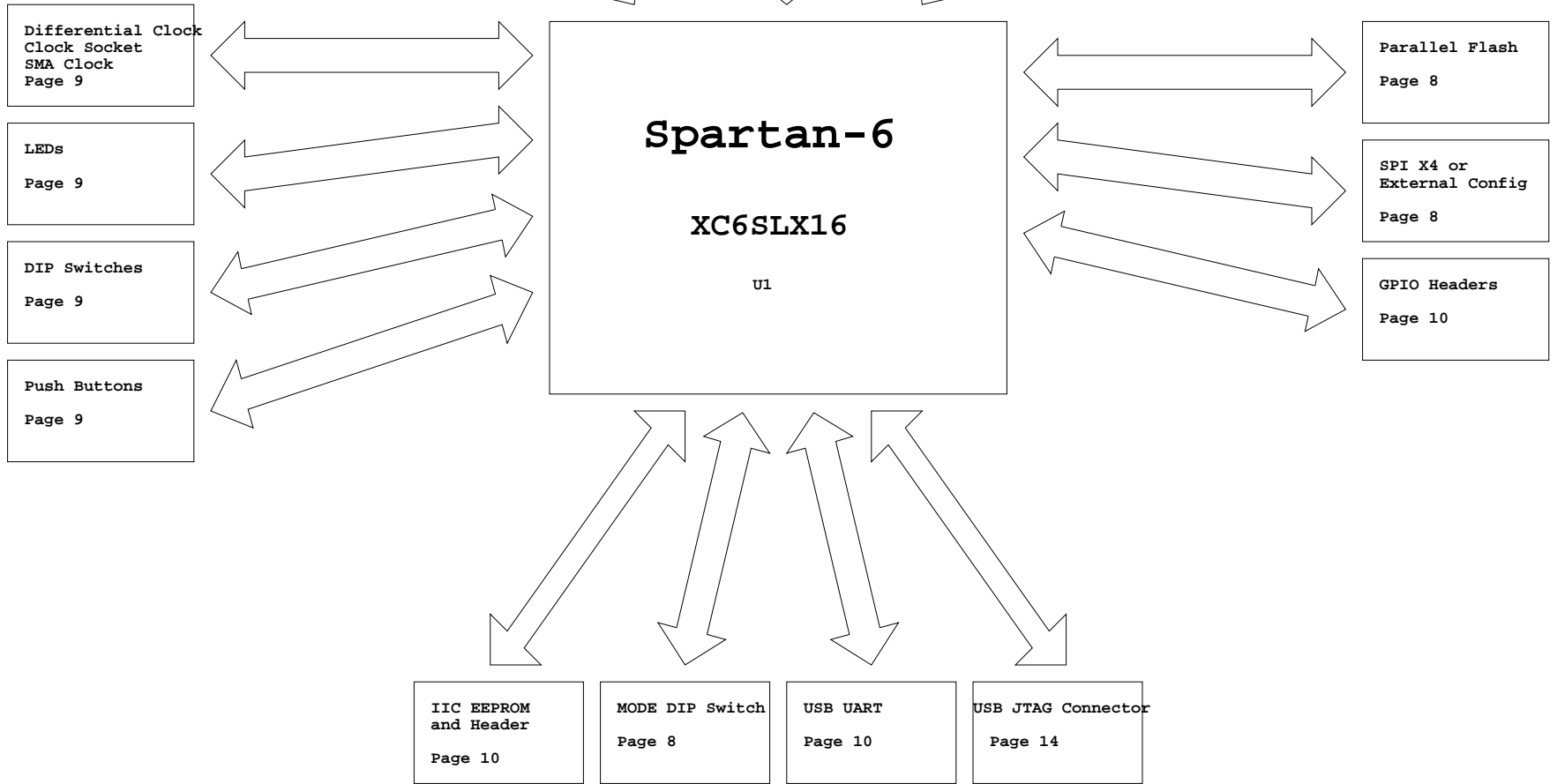


DDR2
Page 5

FMC LPC Expansion Connector
Page 6

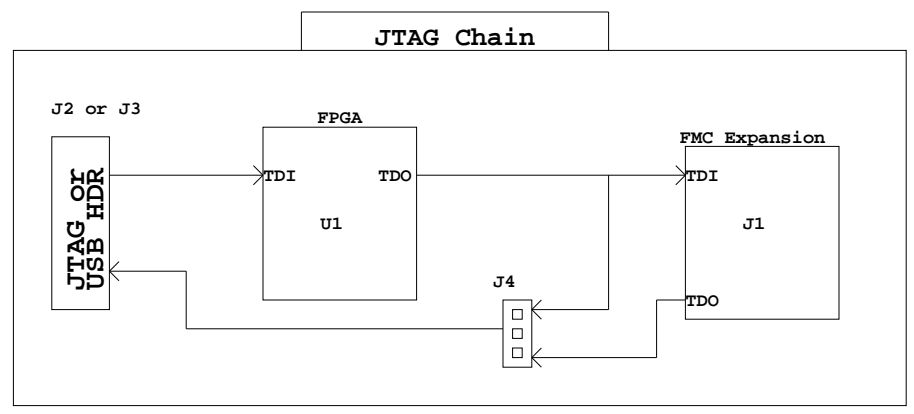
10/100/1000 Ethernet GMII
Page 7

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IIC Addresssing

U5	0b1010100
J1	EEPROM: 0b1010010 Other Devices: 0bXXXXX10



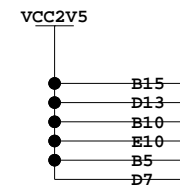
XILINX

Title: SP601 Block Diagram SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM
PCB P/N: 0431512, 0431608
SCH P/N: 0381290
Test P/N: TSS0121
ART P/N: 1280464

Date: 10-20-2009_14:54 Ver: C
Sheet Size: B Rev: 04
Sheet **1** of **16** Drawn By BF

**SOCKET
BANK 0
sa16cs324**

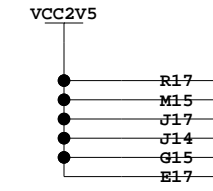
IO_L30N_0_SCP0_A16	A16	FMC LA04 N	6
IO_L30P_0_SCP1_B16	B16	FMC LA04 P	6
IO_L29N_0_SCP2_C14	C14	GPIO LED 1	9
IO_L29P_0_SCP3_D14	D14	GPIO SWITCH 0	9
IO_L28N_0_SCP4_A15	A15	FMC LA02 N	6
IO_L28P_0_SCP5_C15	C15	FMC LA02 P	6
IO_L27N_0_SCP6_E13	E13	GPIO LED 0	9
IO_L27P_0_SCP7_F13	F13	GPIO HDR6	10
IO_L26N_0_VREF_0_A14	A14	FMC LA05 N	6
IO_L26P_0_B14	B14	FMC LA05 P	6
IO_L25N_0_E12	E12	GPIO SWITCH 1	9
IO_L25P_0_F12	F12	GPIO SWITCH 2	9
IO_L24N_0_A13	A13	FMC LA03 N	6
IO_L24P_0_C13	C13	FMC LA03 P	6
IO_L23N_0_C12	C12	FMC LA06 N	6
IO_L23P_0_D12	D12	FMC LA06 P	6
IO_L22N_0_E11	E11	FMC LA08 N	6
IO_L22P_0_F11	F11	FMC LA08 P	6
IO_L21N_0_A12	A12	FMC LA11 N	6
IO_L21P_0_B12	B12	FMC LA11 P	6
IO_L20N_0_F10	F10	FMC LA09 N	6
IO_L20P_0_G11	G11	FMC LA09 P	6
IO_L19N_0_A11	A11	FMC LA13 N	6
IO_L19P_0_B11	B11	FMC LA13 P	6
IO_L18N_0_VREF_0_F9	F9	FMC LA15 N	6
IO_L18P_0_G9	G9	FMC LA15 P	6
IO_L17N_0_GCLK12_A10	A10	FMC CLK0 M2C N	6
IO_L17P_0_GCLK13_C10	C10	FMC CLK0 M2C P	6
IO_L16N_0_GCLK14_C11	C11	FMC LA01 CC N	6
IO_L16P_0_GCLK15_D11	D11	FMC LA01 CC P	6
IO_L15N_0_GCLK16_A9	A9	PHY TXCLK	7
IO_L15P_0_GCLK17_B9	B9	PHY TXCLK	7
IO_L14N_0_GCLK18_C9	C9	FMC LA00 CC N	6
IO_L14P_0_GCLK19_D9	D9	FMC LA00 CC P	6
IO_L13N_0_A8	A8	PHY TXER	7
IO_L13P_0_B8	B8	PHY TXCTL TXEN	7
IO_L12N_0_F8	F8	PHY TXD0	7
IO_L12P_0_G8	G8	PHY TXD1	7
IO_L11N_0_C8	C8	FMC LA10 N	6
IO_L11P_0_D8	D8	FMC LA10 P	6
IO_L10N_0_A7	A7	FMC LA16 N	6
IO_L10P_0_C7	C7	FMC LA16 P	6
IO_L09N_0_E8	E8	FMC LA07 N	6
IO_L09P_0_E7	E7	FMC LA07 P	6
IO_L08N_0_VREF_0_A6	A6	PHY TXD2	7
IO_L08P_0_B6	B6	PHY TXD3	7
IO_L07N_0_E6	E6	PHY TXD4	7
IO_L07P_0_F7	F7	PHY TXD5	7
IO_L06N_0_A5	A5	PHY TXD6	7
IO_L06P_0_C5	C5	PHY TXD7	7
IO_L05N_0_A4	A4	GPIO LED 3	9
IO_L05P_0_B4	B4	GPIO HDR5	10
IO_L04N_0_A3	A3	GPIO HDR2	10
IO_L04P_0_B3	B3	FMC PWR GOOD FLASH_RST	6,8
IO_L03N_0_C6	C6	FMC LA12 N	6
IO_L03P_0_D6	D6	FMC LA12 P	6
IO_L02N_0_A2	A2	FMC LA14 N	6
IO_L02P_0_B2	B2	FMC LA14 P	6
IO_L01N_0_VREF_0_C4	C4	GPIO LED 2	9
IO_L01P_0_HSWAPEN_D4	D4	FPGA HSWAPEN	9



VCC0_0_B15
VCC0_0_D13
VCC0_0_B10
VCC0_0_E10
VCC0_0_B5
VCC0_0_D7

**SOCKET
BANK 1
sa16cs324**

IO_L28N_1_DOUT_P16	P16	PHY MDIO	7
IO_L28P_1_AWAKE_P15	P15	FPGA AWAKE	8
IO_L27N_1_M13	M13	PHY CRS	7
IO_L27P_1_L14	L14	PHY COL	7
IO_L26N_1_VREF_1_N14	N14	PHY MDC	7
IO_L26P_1_M14	M14	PHY RXD0	7
IO_L25N_1_M1DQ15_U18	U18	PHY RXD1	7
IO_L25P_1_M1DQ14_U17	U17	PHY RXD2	7
IO_L24N_1_M1DQ13_T18	T18	PHY RXD3	7
IO_L24P_1_M1DQ12_T17	T17	PHY RXD4	7
IO_L23N_1_M1UDQSN_N16	N16	PHY RXD5	7
IO_L23P_1_M1UDQS_N15	N15	PHY RXD6	7
IO_L22N_1_M1DQ11_P18	P18	PHY RXD7	7
IO_L22P_1_M1DQ10_P17	P17	PHY RXER	7
IO_L21N_1_M1DQ9_N18	N18	PHY RXCTL_RXDV	7
IO_L21P_1_HDC_M1DQ8_N17	N17	GPIO HDR0	10
IO_L20N_1_LDC_M1DQ1_M18	M18	GPIO HDR1	10
IO_L20P_1_FWE_B_M1DQ0_M16	M16	FLASH WE_B	8
IO_L19N_1_FOE_B_M1DQ3_L18	L18	FLASH OE_B	8
IO_L19P_1_FCS_B_M1DQ2_L17	L17	FLASH CE_B	8
IO_L18N_1_A0_M1DQSN_K18	K18	FLASH A0	8
IO_L18P_1_A1_M1DQSN_K17	K17	FLASH A1	8
IO_L17N_1_A2_M1DQ7_J18	J18	FLASH A2	8
IO_L17P_1_A3_M1DQ6_J16	J16	FLASH A3	8
IO_L16N_1_GCLK4_M1DQ5_H18	H18	SMACLK_N	9
IO_L16P_1_GCLK5_M1DQ4_H17	H17	SMACLK_P	9
IO_L15N_1_GCLK6_TRDY1_M1LDM_L16	L16	PHY RXCLK	7
IO_L15P_1_GCLK7_M1UDM_L15	L15	GPIO HDR3	10
IO_L14N_1_GCLK8_M1CASN_K16	K16	SYSCLK_N	9
IO_L14P_1_GCLK9_IRDY1_MIRASNK15	K15	SYSCLK_P	9
IO_L13N_1_GCLK10_M1A6_L13	L13	PHY RESET	7
IO_L13P_1_GCLK11_M1A5_L12	L12	USB 1_RX	10
IO_L12N_1_M1ODT_K14	K14	USB 1_TX	10
IO_L12P_1_M1A3_J13	J13	PHY_INT	7
IO_L11N_1_A4_M1CLKN_G18	G18	FLASH A4	8
IO_L11P_1_A5_M1CLK_G16	G16	FLASH A5	8
IO_L10N_1_A6_M1A1_H16	H16	FLASH A6	8
IO_L10P_1_A7_M1A0_H15	H15	FLASH A7	8
IO_L09N_1_A8_M1BA1_H14	H14	FLASH A8	8
IO_L09P_1_A9_M1BA0_H13	H13	FLASH A9	8
IO_L08N_1_A10_M1A2_F18	F18	FLASH A10	8
IO_L08P_1_A11_M1A7_F17	F17	FLASH A11	8
IO_L07N_1_A12_M1BA2_K13	K13	FLASH A12	8
IO_L07P_1_A13_M1WE_K12	K12	FLASH A13	8
IO_L06N_1_A14_M1A4_E18	E18	FLASH A14	8
IO_L06P_1_A15_M1A10_E16	E16	FLASH A15	8
IO_L05N_1_A16_M1A9_G13	G13	FLASH A16	8
IO_L05P_1_A17_M1A8_H12	H12	FLASH A17	8
IO_L04N_1_A18_M1A12_D18	D18	FLASH A18	8
IO_L04P_1_A19_M1CKE_D17	D17	FLASH A19	8
IO_L03N_1_A20_M1A11_G14	G14	FLASH A20	8
IO_L03P_1_A21_M1RESET_F14	F14	FLASH A21	8
IO_L02N_1_A22_M1A14_C18	C18	FLASH A22	8
IO_L02P_1_A23_M1A13_C17	C17	FLASH A23	8
IO_L01N_1_A24_VREF_1_F16	F16	FLASH A24	8
IO_L01P_1_A25_F15	F15	GPIO HDR4	10

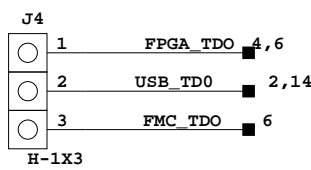


VCC0_1_R17
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VCC0_1_J17
VCC0_1_J14
VCC0_1_G15
VCC0_1_E17

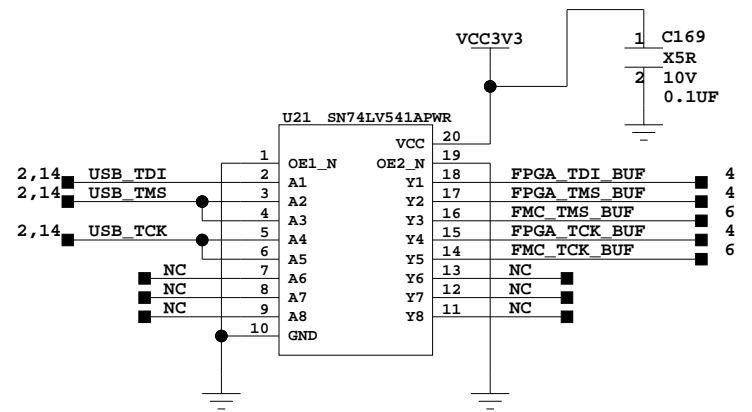


U1

U1



**Jumper to include FMC
in JTAG chain**



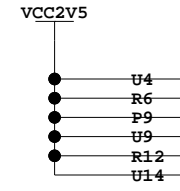
Banks 0, 1



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Date: 10-20-2009_14:56	Ver: C		
Sheet Size: B	Rev: 04		
Sheet 2 of 16	Drawn By BF		

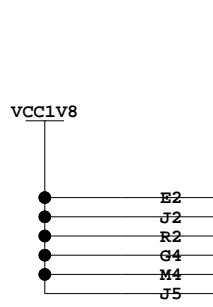
**SOCKET
BANK 2
sa16cs324**

PROGRAM_B_V2	V2	FPGA PROG B	8,9
IO_L30N_2_CS0_B_V3	V3	SPI_CS_B	8
IO_L30P_2_INIT_B_U3	U3	FPGA_INIT_B	9
IO_L29N_2_D9_P6	P6	FMC LA23 N	6
IO_L29P_2_D8_N5	N5	FMC LA23 P	6
IO_L28N_2_V4	V4	FMC LA21 N	6
IO_L28P_2_T4	T4	FMC LA21 P	6
IO_L27N_2_D6_T3	T3	FLASH D6	8
IO_L27P_2_D5_R3	R3	FLASH D5	8
IO_L26N_2_D4_V5	V5	FLASH D4	8
IO_L26P_2_D3_U5	U5	FLASH D3	8
IO_L25N_2_RDWR_B_VREF_2_T5	T5	USB_1_RTS	10
IO_L25P_2_D7_R5	R5	FLASH D7	8
IO_L24N_2_P7	P7	FMC LA19 N	6
IO_L24P_2_N6	N6	FMC LA19 P	6
IO_L23N_2_T7	T7	FMC LA22 N	6
IO_L23P_2_R7	R7	FMC LA22 P	6
IO_L22N_2_V6	V6	FMC LA31 N	6
IO_L22P_2_T6	T6	FMC LA31 P	6
IO_L21N_2_P8	P8	FMC LA20 N	6
IO_L21P_2_N7	N7	FMC LA20 P	6
IO_L20N_2_V7	V7	FMC LA26 N	6
IO_L20P_2_U7	U7	FMC LA26 P	6
IO_L19N_2_VREF_2_V8	V8	FMC LA24 N	6
IO_L19P_2_U8	U8	FMC LA24 P	6
IO_L18N_2_N8	N8	FMC LA29 N	6
IO_L18P_2_M8	M8	FMC LA29 P	6
IO_L17N_2_GCLK28_V9	V9	FMC CLK1 M2C N	6
IO_L17P_2_GCLK29_T9	T9	FMC CLK1 M2C P	6
IO_L16N_2_GCLK30_D15_T8	T8	FMC LA17 CC N	6
IO_L16P_2_GCLK31_D14_R8	R8	FMC LA17 CC P	6
IO_L15N_2_GCLK0_CFGMCLK_V10	V10	USER_CLOCK	9
IO_L15P_2_GCLK1_D13_U10	U10	USB_1_CTS	10
IO_L14N_2_GCLK2_T10	T10	FMC LA18 CC N	6
IO_L14P_2_GCLK3_R10	R10	FMC LA18 CC P	6
IO_L13N_2_V11	V11	FMC LA28 N	6
IO_L13P_2_U11	U11	FMC LA28 P	6
IO_L12N_2_N9	N9	FMC LA33 N	6
IO_L12P_2_M10	M10	FMC LA33 P	6
IO_L11N_2_P11	P11	IIC_SCL_MAIN	10
IO_L11P_2_N10	N10	IIC_SDA_MAIN	10
IO_L10N_2_V12	V12	FMC LA30 N	6
IO_L10P_2_T12	T12	FMC LA30 P	6
IO_L09N_2_VREF_2_T11	T11	FMC LA27 N	6
IO_L09P_2_R11	R11	FMC LA27 P	6
IO_L08N_2_N11	N11	FMC LA25 N	6
IO_L08P_2_M11	M11	FMC LA25 P	6
IO_L07N_2_D12_V13	V13	GPIO_SWITCH_3	9
IO_L07P_2_D11_U13	U13	FMC PRSNT M2C L	10
IO_L06N_2_D10_P12	P12	GPIO_HDR7	10
IO_L06P_2_M1_N12	N12	FPGA_M1	8
IO_L05N_2_D2_MISO3_V14	V14	FPGA_D2_MISO3	8
IO_L05P_2_D1_MISO2_T14	T14	FPGA_D1_MISO2	8
IO_L04N_2_V15	V15	FMC LA32 N	6
IO_L04P_2_U15	U15	FMC LA32 P	6
IO_L03N_2_MOSI_CSI_B_MISO0_T13	T13	FPGA_MOSI_CSI_B_MISO0	8
IO_L03P_2_D0_DIN_MISO_MISO1_R13	R13	FPGA_D0_DIN_MISO_MISO1	8
IO_L02N_2_CMP_MOSI_V16	V16	FPGA_CMP_MOSI	8
IO_L02P_2_CMP_CLK_U16	U16	FPGA_CMP_CLK	8
IO_L01N_2_M0_CMP_MISO_T15	T15	FPGA_M0_CMP_MISO	8
IO_L01P_2_CCLK_R15	R15	FPGA_CCLK	8
DONE_V17	V17	FPGA_DONE	9
CMP_CS_B_P13	P13	FPGA_CMP_CS_B	8



**SOCKET
BANK 3
sa16cs324**

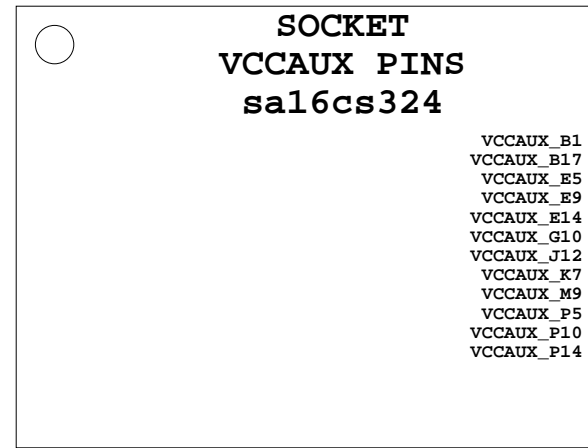
IO_L28N_3_VREF_3_C1	C1	FPGA_ONCHIP_TERM2	9
IO_L28P_3_C2	C2	GPIO_BUTTON3	9
IO_L27N_3_M3A14_F5	F5	GPIO_BUTTON1	9
IO_L27P_3_M3A13_F6	F6	DDR2_A11	5
IO_L26N_3_M3A11_D3	D3	GPIO_BUTTON2	9
IO_L26P_3_M3RESET_E4	E4	DDR2_A12	5
IO_L25N_3_M3A12_G6	G6	DDR2_CKE	5
IO_L25P_3_M3CKE_H7	H7	DDR2_A9	5
IO_L24N_3_M3A9_D1	D1	DDR2_A8	5
IO_L24P_3_M3A8_D2	D2	DDR2_A4	5
IO_L23N_3_M3A4_F3	F3	DDR2_A10	5
IO_L23P_3_M3A10_F4	F4	DDR2_BA2	5
IO_L22N_3_M3BA2_E1	E1	DDR2_WE_B	5
IO_L22P_3_M3WE_E3	E3	DDR2_A2	5
IO_L21N_3_M3A2_H5	H5	DDR2_A7	5
IO_L21P_3_M3A7_H6	H6	DDR2_BA1	5
IO_L20N_3_M3BA1_F1	F1	DDR2_BA0	5
IO_L20P_3_M3BA0_F2	F2	DDR2_A1	5
IO_L19N_3_M3A1_J6	J6	DDR2_A0	5
IO_L19P_3_M3A0_J7	J7	DDR2_CLK_N	5
IO_L18N_3_M3CLKN_G1	G1	DDR2_CLK_P	5
IO_L18P_3_M3CLK_G3	G3	DDR2_ODT	5
IO_L17N_3_M3ODT_K6	K6	DDR2_A3	5
IO_L17P_3_M3A3_L7	L7	DDR2_A6	5
IO_L16N_3_GCLK20_M3A6_H3	H3	DDR2_A5	5
IO_L16P_3_GCLK21_M3A5_H4	H4	DDR2_CAS_B	5
IO_L15N_3_GCLK22_IRDY2_M3CASNK5	K5	DDR2_RAS_B	5
IO_L15P_3_GCLK23_M3RASN_L5	L5	DDR2_LDM	5
IO_L14N_3_GCLK24_M3LDM_K3	K3	DDR2_UDM	5
IO_L14P_3_GCLK25_TRDY2_M3UDM_K4	K4	DDR2_DQ5	5
IO_L13N_3_GCLK26_M3DQ5_H1	H1	DDR2_DQ4	5
IO_L13P_3_GCLK27_M3DQ4_H2	H2	DDR2_DQ7	5
IO_L12N_3_M3DQ7_J1	J1	DDR2_DQ6	5
IO_L12P_3_M3DQ6_J3	J3	DDR2_LDQS_N	5
IO_L11N_3_M3LDQSN_L3	L3	DDR2_LDQS_P	5
IO_L11P_3_M3LDQS_L4	L4	DDR2_DQ3	5
IO_L10N_3_M3DQ3_K1	K1	DDR2_DQ2	5
IO_L10P_3_M3DQ2_K2	K2	DDR2_DQ1	5
IO_L09N_3_M3DQ1_L1	L1	DDR2_DQ0	5
IO_L09P_3_M3DQ0_L2	L2	DDR2_DQ9	5
IO_L08N_3_M3DQ9_M1	M1	DDR2_DQ8	5
IO_L08P_3_M3DQ8_M3	M3	DDR2_DQ11	5
IO_L07N_3_M3DQ11_N1	N1	DDR2_DQ10	5
IO_L07P_3_M3DQ10_N2	N2	DDR2_UDQS_N	5
IO_L06N_3_M3UDQSN_P1	P1	DDR2_UDQS_P	5
IO_L06P_3_M3UDQS_P2	P2	DDR2_DQ13	5
IO_L05N_3_M3DQ13_T1	T1	DDR2_DQ12	5
IO_L05P_3_M3DQ12_T2	T2	DDR2_DQ15	5
IO_L04N_3_M3DQ15_U1	U1	DDR2_DQ14	5
IO_L04P_3_M3DQ14_U2	U2	FPGA_DDR2_VREF	5
IO_L03N_3_VREF_3_M5	M5	FPGA_ONCHIP_TERM1	9
IO_L03P_3_L6	L6	FPGA_VTEMP	9
IO_L02N_3_P3	P3	GPIO_BUTTON0	9
IO_L02P_3_P4	P4	CPU_RESET	9
IO_L01N_3_VREF_3_N3	N3		
IO_L01P_3_N4	N4		



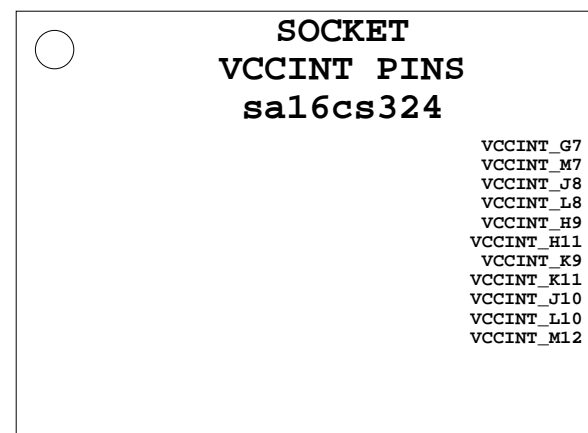
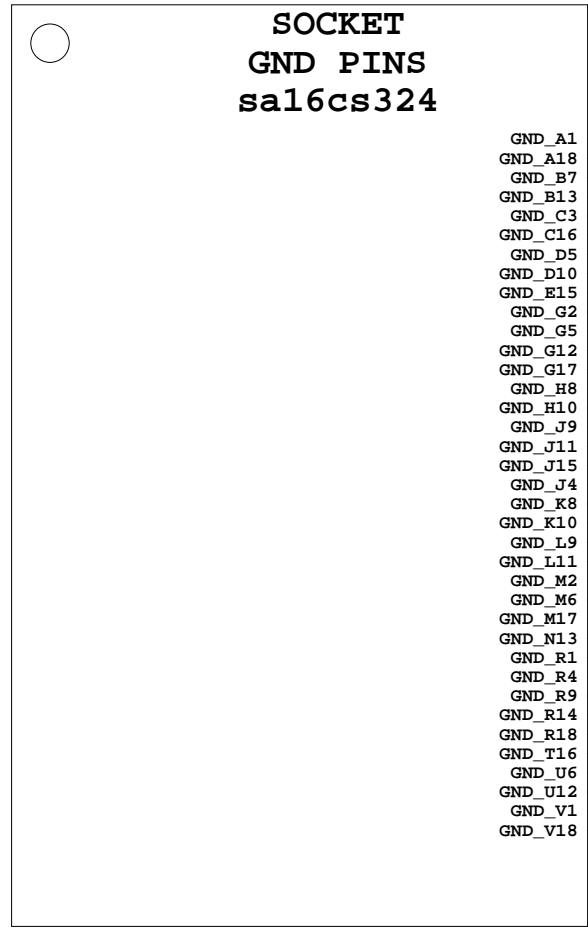
Banks 2, 3



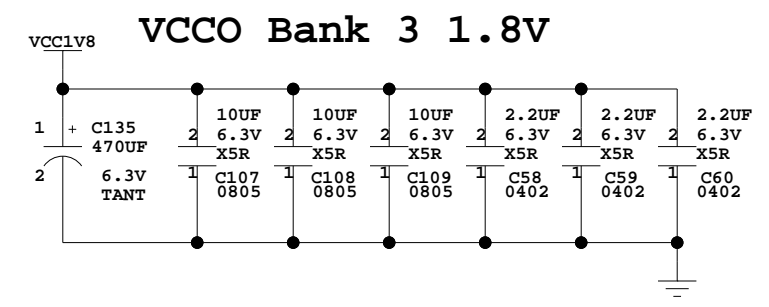
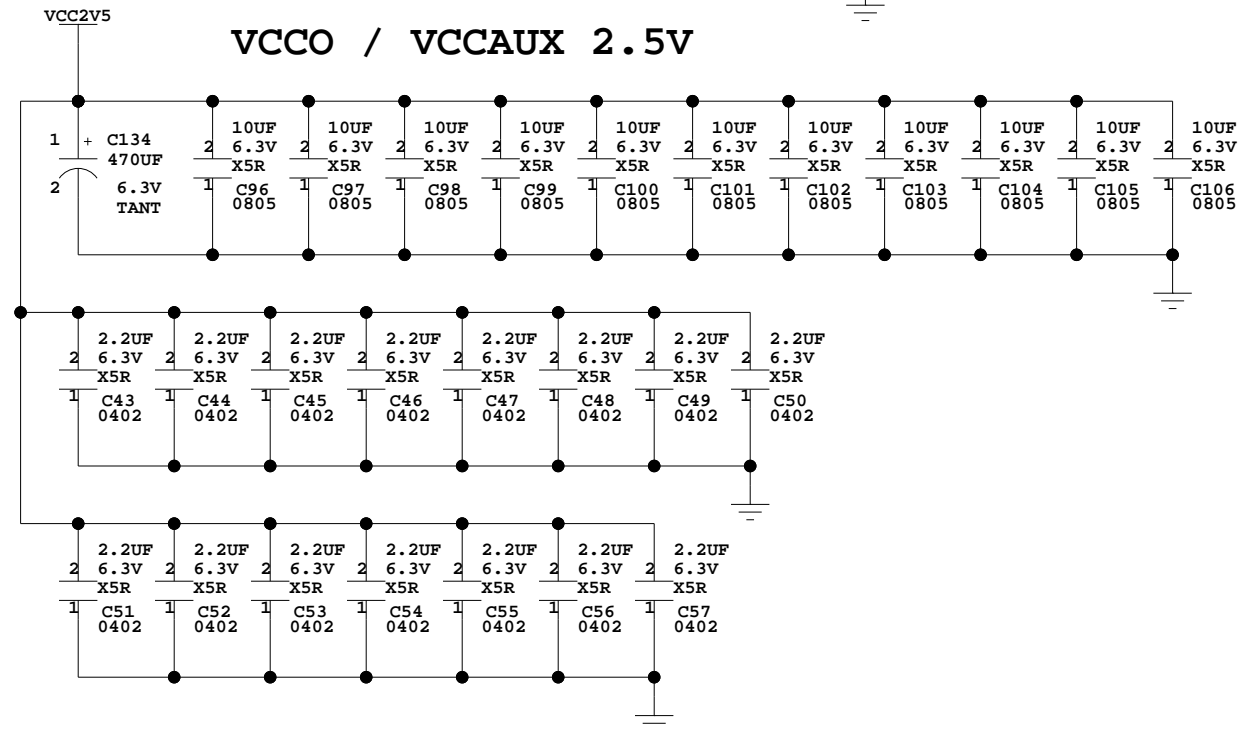
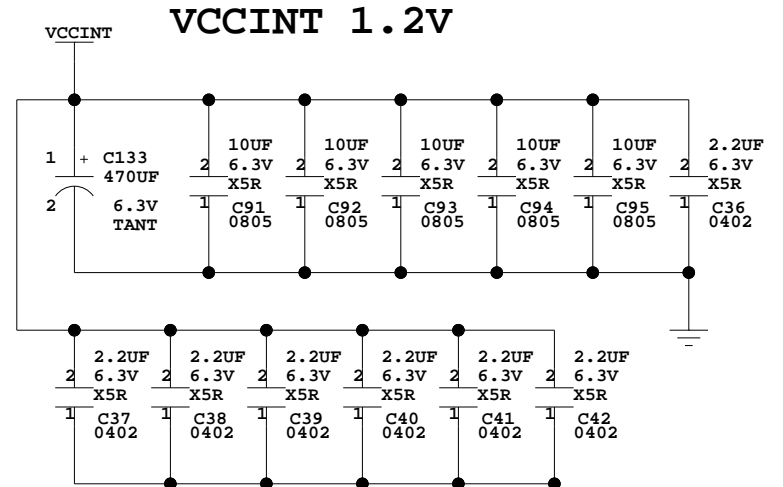
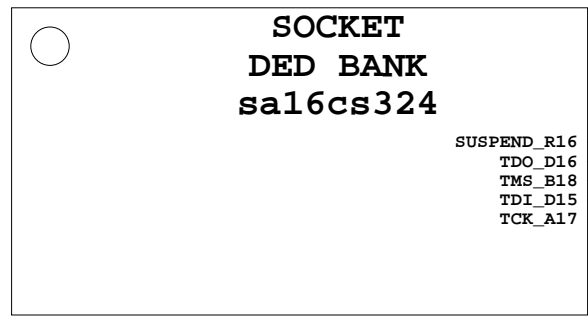
Title: Banks 2, 3 SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:56	Ver: C		
Sheet Size: B	Rev: 04		
Sheet 3 of 16	Drawn By BF		



VCC2V5



VCCINT U1

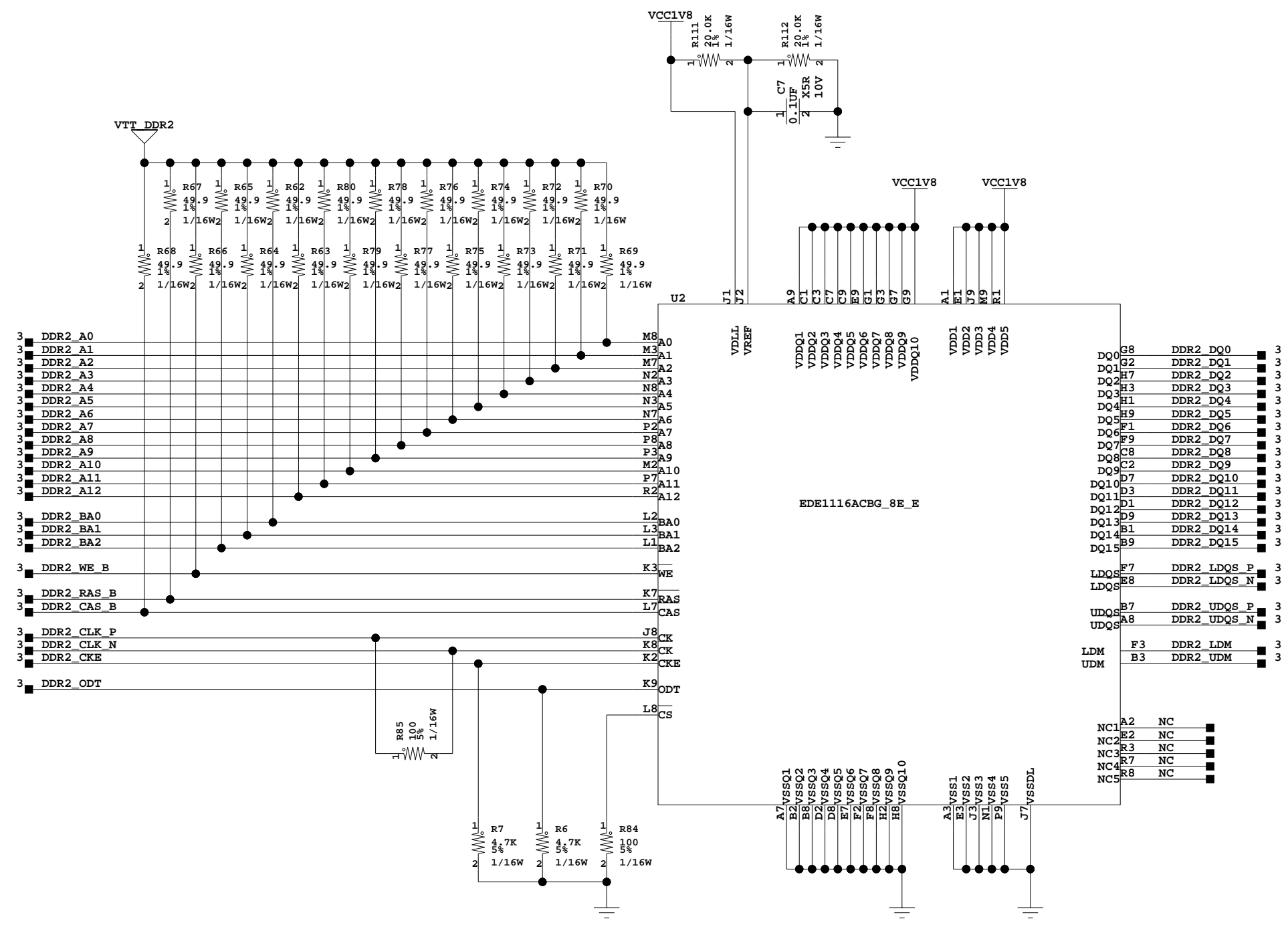


GND Bank, Decoupling caps

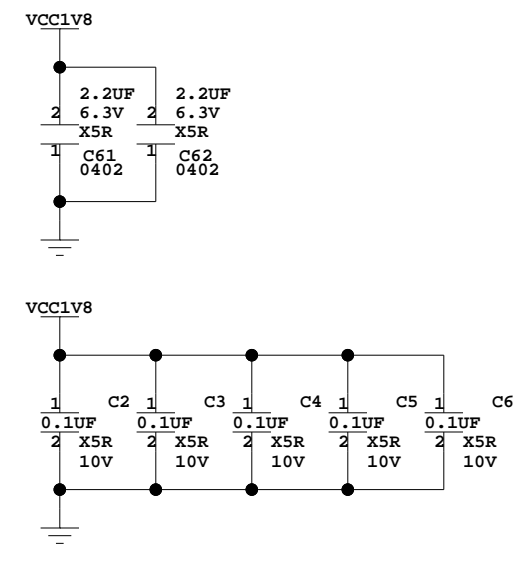


Title: GND Bank, Decoupling caps SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM
 PCB P/N: 0431512, 0431608
 SCH P/N: 0381290
 Test P/N: TSS0121
 ART P/N: 1280464

Date: 10-20-2009_14:54	Ver: C
Sheet Size: B	Rev: 04
Sheet 4 of 16	Drawn By BF



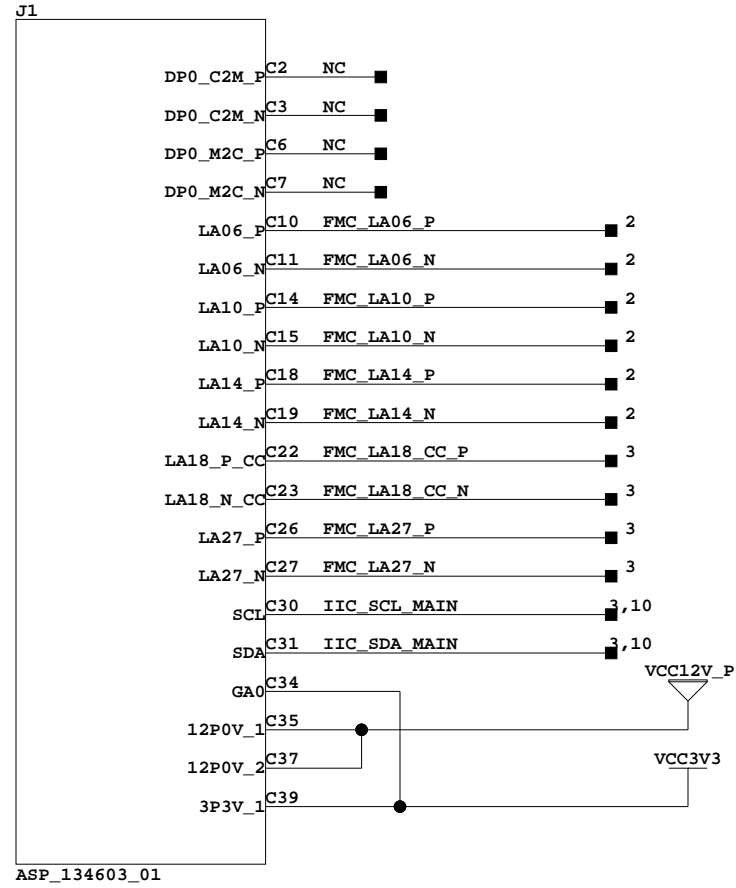
DDR2 Decoupling



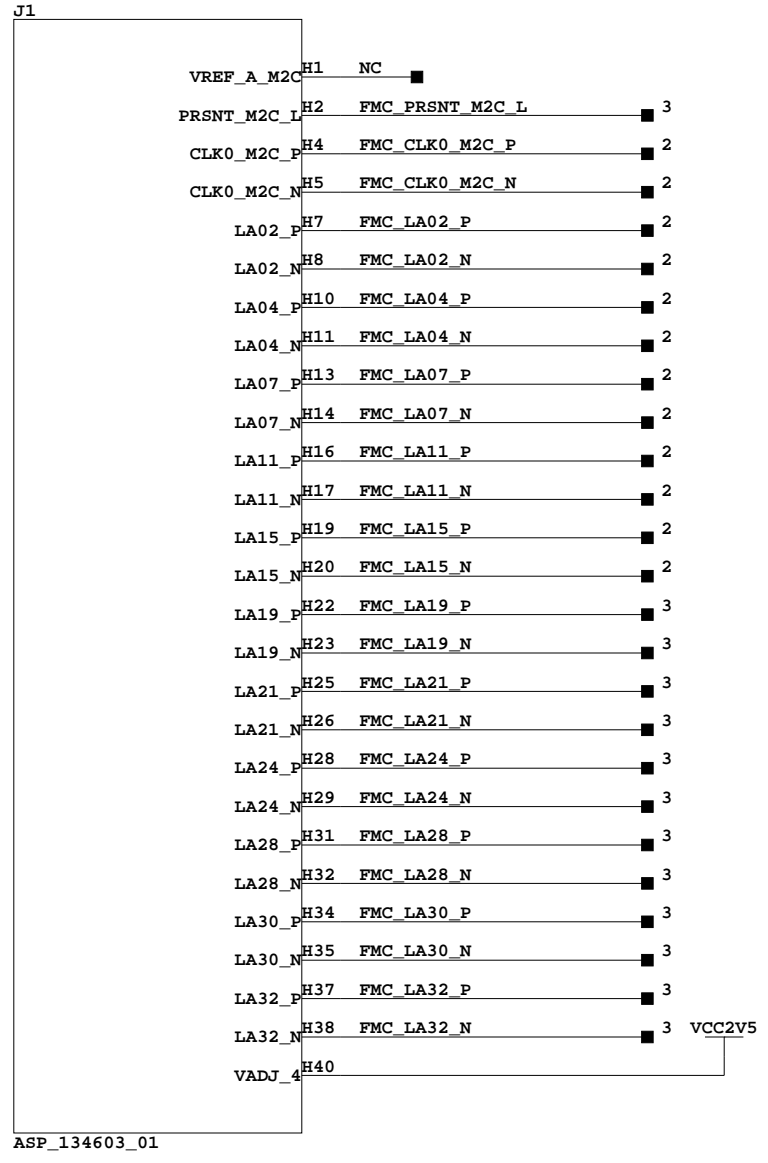
DDR2 SDRAM



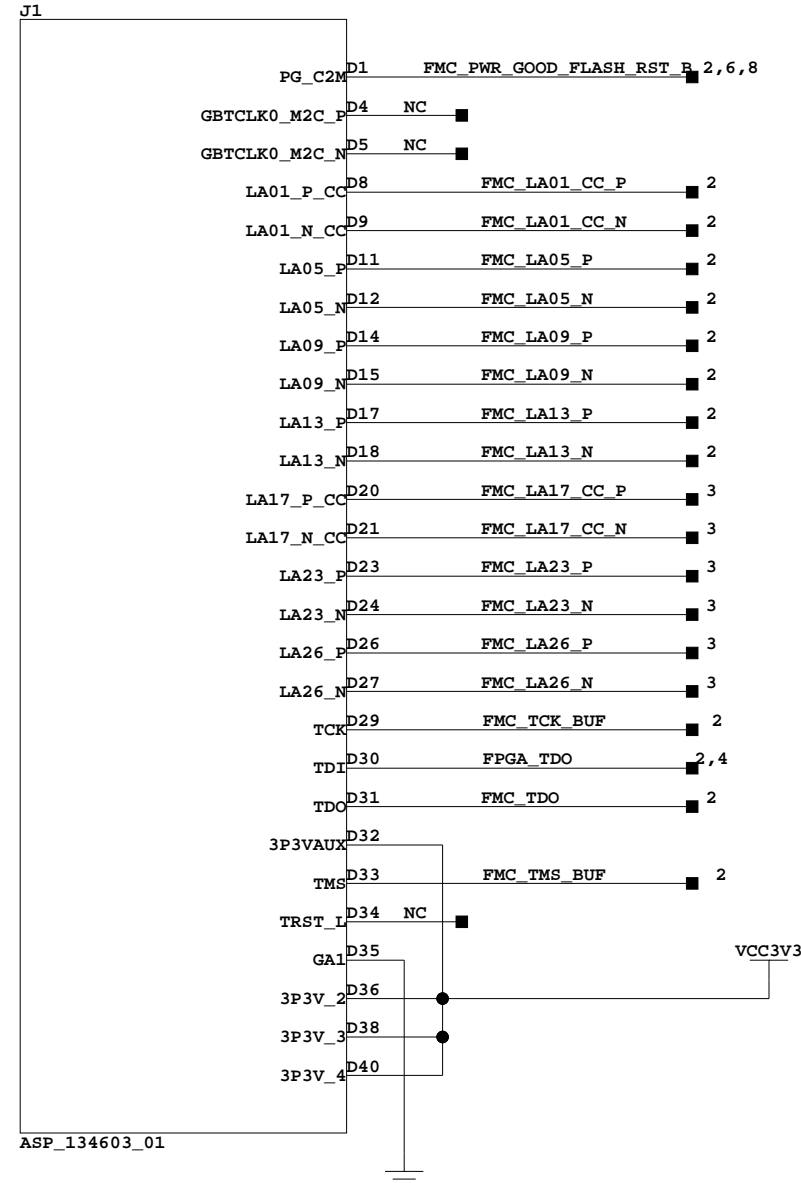
Title: DDR2 SDRAM SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:56	Ver: C		
Sheet Size: B	Rev: 04		
Sheet 5 of 16	Drawn By BF		



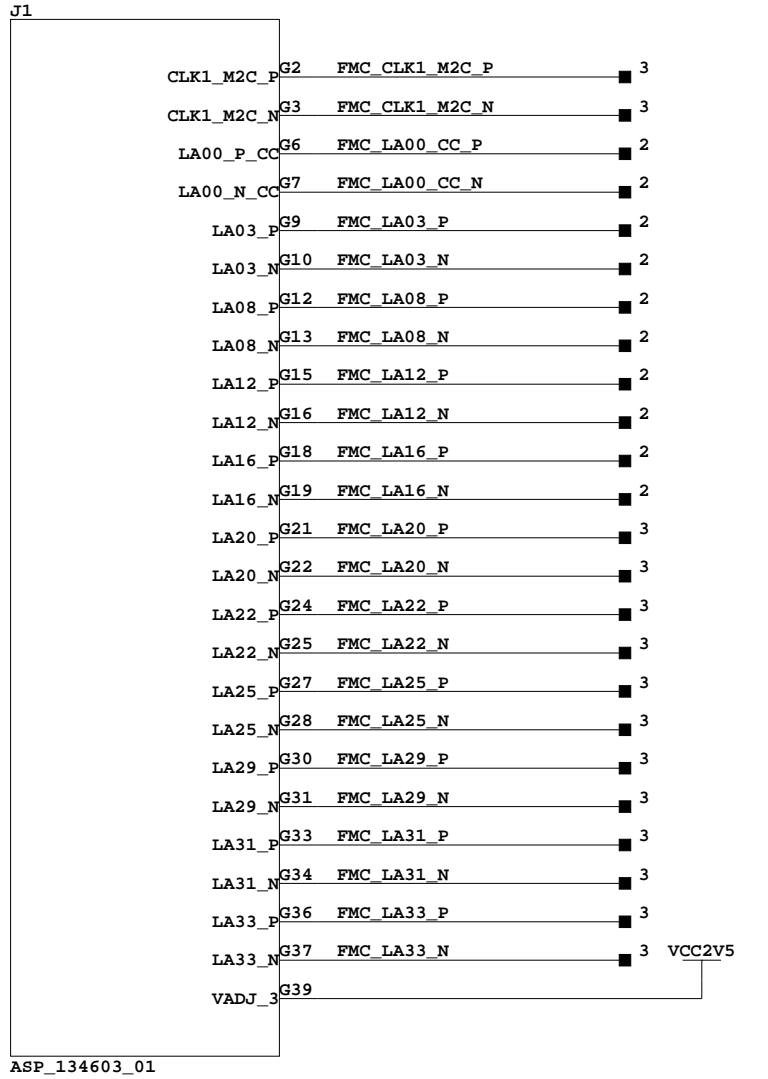
ASP_134603_01



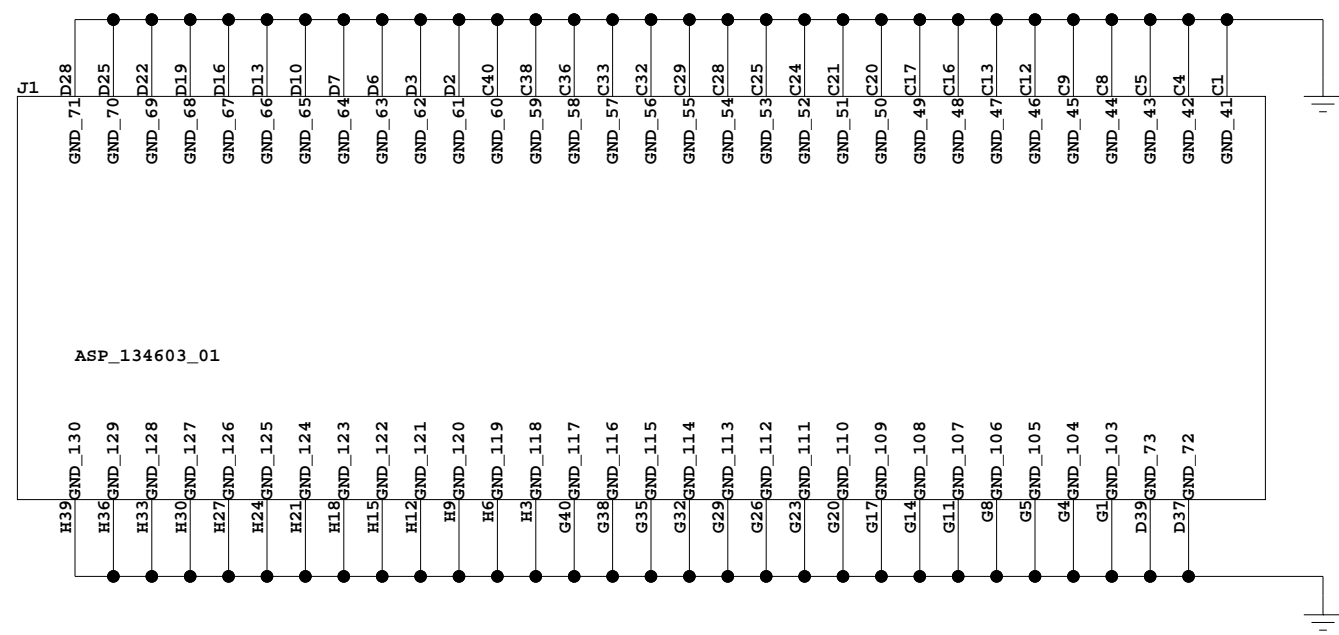
ASP_134603_01



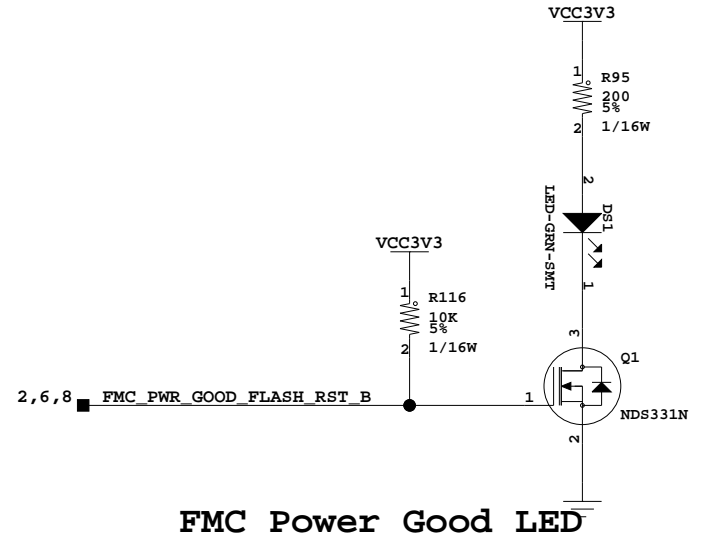
ASP_134603_01



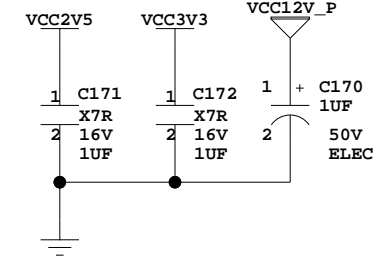
ASP_134603_01



ASP_134603_01



FMC Power Good LED



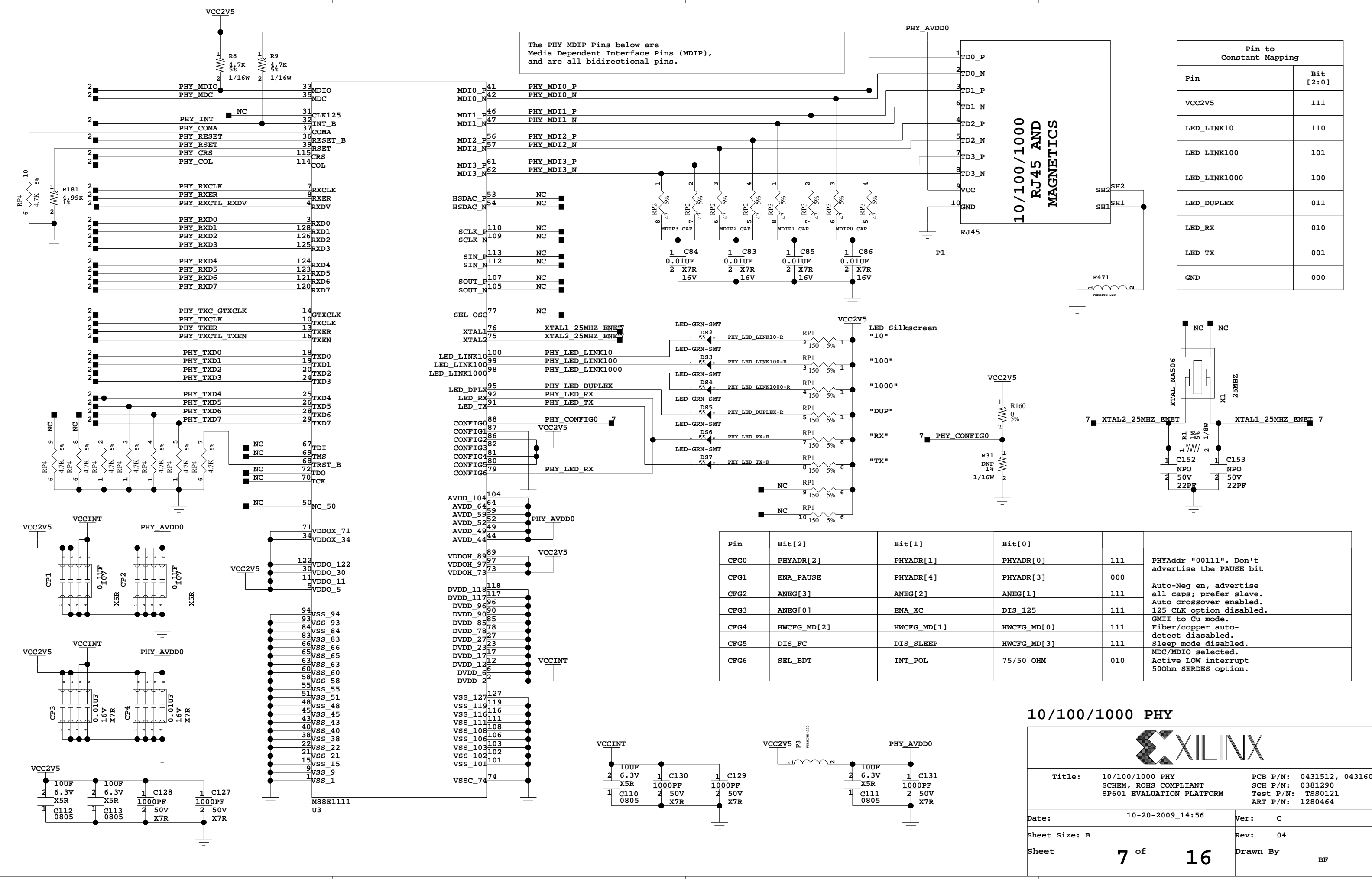
ANSI/VITA 57.1-2008 Version 1.1
FMC LPC Connector



Title:	FMC LPC Connector SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM	PCB P/N:	0431512, 0431608
		SCH P/N:	0381290
		Test P/N:	TSS0121
		ART P/N:	1280464

Date:	10-20-2009_14:56	Ver:	C
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The PHY MDIP Pins below are Media Dependent Interface Pins (MDIP), and are all bidirectional pins.



Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

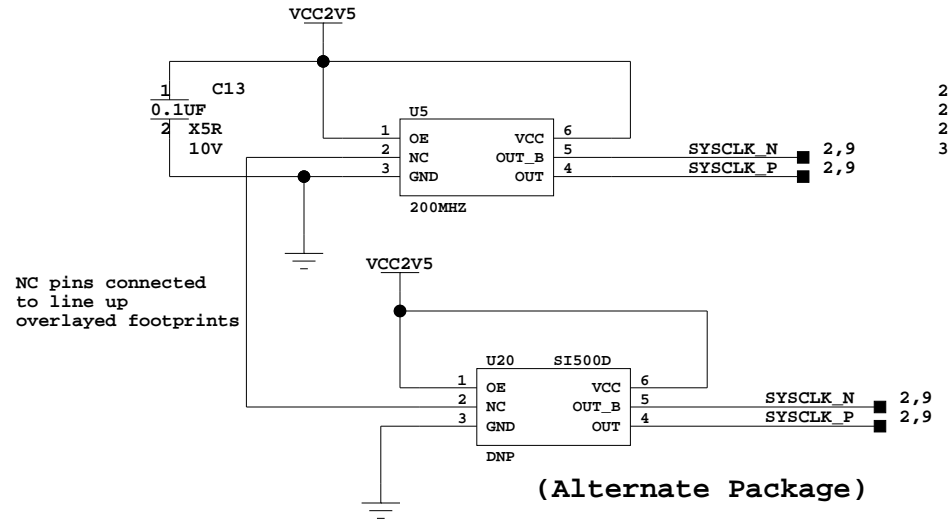
Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled.
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	MDC/MDIO selected. Active LOW interrupt 500hm SERDES option.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	

10/100/1000 PHY



Title: 10/100/1000 PHY SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM
 PCB P/N: 0431512, 0431608
 SCH P/N: 0381290
 Test P/N: TSS0121
 ART P/N: 1280464

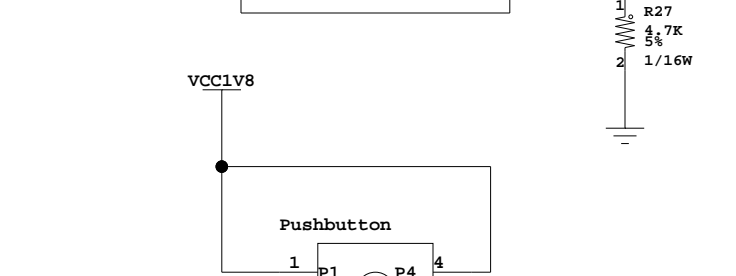
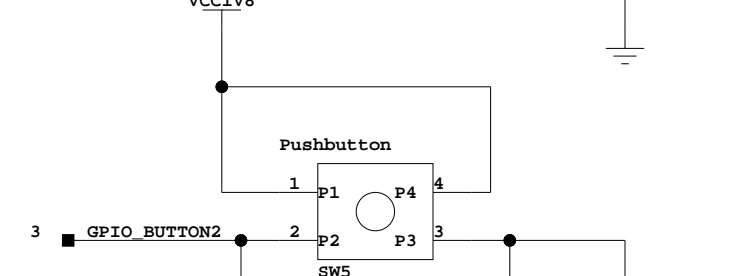
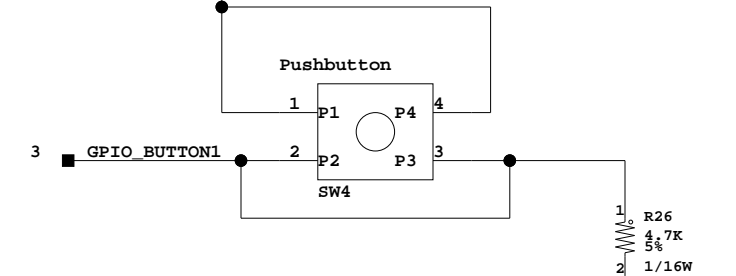
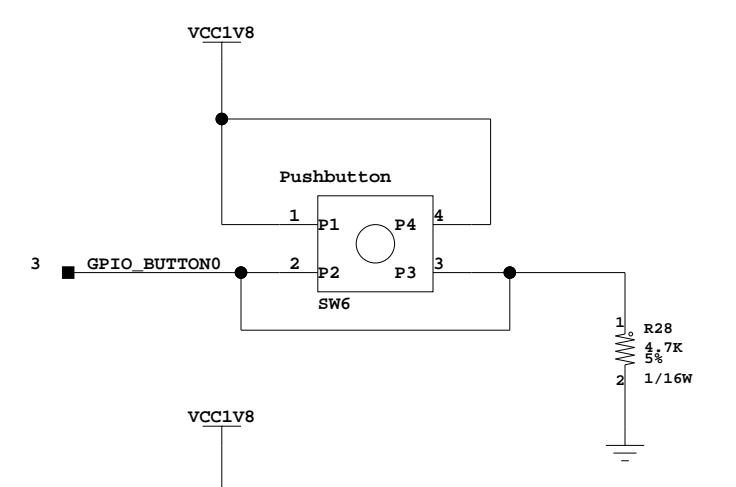
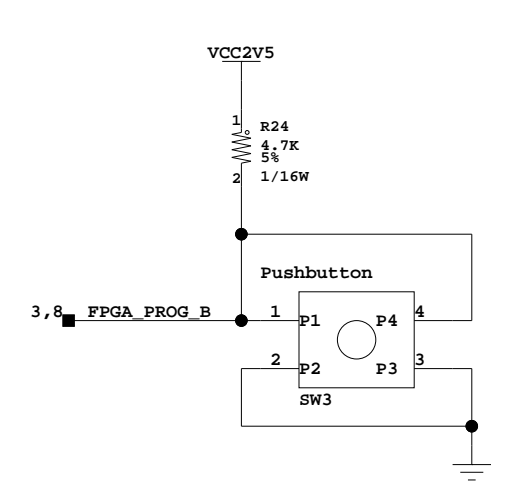
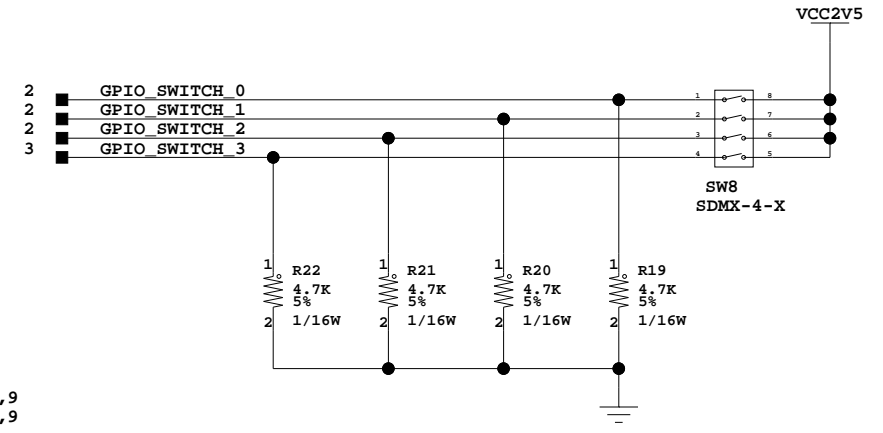
Date: 10-20-2009_14:56 Ver: C
 Sheet Size: B Rev: 04
 Sheet 7 of 16 Drawn By BF



(Alternate Package)

Differential System Clock

NC pins connected to line up overlaid footprints

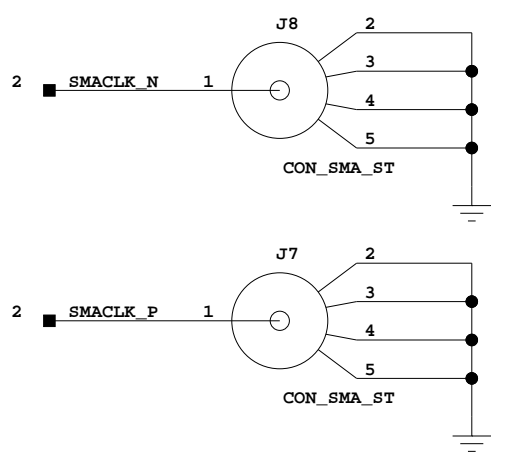


Clocks, LEDs, Buttons, Switches

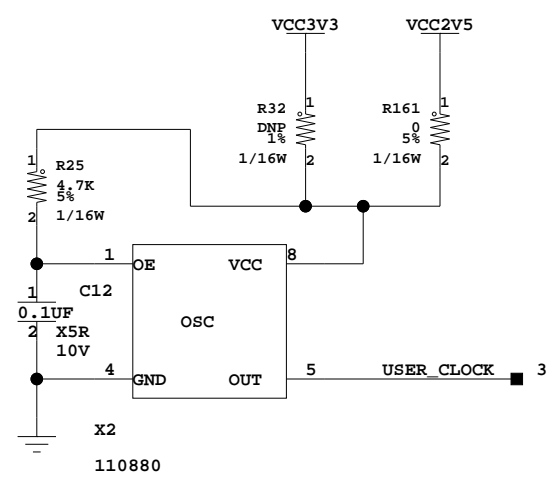
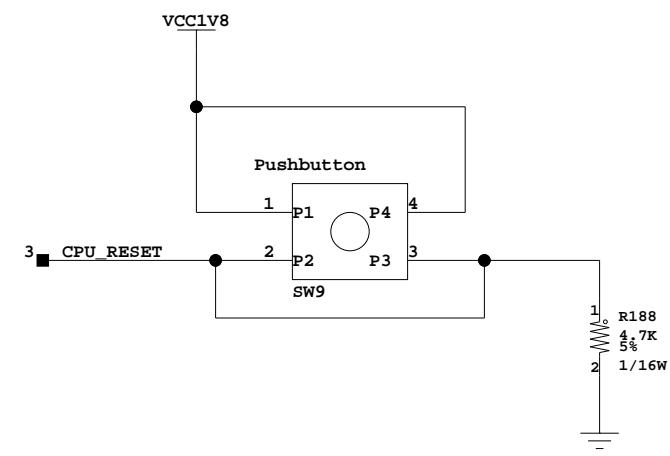
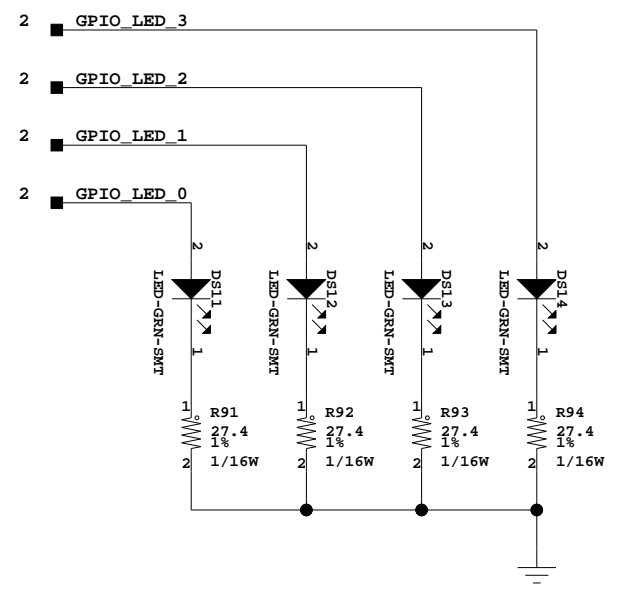


Title: Clocks, LEDs, Buttons, SwitchesPCB P/N: 0431512, 0431608
 SCHEM, ROHS COMPLIANT SCH P/N: 0381290
 SP601 EVALUATION PLATFORM Test P/N: TSS0121
 ART P/N: 1280464

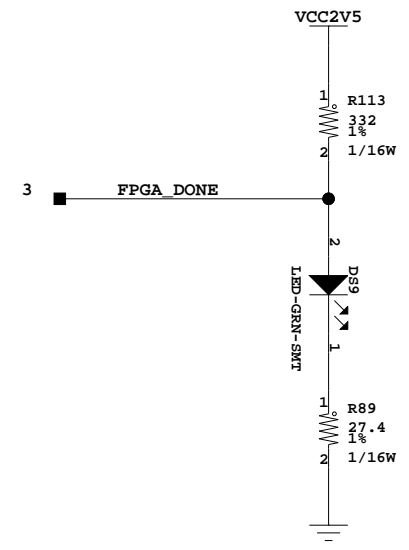
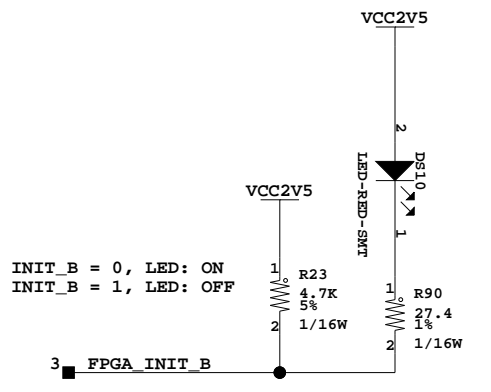
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Sheet Size:	B	Rev:	04
Sheet	9 of 16	Drawn By	BF

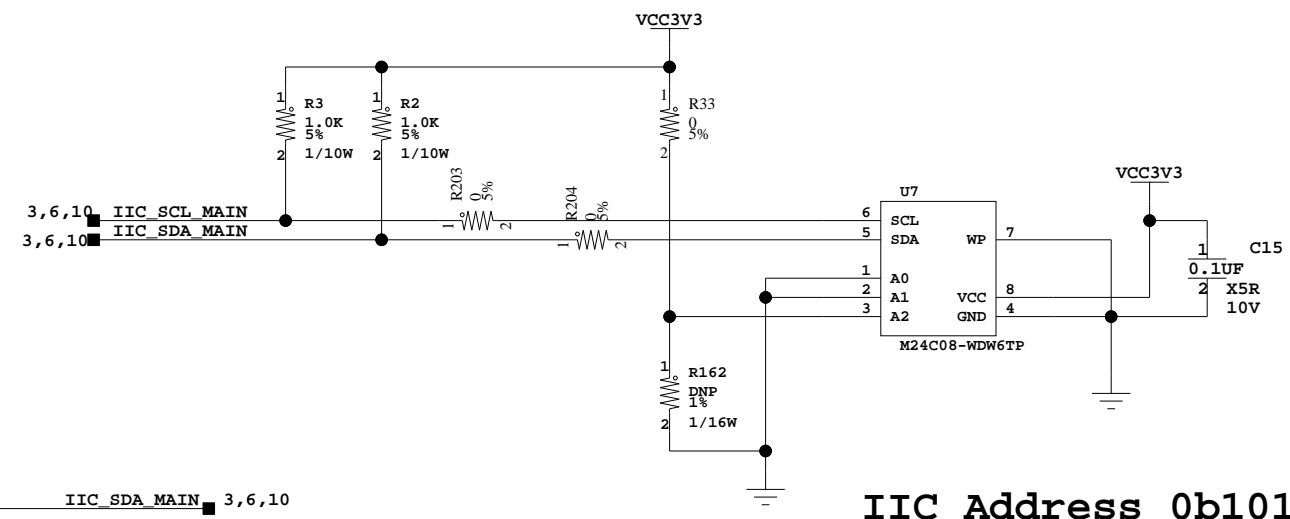


SMA Differential Clock

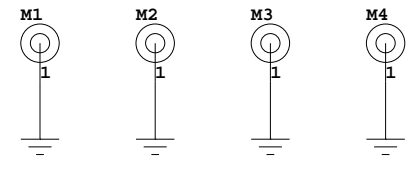


Single Ended User Clock

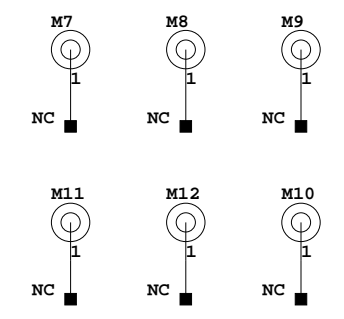




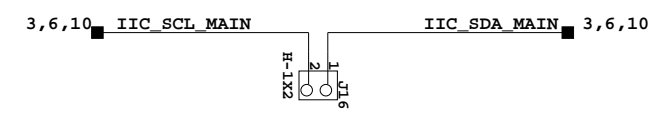
IIC Address 0b1010100



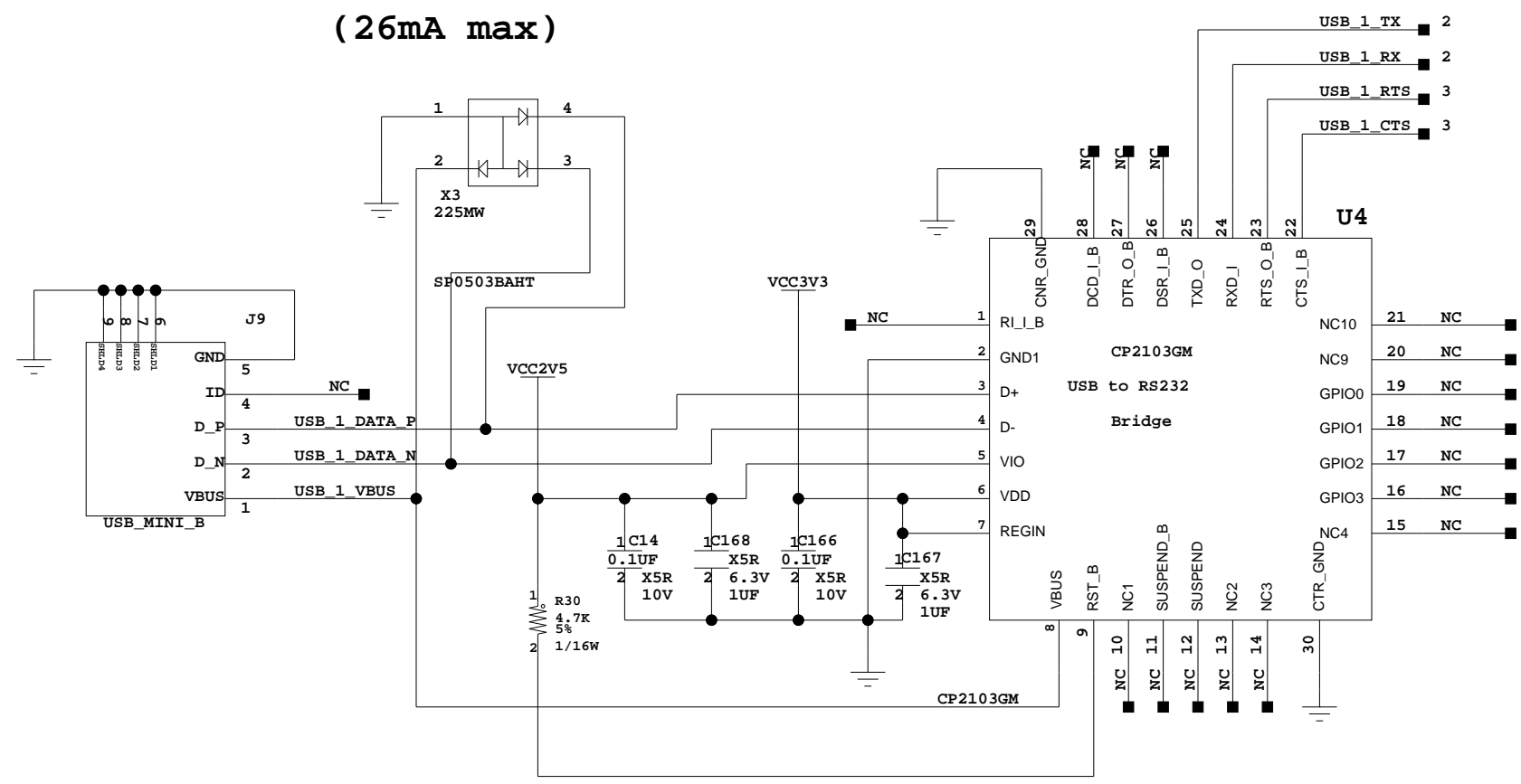
Mounting Holes



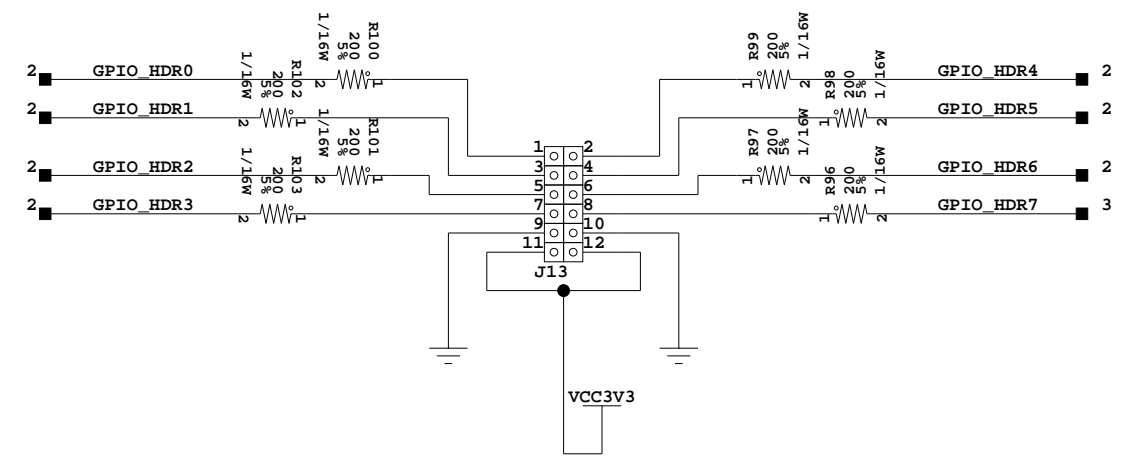
Fiducials



CP2103 USB Self-Powered
(26mA max)

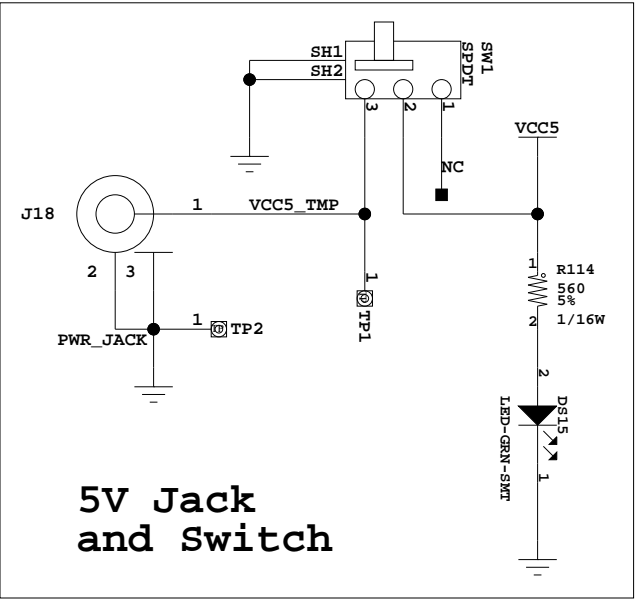
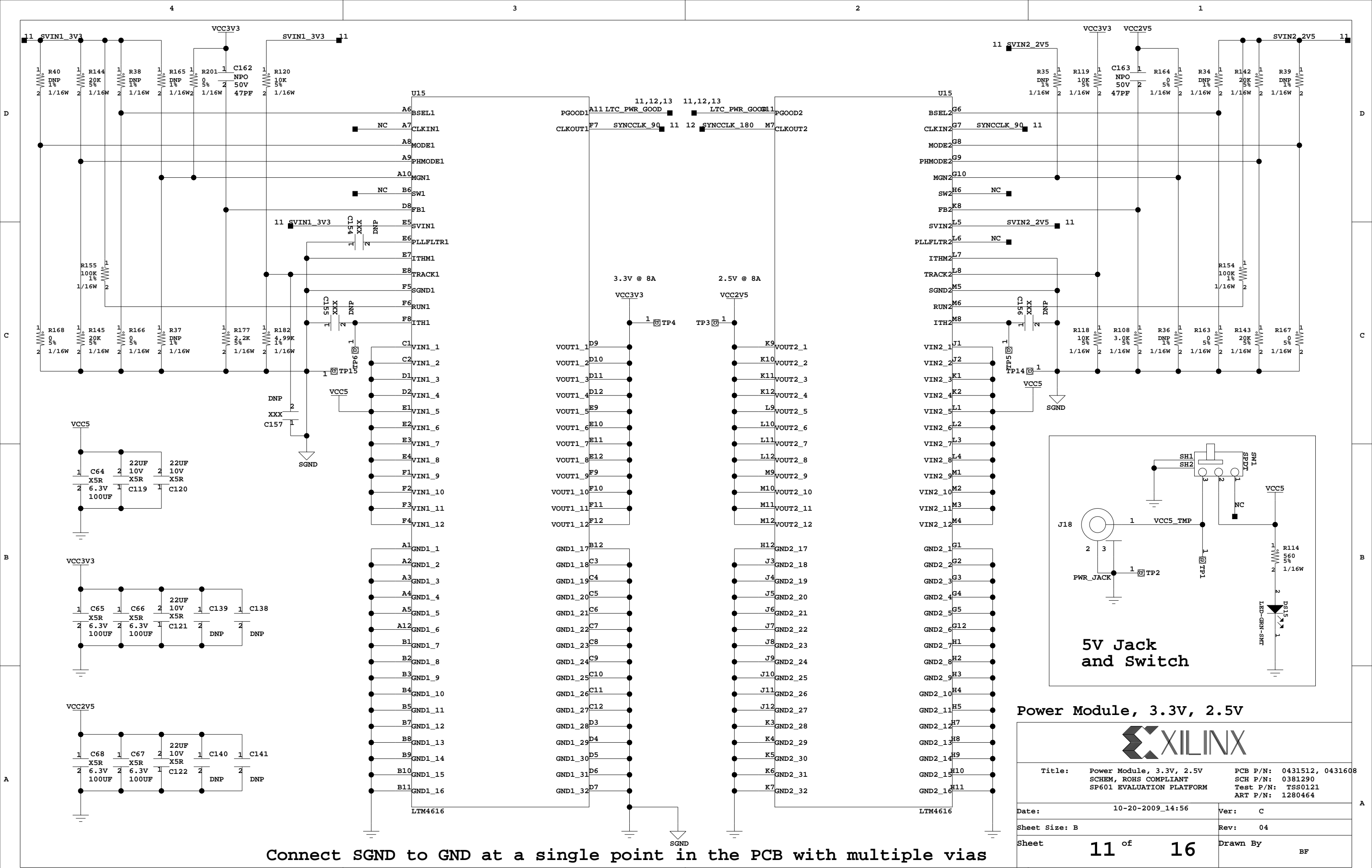


The VIO voltage must match the appropriate bank IO voltage



UART, IIC Header/EEPROM, GPIO Headers

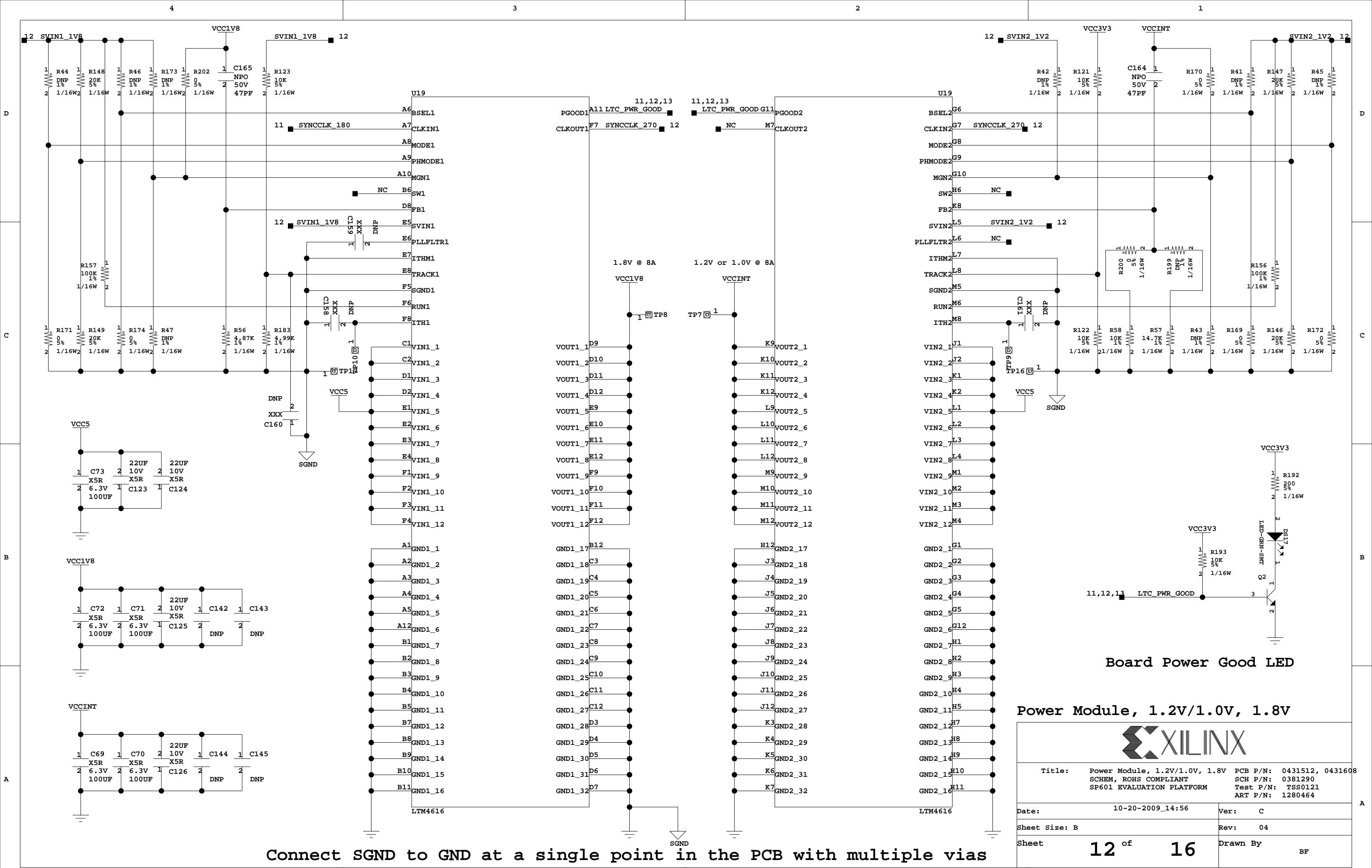
Title: UART, IIC Header/EEPROM, GPIO Headers	
PCB P/N: 0431512, 0431608	
SCH P/N: 0381290	
SCHEM, ROHS COMPLIANT	
Test P/N: TSS0121	
SP601 EVALUATION PLATFORM	
ART P/N: 1280464	
Date: 10-20-2009_14:56	Ver: C
Sheet Size: B	Rev: 04
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Power Module, 3.3V, 2.5V

Title: Power Module, 3.3V, 2.5V SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM	
PCB P/N: 0431512, 0431608	
SCH P/N: 0381290	
Test P/N: TSS0121	
ART P/N: 1280464	
Date: 10-20-2009_14:56	Ver: C
Sheet Size: B	Rev: 04
Sheet 11 of 16	Drawn By BF

Connect SGND to GND at a single point in the PCB with multiple vias



Connect SGND to GND at a single point in the PCB with multiple vias

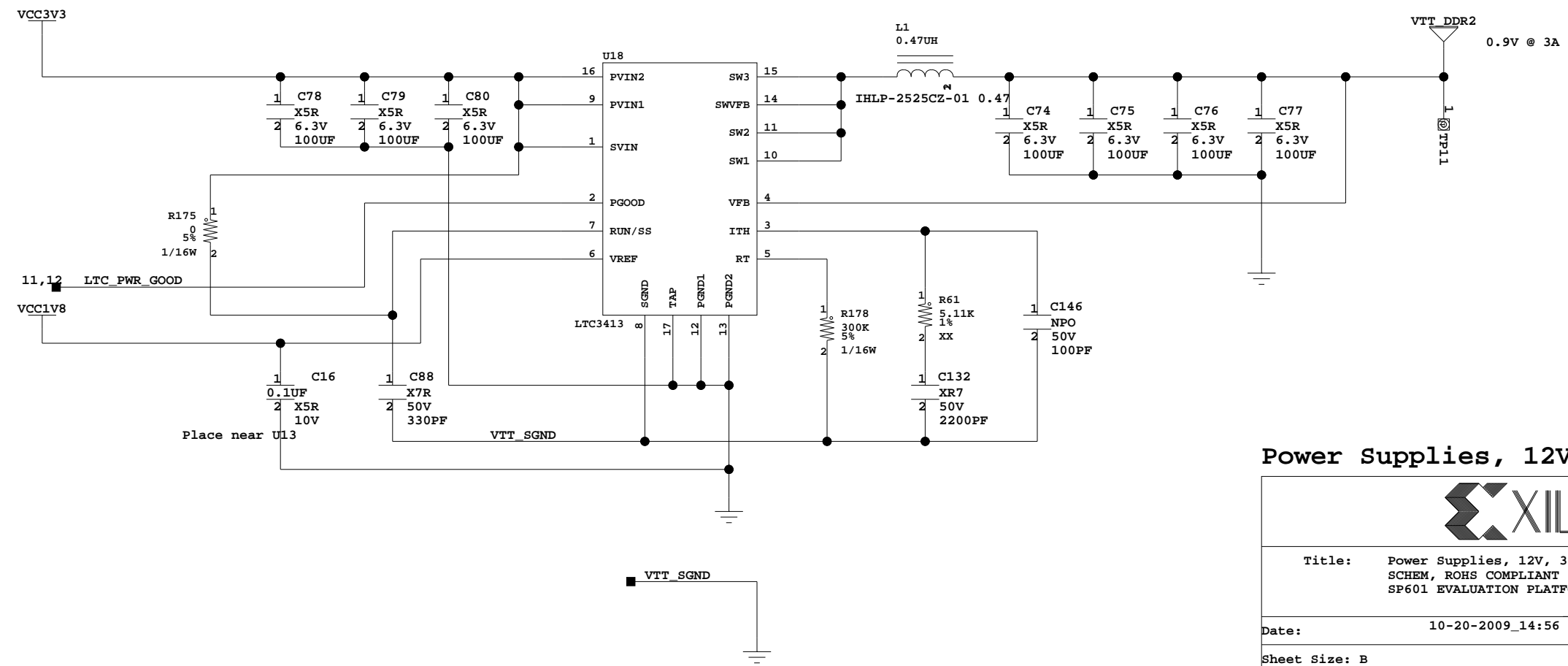
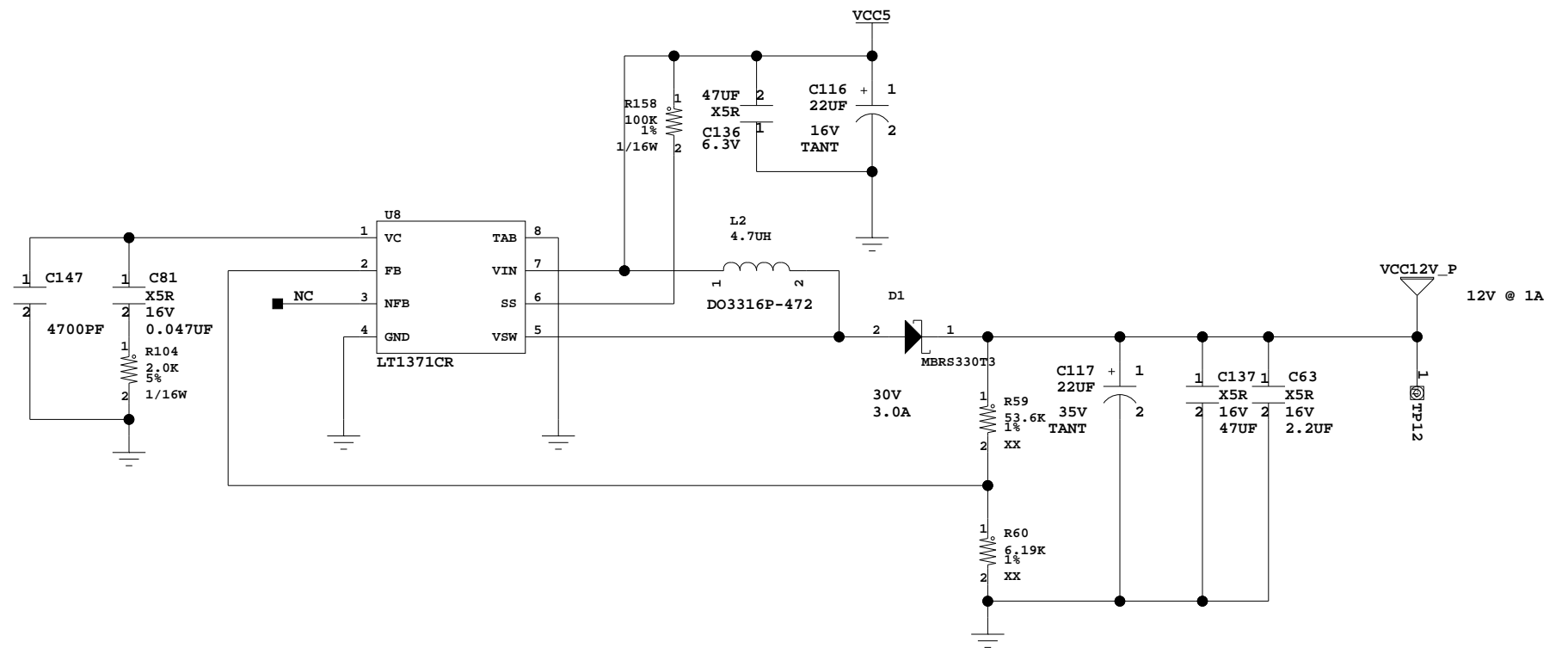
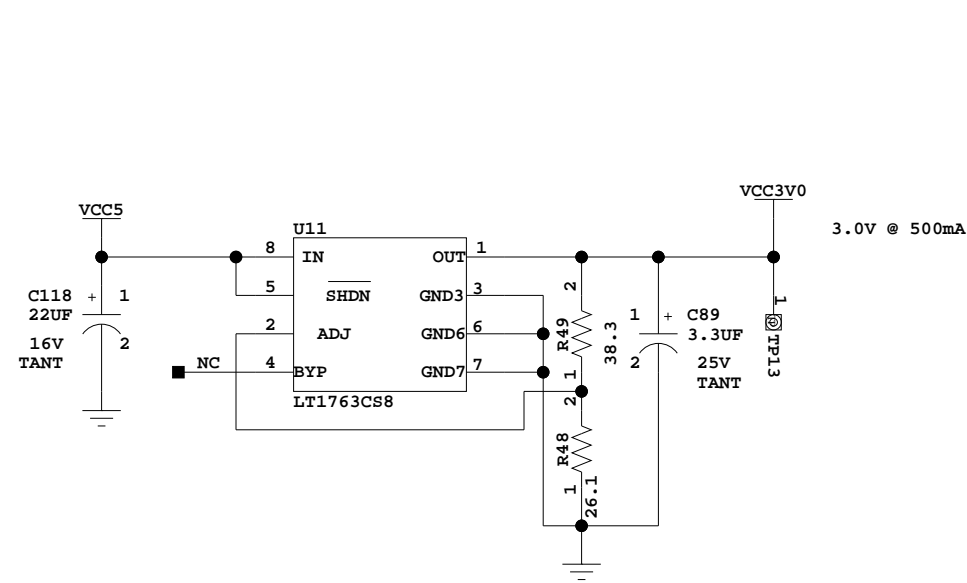
Board Power Good LED

Power Module, 1.2V/1.0V, 1.8V



Title: Power Module, 1.2V/1.0V, 1.8V PCB P/N: 0431512, 0431608
 SCHEM, ROHS COMPLIANT SCH P/N: 0381290
 SP601 EVALUATION PLATFORM Test P/N: TSS0121
 ART P/N: 1280464

Date:	10-20-2009_14:56	Ver:	C
Sheet Size:	B	Rev:	04
Sheet	12 of 16	Drawn By	BF



Power Supplies, 12V, 3.0V, 0.9V

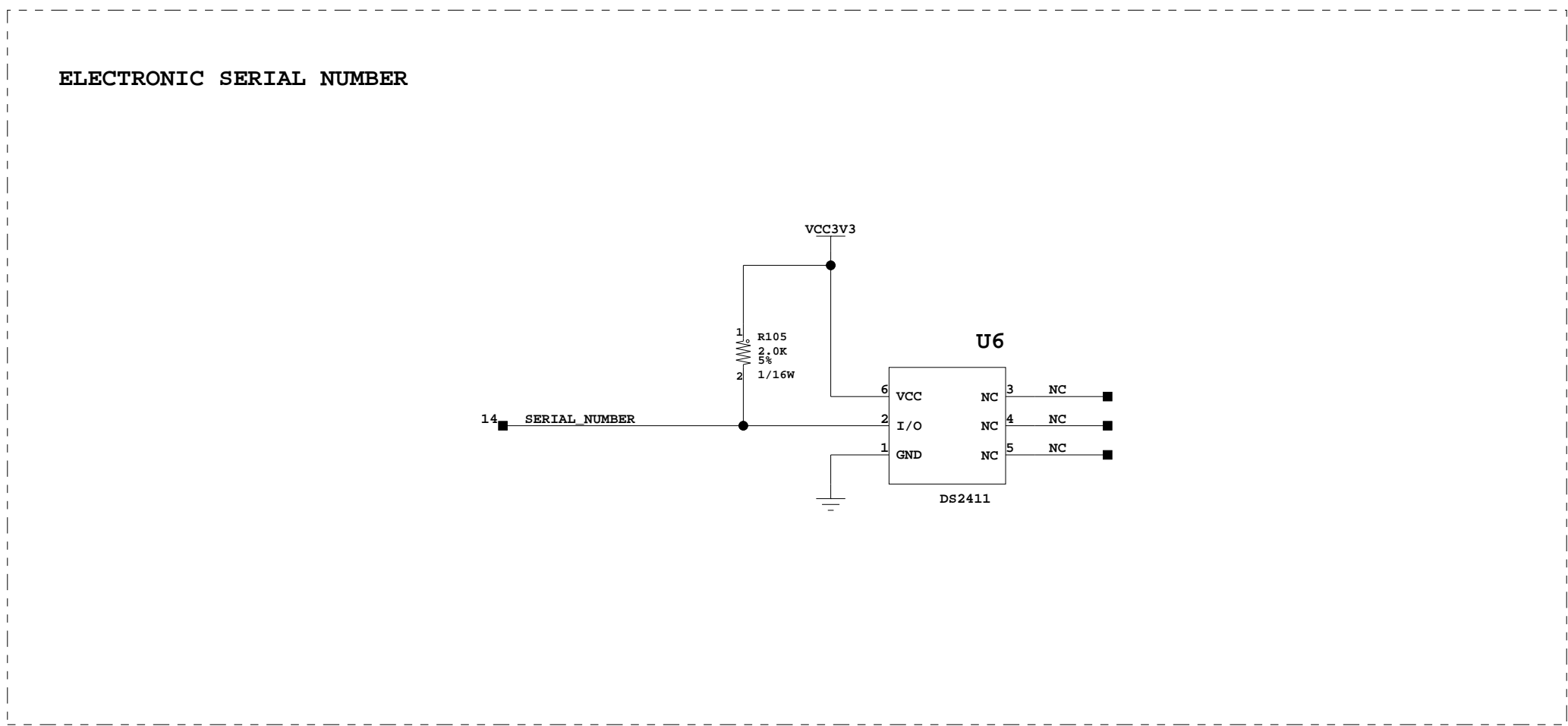
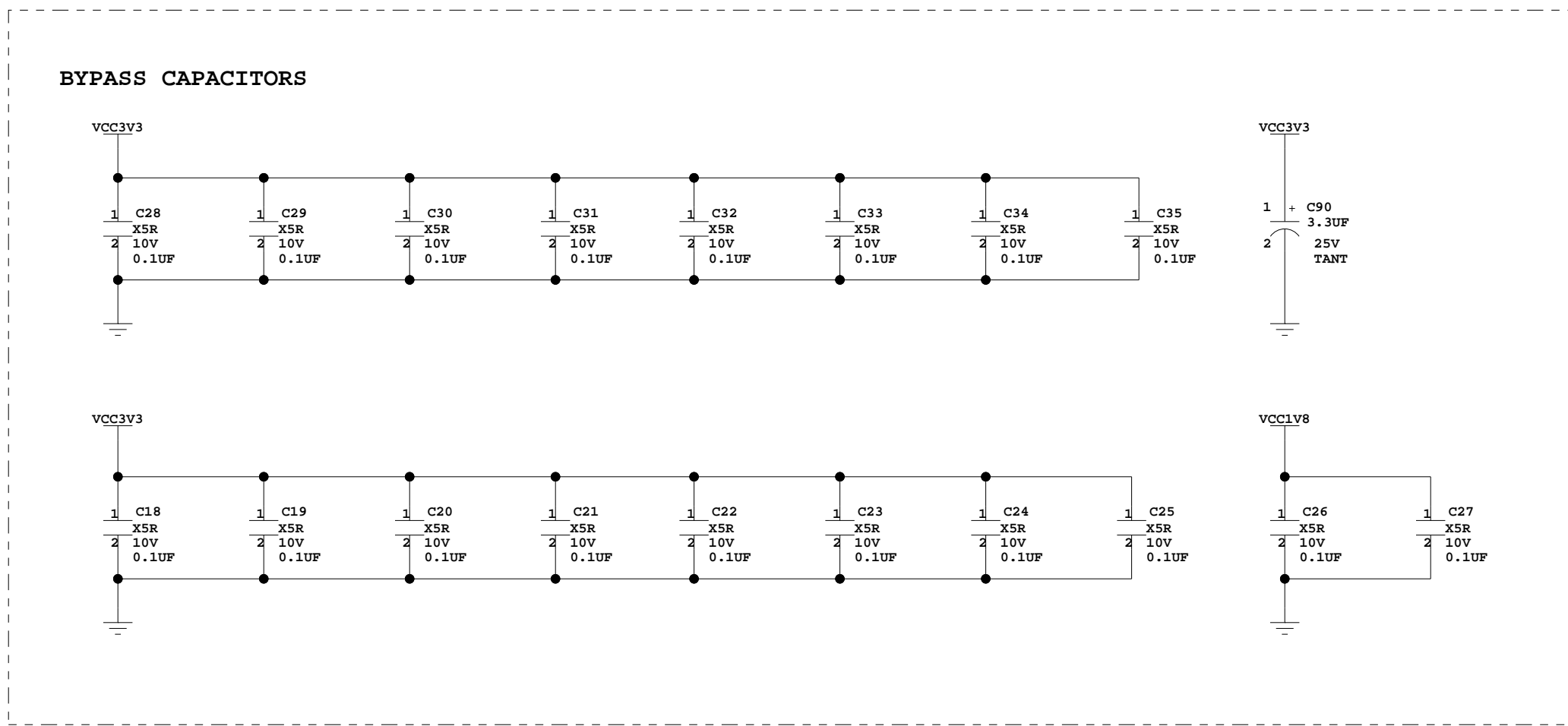
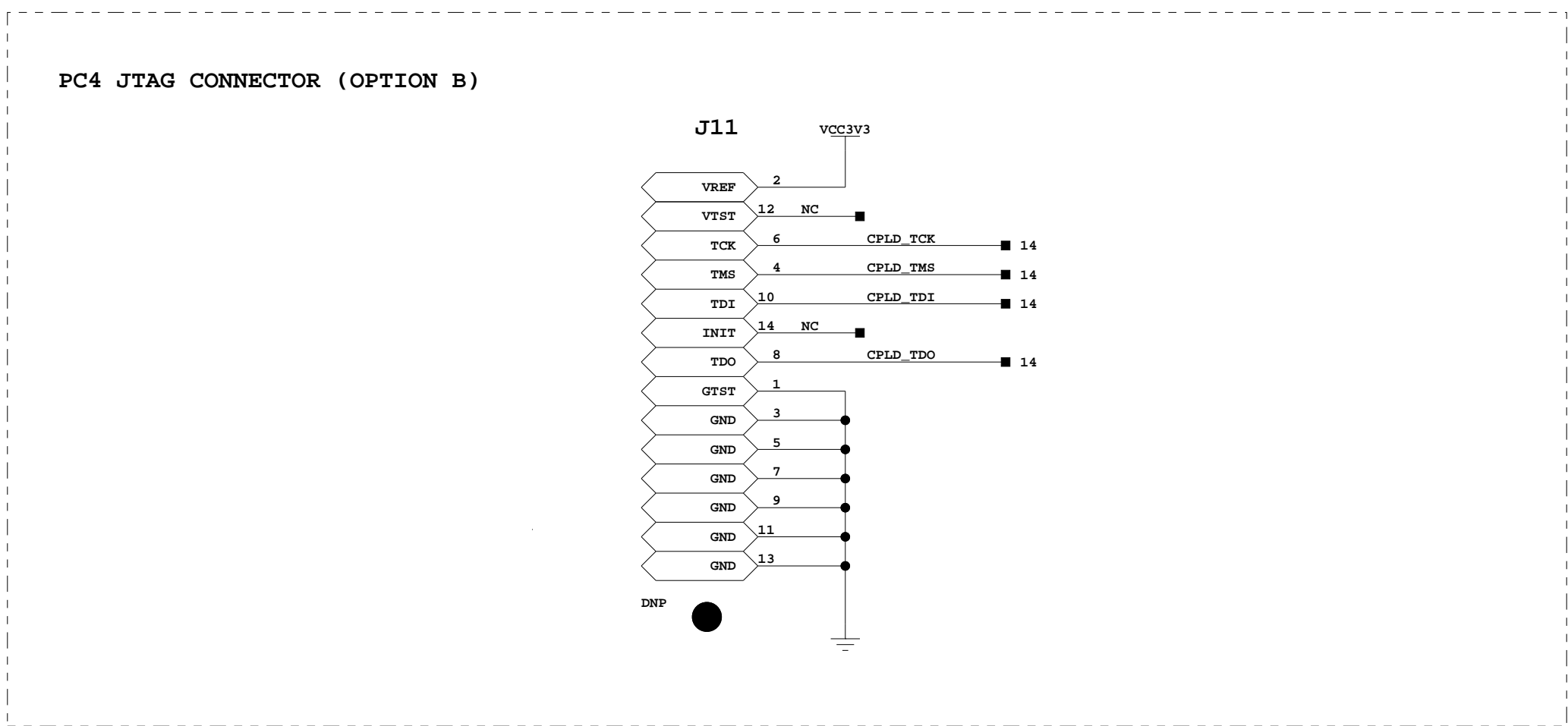
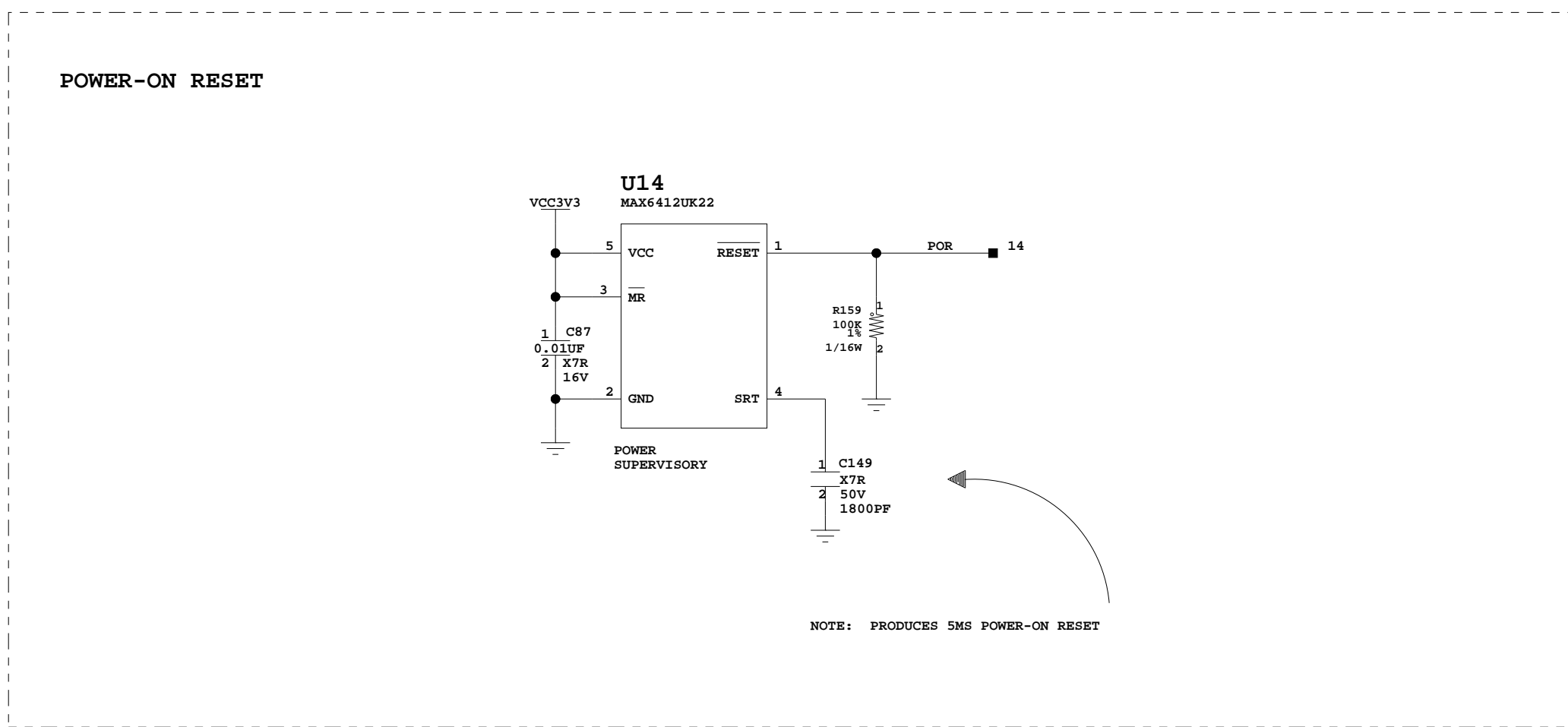
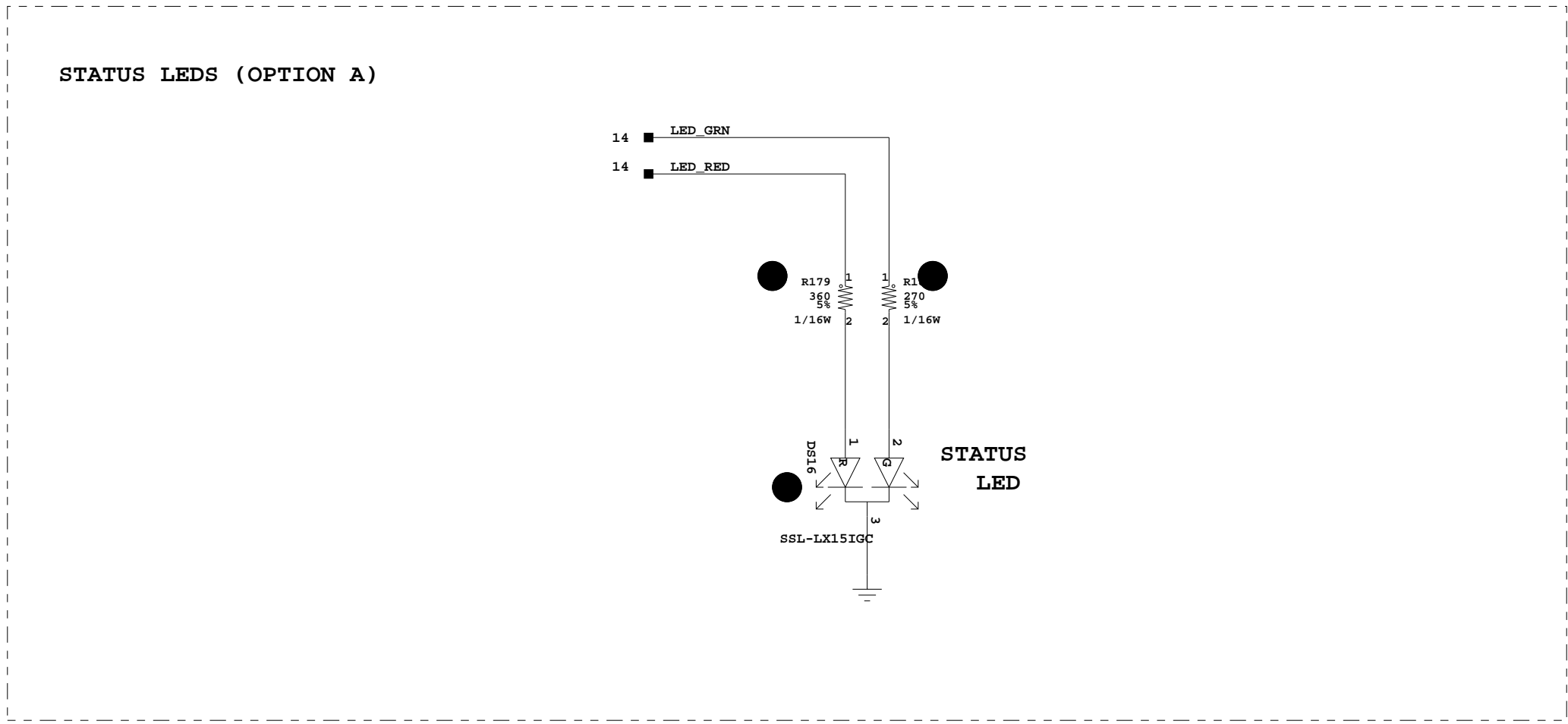
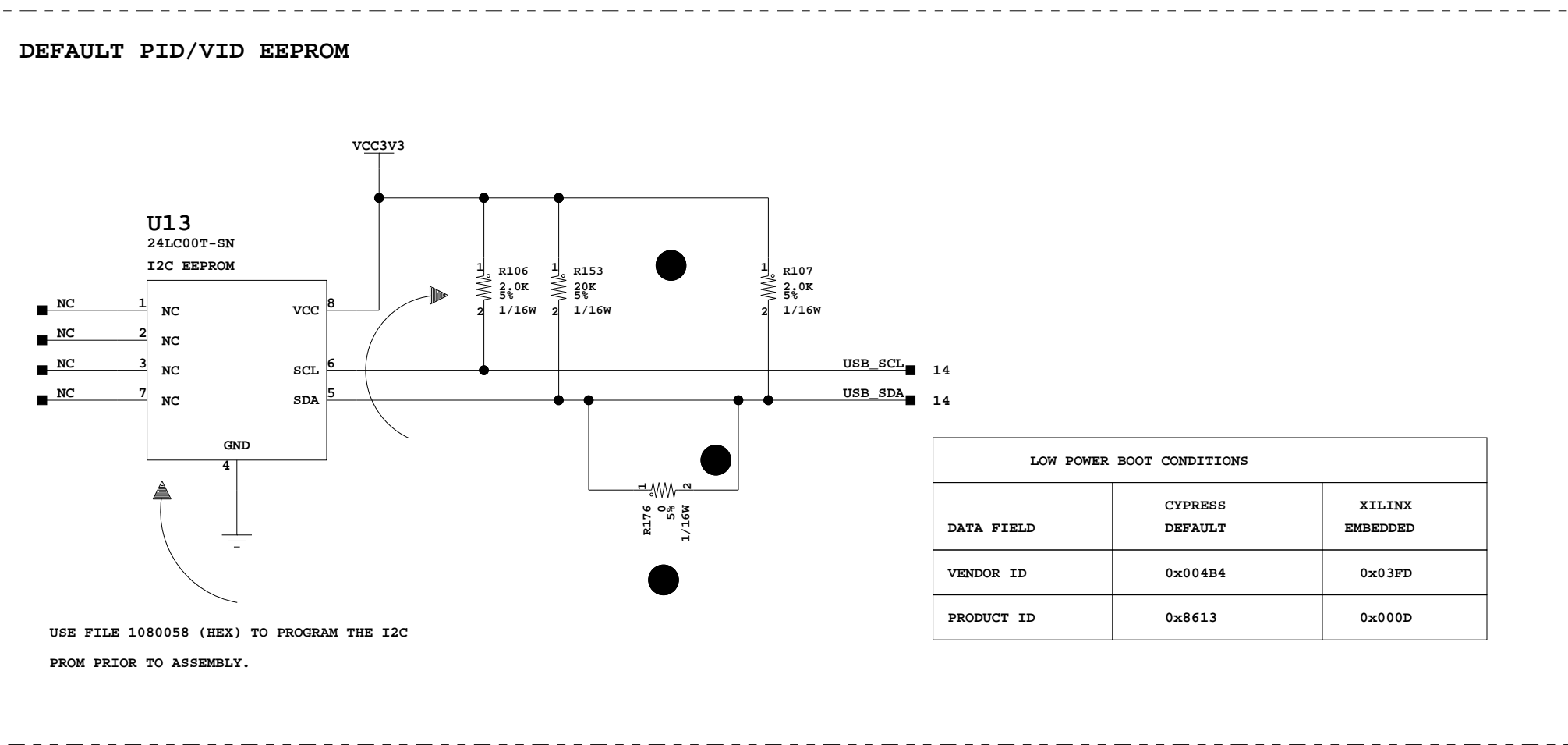


Title: Power Supplies, 12V, 3.0V, 0.9VPCB P/N: 0431512, 0431608
 SCHEM, ROHS COMPLIANT SCH P/N: 0381290
 SP601 EVALUATION PLATFORM Test P/N: TSS0121
 ART P/N: 1280464

Date:	10-20-2009_14:56	Ver:	C
Sheet Size:	B	Rev:	04
Sheet	13 of 16	Drawn By	BF

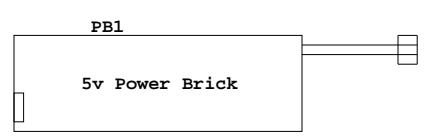
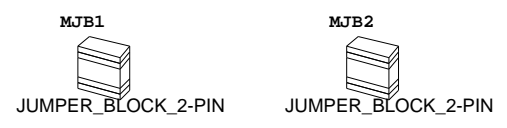
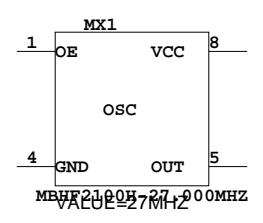
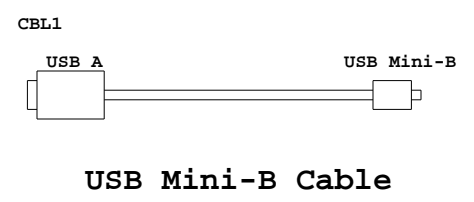
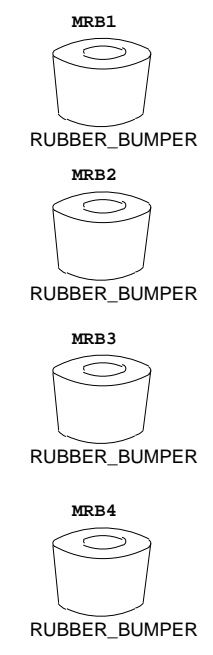
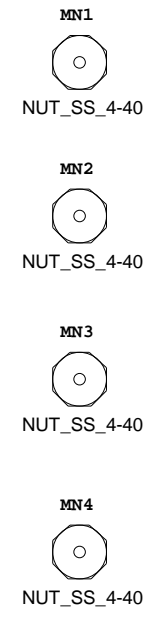
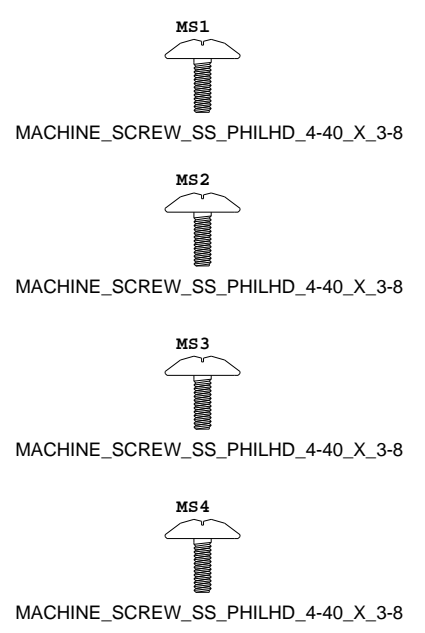
Connect SGND to PGND at a single point with multiple vias

The Embedded USB JTAG Download circuit on this page is for reference only!
 This circuit should not be designed into an end customer product or solution.
 Xilinx will not provide support on this embedded USB JTAG Download circuit.



Embedded USB JTAG: IIC, POR, Decoupling, LED, JTAG Header, Serial Number

Drawing Number:	0381242	PCB P/N:	0431512, 0431608
Date:	14-JUNE-2006	SCR P/N:	0381290
Sheet Size:	D	Part P/N:	1280121
Sheet	15 of 16	Rev:	04
		Drawn By:	SCHWEIGLER



Mechanical Components



Title: Mechanical Components SCHEM, ROHS COMPLIANT SP601 EVALUATION PLATFORM		PCB P/N: 0431512, 0431608 SCH P/N: 0381290 Test P/N: TSS0121 ART P/N: 1280464	
Date: 10-20-2009_14:56		Ver: C	
Sheet Size: B		Rev: 04	
Sheet 16 of 16		Drawn By BF	