

# **SP601 Standalone Applications**

**December 2009**

# Overview

- **Xilinx SP601 Board**
- **Software Requirements**
- **SP601 Setup**
- **Multi-pin Wake-up**
- **GPIO Header**
- **References**

**Note:** This presentation applies to the SP601

# SP601 Standalone Apps

## ▪ Description

- The standalone applications tutorial extends the board feature tests offered through the BIST. A derived EDK design with additional software is used to test features such as the GPIO header pins

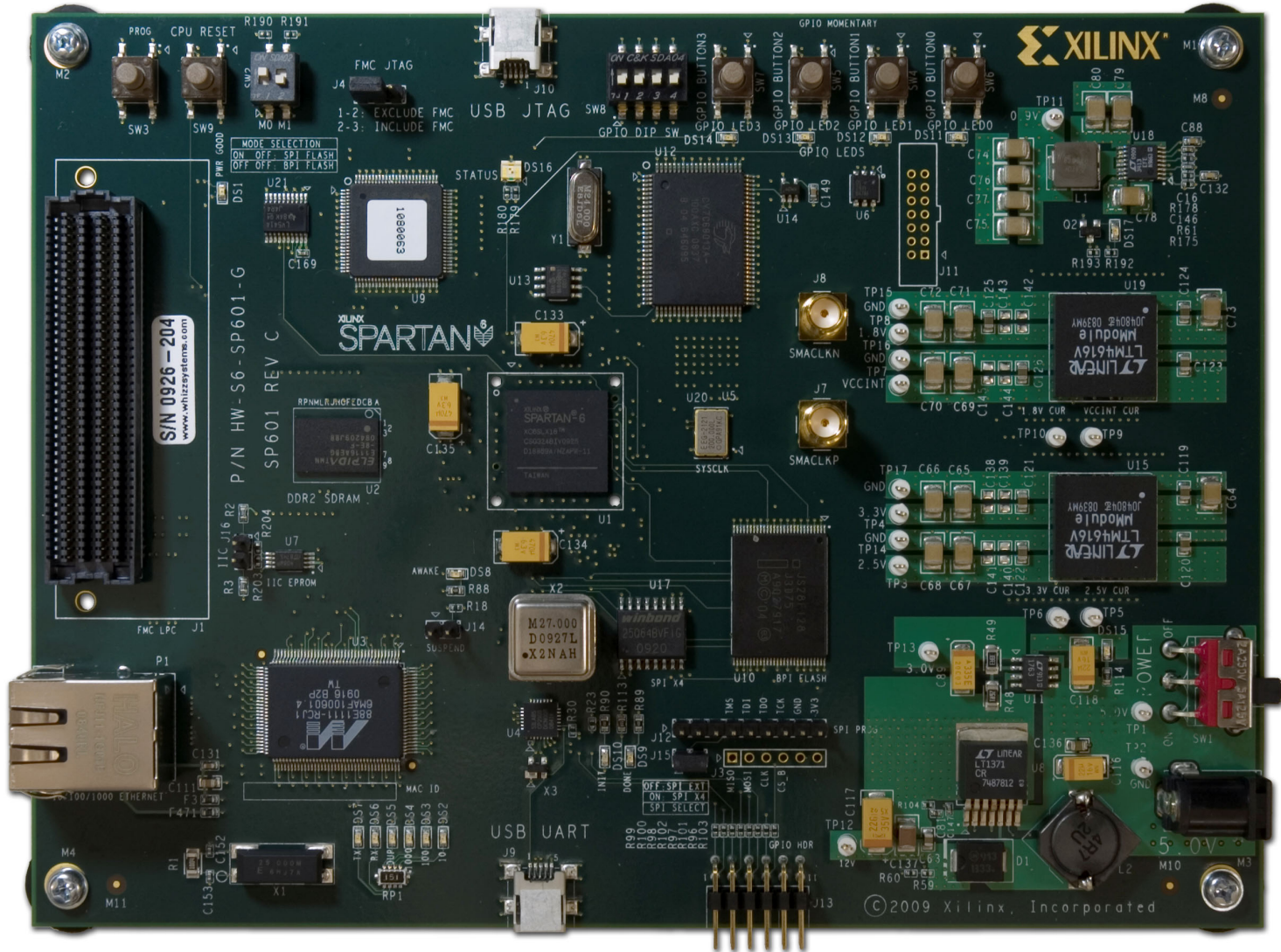
## ▪ Multi-pin Wake-up Design

- Simple counter design show the Multi-pin Wake-up functionality of the Spartan-6 FPGA Family

## ▪ GPIO Header Loopback Test

- EDK IP: MicroBlaze system derived from EDK BIST design
  - Embedded System Tools Reference Guide (UG111)
  - [http://www.xilinx.com/ise/embedded/edk\\_ip.htm](http://www.xilinx.com/ise/embedded/edk_ip.htm)

# Xilinx SP601 Board



# ISE Software Requirement

- **Xilinx ISE 11.4 software**

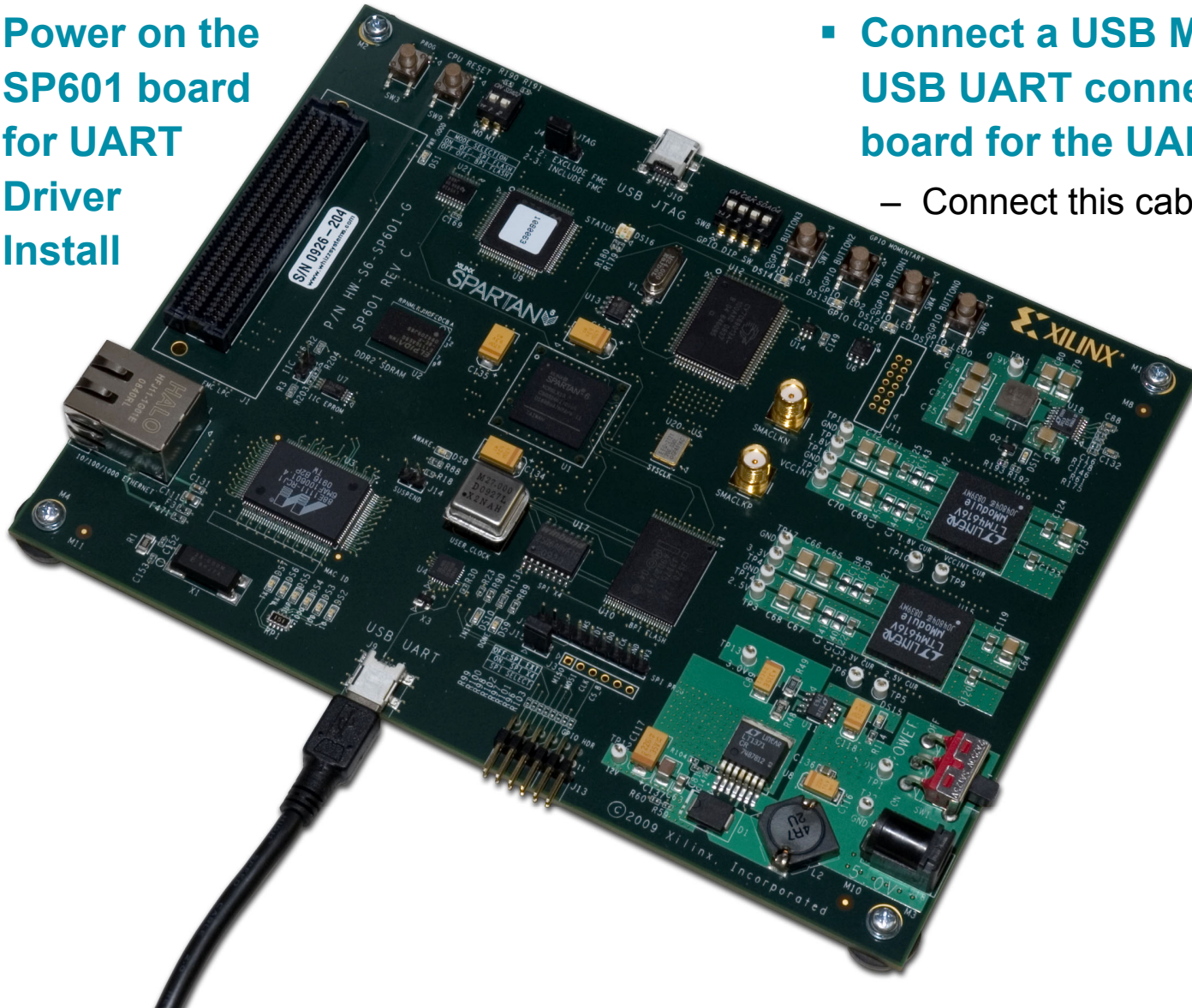
- Install the WebPACK for the Spartan-6 LX16 devices
- Run XilinxUpdate and download the WebPACK devices





# SP601 Setup

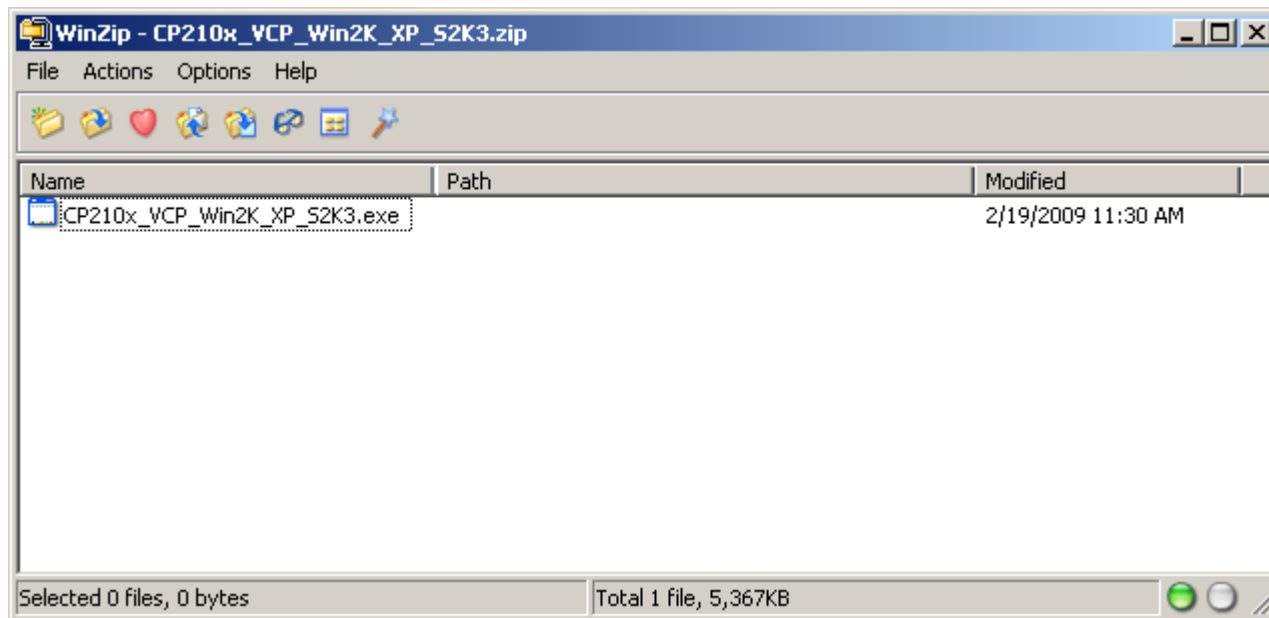
- Power on the SP601 board for UART Driver Install
- Connect a USB Mini-B Cable to the USB UART connector on the SP601 board for the UART Driver install
  - Connect this cable to your PC



# SP601 Setup

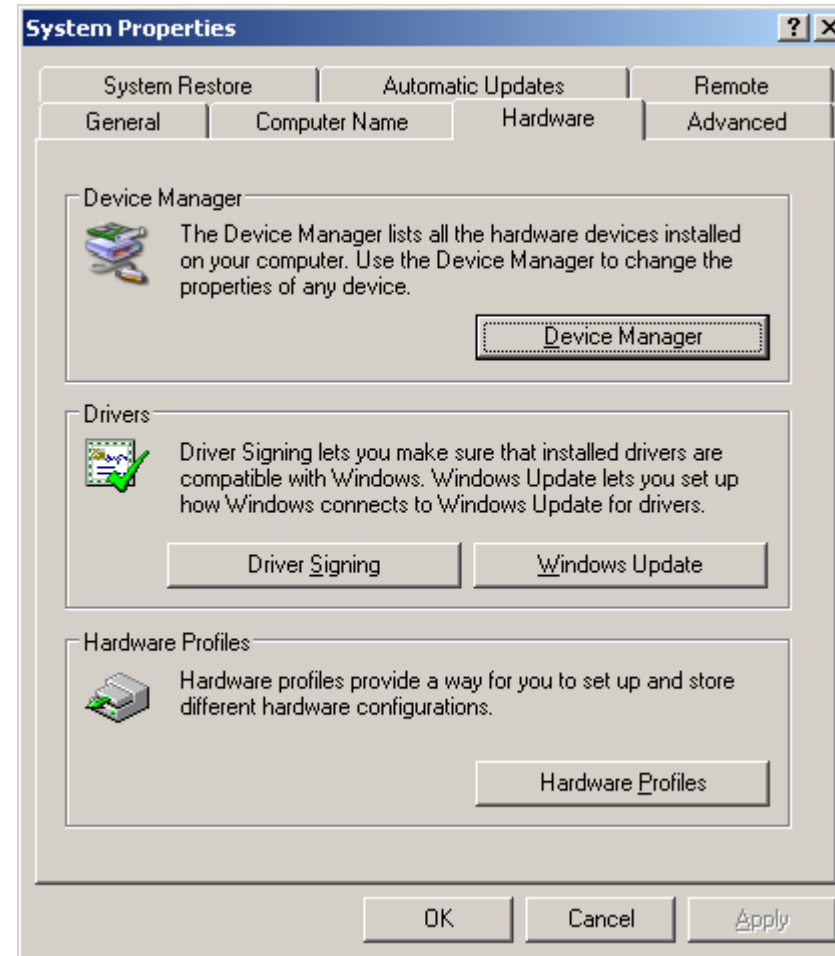
## ■ Install USB UART Drivers

- [https://www.silabs.com/Support Documents/Software/CP210x\\_VCP\\_Win2K\\_XP\\_S2K3.zip](https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip)



# SP601 Setup

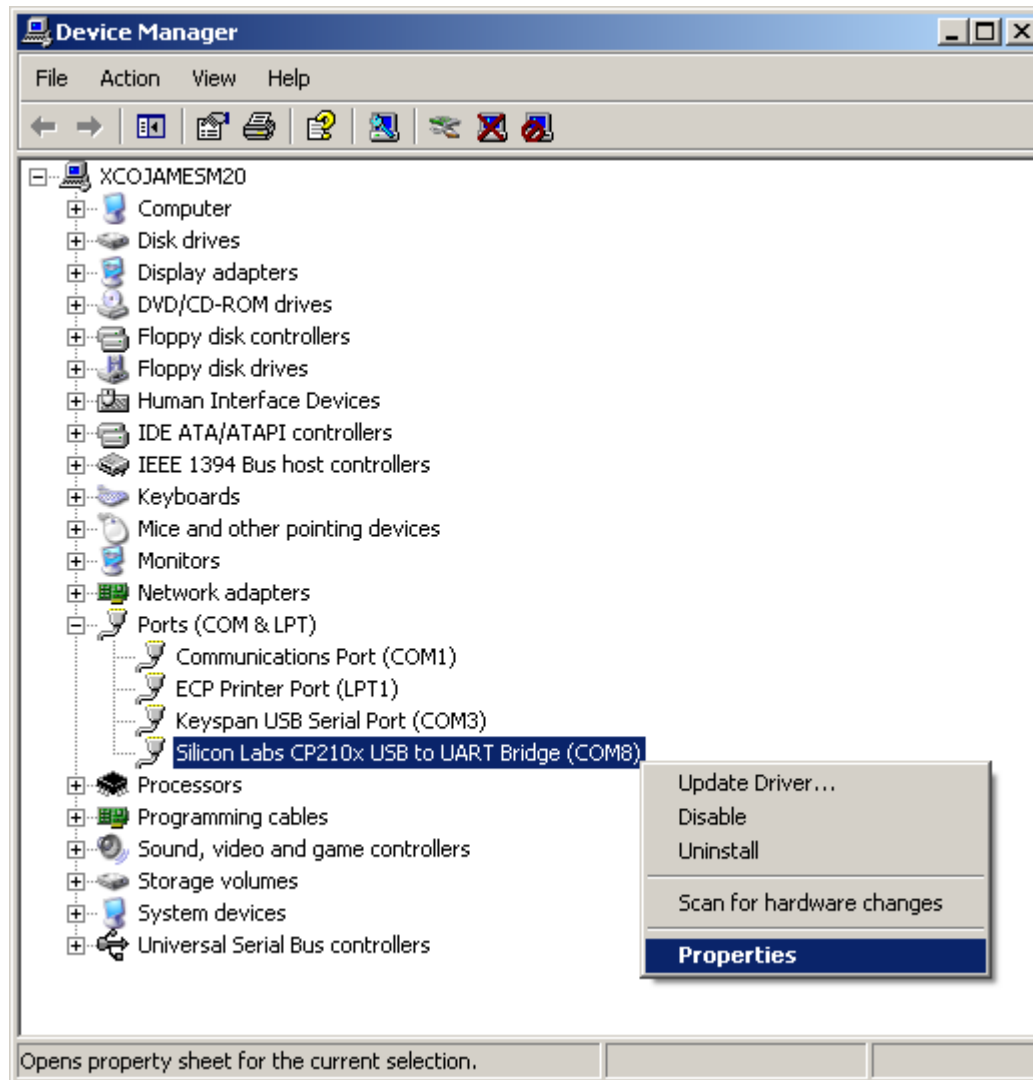
- **Right-click on My Computer and select Properties**
  - Select the Hardware tab
  - Click on Device Manager





# SP601 Setup

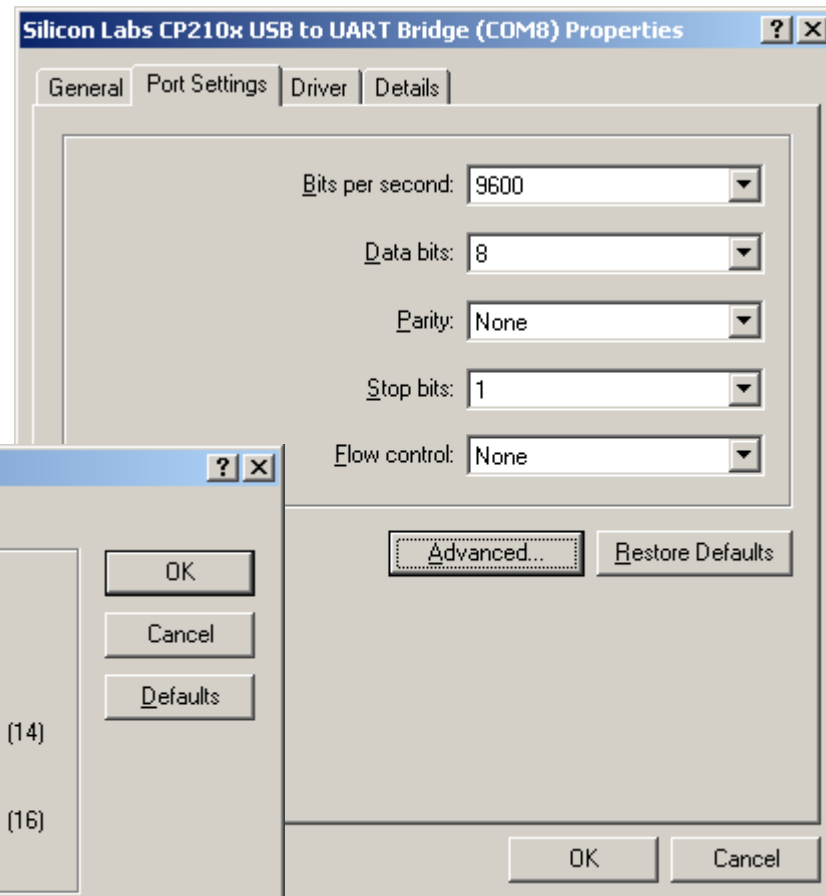
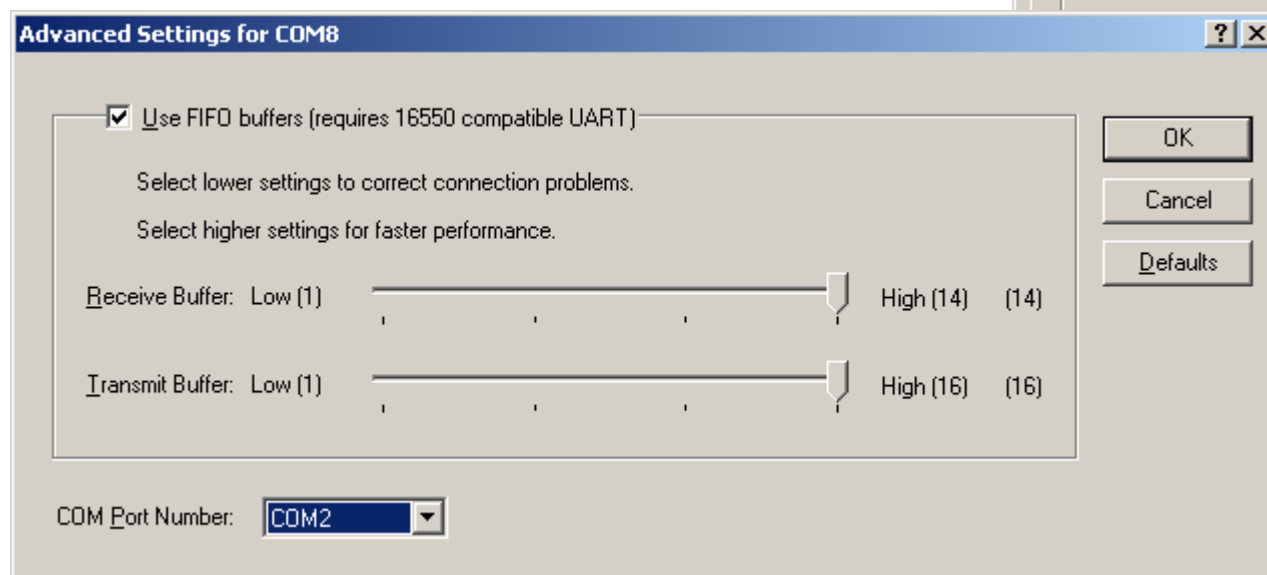
- **Expand the Ports Hardware**
  - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select **Properties**



# SP601 Setup

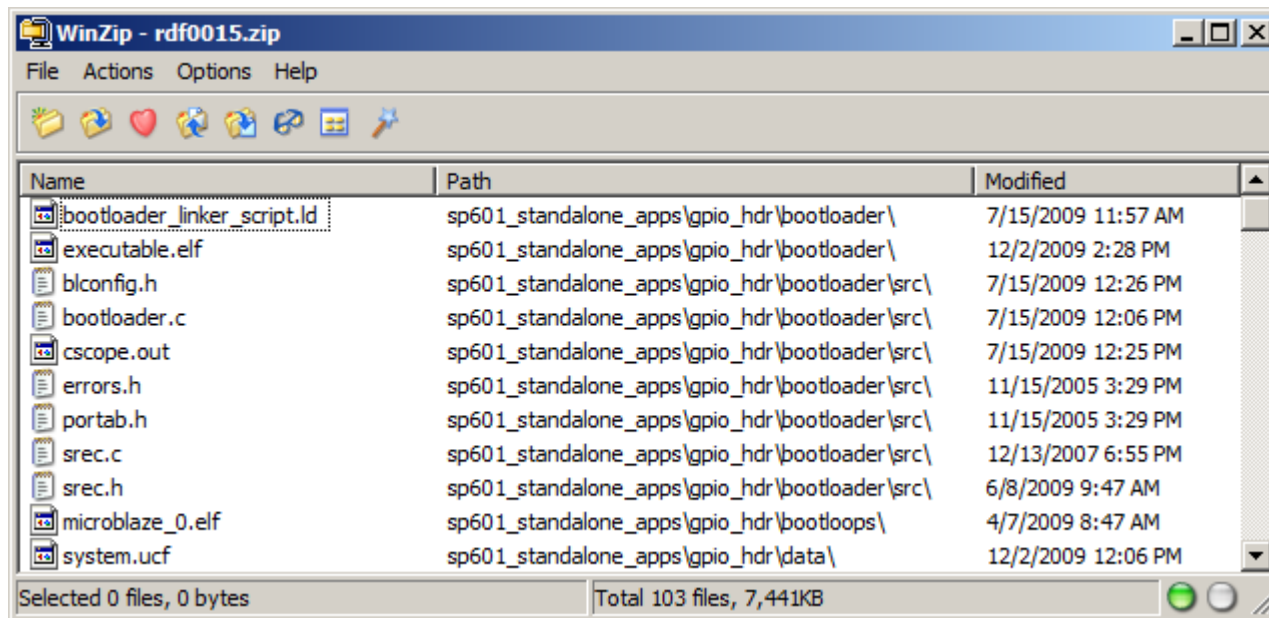
## ■ Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



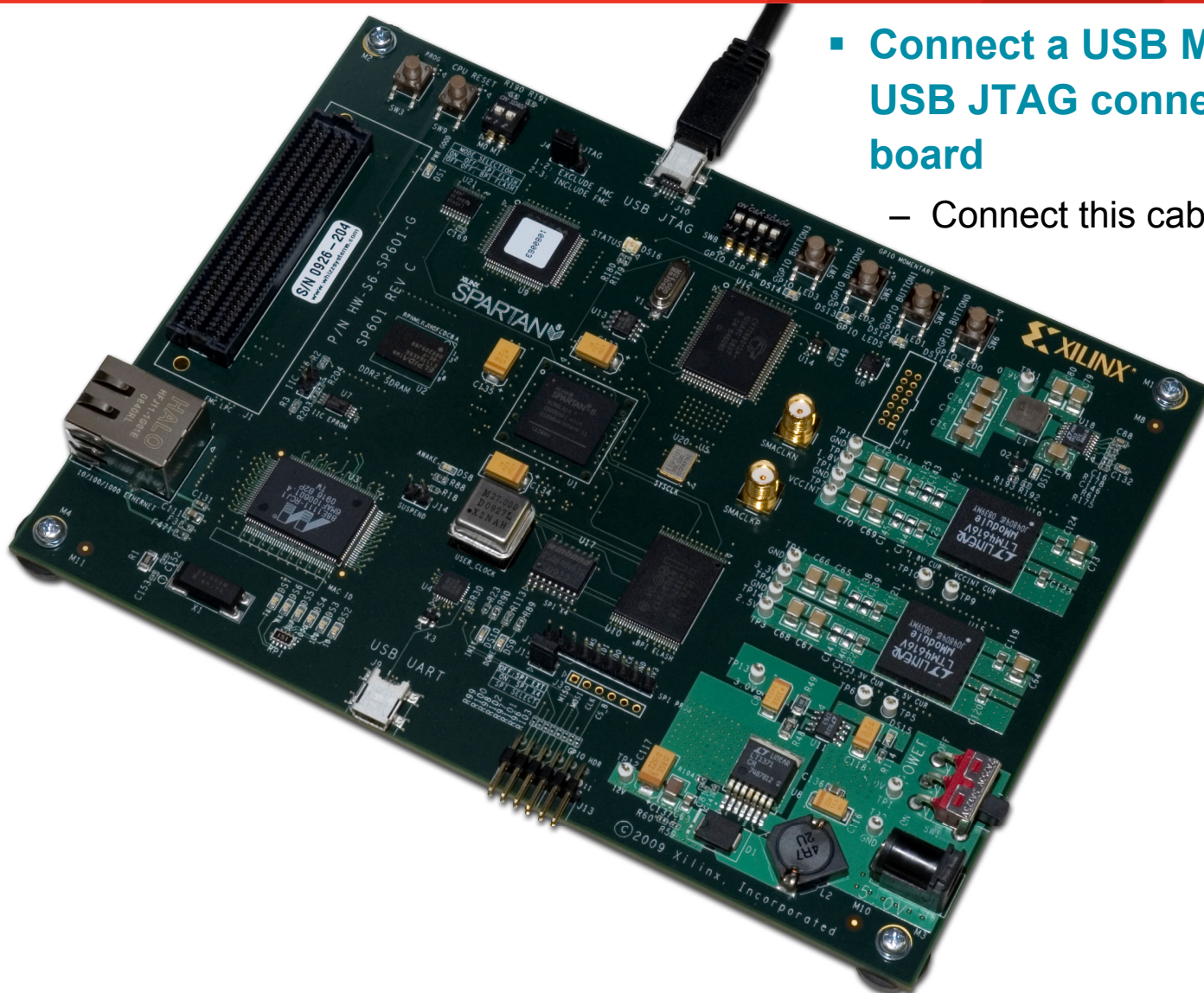
# SP601 Setup

- Unzip the rdf0015.zip file to your C:\ drive
  - <https://secure.xilinx.com/webreg/clickthrough.do?cid=139121>



# Multi-pin Wake-up

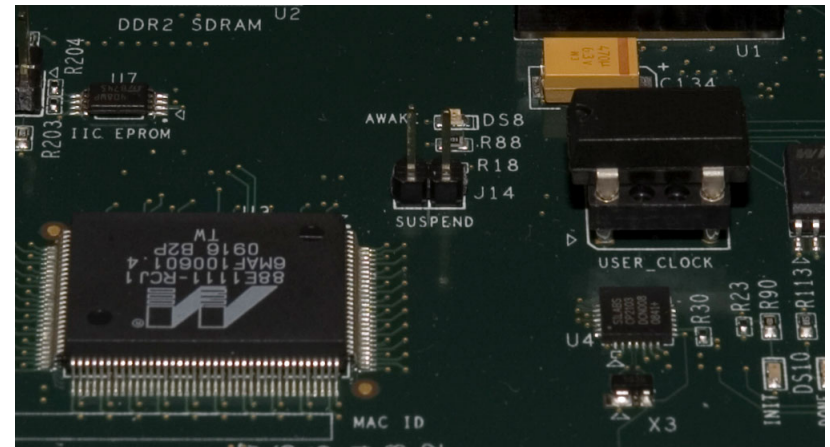
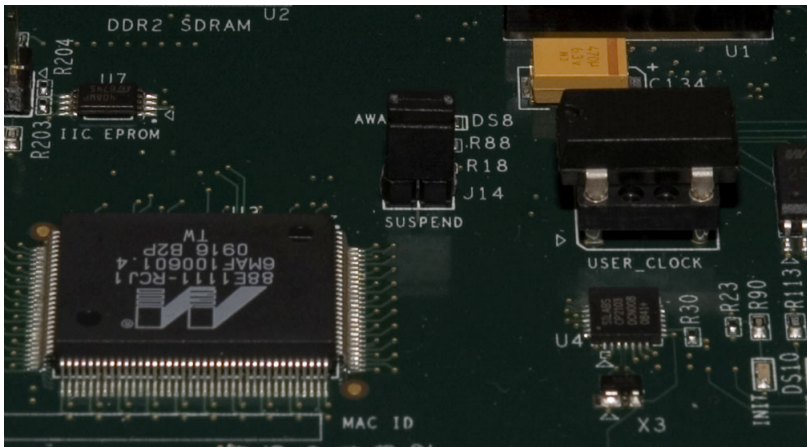
# Multi-pin Wake-up



- Connect a USB Mini-B Cable to the USB JTAG connector on the SP601 board
  - Connect this cable to your PC

# Multi-pin Wake-up

- **This test will involve removing the Suspend Jumper, seen below**
  - In this design, when an internal FPGA condition occurs and the suspend jumper is in place, suspend is initiated
  - The FPGA condition is when the two bit counter reaches “11”





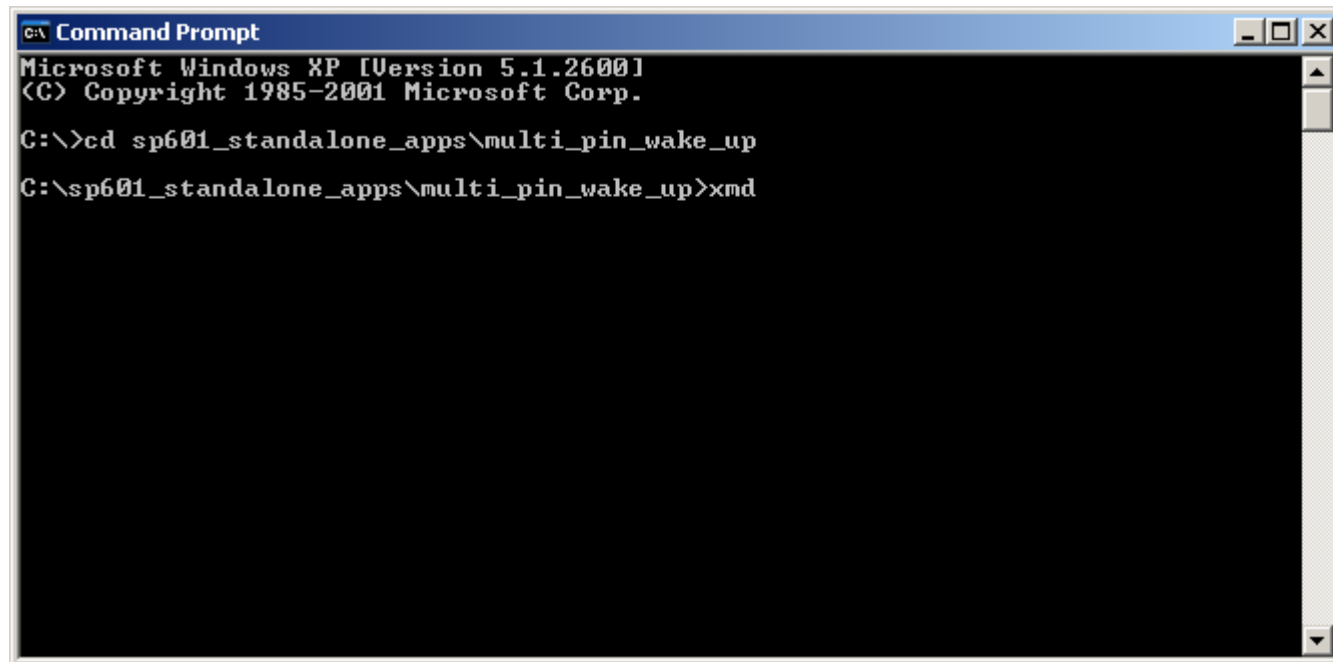
# Multi-pin Wake-up

- **Run xmd to download the Bitstream file**

- The xmd.ini file will enter the required download commands

**cd sp601\_standalone\_apps\multi\_pin\_wake\_up**

**xmd**



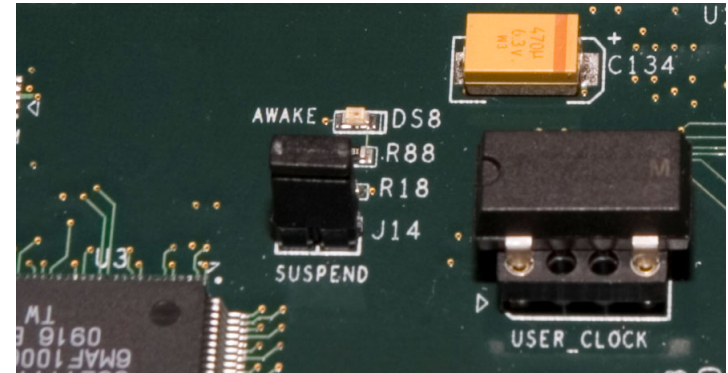
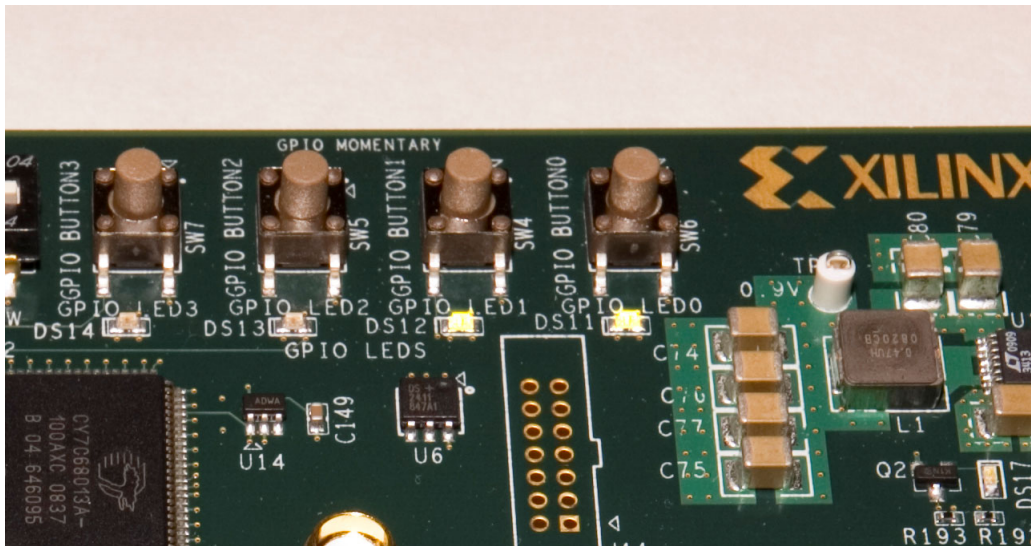
```
Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd sp601_standalone_apps\multi_pin_wake_up
C:\sp601_standalone_apps\multi_pin_wake_up>xmd
```

**Note:** Suspend jumper can be on or off during programming

# Multi-pin Wake-up

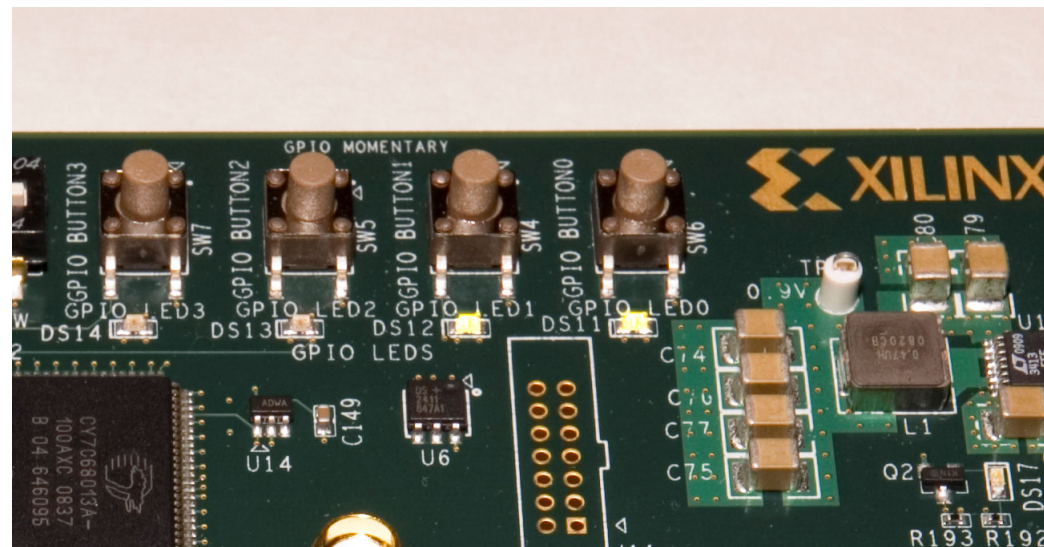
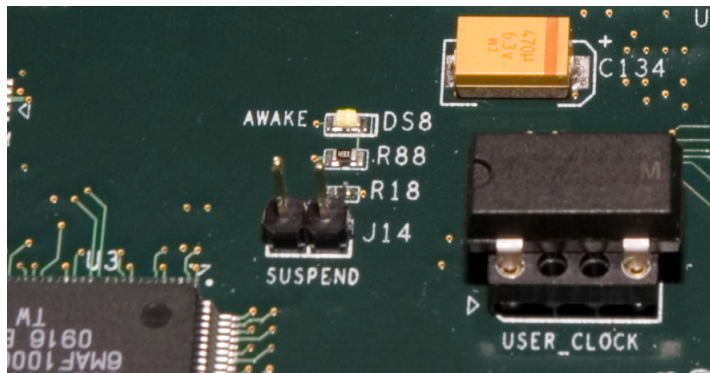
- Install a jumper on J14
- The Counter LEDs continues to “11” and then stops counting (DS11 & 12)
- The Awake LED goes out



**Note:** Presentation applies to the SP601

# Multi-pin Wake-up

- Remove the jumper on J14
- The Awake LED comes on
- The Counter LEDs resume counting at “11”



**Note:** Presentation applies to the SP601

# GPIO Header Loopback Test

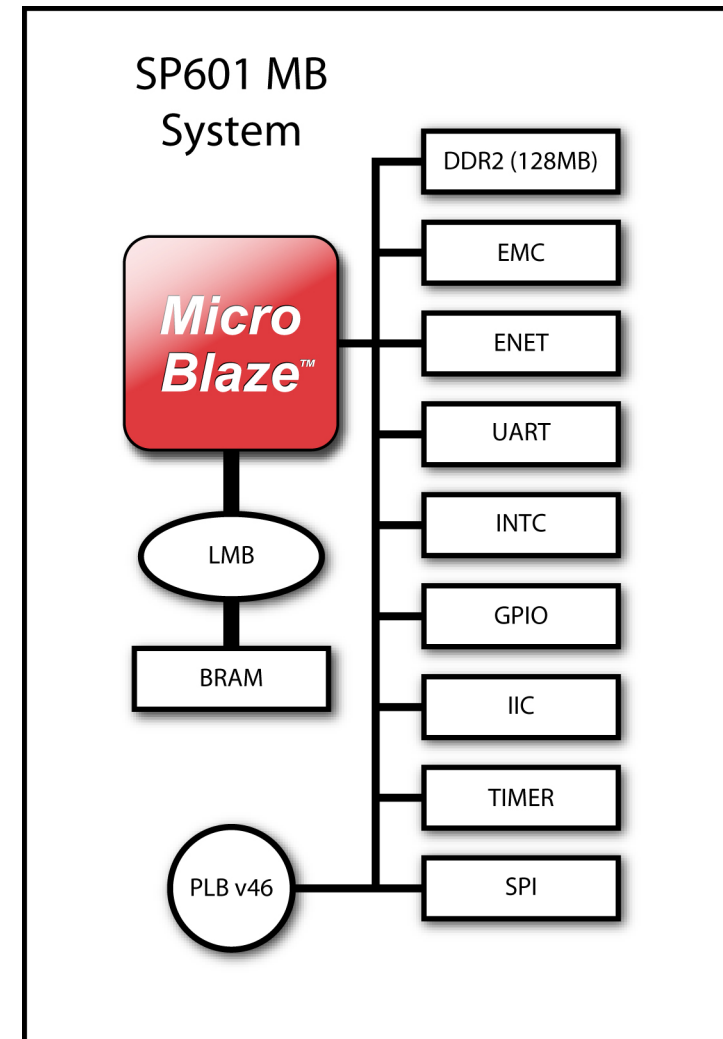
# Embedded Processor Design

- **The provided embedded reference design is supported “as is”**
  - Please refer to the click through license agreement
- **Embedded reference design has been verified on the SP601 Evaluation Kit**
  - Design consists of Early Access IP
  - Design may change in subsequent releases
- **The reference design will allow users to:**
  - Re-build and verify functionality on the SP601 evaluation kit

# SP601 MicroBlaze Hardware

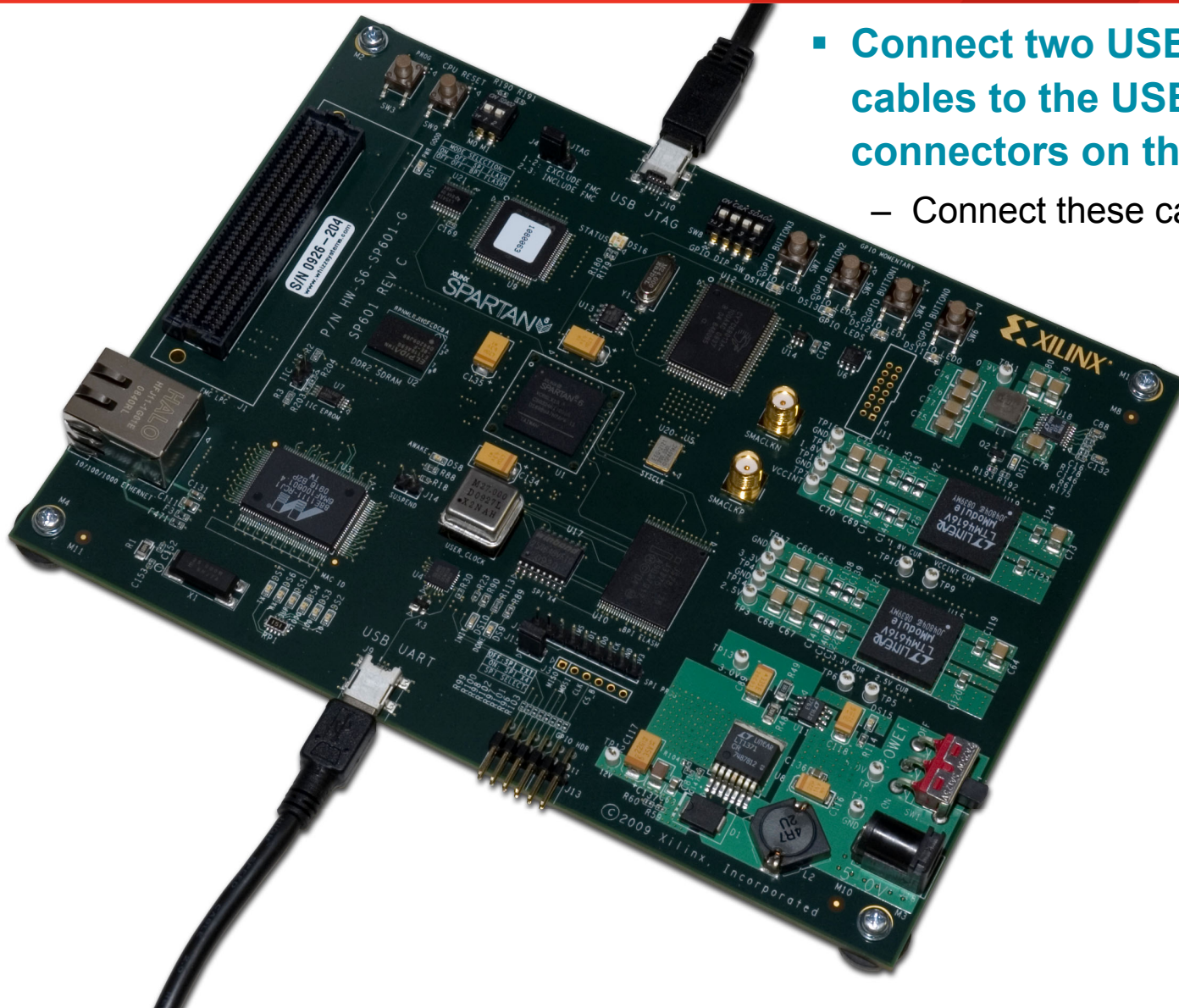
## ▪ The SP601 MicroBlaze Design Hardware includes:

- DDR2 Interface (128 MB)
- BRAM
- External Memory Controller (EMC)
  - Flash Memory
- Networking
- UART
- Interrupt Controller
- GPIO (HDR Pins, IIC, LEDs)
- PLB Arbiter
- SPI





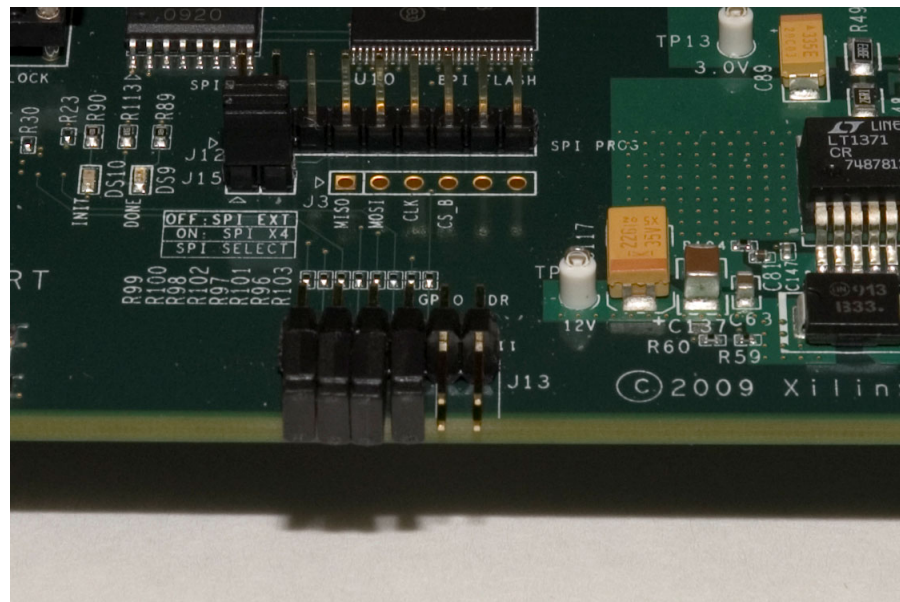
# GPIO Header Loopback Test



- Connect two USB Type-A to Mini-B cables to the USB JTAG and UART connectors on the SP601 board
  - Connect these cables to your PC

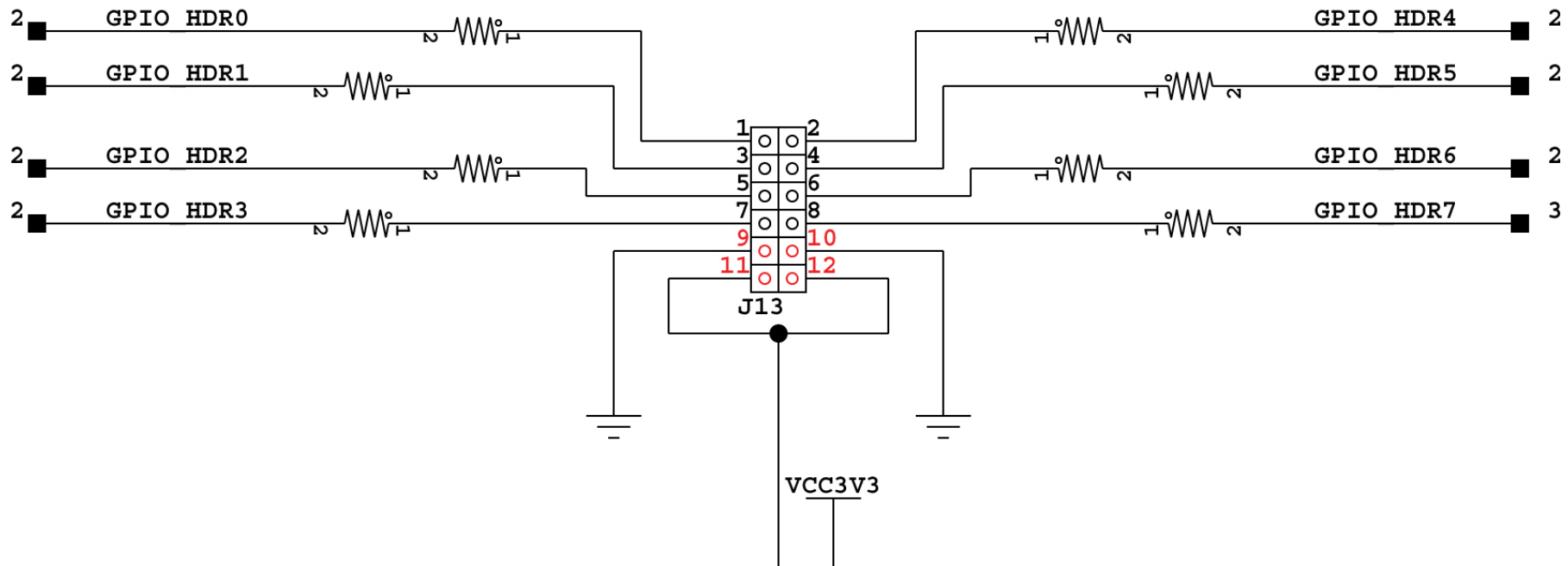
# GPIO Header Loopback Test

- Connect jumpers across J13 as shown here



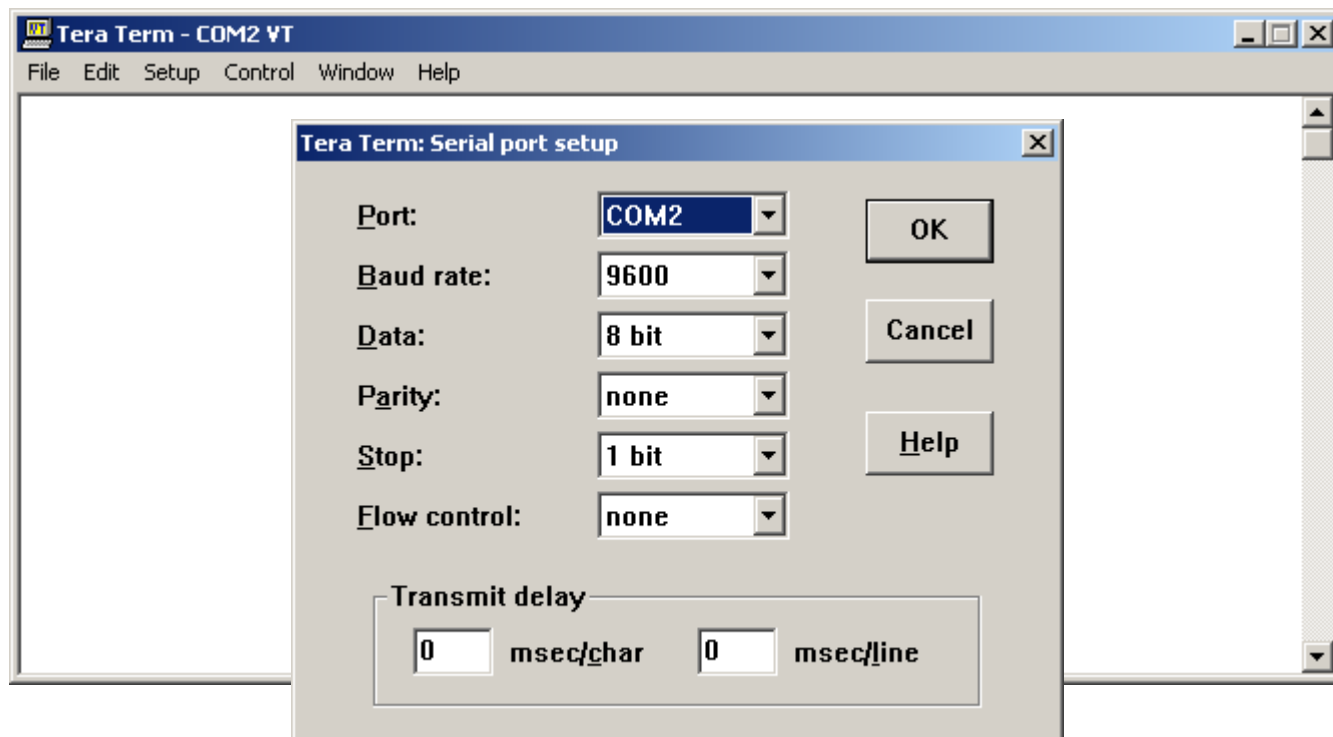
# GPIO Header Loopback Test

- Do not connect any jumpers across pins 9, 10, 11, or 12
  - These pins are connected to power and ground



# GPIO Header Loopback Test

- **Board Power must be on before starting Tera Term**
- **Start the Terminal Program**
  - Select your USB Com Port
  - Set the baud to 9600



**Note:** Tera Term may need to be restarted if board power is cycled

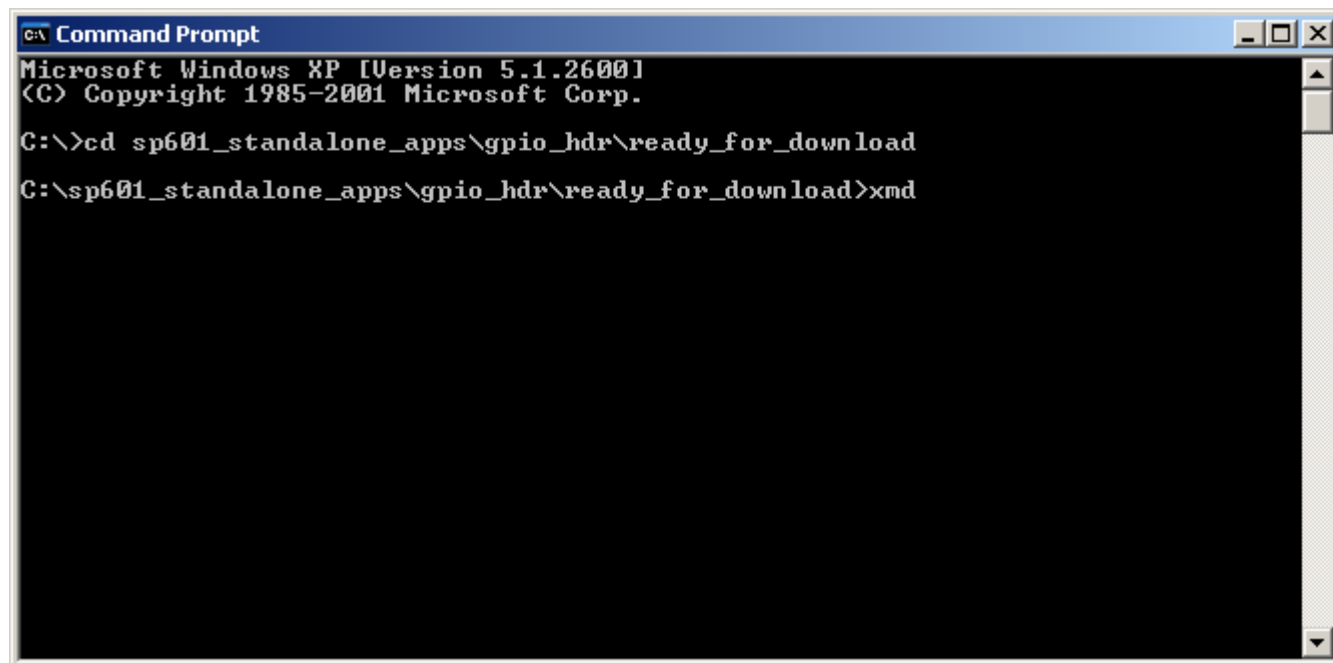
# GPIO Header Loopback Test

- **Run xmd to download the Bitstream and ELF file**

- The xmd.ini file will enter the required download commands

- cd sp601\_standalone\_apps\gpio\_hdr\ready\_for\_download**

- xmd**

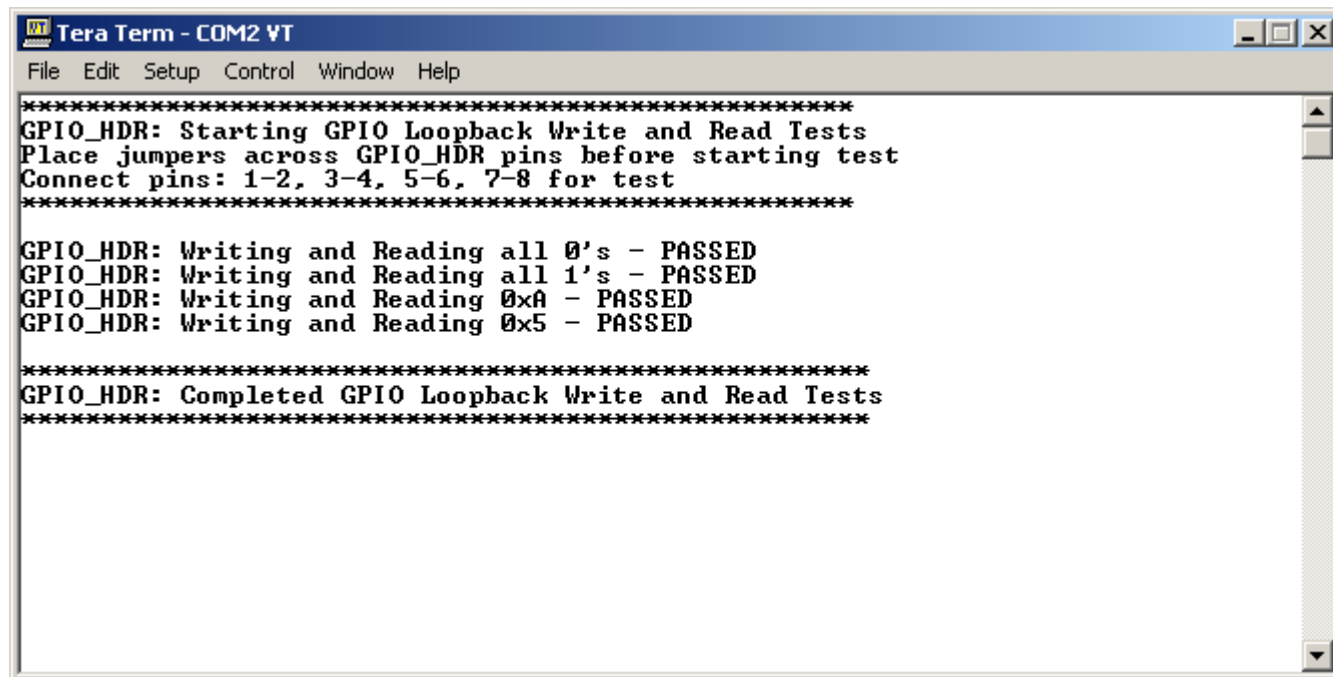


```
Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>cd sp601_standalone_apps\gpio_hdr\ready_for_download
C:\sp601_standalone_apps\gpio_hdr\ready_for_download>xmd
```

# GPIO Header Loopback Test

- The test results will appear in the terminal window



The screenshot shows a Tera Term terminal window titled "Tera Term - COM2 VT". The window has a menu bar with "File", "Edit", "Setup", "Control", "Window", and "Help". The terminal text is as follows:

```
*****
GPIO_HDR: Starting GPIO Loopback Write and Read Tests
Place jumpers across GPIO_HDR pins before starting test
Connect pins: 1-2, 3-4, 5-6, 7-8 for test
*****

GPIO_HDR: Writing and Reading all 0's - PASSED
GPIO_HDR: Writing and Reading all 1's - PASSED
GPIO_HDR: Writing and Reading 0xA - PASSED
GPIO_HDR: Writing and Reading 0x5 - PASSED

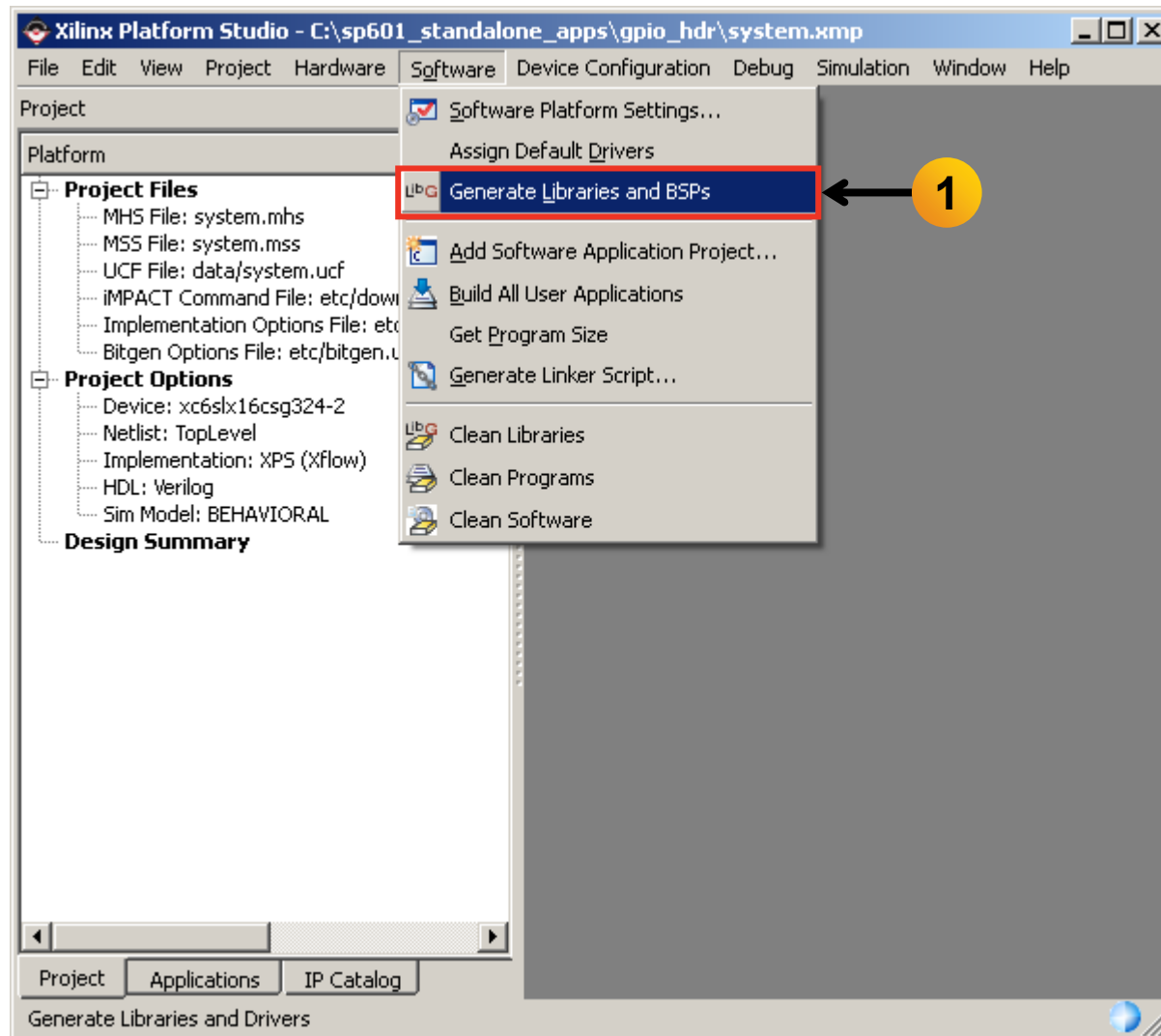
*****
GPIO_HDR: Completed GPIO Loopback Write and Read Tests
*****
```



# Compile SP601 GPIO Header Loopback Design

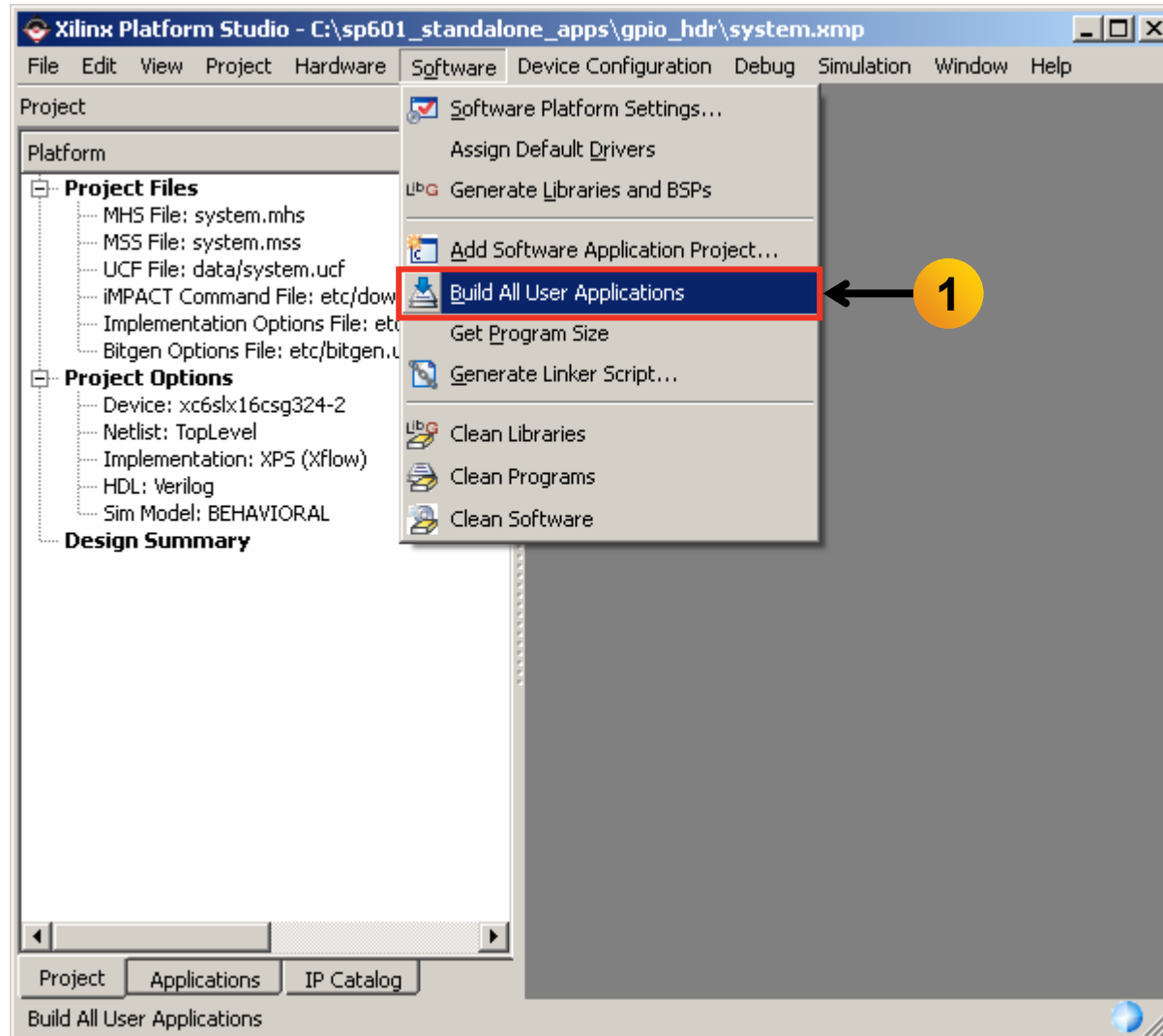
# Compile SP601 GPIO Header Loopback Design

- The GPIO Header Design can be compiled with EDK
- Open XPS project <design path>\gpio\_hdr\system.xmp
- Generate the libraries needed to create the bitstream
  - Select **Software** → **Generate Libraries and BSPs** (1)



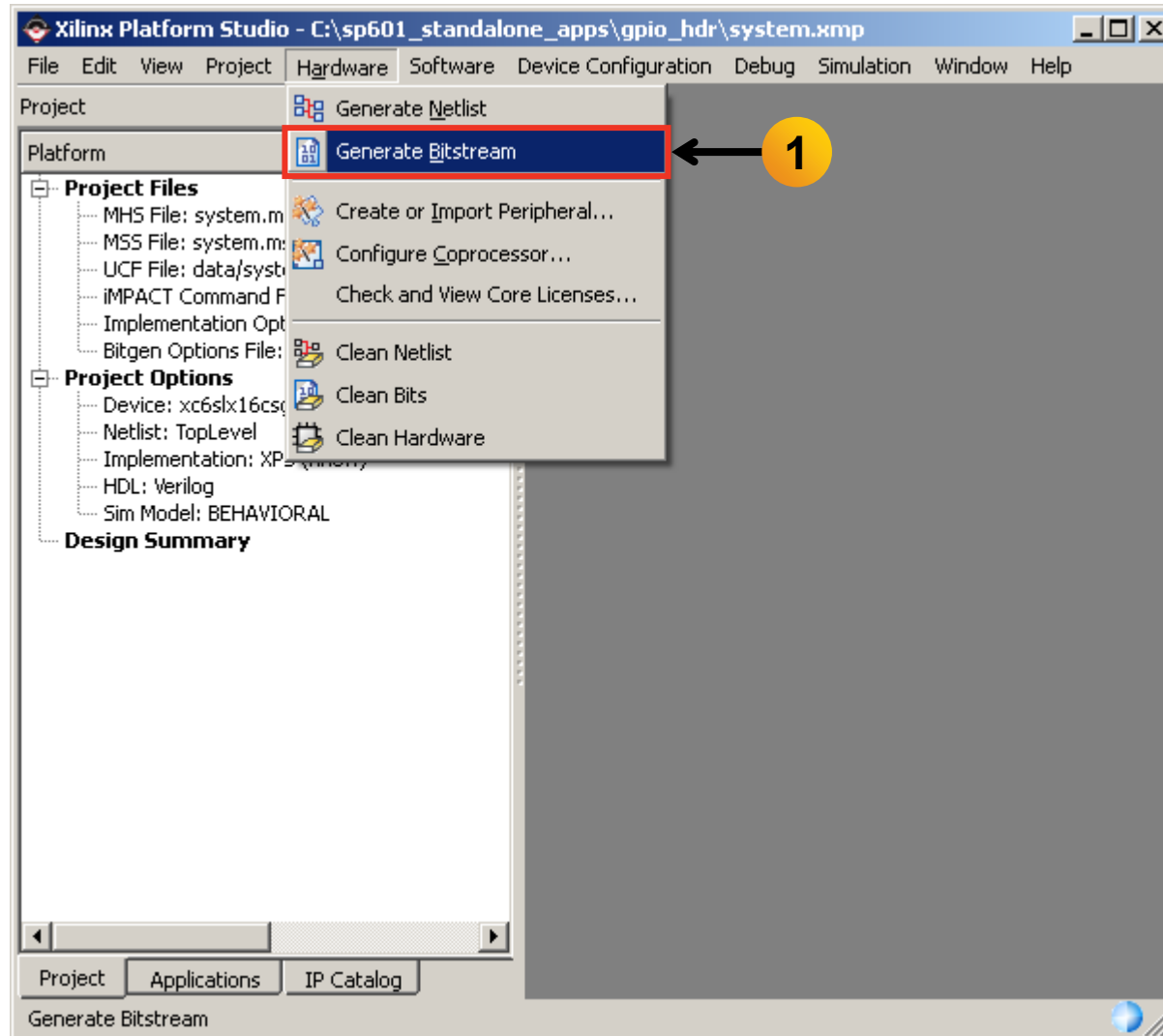
# Compile SP601 GPIO Header Loopback Design

- **Compile the Software Applications and create the application ELF files**
  - Select **Software** → **Build All User Applications** (1)



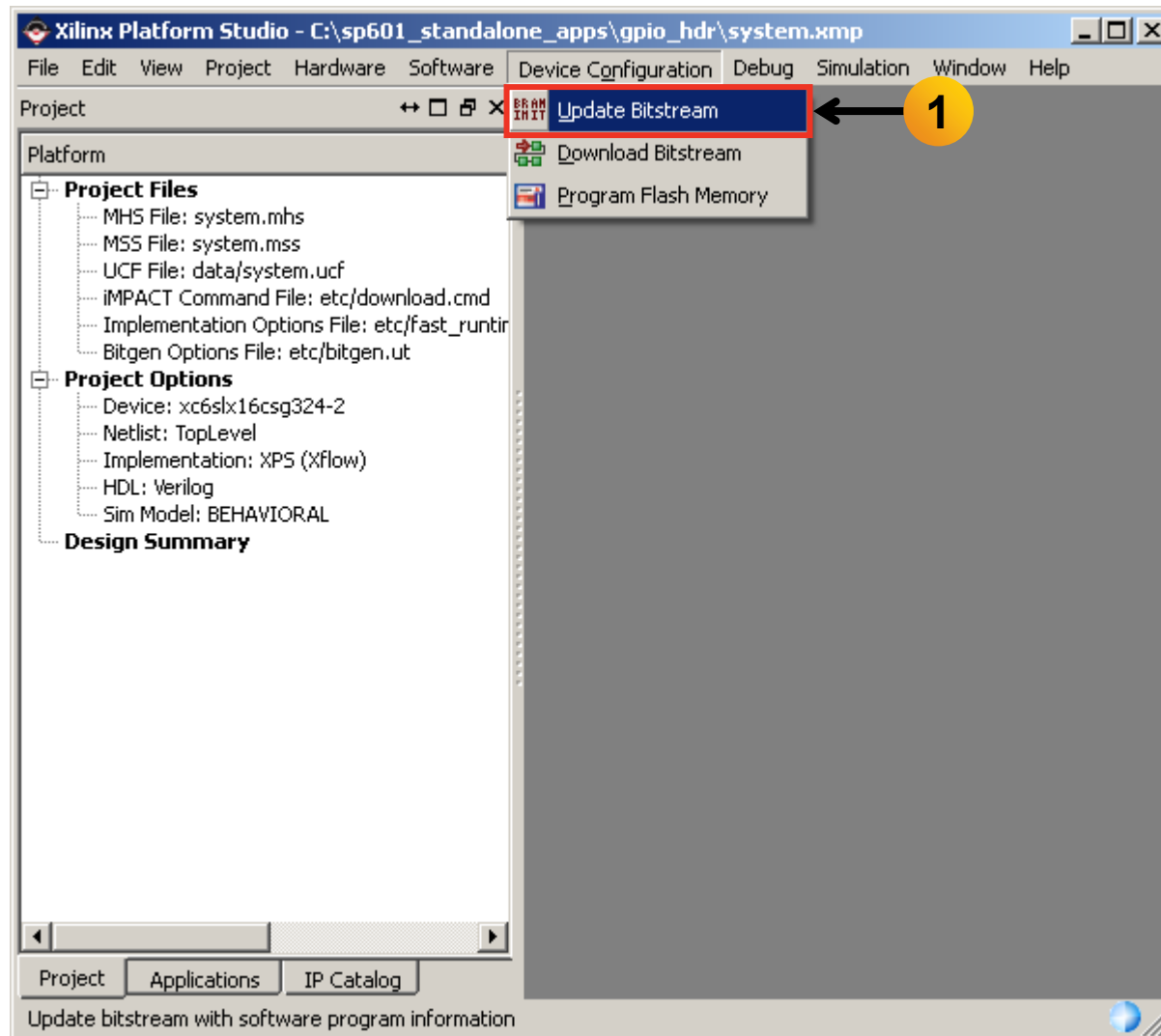
# Compile SP601 GPIO Header Loopback Design

- Create the hardware design, system.bit, located in <project directory>/implementation
  - Select Hardware → **Generate Bitstream** (1)



# Compile SP601 GPIO Header Loopback Design

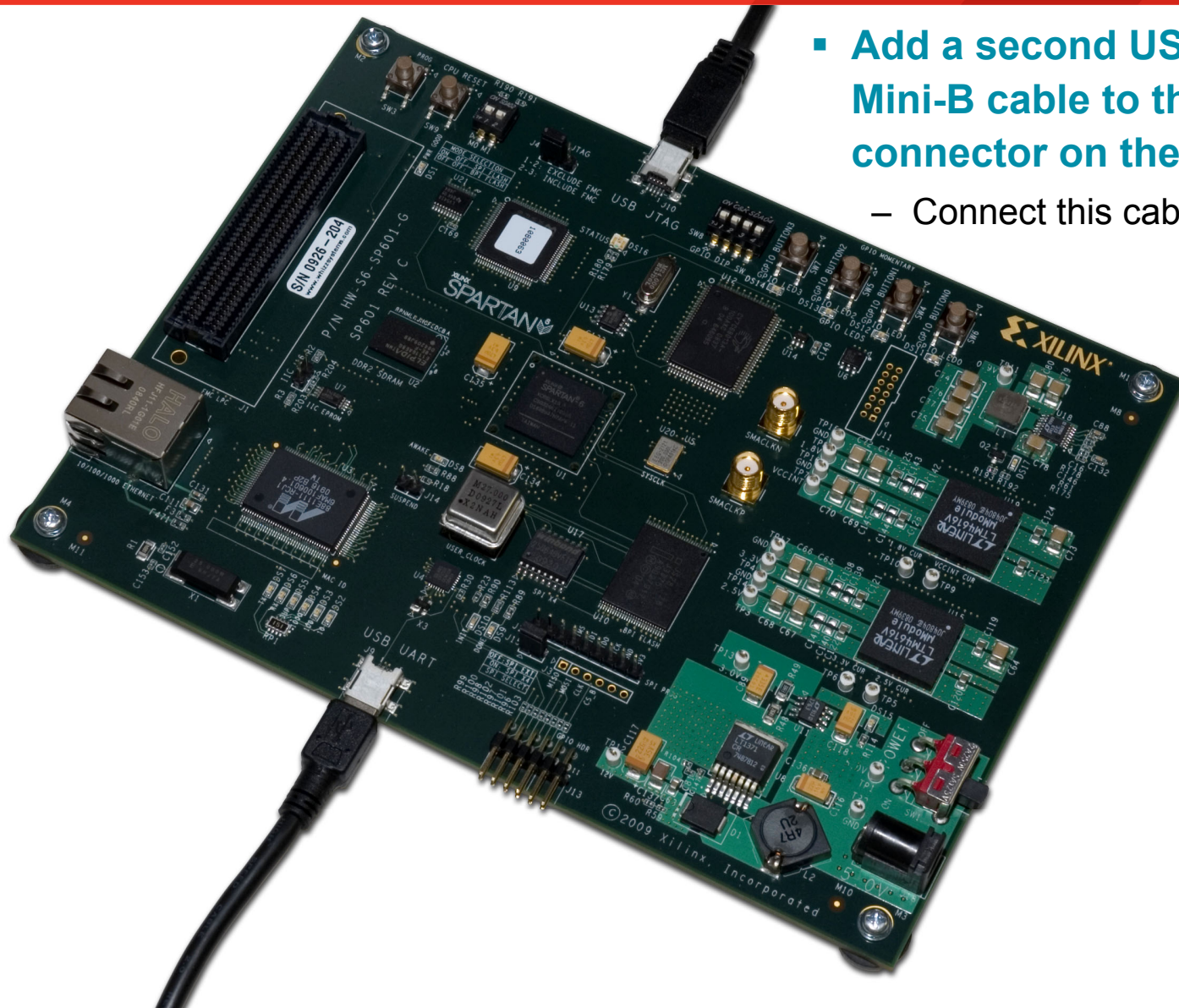
- **Init memory with the Bootloader Application ELF**
  - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
  - Select **Device Configuration** → **Update Bitstream** (1)



**Download SP601 GPIO Header Loopback Design**



# Download SP601 GPIO Header Loopback Design

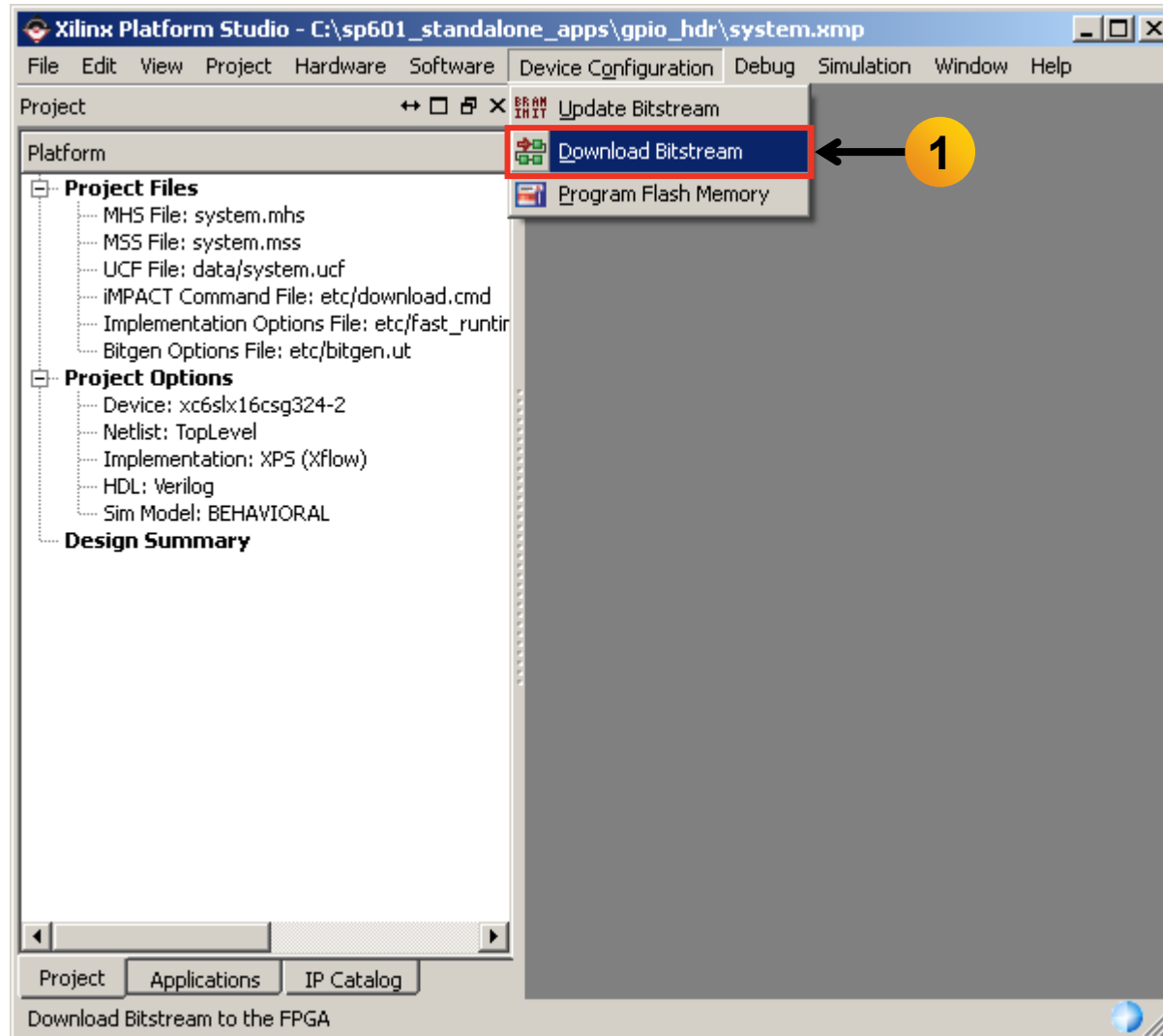


- Add a second USB Type-A to Mini-B cable to the USB JTAG connector on the SP601 board
  - Connect this cable to your PC

# Compile SP601 GPIO Header Loopback Design

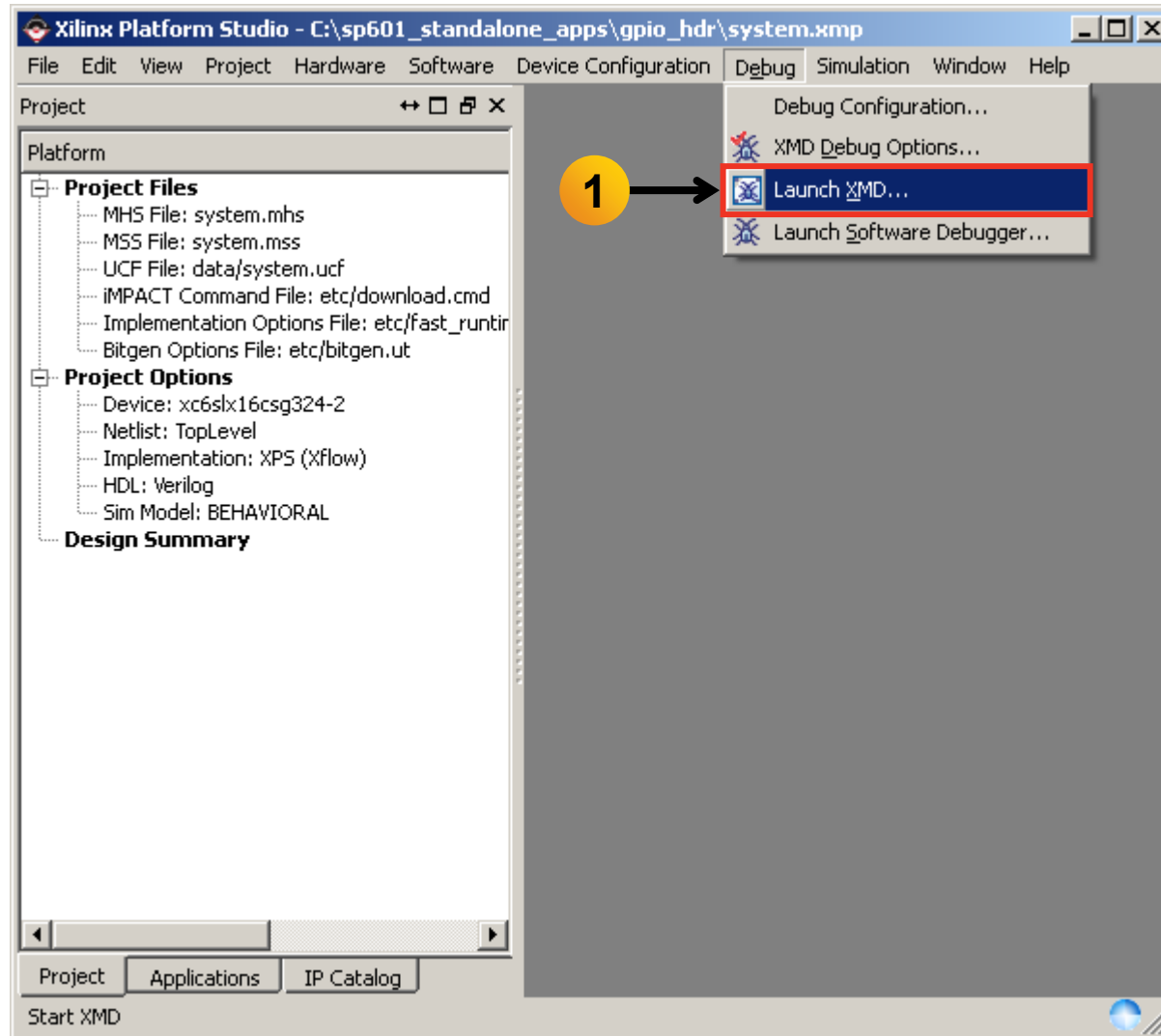
## ■ Download Bitstream

- Select **Device Configuration** → **Download Bitstream** (1)



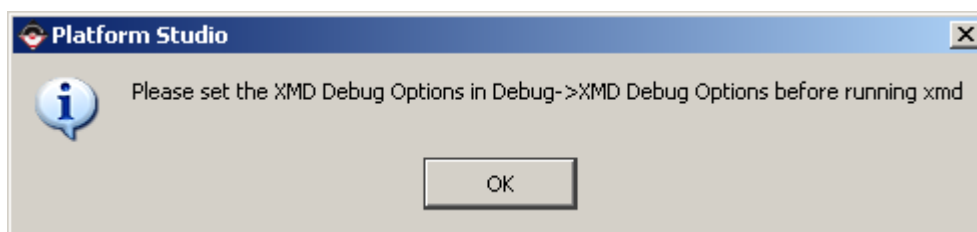
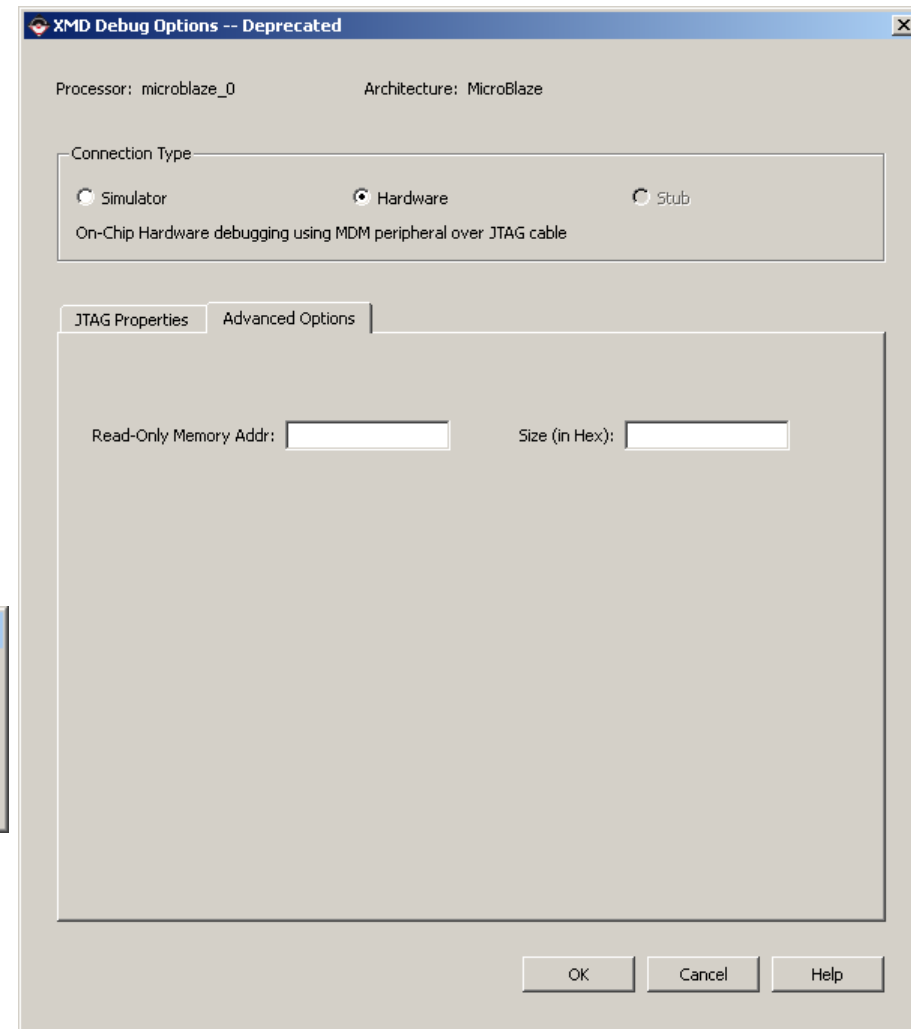
# Download SP601 GPIO Header Loopback Design

- **Download the System Monitor ELF with XMD**
  - Select **Debug** → **Launch XMD** (1)



# Download SP601 GPIO Header Loopback Design

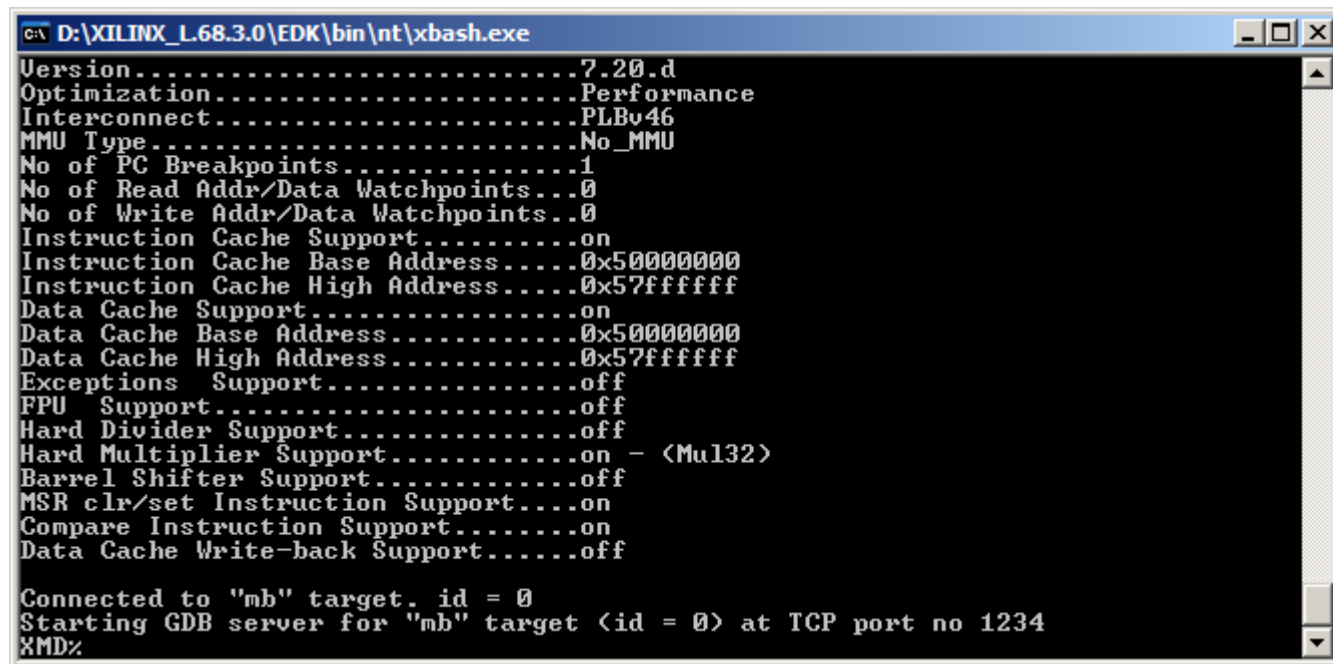
- The first time XMD runs on a project, the XMD Debug options must be set



Note: Presentation applies to the SP601

# Download SP601 GPIO Header Loopback Design

- XMD opens and connects to the processor, using the default options

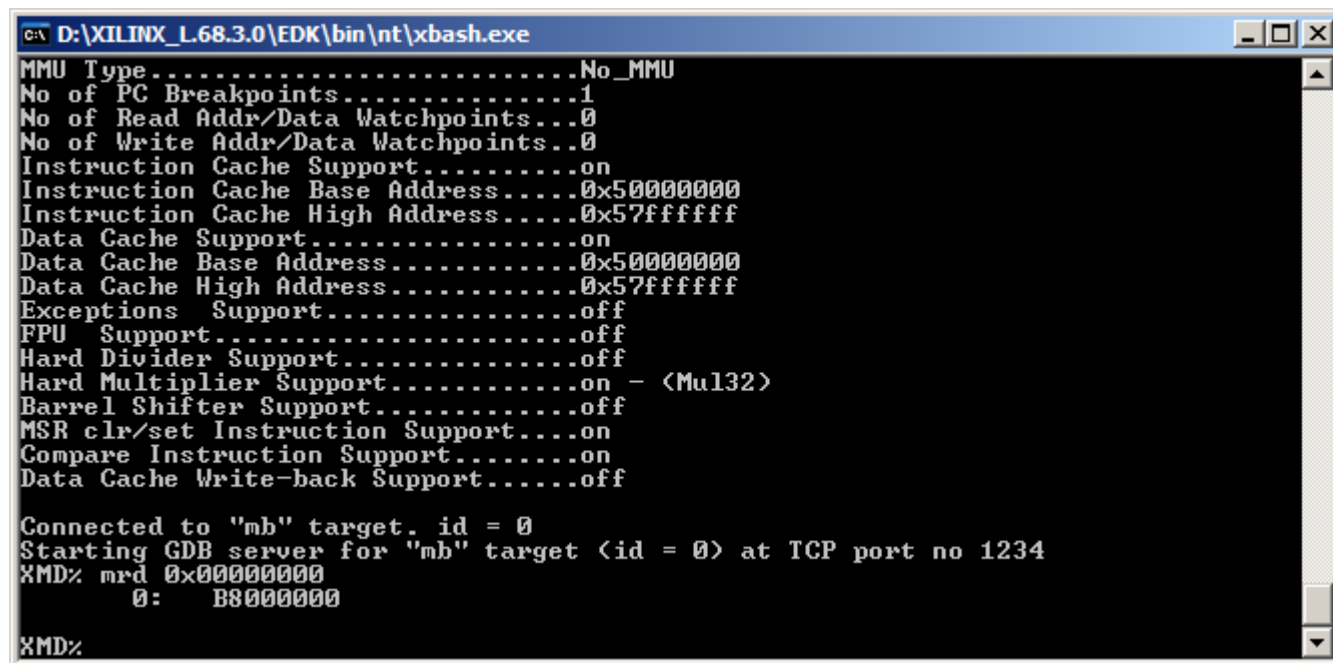


```
C:\D:\XILINX_L.68.3.0\EDK\bin\nt\xbash.exe
Version.....7.20.d
Optimization.....Performance
Interconnect.....PLBv46
MMU Type.....No_MMU
No of PC Breakpoints.....1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....on
Instruction Cache Base Address.....0x50000000
Instruction Cache High Address.....0x57ffffff
Data Cache Support.....on
Data Cache Base Address.....0x50000000
Data Cache High Address.....0x57ffffff
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - <Mul132>
Barrel Shifter Support.....off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on
Data Cache Write-back Support.....off

Connected to "mb" target. id = 0
Starting GDB server for "mb" target <id = 0> at TCP port no 1234
XMD%
```

# Download SP601 GPIO Header Loopback Design

- To execute a memory read, type  
**mrd 0x00000000**
- This will read the memory address at the reset vector; the value should be 0xB8000000 as shown below



```
C:\XILINX_L68.3.0\EDK\bin\nt\xbash.exe
MMU Type.....No_MMU
No of PC Breakpoints.....1
No of Read Addr/Data Watchpoints...0
No of Write Addr/Data Watchpoints..0
Instruction Cache Support.....on
Instruction Cache Base Address.....0x50000000
Instruction Cache High Address.....0x57ffffff
Data Cache Support.....on
Data Cache Base Address.....0x50000000
Data Cache High Address.....0x57ffffff
Exceptions Support.....off
FPU Support.....off
Hard Divider Support.....off
Hard Multiplier Support.....on - (Mul32)
Barrel Shifter Support.....off
MSR clr/set Instruction Support....on
Compare Instruction Support.....on
Data Cache Write-back Support.....off

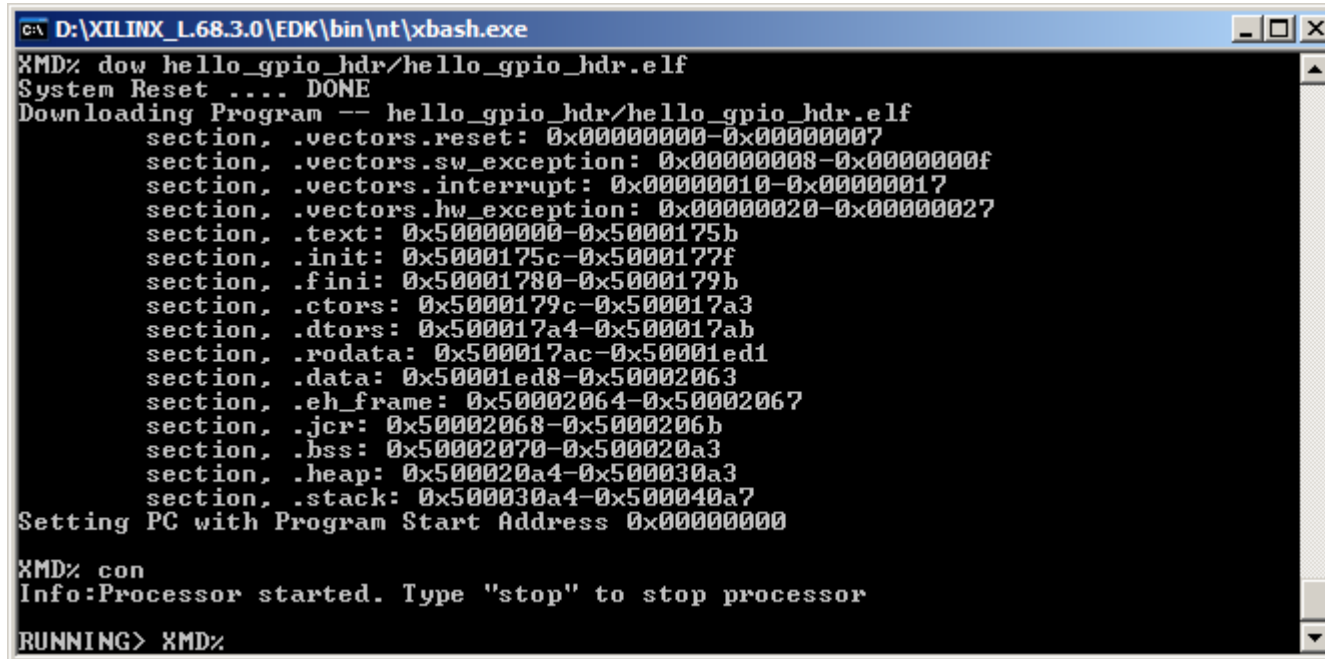
Connected to 'mb' target. id = 0
Starting GDB server for 'mb' target (id = 0) at TCP port no 1234
XMD% mrd 0x00000000
      0:  B8000000
XMD%
```

# Download SP601 GPIO Header Loopback Design

- Download and run the System Monitor ELF file:

dow hello\_gpio\_hdr/hello\_gpio\_hdr.elf

con

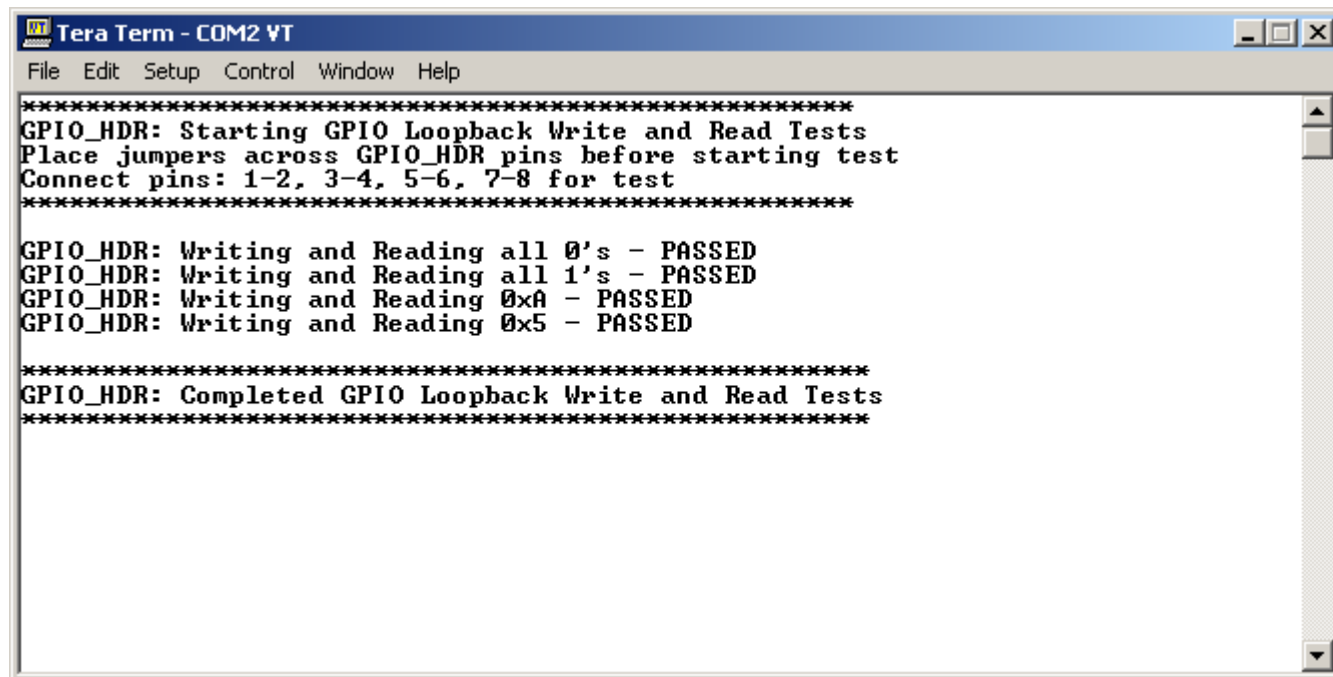


```
C:\D:\XILINX_L68.3.0\EDK\bin\nt\xbash.exe
XMD% dow hello_gpio_hdr/hello_gpio_hdr.elf
System Reset .... DONE
Downloading Program -- hello_gpio_hdr/hello_gpio_hdr.elf
section, .vectors.reset: 0x00000000-0x00000007
section, .vectors.sw_exception: 0x00000008-0x0000000f
section, .vectors.interrupt: 0x00000010-0x00000017
section, .vectors.hw_exception: 0x00000020-0x00000027
section, .text: 0x50000000-0x5000175b
section, .init: 0x5000175c-0x5000177f
section, .fini: 0x50001780-0x5000179b
section, .ctors: 0x5000179c-0x500017a3
section, .dtors: 0x500017a4-0x500017ab
section, .rodata: 0x500017ac-0x50001ed1
section, .data: 0x50001ed8-0x50002063
section, .eh_frame: 0x50002064-0x50002067
section, .jcr: 0x50002068-0x5000206b
section, .bss: 0x50002070-0x500020a3
section, .heap: 0x500020a4-0x500030a3
section, .stack: 0x500030a4-0x500040a7
Setting PC with Program Start Address 0x00000000
XMD% con
Info:Processor started. Type "stop" to stop processor
RUNNING> XMD%
```



# Download SP601 GPIO Header Loopback Design

- The test results will appear in the terminal window



The image shows a screenshot of a Tera Term terminal window titled "Tera Term - COM2 VT". The window has a menu bar with "File", "Edit", "Setup", "Control", "Window", and "Help". The terminal output displays the following text:

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GPIO_HDR: Writing and Reading all 1's - PASSED
GPIO_HDR: Writing and Reading 0xA - PASSED
GPIO_HDR: Writing and Reading 0x5 - PASSED

*****
GPIO_HDR: Completed GPIO Loopback Write and Read Tests
*****
```

# References

# References

- **SP601 Documentation**

- SP601 Hardware User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug518.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf)

- **Spartan-6**

- Spartan-6 Family Overview

- [http://www.xilinx.com/support/documentation/data\\_sheets/ds160.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf)

# Documentation

# Documentation

- **Spartan-6**

- Spartan-6 FPGA Family

- <http://www.xilinx.com/products/spartan6/index.htm>

- **SP601 Documentation**

- Spartan-6 FPGA SP601 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-S6-SP601-G.htm>

- SP601 Getting Started Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug523.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug523.pdf)

- SP601 Hardware User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug518.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf)

- SP601 Reference Design User Guide

- [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ug524.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug524.pdf)