SP601 Standalone Applications

December 2009

XTP053

Overview

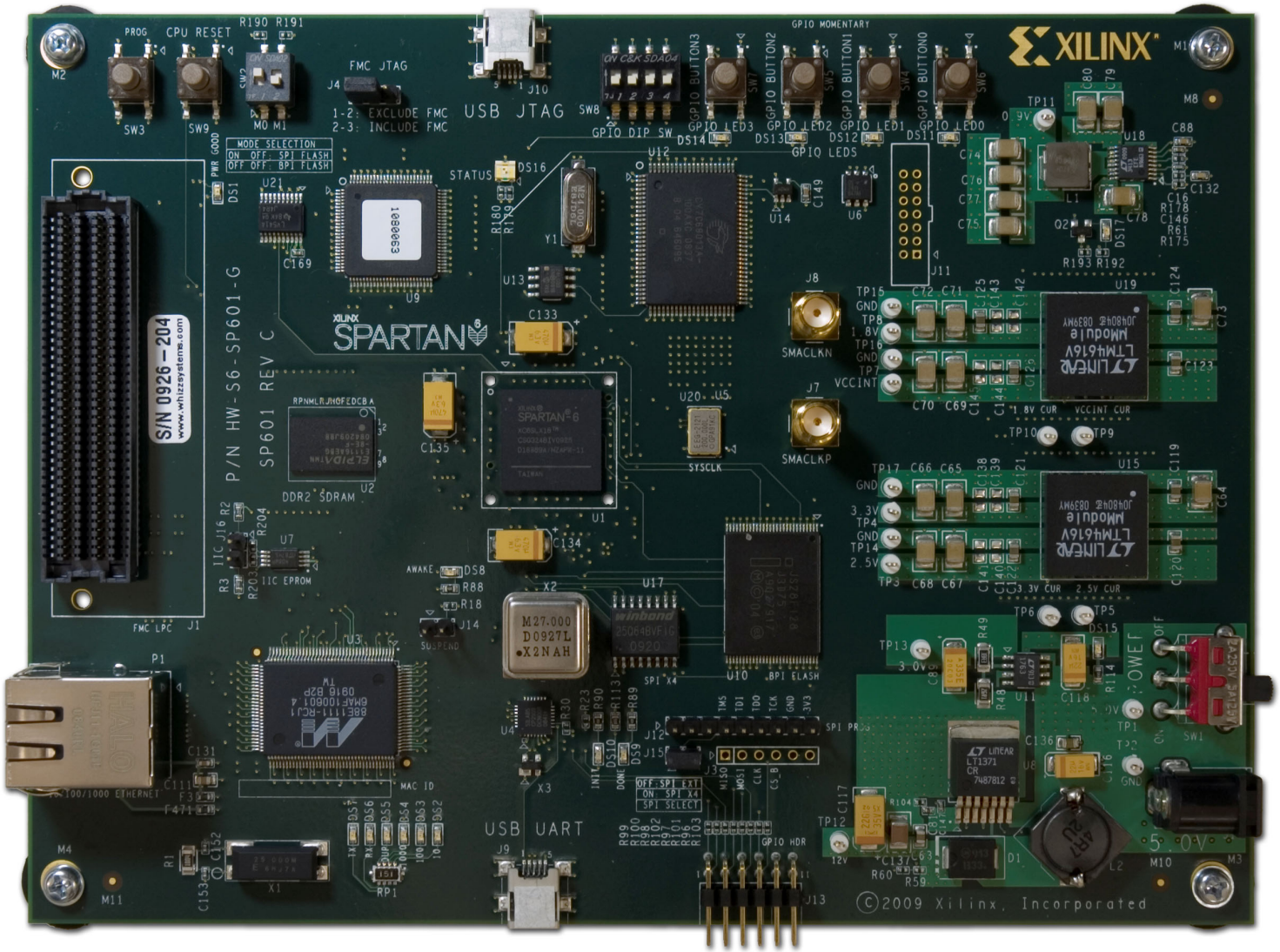
- Xilinx SP601 Board
- Software Requirements
- SP601 Setup
- Multi-pin Wake-up
- GPIO Header
- References

Note: This presentation applies to the SP601

SP601 Standalone Apps

- **Description**
  - The standalone applications tutorial extends the board feature tests offered through the BIST. A derived EDK design with additional software is used to test features such as the GPIO header pins
- **Multi-pin Wake-up Design**
  - Simple counter design show the Multi-pin Wake-up functionality of the Spartan-6 FPGA Family
- **GPIO Header Loopback Test**
  - EDK IP: MicroBlaze system derived from EDK BIST design
    - Embedded System Tools Reference Guide (UG111)
    - http://www.xilinx.com/ise/embedded/edk_ip.htm

Xilinx SP601 Board



Note: Presentation applies to the SP601

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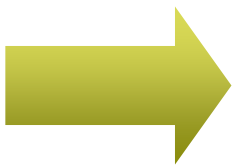
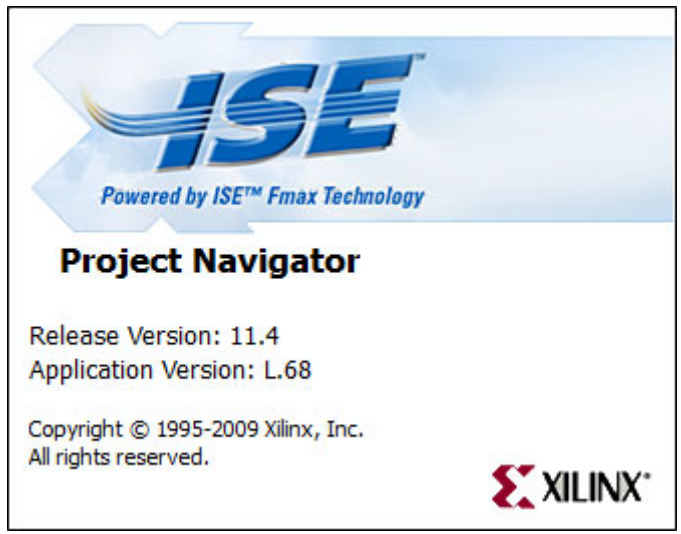
ISE Software Requirement

- **Xilinx ISE 11.4 software**
  - Install the WebPACK for the Spartan-6 LX16 devices
  - Run XilinxUpdate and download the WebPACK devices

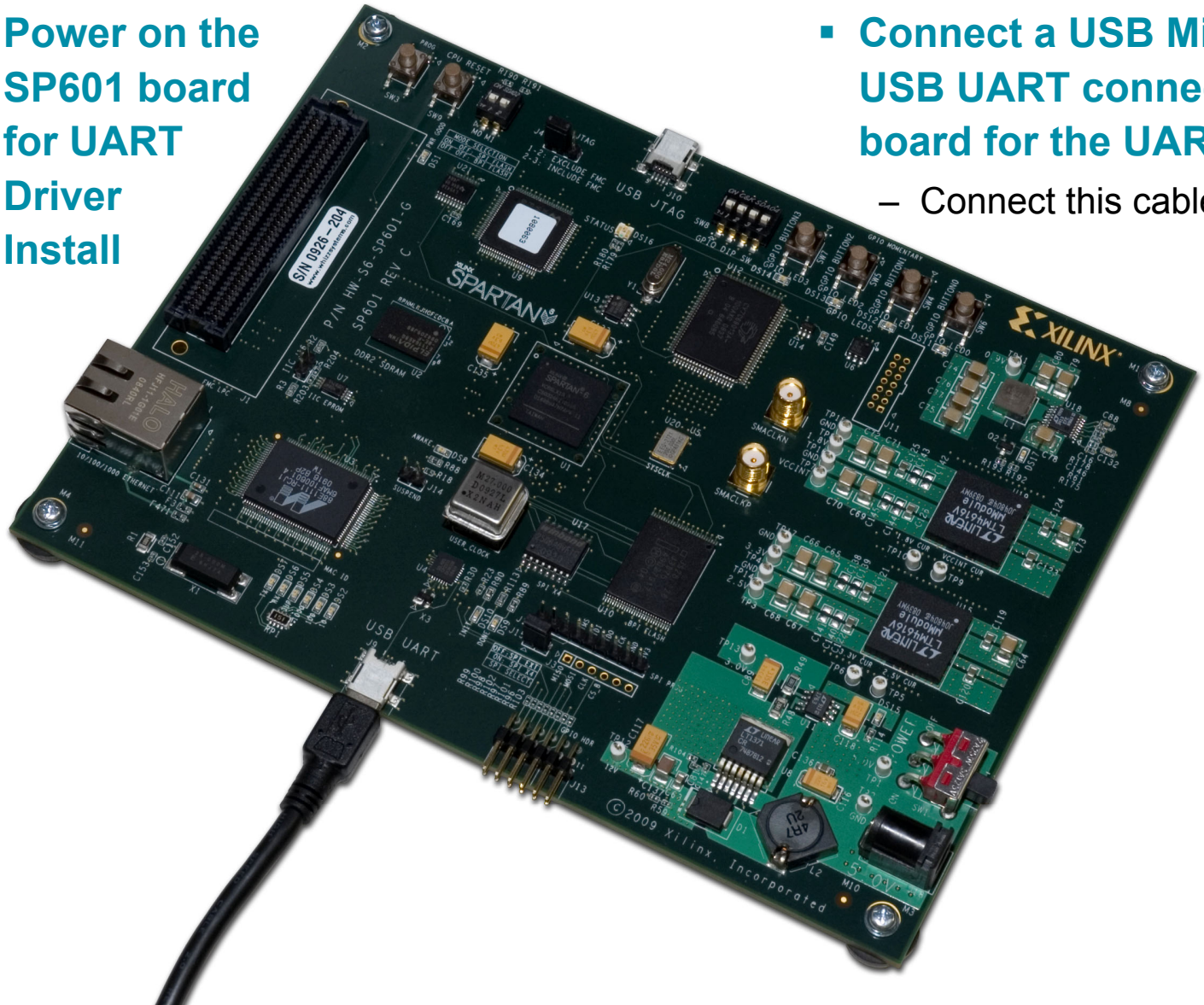




Note: Presentation applies to the SP601

SP601 Setup

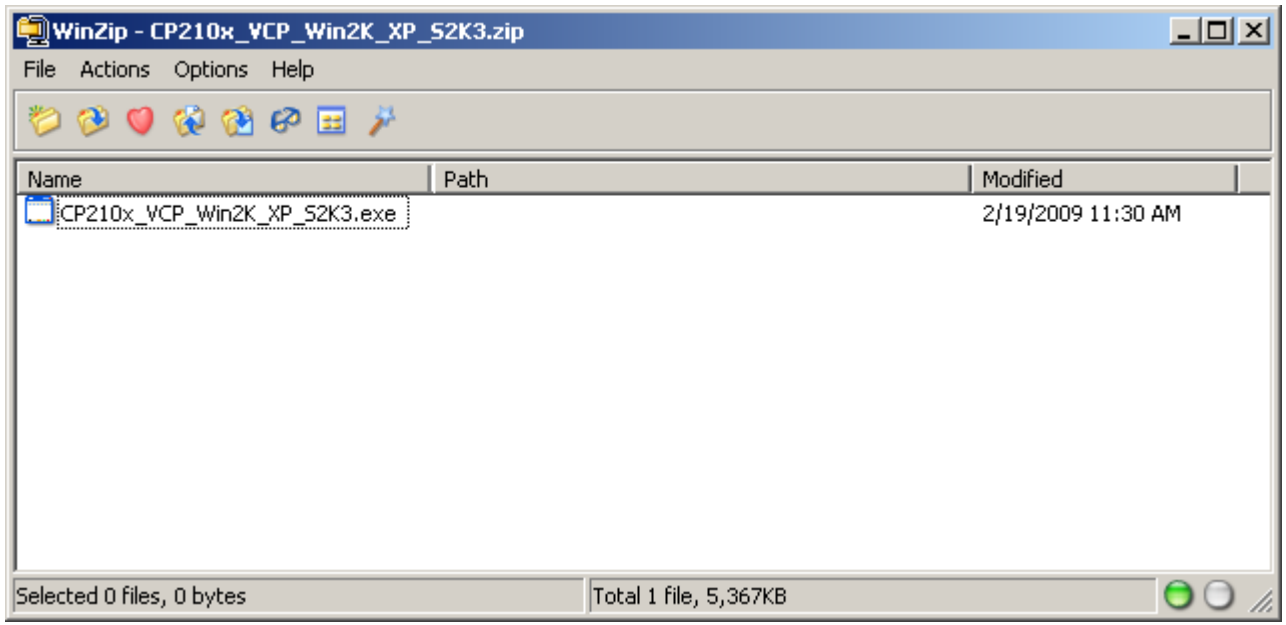
- Power on the SP601 board for UART Driver Install



- Connect a USB Mini-B Cable to the USB UART connector on the SP601 board for the UART Driver install
  - Connect this cable to your PC

SP601 Setup

- **Install USB UART Drivers**
  - https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip



Note: Presentation applies to the SP601

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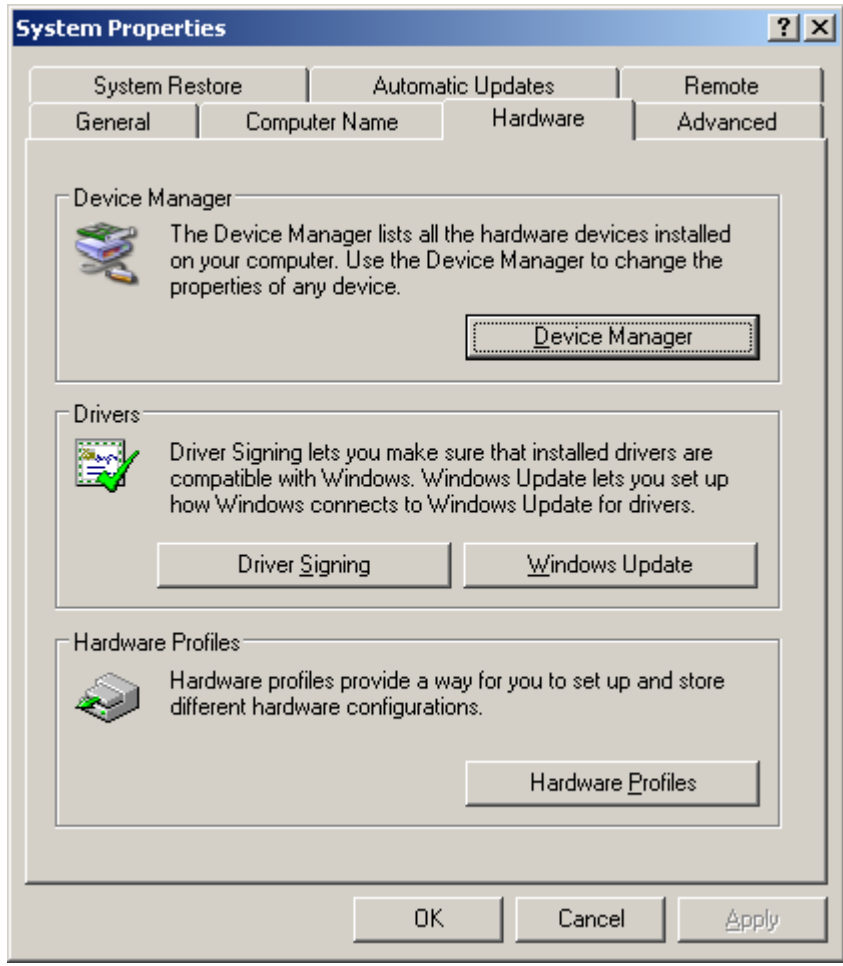
SP601 Setup

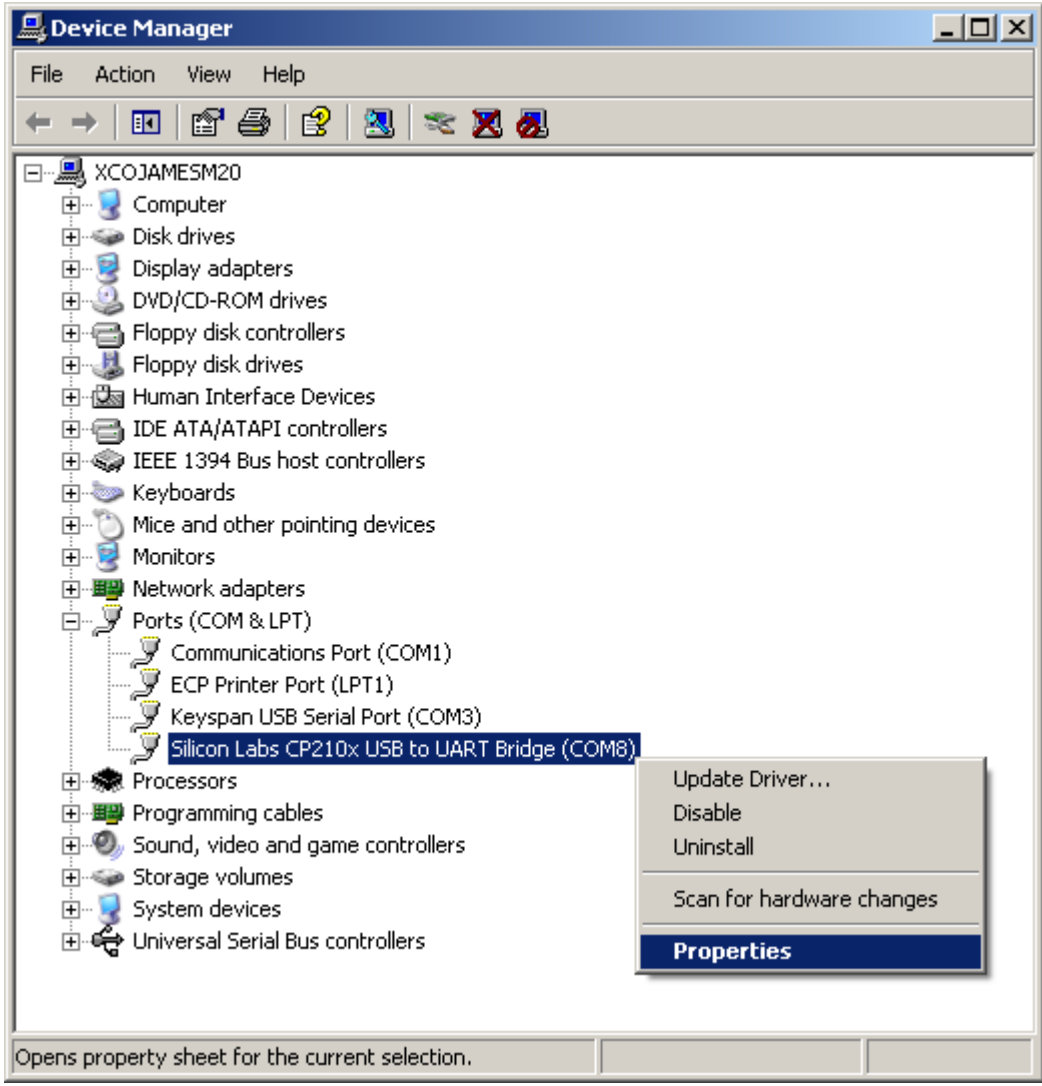
- **Right-click on My Computer and select Properties**
  - Select the Hardware tab
  - Click on Device Manager



Note: Presentation applies to the SP601

SP601 Setup

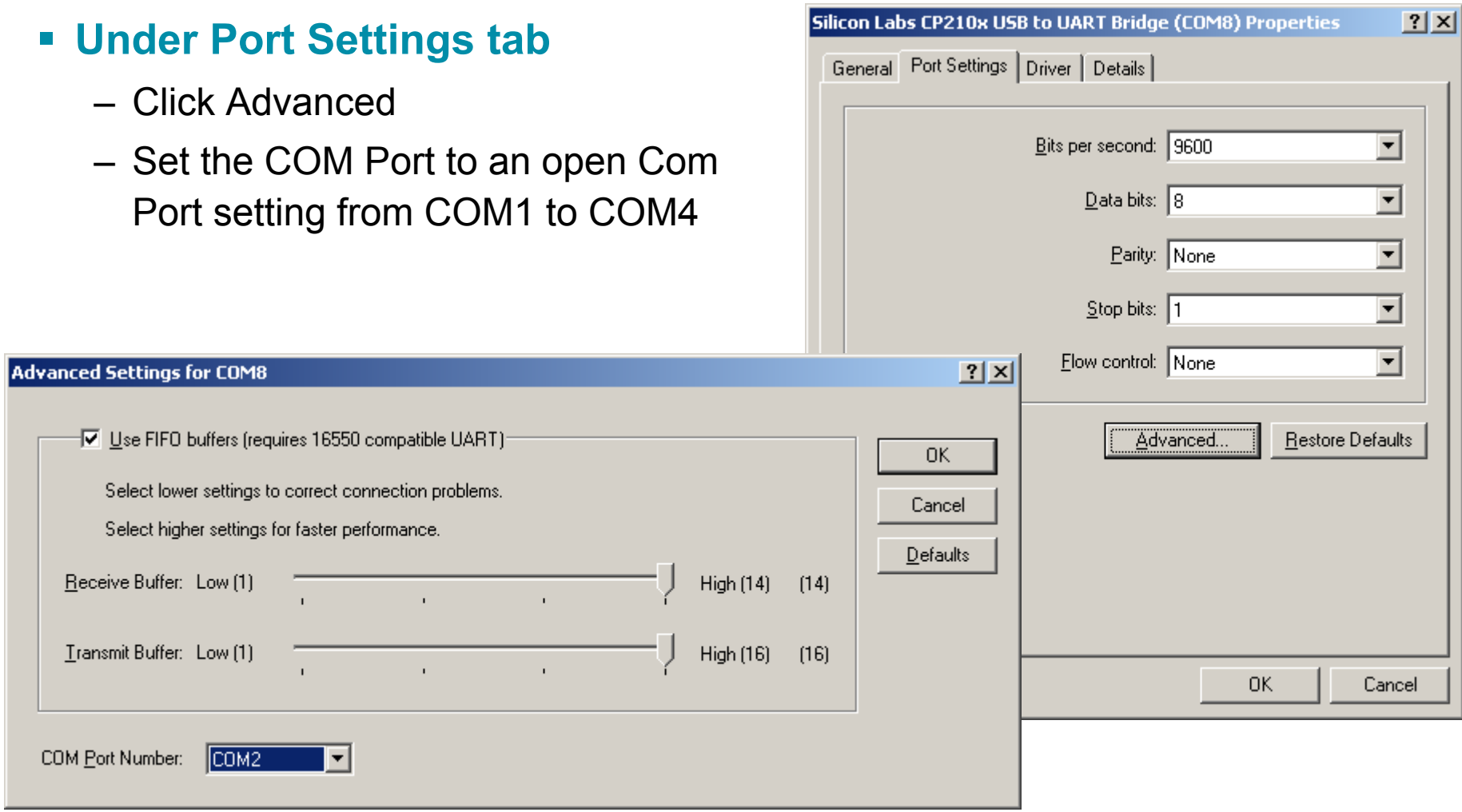
- **Expand the Ports Hardware**
  - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select Properties



Note: Presentation applies to the SP601

SP601 Setup

- **Under Port Settings tab**
  - Click Advanced
  - Set the COM Port to an open Com Port setting from COM1 to COM4



Note: Presentation applies to the SP601

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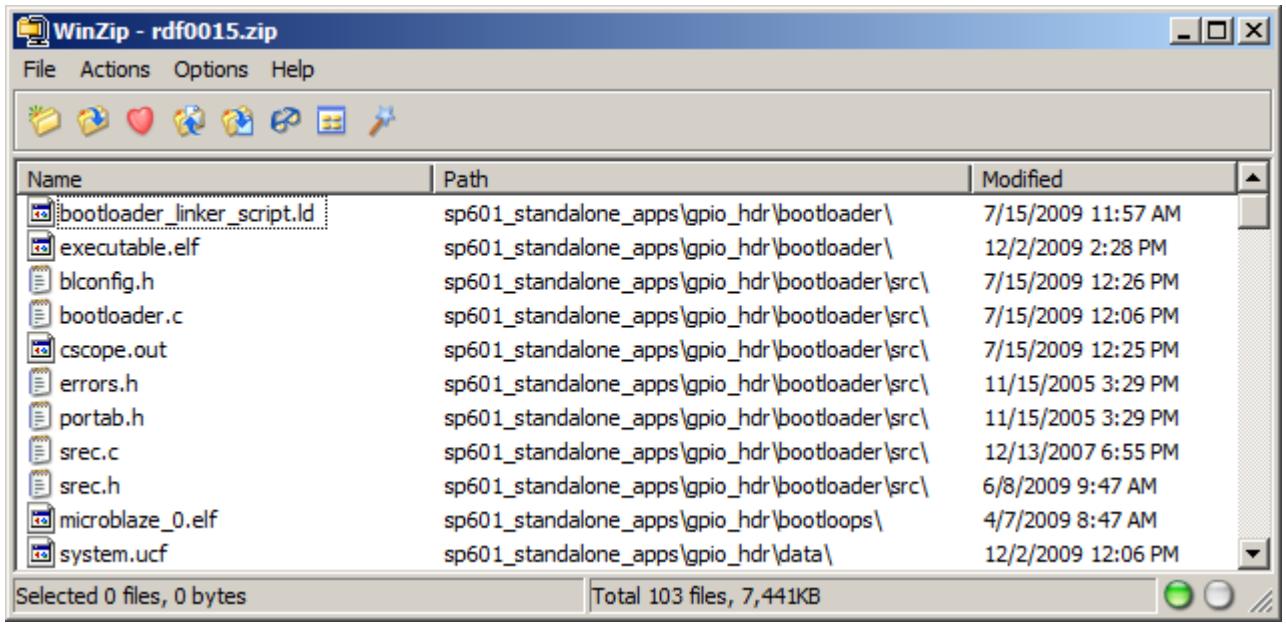
SP601 Setup

- **Unzip the rdf0015.zip file to your C:\ drive**
  - https://secure.xilinx.com/webreg/clickthrough.do?cid=139121



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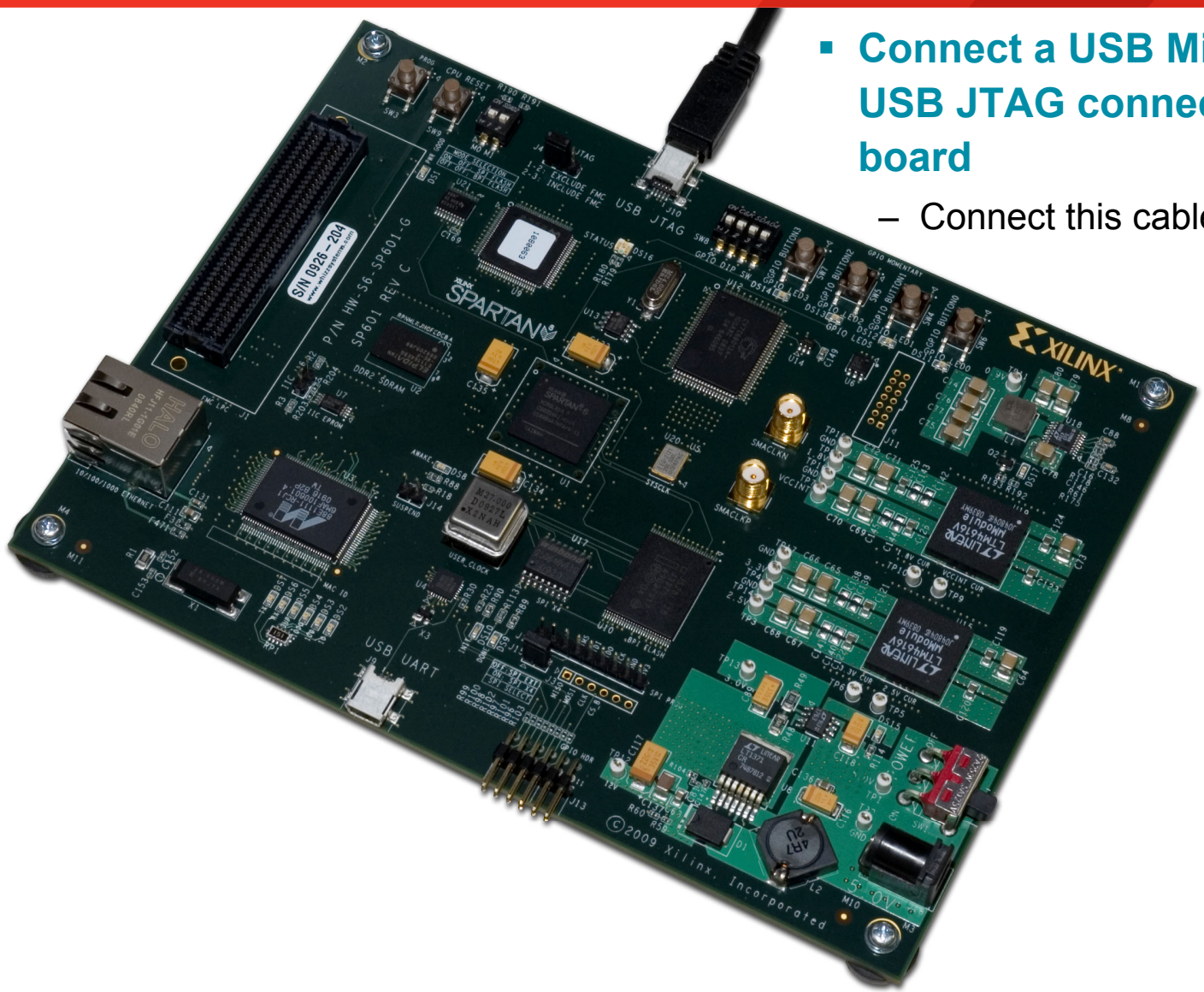
Multi-pin Wake-up

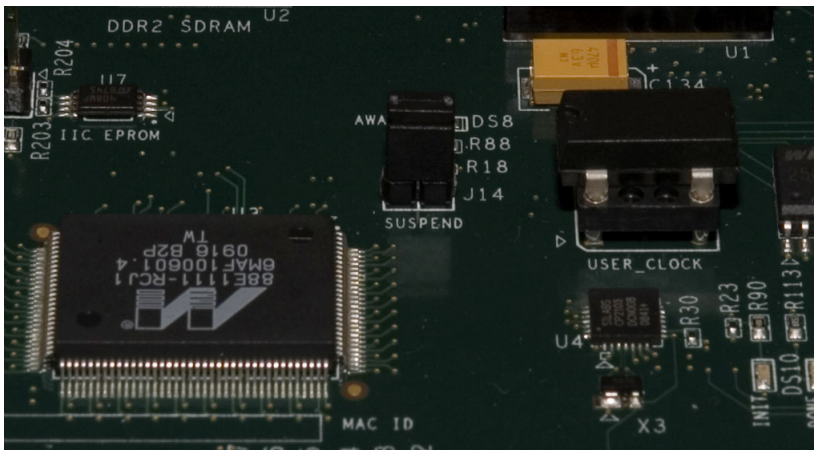
Multi-pin Wake-up

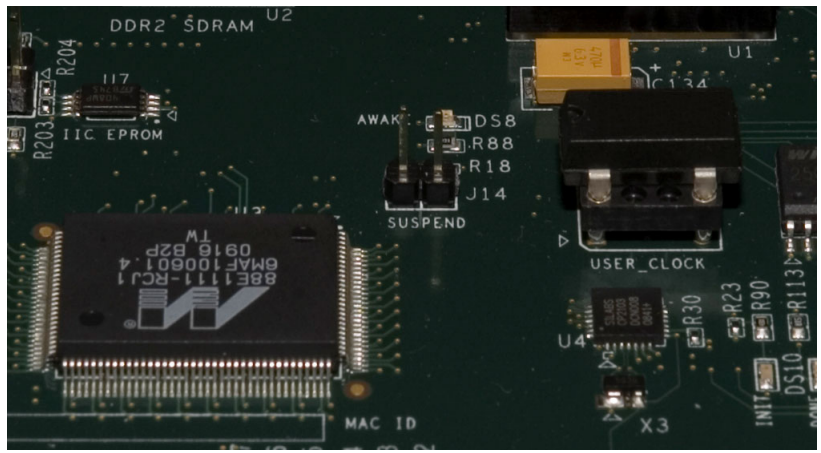


- **Connect a USB Mini-B Cable to the USB JTAG connector on the SP601 board**
  - Connect this cable to your PC

Multi-pin Wake-up

- **This test will involve removing the Suspend Jumper, seen below**
  - In this design, when an internal FPGA condition occurs and the suspend jumper is in place, suspend is initiated
  - The FPGA condition is when the two bit counter reaches “11”





Note: Presentation applies to the SP601

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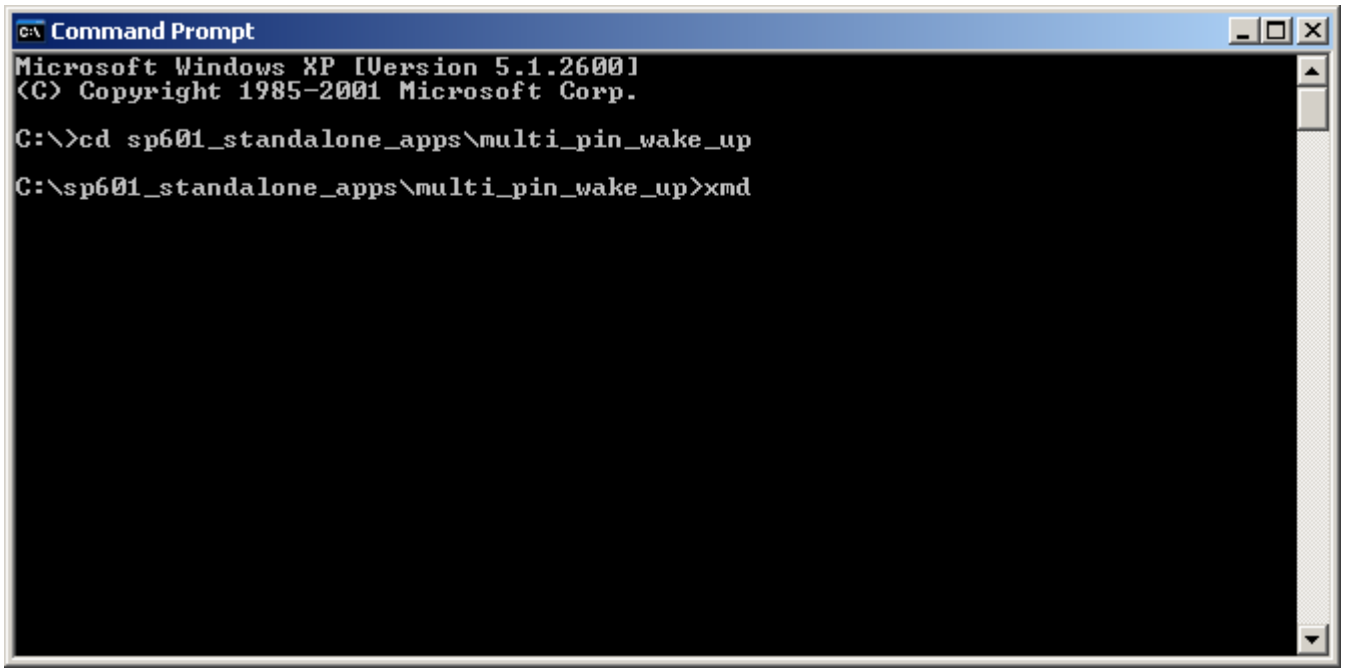
Multi-pin Wake-up

- **Run xmd to download the Bitstream file**
  - The xmd.ini file will enter the required download commands

cd sp601_standalone_apps\multi_pin_wake_up

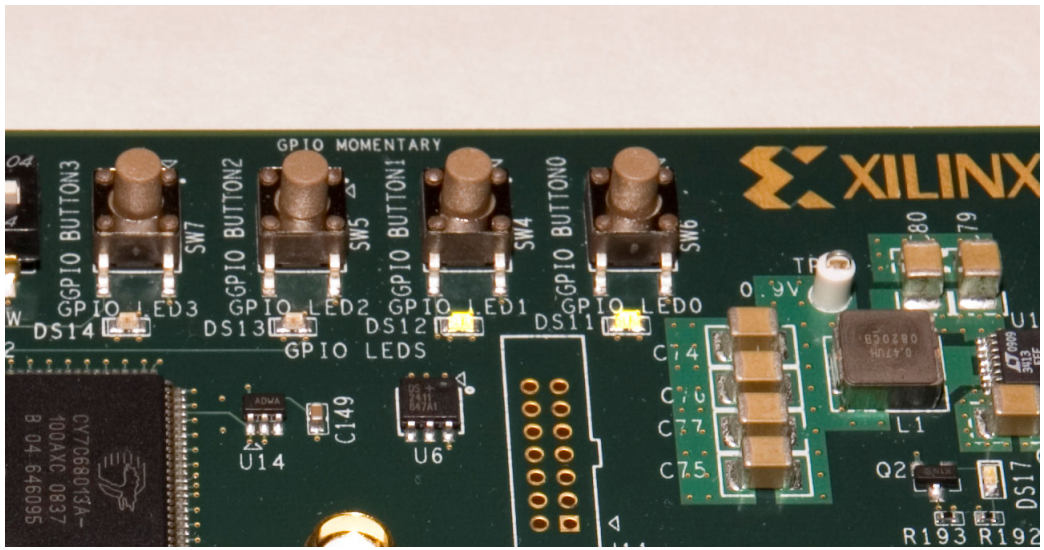
xmd

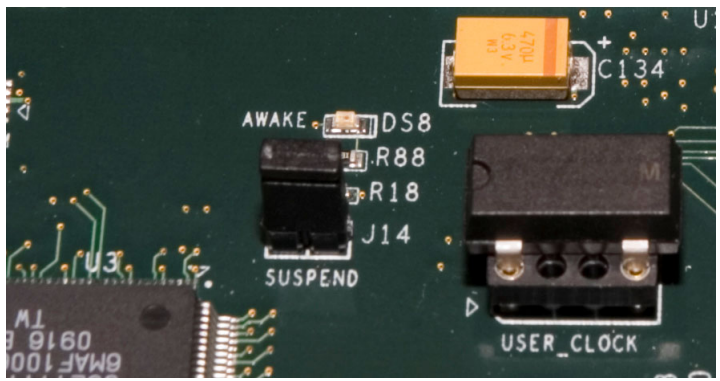


Note: Suspend jumper can be on or off during programming

Multi-pin Wake-up

- Install a jumper on J14
- The Counter LEDs continues to “11” and then stops counting (DS11 & 12)
- The Awake LED goes out





Note: Presentation applies to the SP601

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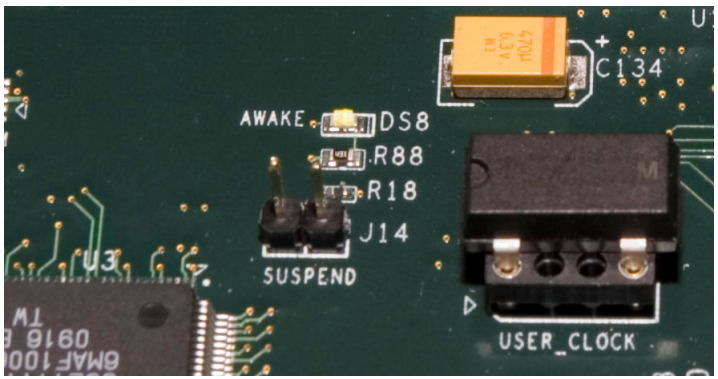
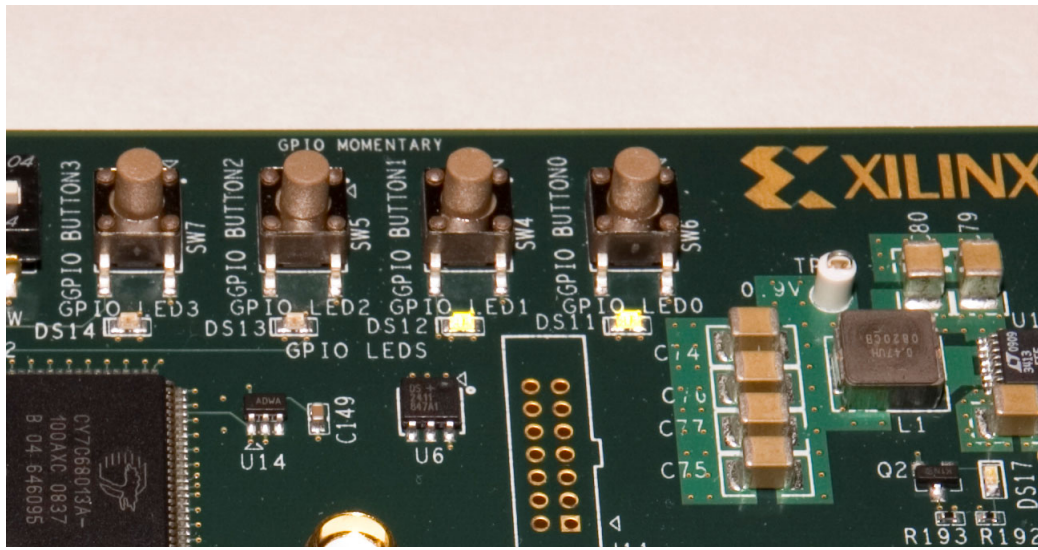
Multi-pin Wake-up

- Remove the jumper on J14
- The Awake LED comes on
- The Counter LEDs resume counting at “11”





Note: Presentation applies to the SP601

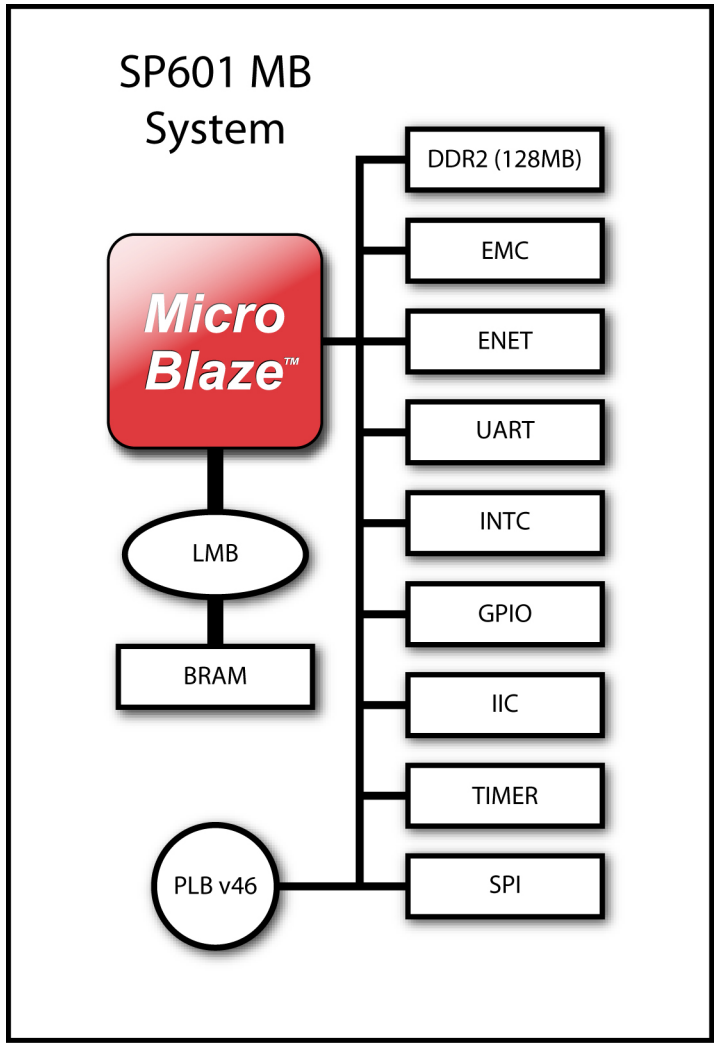
GPIO Header Loopback Test

Embedded Processor Design

- **The provided embedded reference design is supported "as is"**
  - Please refer to the click through license agreement
- **Embedded reference design has been verified on the SP601 Evaluation Kit**
  - Design consists of Early Access IP
  - Design may change in subsequent releases
- **The reference design will allow users to:**
  - Re-build and verify functionality on the SP601 evaluation kit

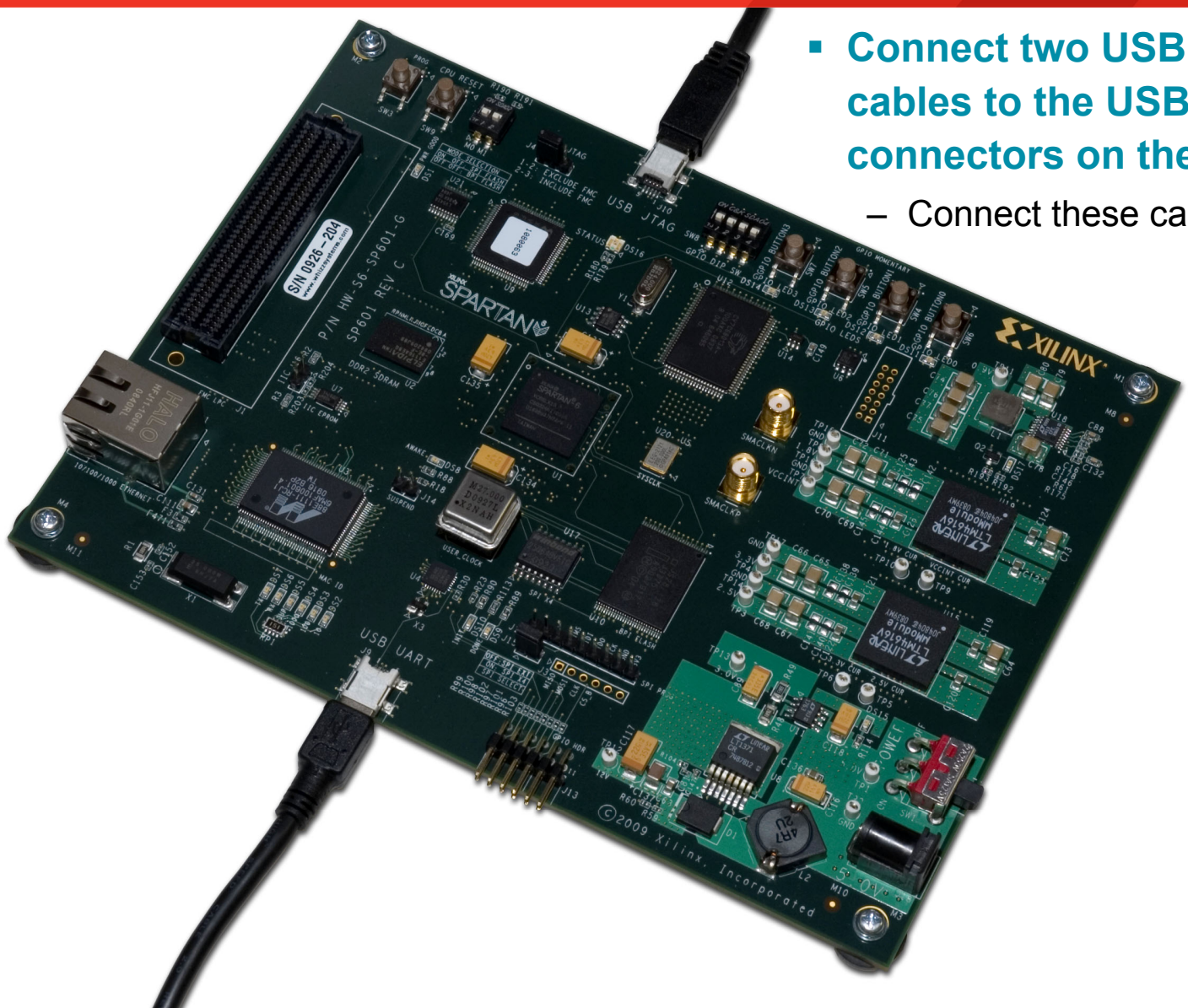
SP601 MicroBlaze Hardware

- **The SP601 MicroBlaze Design Hardware includes:**
  - DDR2 Interface (128 MB)
  - BRAM
  - External Memory Controller (EMC)
    - Flash Memory
  - Networking
  - UART
  - Interrupt Controller
  - GPIO (HDR Pins, IIC, LEDs)
  - PLB Arbiter
  - SPI



Note: Presentation applies to the SP601

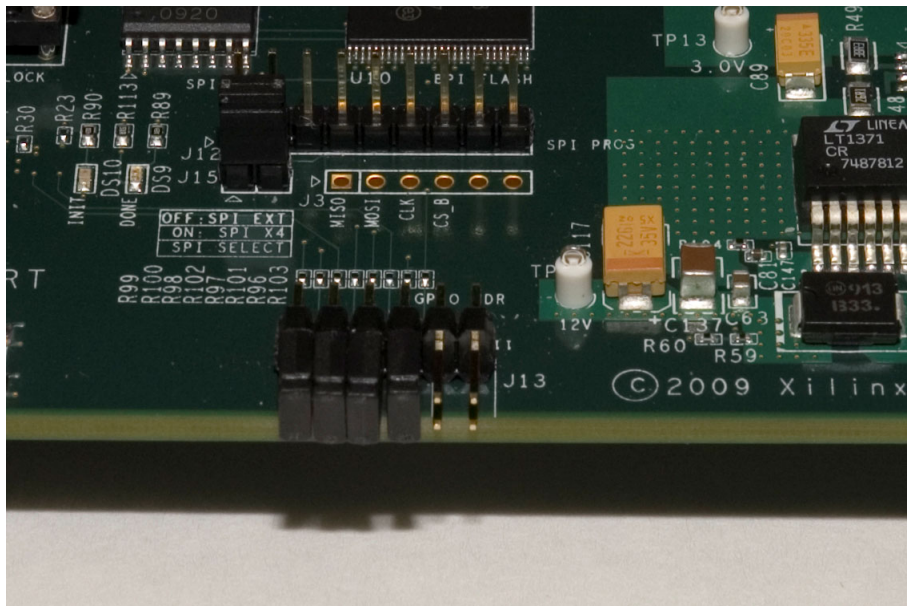
GPIO Header Loopback Test



- **Connect two USB Type-A to Mini-B cables to the USB JTAG and UART connectors on the SP601 board**
  - Connect these cables to your PC

GPIO Header Loopback Test

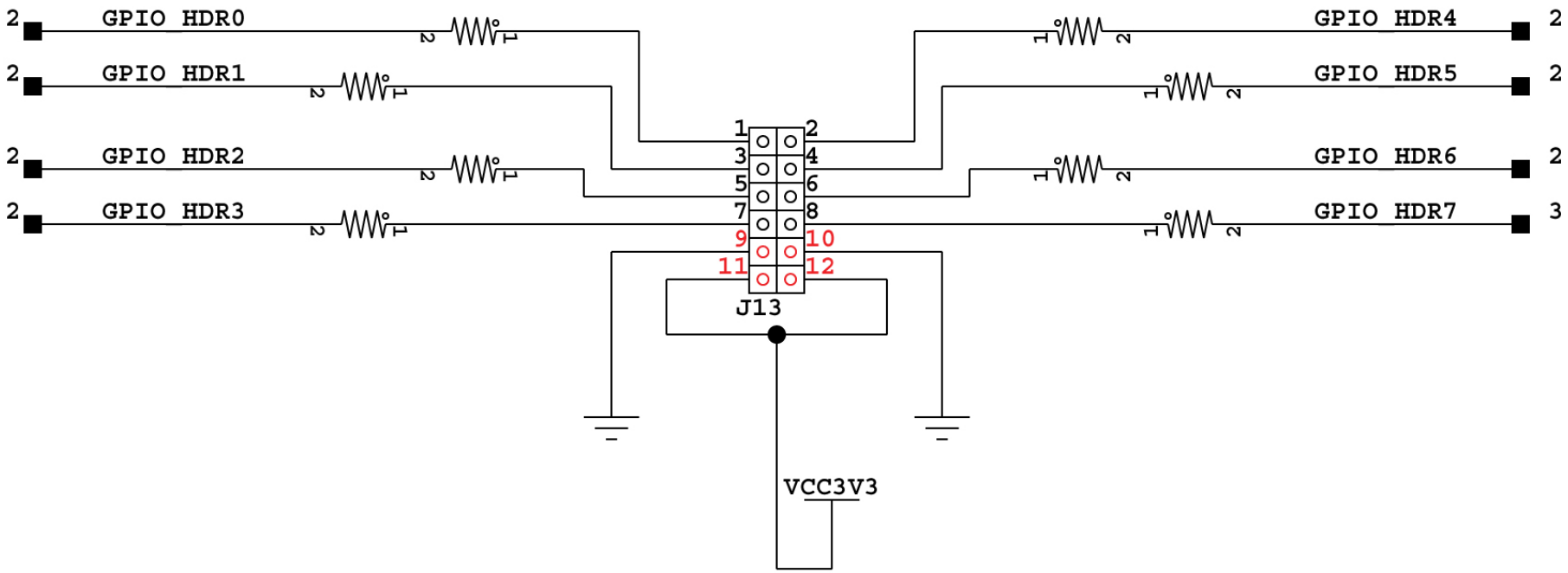
- **Connect jumpers across J13 as shown here**



Note: Presentation applies to the SP601

GPIO Header Loopback Test

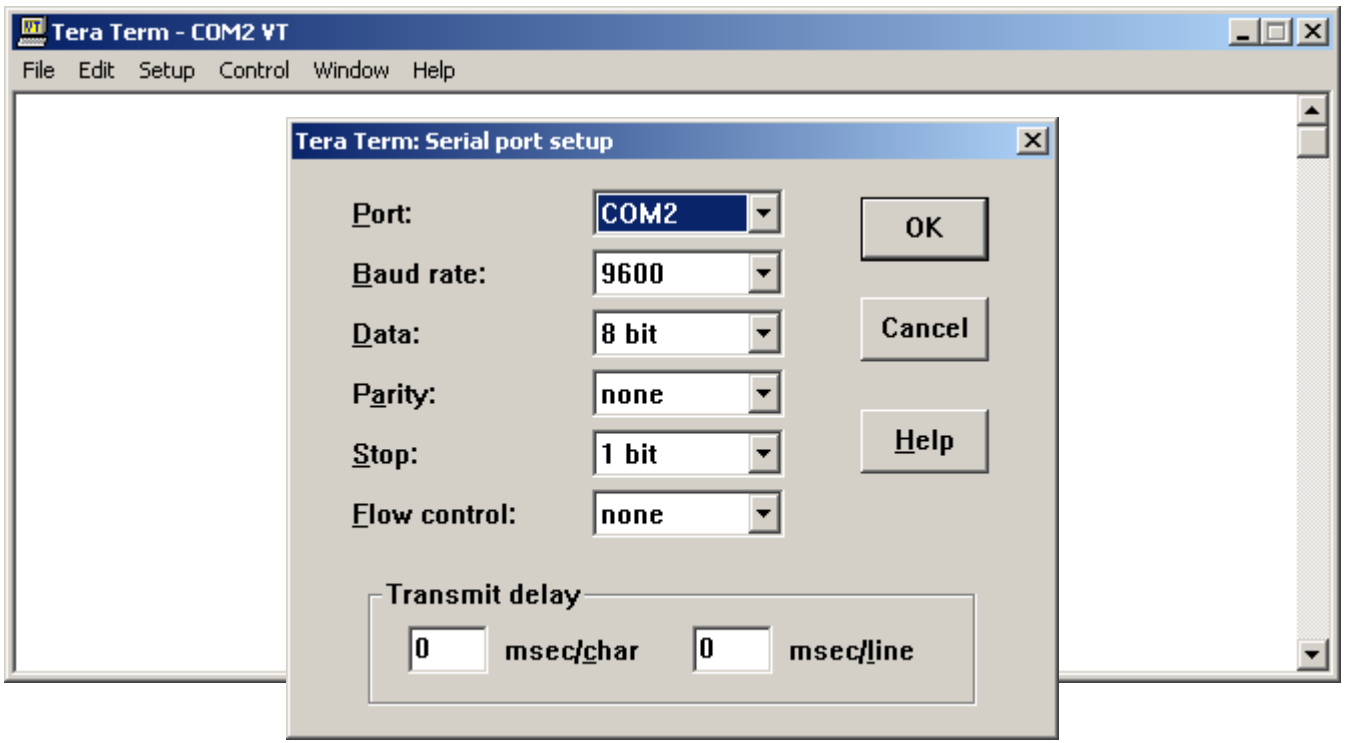
- **Do not connect any jumpers across pins 9, 10, 11, or 12**
  - These pins are connected to power and ground



Note: Presentation applies to the SP601

GPIO Header Loopback Test

- **Board Power must be on before starting Tera Term**
- **Start the Terminal Program**
  - Select your USB Com Port
  - Set the baud to 9600



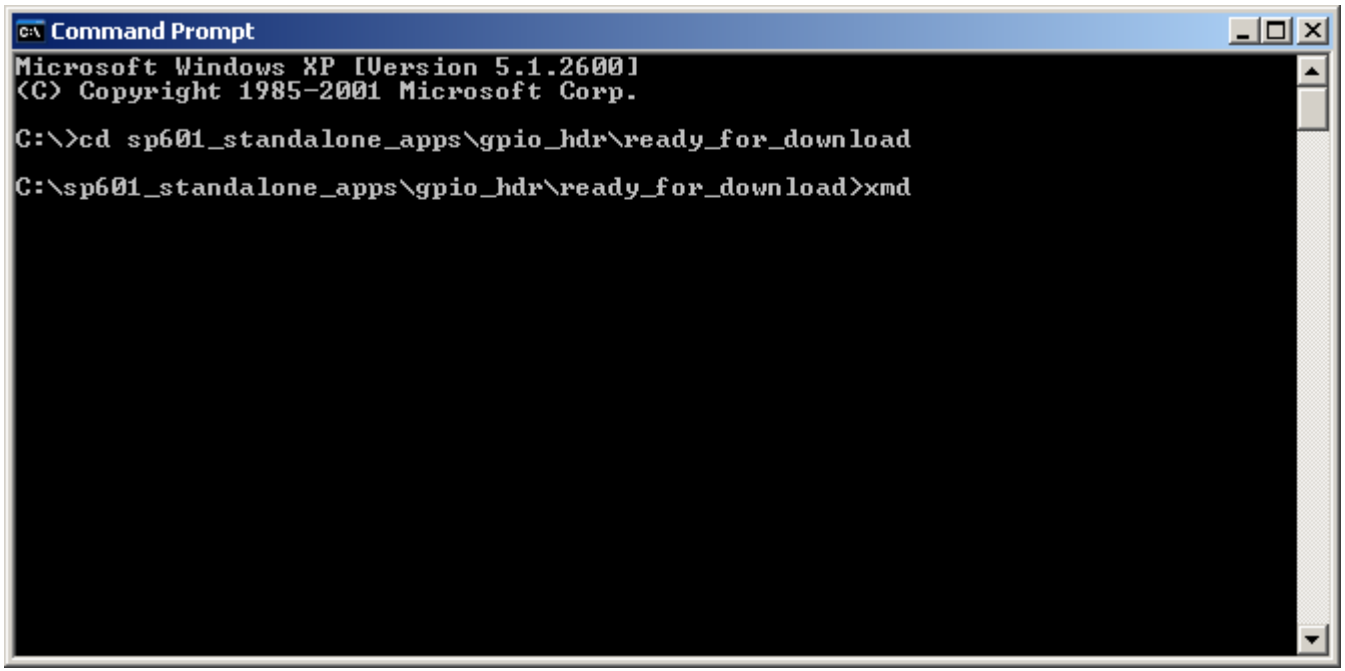
Note: Tera Term may need to be restarted if board power is cycled

GPIO Header Loopback Test

- **Run xmd to download the Bitstream and ELF file**
  - The xmd.ini file will enter the required download commands

  cd sp601_standalone_apps\gpio_hdr\ready_for_download

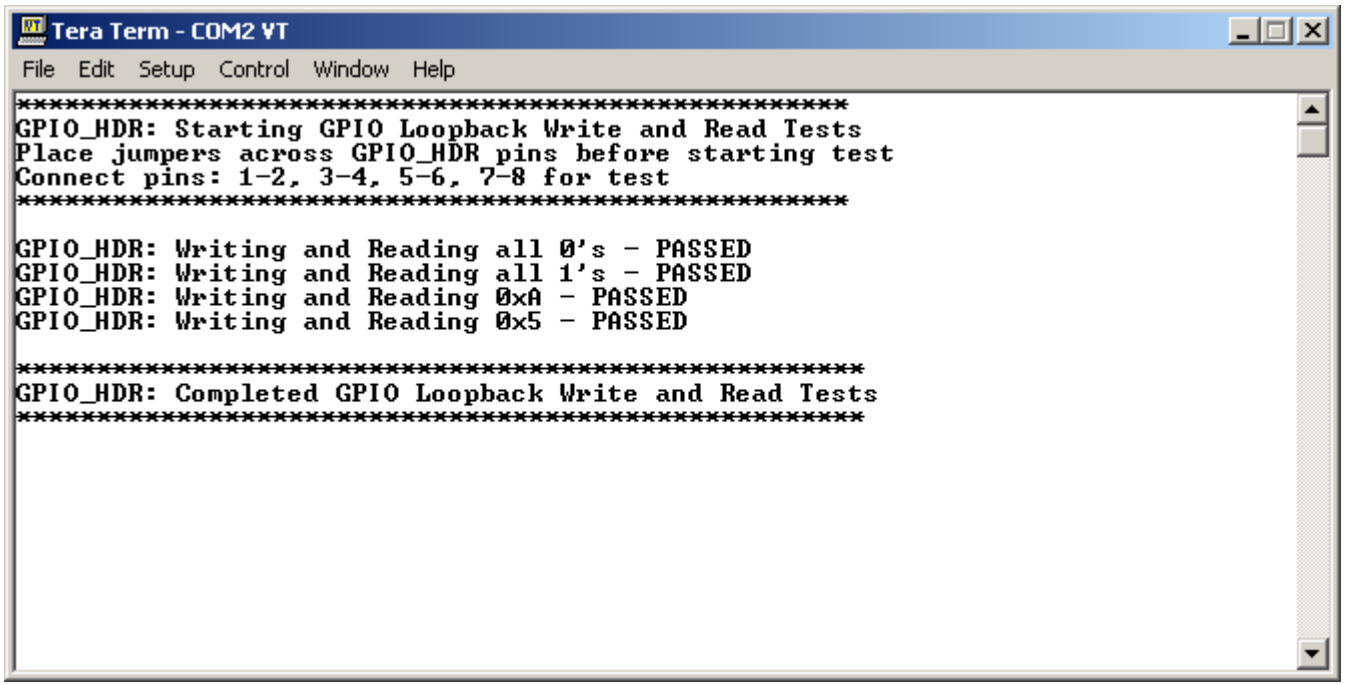
  xmd



Note: Presentation applies to the SP601

GPIO Header Loopback Test

- The test results will appear in the terminal window

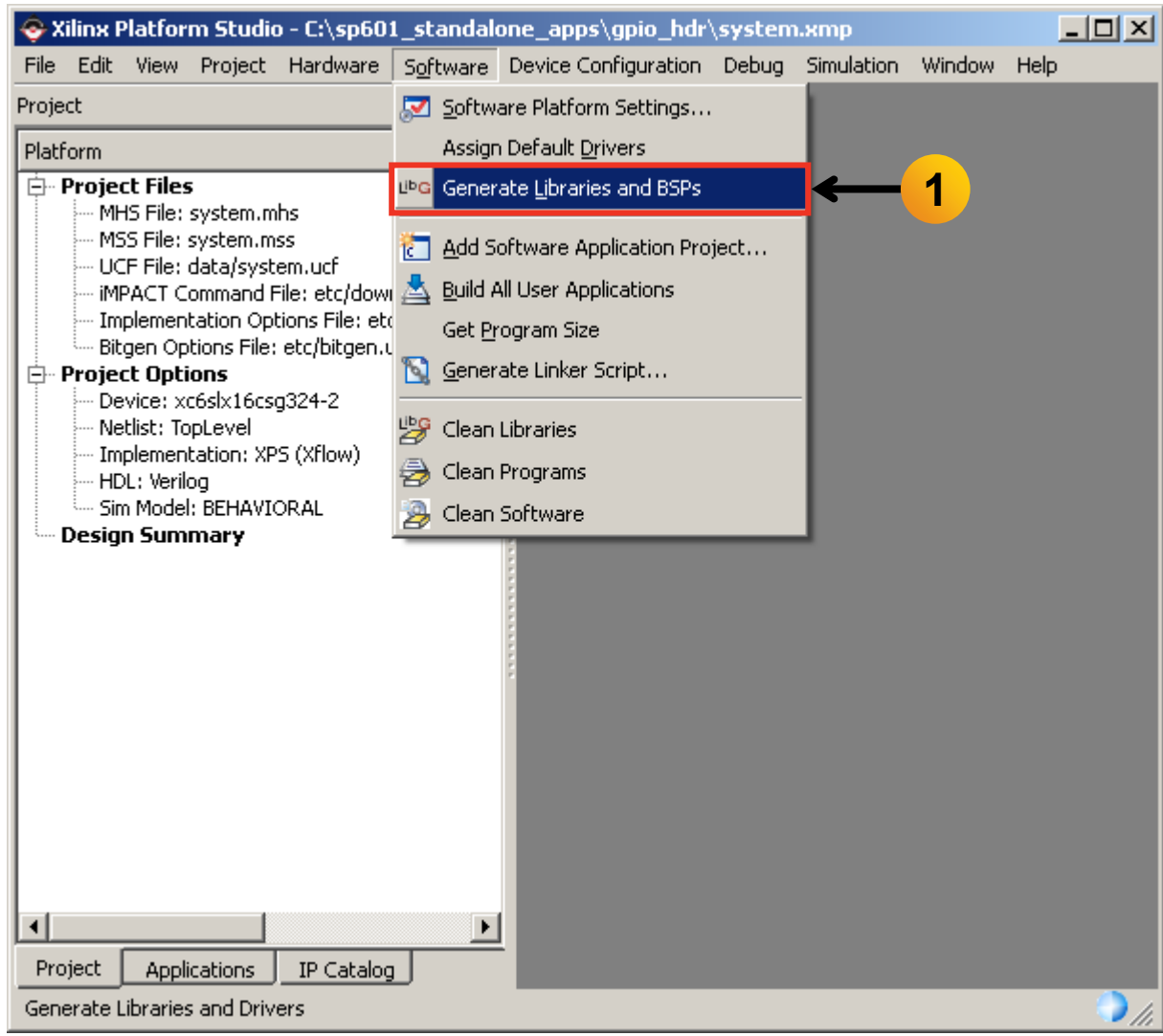


Note: Presentation applies to the SP601

Compile SP601 GPIO Header Loopback Design

Compile SP601 GPIO Header Loopback Design

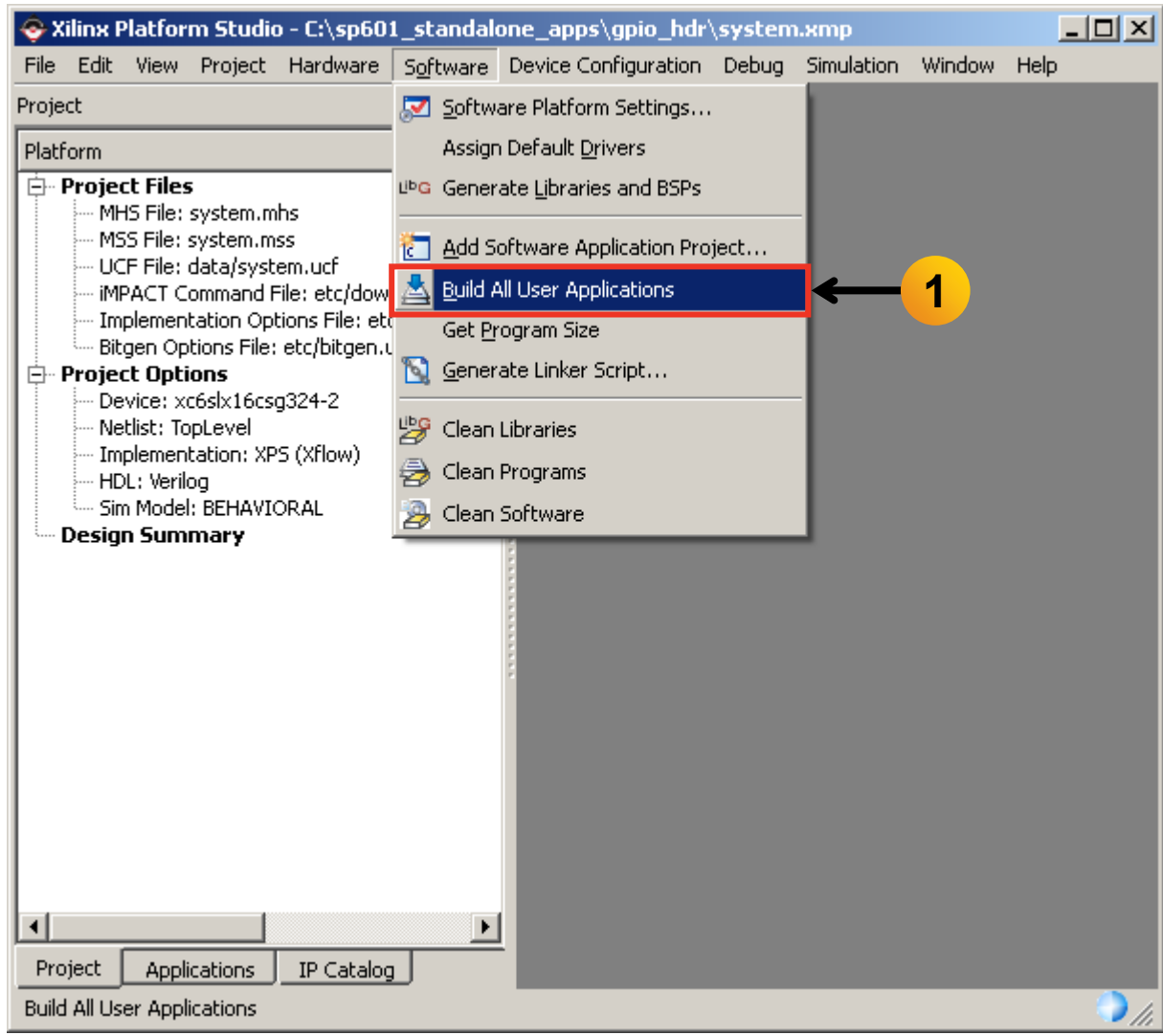
- The GPIO Header Design can be compiled with EDK
- Open XPS project <design path>\ gpio_hdr\ system.xmp
- Generate the libraries needed to create the bitstream
  - Select **Software → Generate Libraries and BSPs** (1)



Note: Presentation applies to the SP601

Compile SP601 GPIO Header Loopback Design

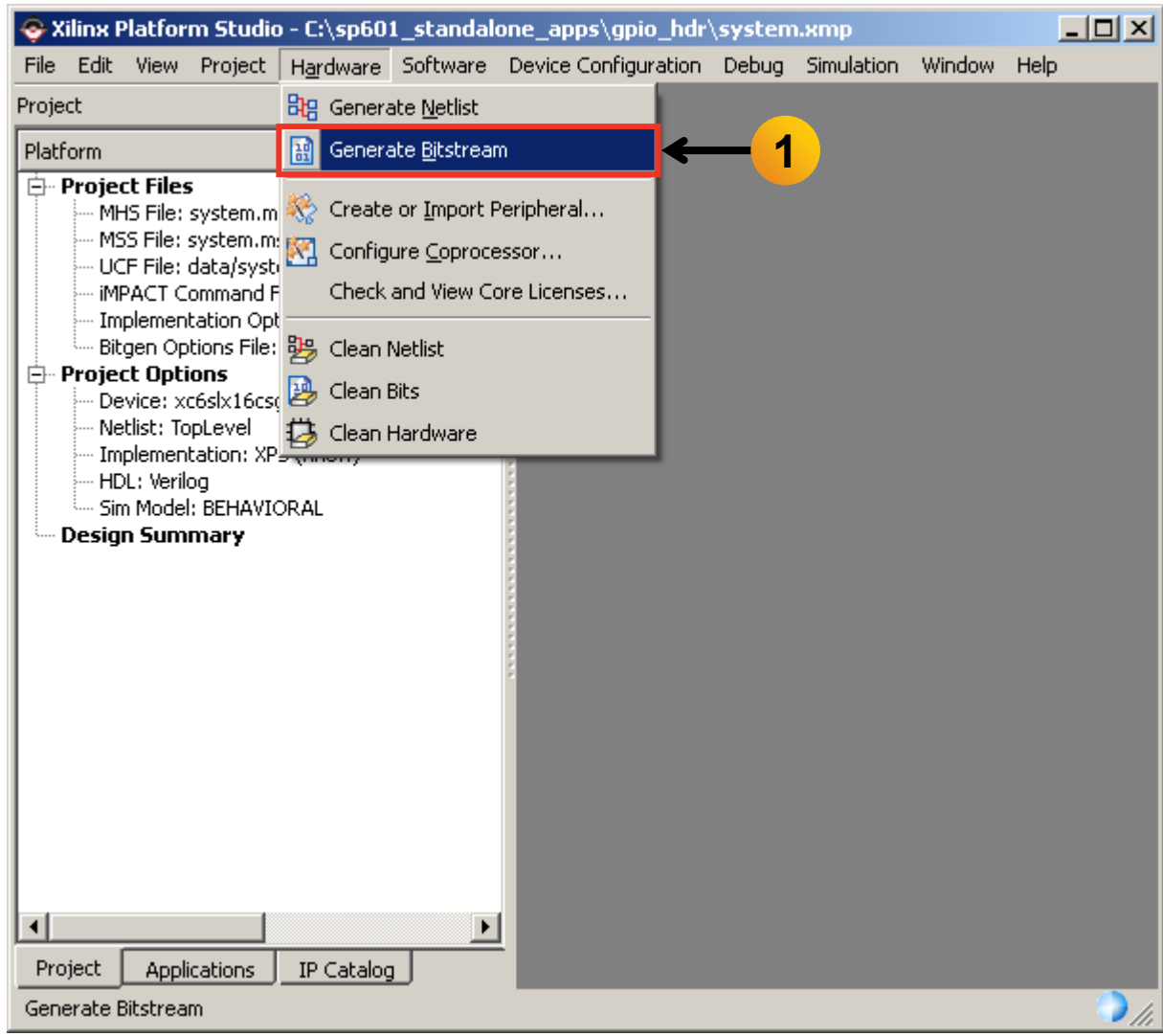
- **Compile the Software Applications and create the application ELF files**
  - Select **Software → Build All User Applications** (1)



Note: Presentation applies to the SP601

Compile SP601 GPIO Header Loopback Design

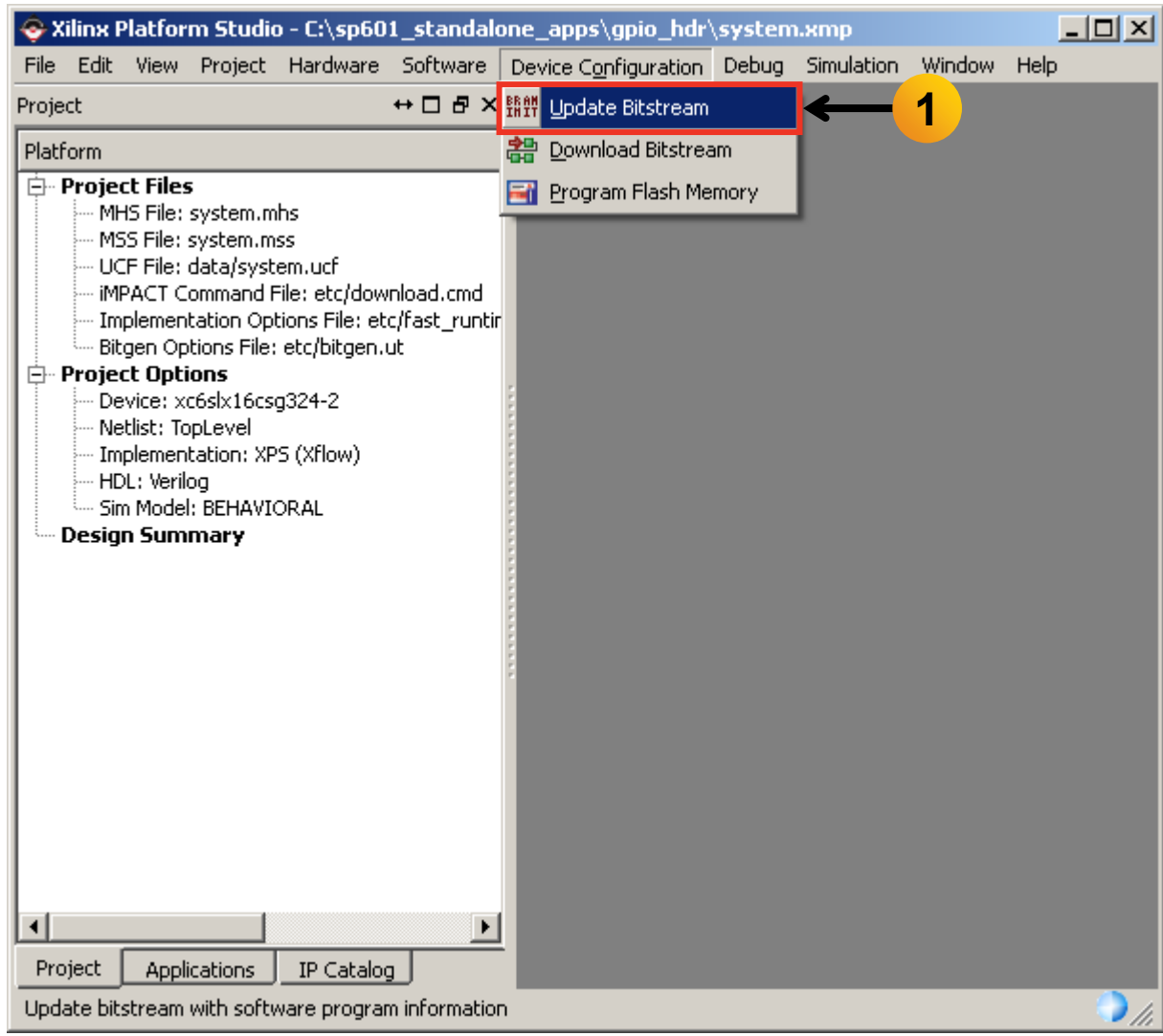
- **Create the hardware design, system.bit, located in <project directory> /implementation**
  - Select **Hardware → Generate Bitstream** (1)



Note: Presentation applies to the SP601

Compile SP601 GPIO Header Loopback Design

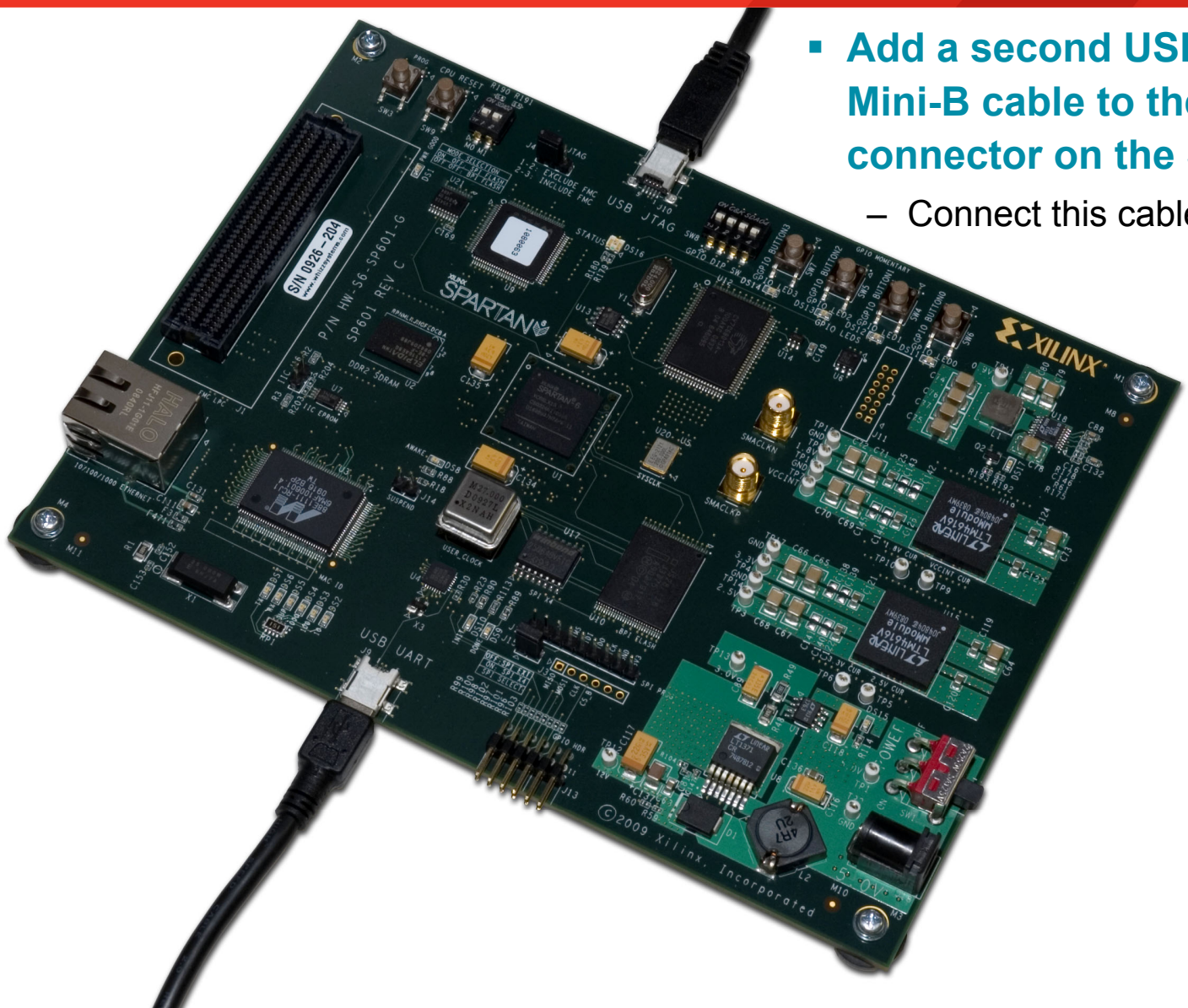
- **Init memory with the Bootloader Application ELF**
  - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
  - Select **Device Configuration → Update Bitstream** (1)



Note: Presentation applies to the SP601

Download SP601 GPIO Header Loopback Design

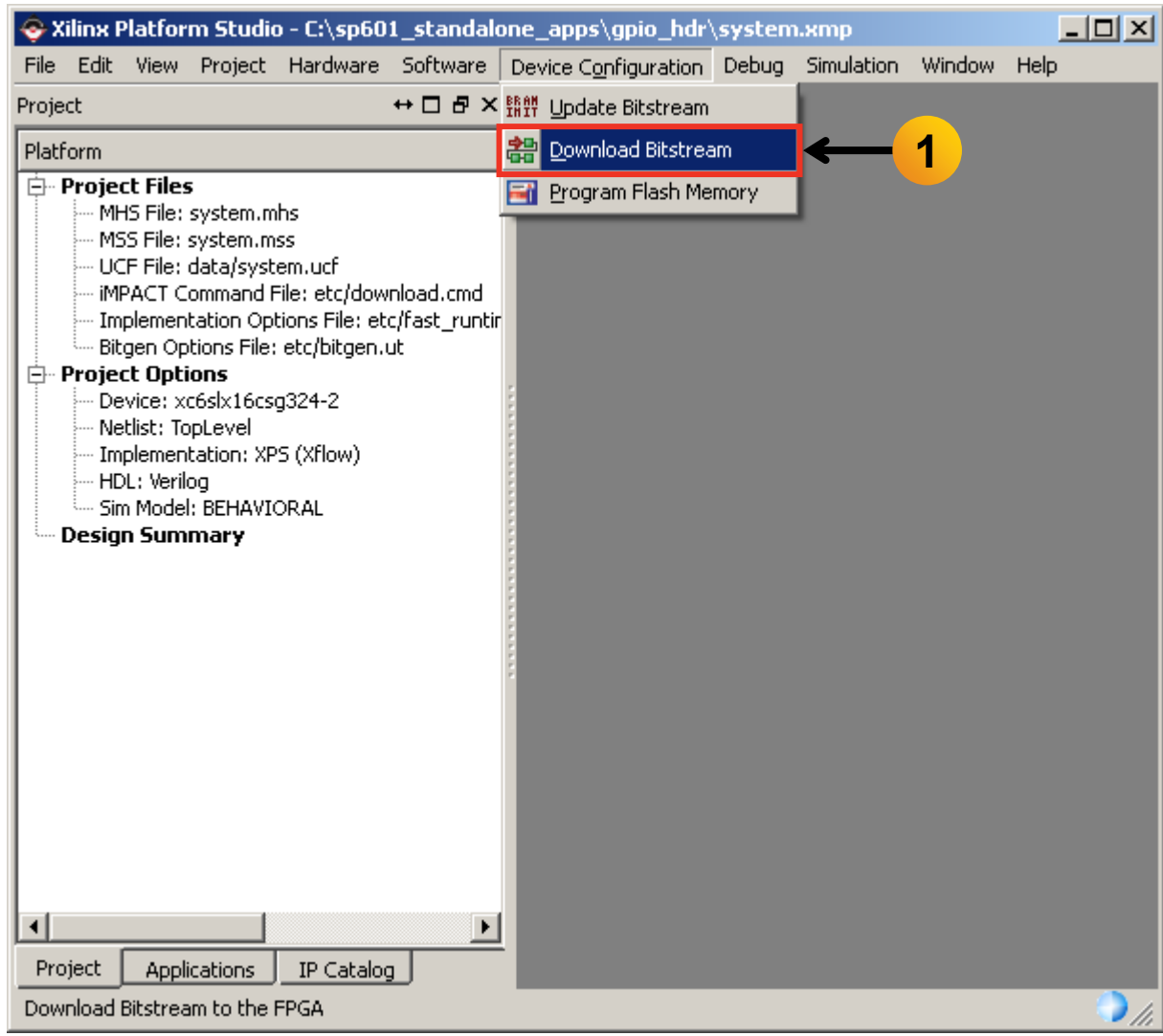
Download SP601 GPIO Header Loopback Design



- **Add a second USB Type-A to Mini-B cable to the USB JTAG connector on the SP601 board**
  - Connect this cable to your PC

Compile SP601 GPIO Header Loopback Design

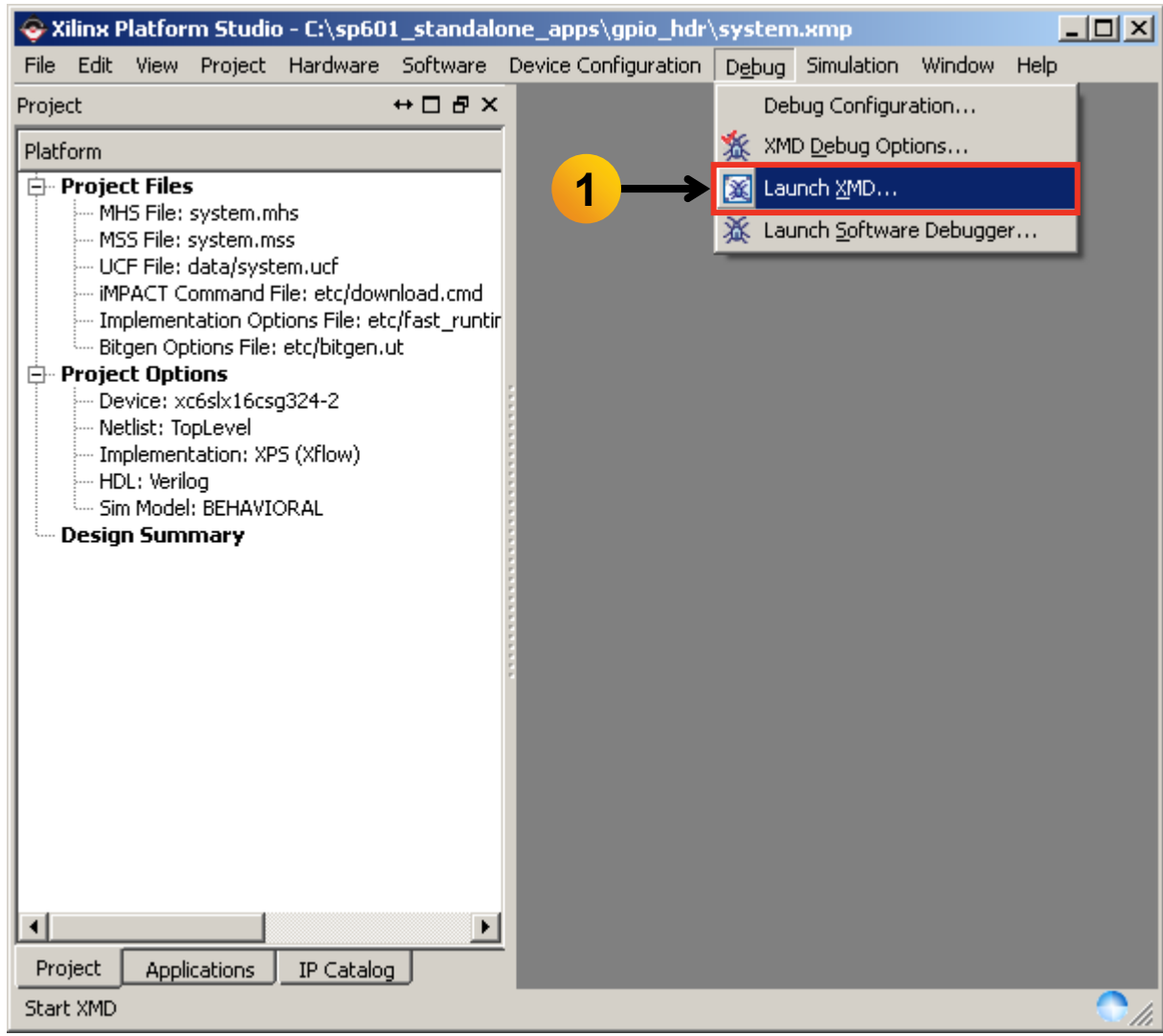
- **Download Bitstream**
  - Select **Device Configuration → Download Bitstream** (1)



Note: Presentation applies to the SP601

Download SP601 GPIO Header Loopback Design

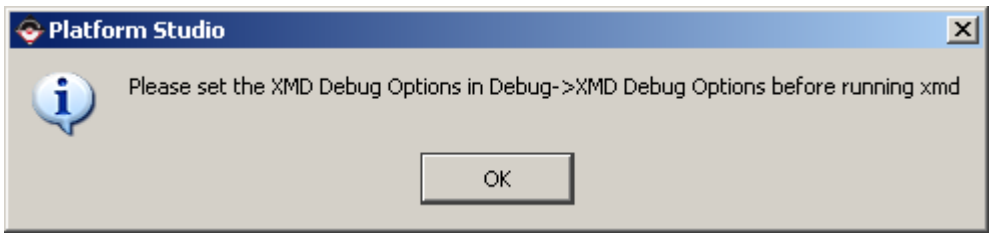
- **Download the System Monitor ELF with XMD**
  - Select **Debug** → **Launch XMD** (1)

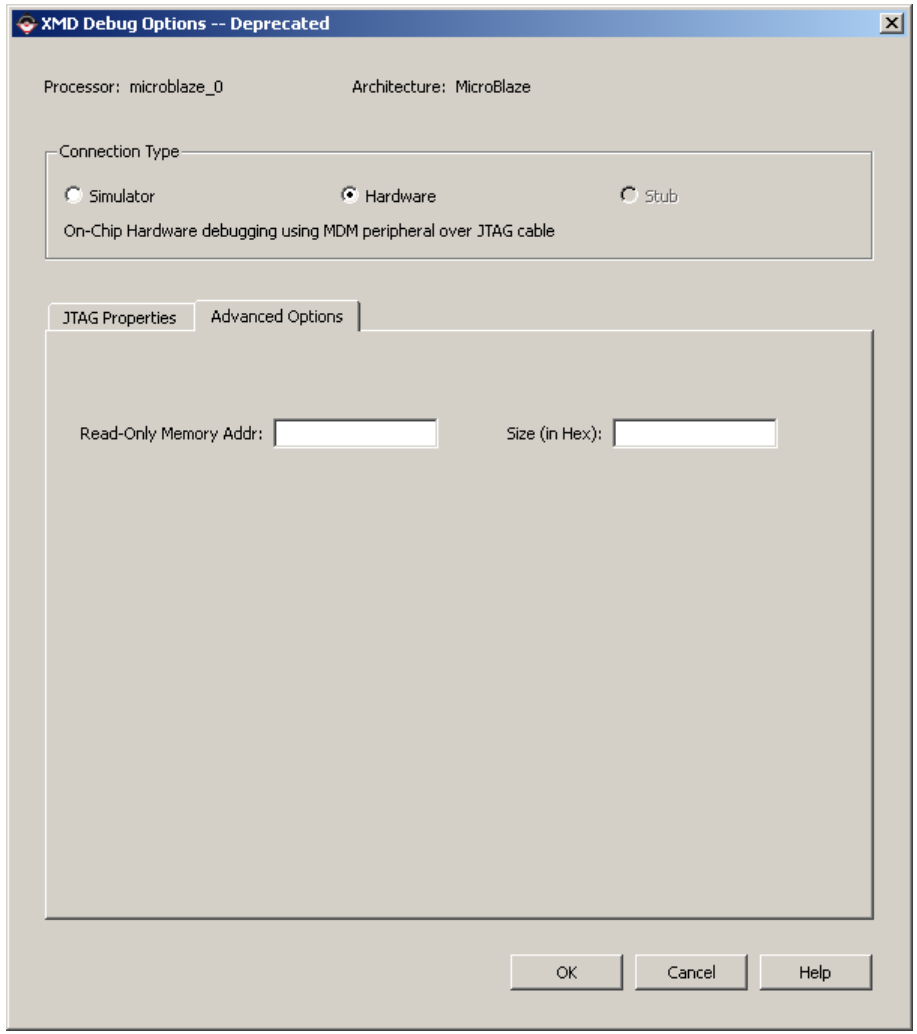


Note: Presentation applies to the SP601

Download SP601 GPIO Header Loopback Design

- The first time XMD runs on a project, the XMD Debug options must be set





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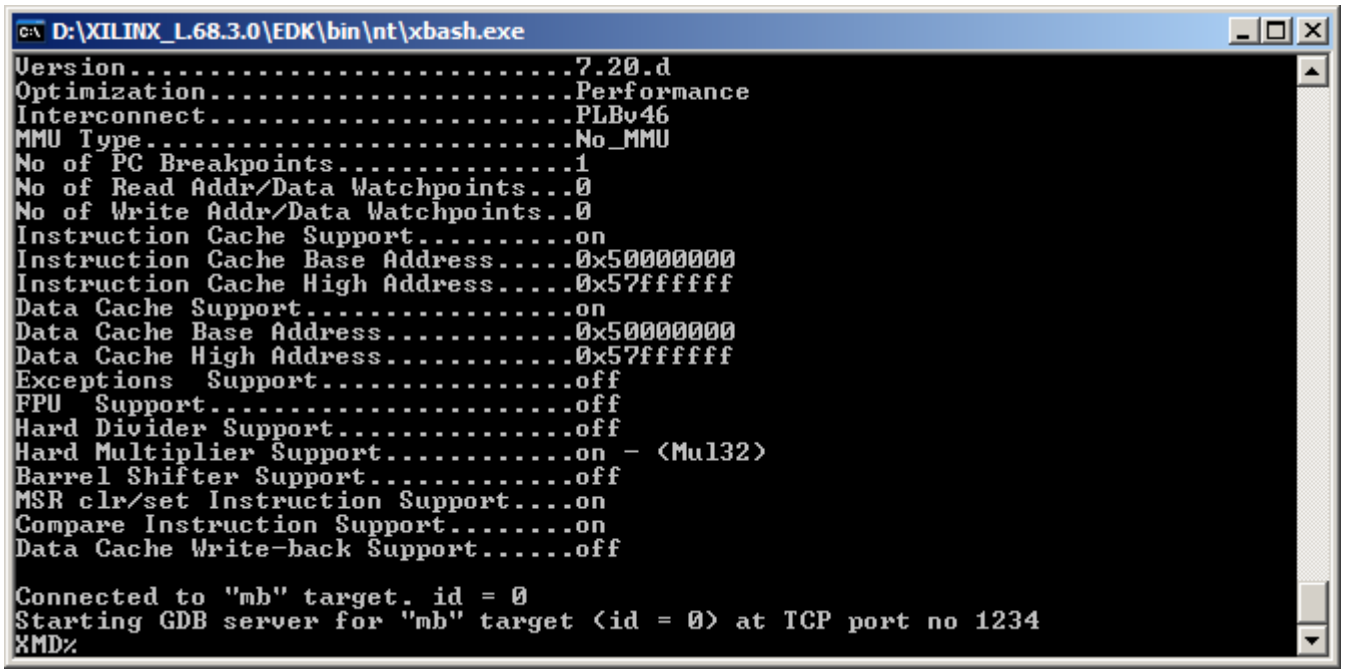
Download SP601 GPIO Header Loopback Design

- XMD opens and connects to the processor, using the default options



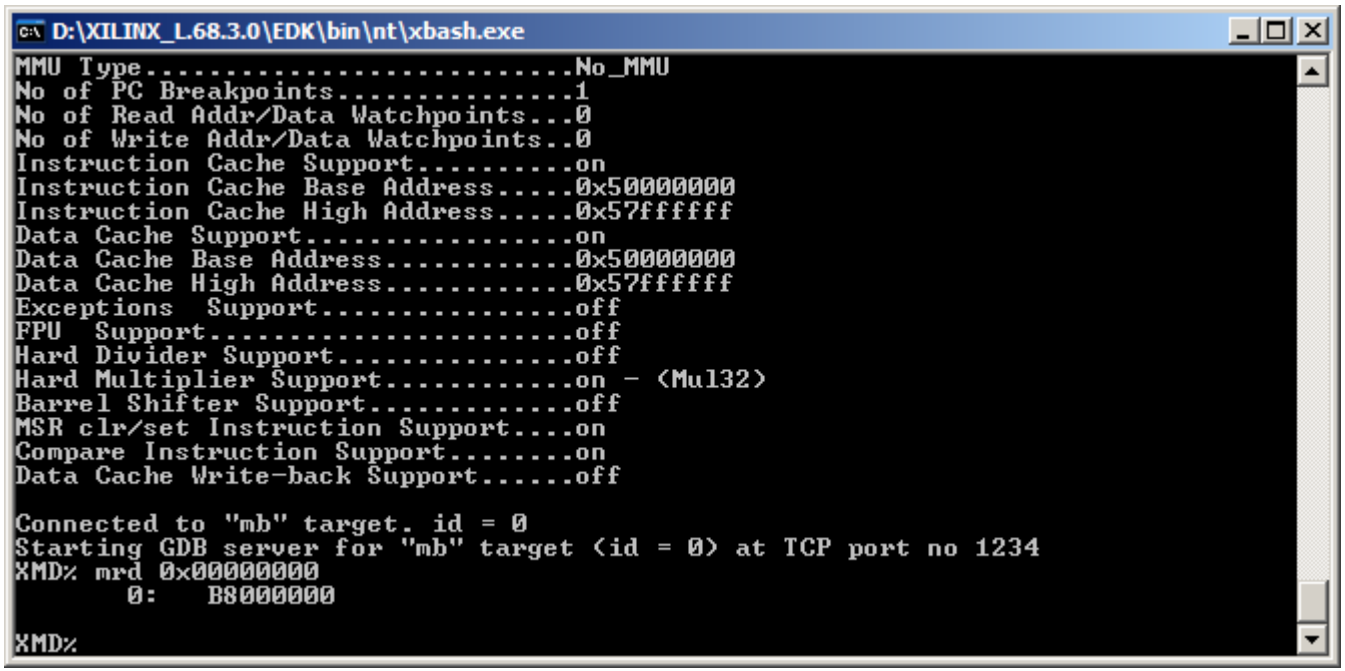
Note: Presentation applies to the SP601

Download SP601 GPIO Header Loopback Design

- To execute a memory read, type

  mrd 0x00000000

- This will read the memory address at the reset vector; the value should be 0xB8000000 as shown below



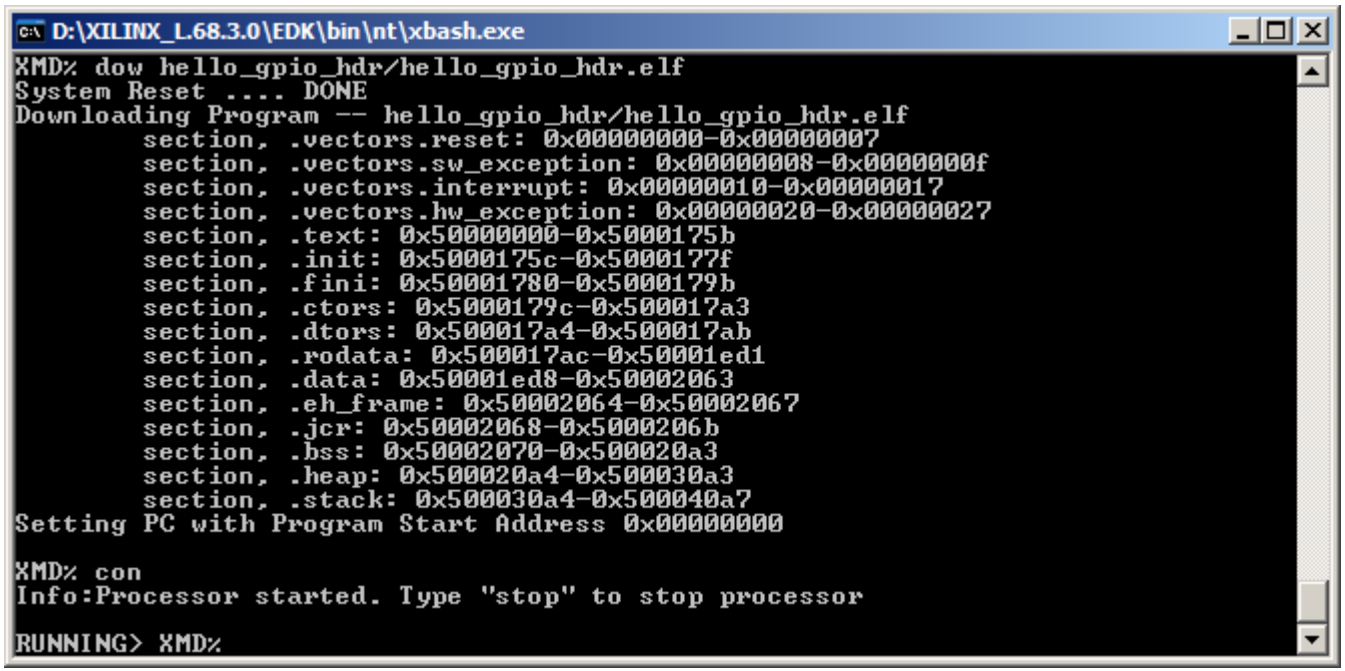
Note: Presentation applies to the SP601

Download SP601 GPIO Header Loopback Design

- **Download and run the System Monitor ELF file:**

  dow hello_gpio_hdr/hello_gpio_hdr.elf

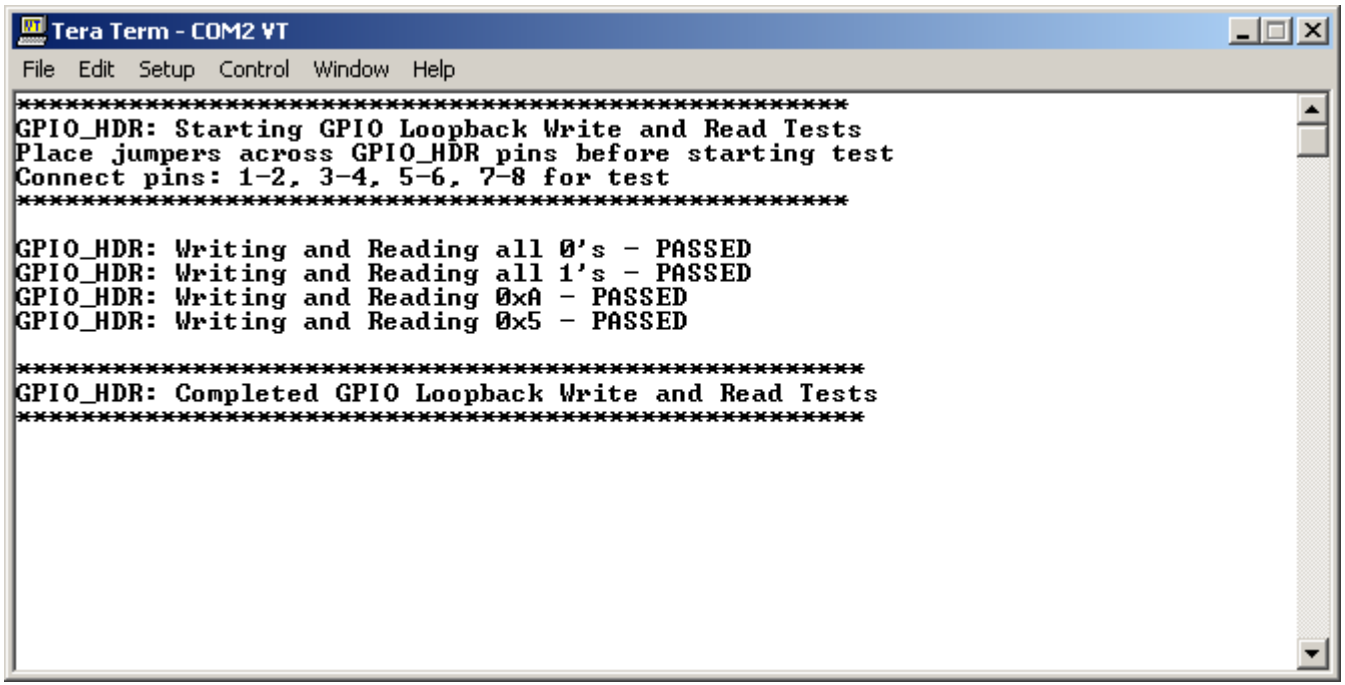
  con



Note: Presentation applies to the SP601

Download SP601 GPIO Header Loopback Design

- The test results will appear in the terminal window



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References

References

- **SP601 Documentation**
  - SP601 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf
- **Spartan-6**
  - Spartan-6 Family Overview
    http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf

Documentation

Documentation

- **Spartan-6**
  - Spartan-6 FPGA Family
    http://www.xilinx.com/products/spartan6/index.htm
- **SP601 Documentation**
  - Spartan-6 FPGA SP601 Evaluation Kit
    http://www.xilinx.com/products/devkits/EK-S6-SP601-G.htm
  - SP601 Getting Started Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug523.pdf
  - SP601 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug518.pdf
  - SP601 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug524.pdf