This document describes known issues for the Spartan®-6 FPGA SP601 printed-circuit board (PCB), Rev. C.

- There are no known issues on the SP601 PCB.
- Known issues related to Xilinx tools and IP as well as user assistance for the SP601 Evaluation Kit is provided in the SP601 Evaluation Kit Release Notes.
- The SP601 Rev. C boards are assembled with XC6SLX16-2CSG324CES devices. Therefore, the SP601 boards are affected by the silicon errata associated with Spartan-6 FPGA LX16 CES devices. Please consult EN113, Spartan-6 FPGA LX16 CES Errata document for more details.
- The SP601 boards were modified to comply with the Spartan-6 FPGA LX16 CES Errata related to $V_{CCINT}$ as noted in the “Operating Conditions Required when Using I/O Delay Variable Mode” section. As per the errata, the $V_{CCINT}$ regulator was adjusted to output 1.25V instead of a nominal 1.2V. This was achieved by changing R58 from 10K ohms to 9.09K ohms on all SP601 Rev. C boards assembled with CES Spartan-6 FGPA.

Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
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<tbody>
<tr>
<td>09/15/09</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
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