SP605 MIG Design Creation

December 2009

XTP060

Overview

- Spartan-6 Memory Controller Block
- Xilinx SP605 Board
- Software Requirements
- SP605 Setup
- Generate MIG Core
- Modifications to Example Design
- Compile Example Design
- ChipScope Pro Setup
- Run MIG
- References

Note: This presentation applies to the SP605

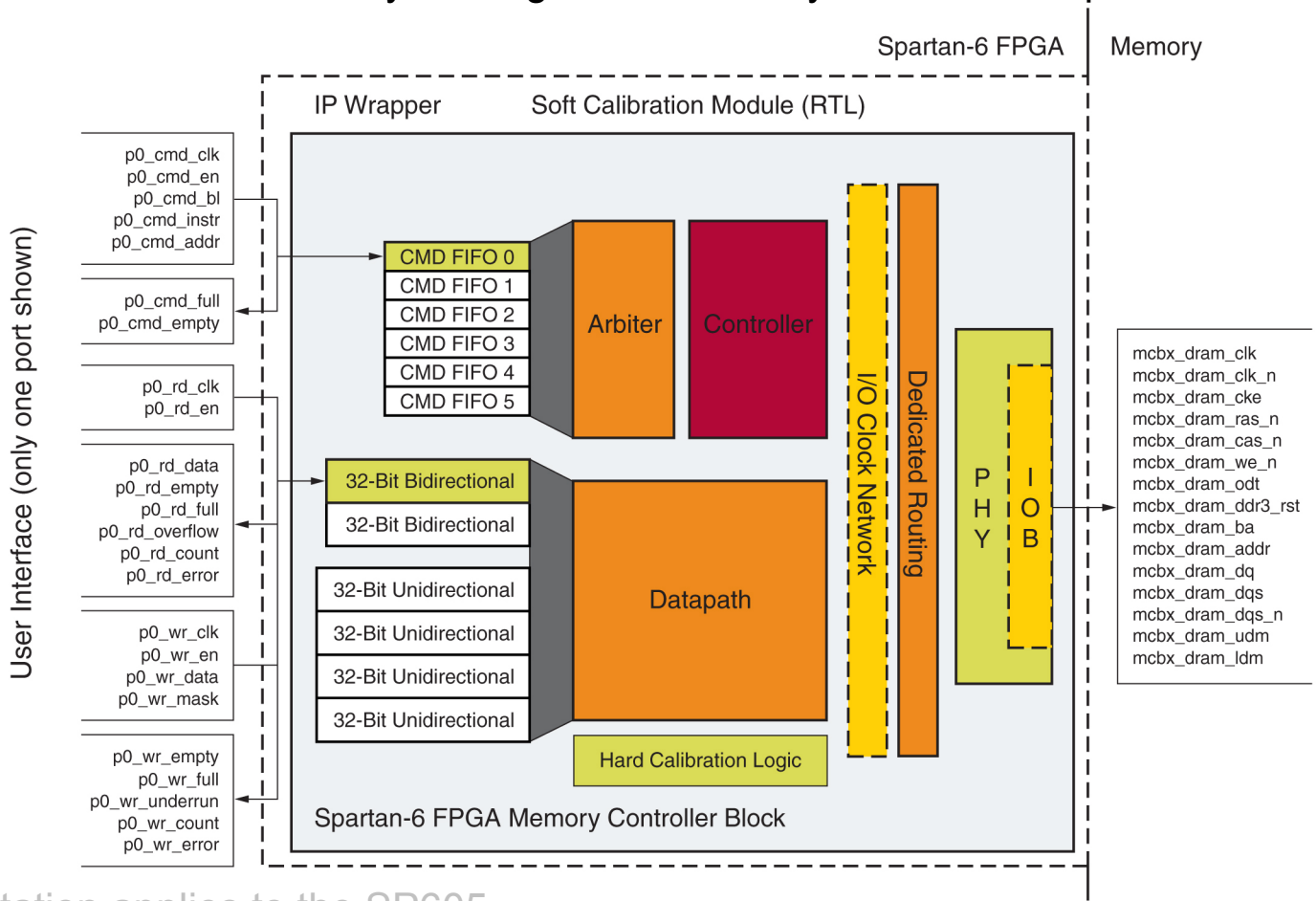
Spartan-6 Memory Controller Block

- **Dedicated Memory Controller Blocks (MCB) for Simplified DRAM interfaces**
  - Up to 4 MCB cores in a single Spartan-6 device
  - Embedded controller and physical (PHY) interface
  - Supports 4-bit, 8-bit, or 16-bit single component memory
  - Memory densities up to 4 Gbit
- **Performance up to 800 Mb/s (400 MHz double data rate)**
- **Configurable dedicated Multi-port user interface to FPGA logic**
  - 1 to 6 ports per MCB depending on configuration
  - Internal 32-, 64-, or 128-bit data bus options

Note: Presentation applies to the SP605

MCB Block Diagram

- **Simple User Interface abstracts away complexity of memory transactions**
- **MIG / EDK wrapper delivers complete interface solution**
  - Internal block assembly and signal connectivity is made transparent to the user



Note: Presentation applies to the SP605

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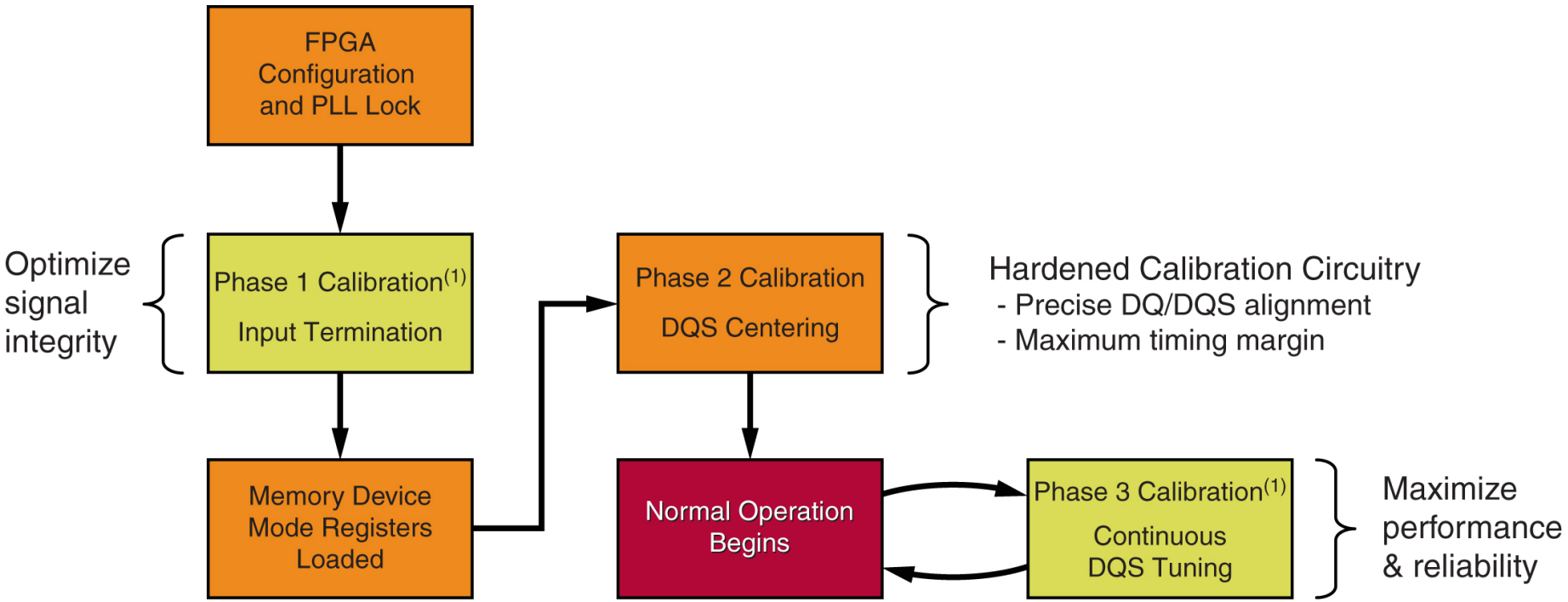
Memory Controller Block Startup

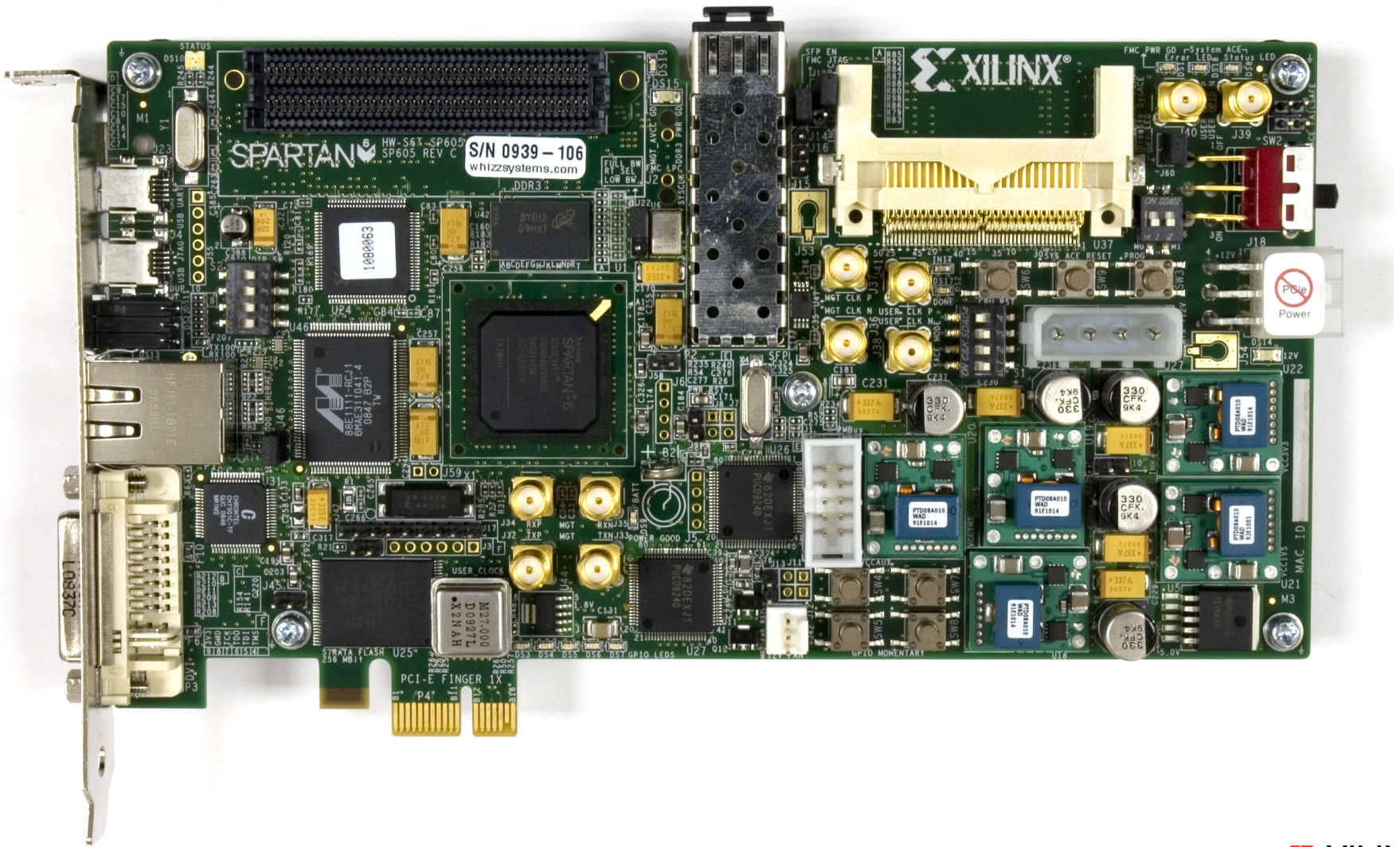


1. Phase 1 & 3 of calibration are controlled by a **soft module** – enabled by MIG or EDK

***Automatic* memory configuration and controller calibration**

Note: Presentation applies to the SP605

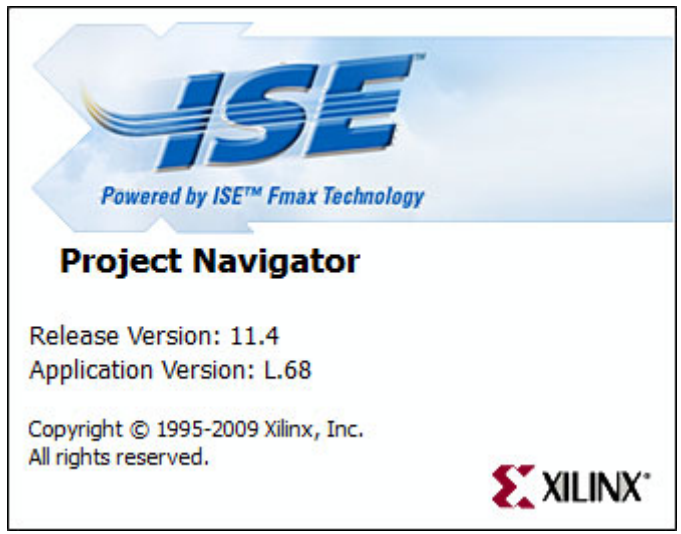
Xilinx SP605 Board



Note: Presentation applies to the SP605

ISE Software Requirement

- Xilinx ISE 11.4 software



Note: Presentation applies to the SP605

ChipScope Pro Software Requirement

- **Xilinx ChipScope Pro 11.4 software**

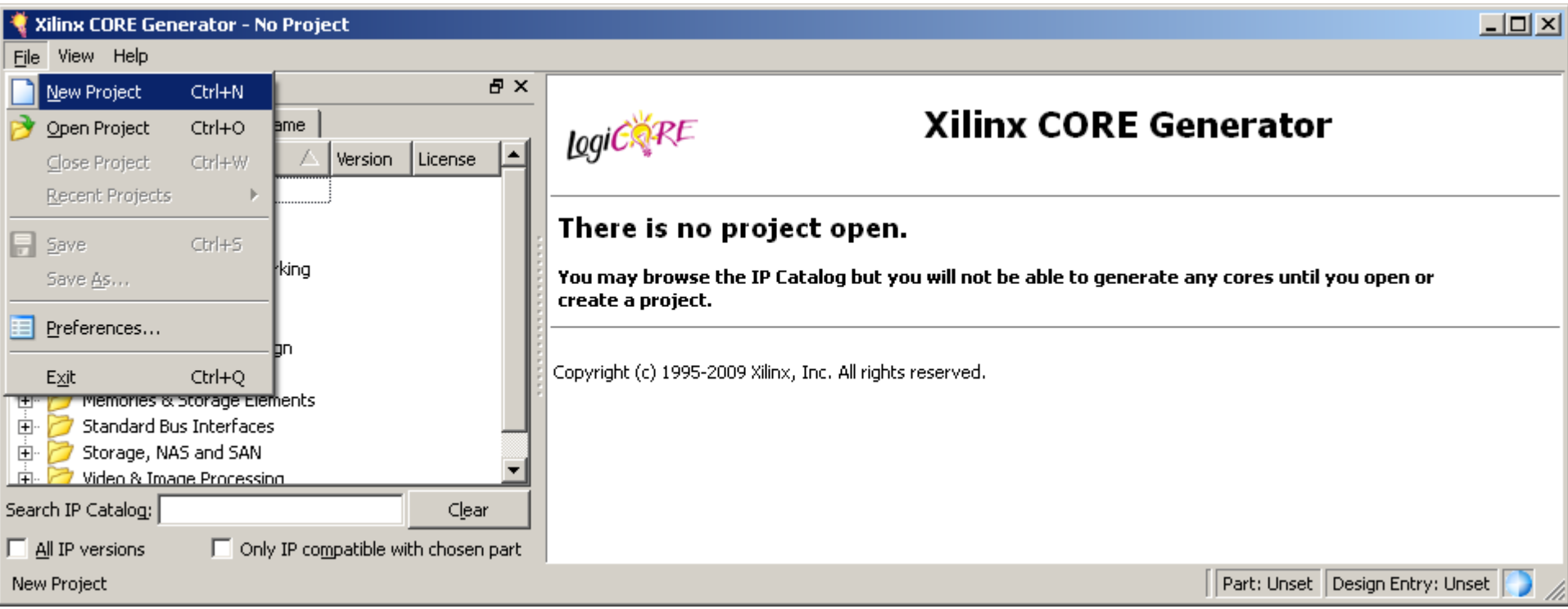
Note: Presentation applies to the SP605

Generate MIG Example Design

- **Open the CORE Generator**

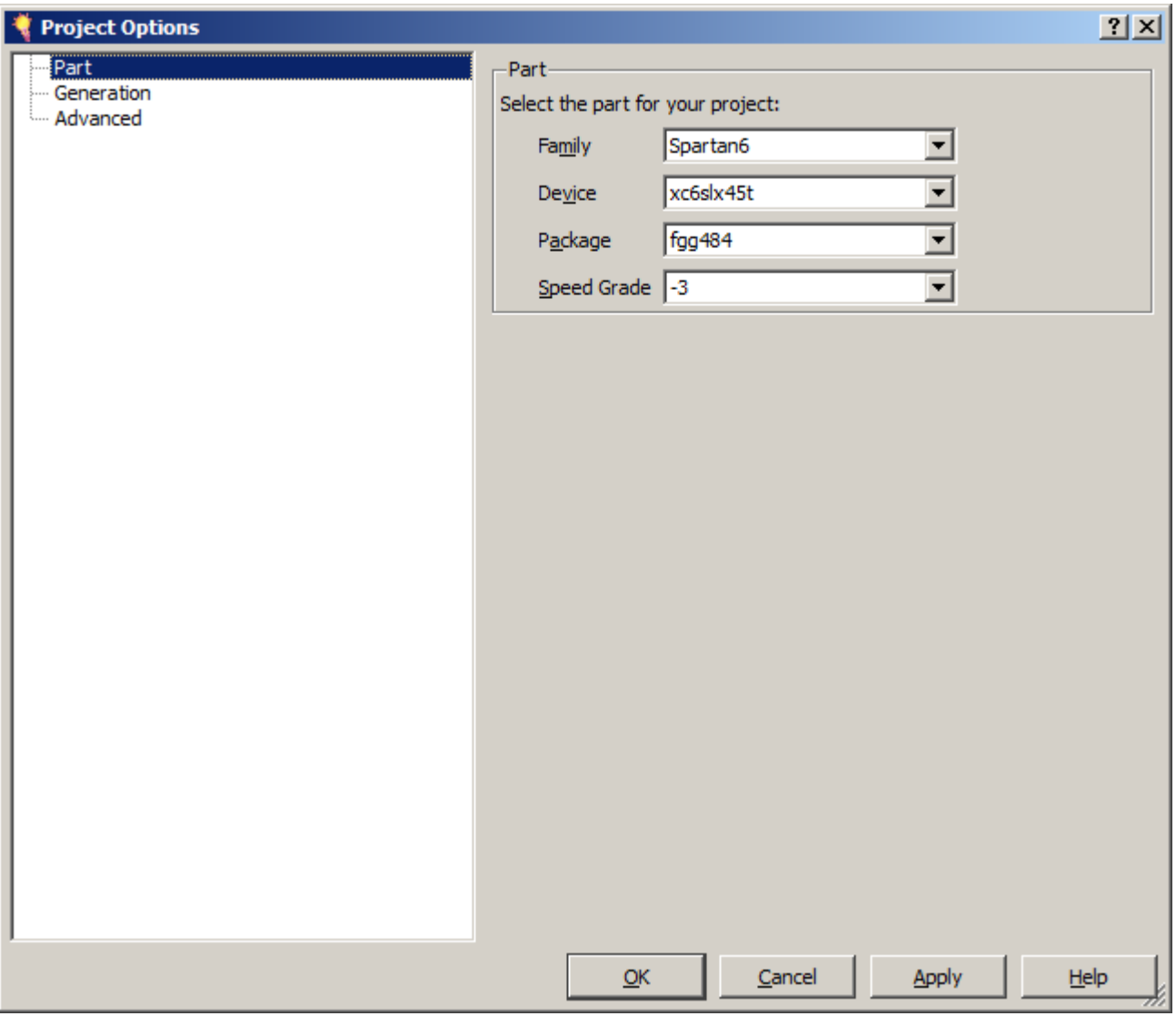
  Start → All Programs → Xilinx ISE Design Suite 11 → ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**



Note: Presentation applies to the SP605

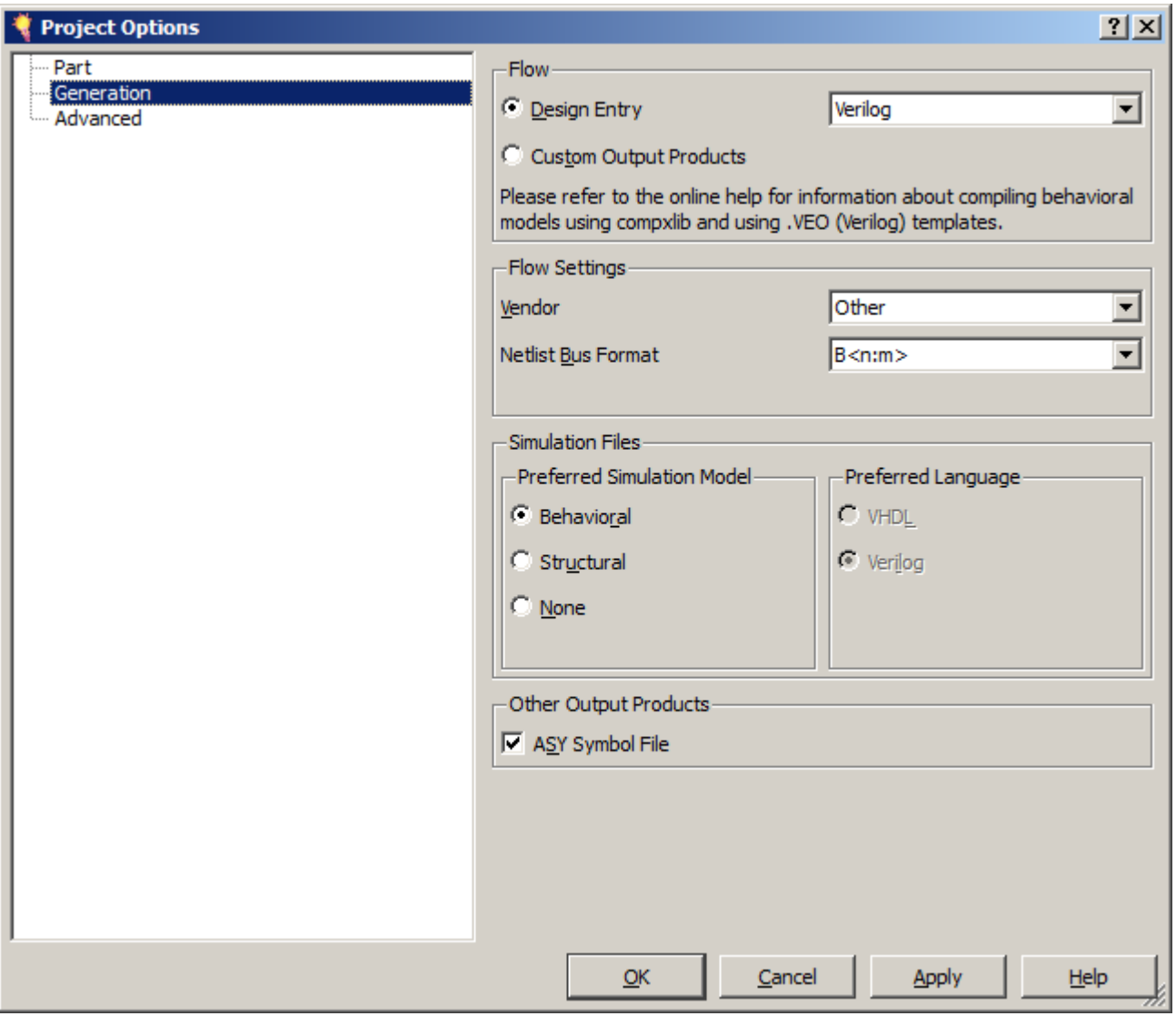
Generate MIG Example Design



- Create a project directory: sp605_mig_design
- Name the project: sp605_mig_design.cgp
- Set the Part (as shipped on the SP605):
  - Family: Spartan6
  - Device: xc6slx45t
  - Package: fgg484
  - Speed Grade: -3

Note: Presentation applies to the SP605

Generate MIG Example Design



- Select Generation
- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the SP605

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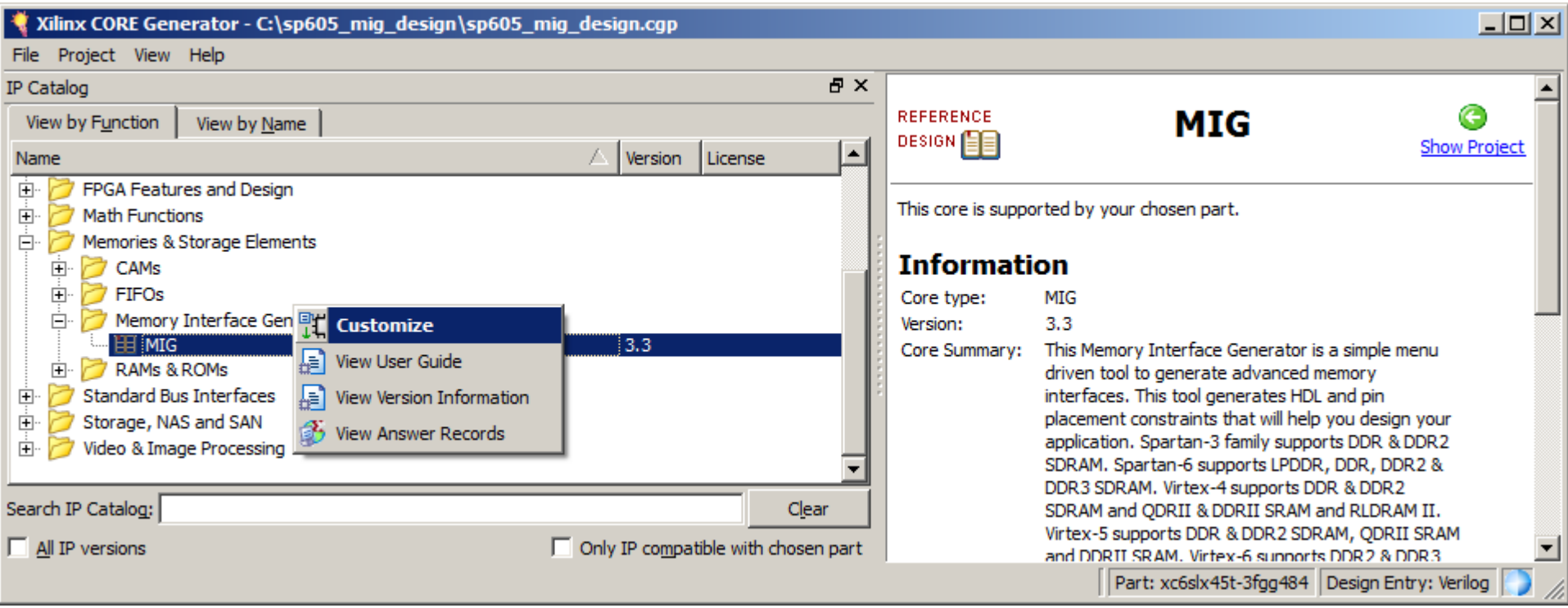
Generate MIG Example Design

- **Right click on MIG Version 3.3**
  - Select **Customize**



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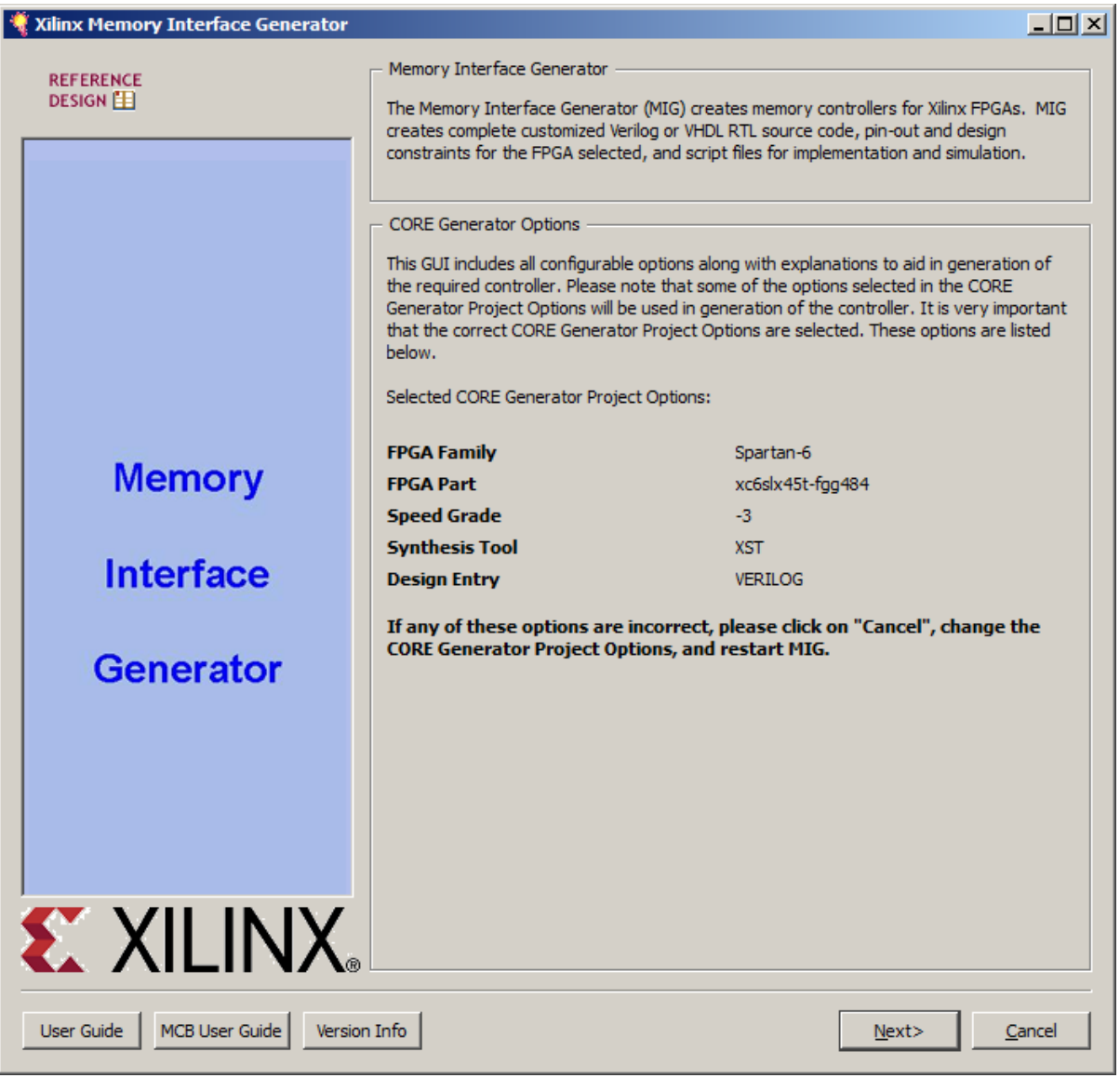
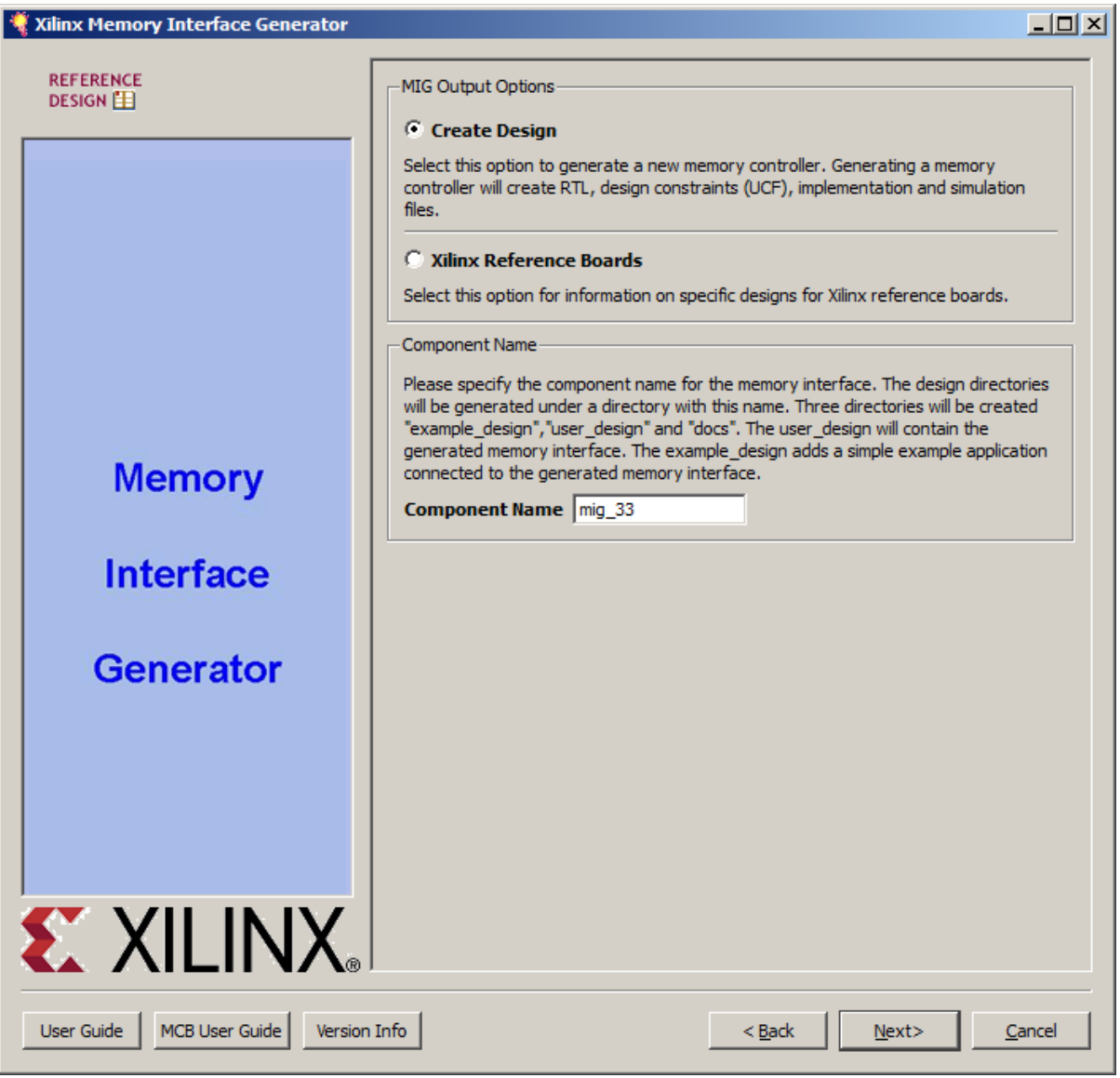
Generate MIG Example Design



- **Leave this page as is**
  - Click Next

Generate MIG Example Design



- **Leave this page as is**
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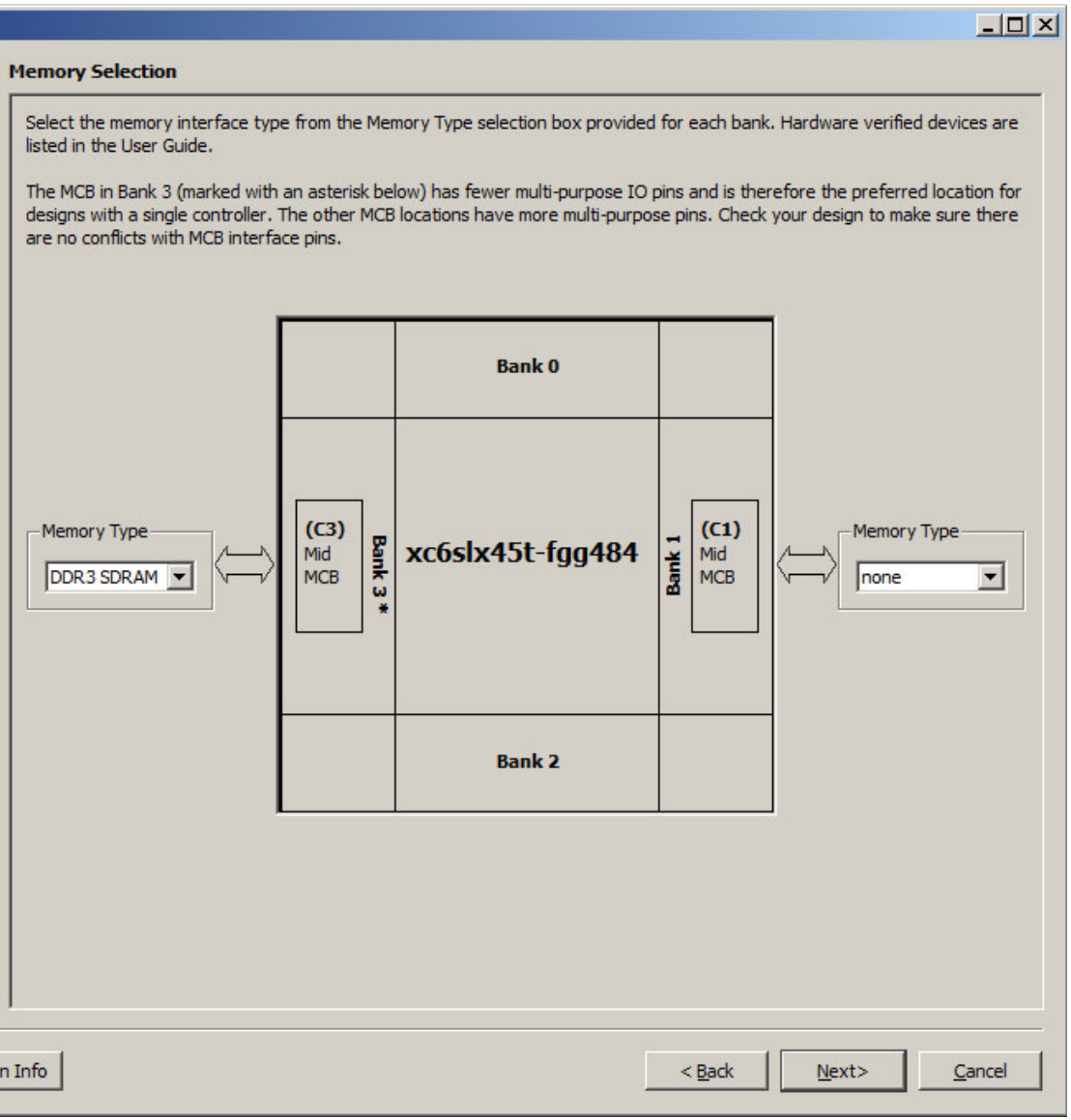
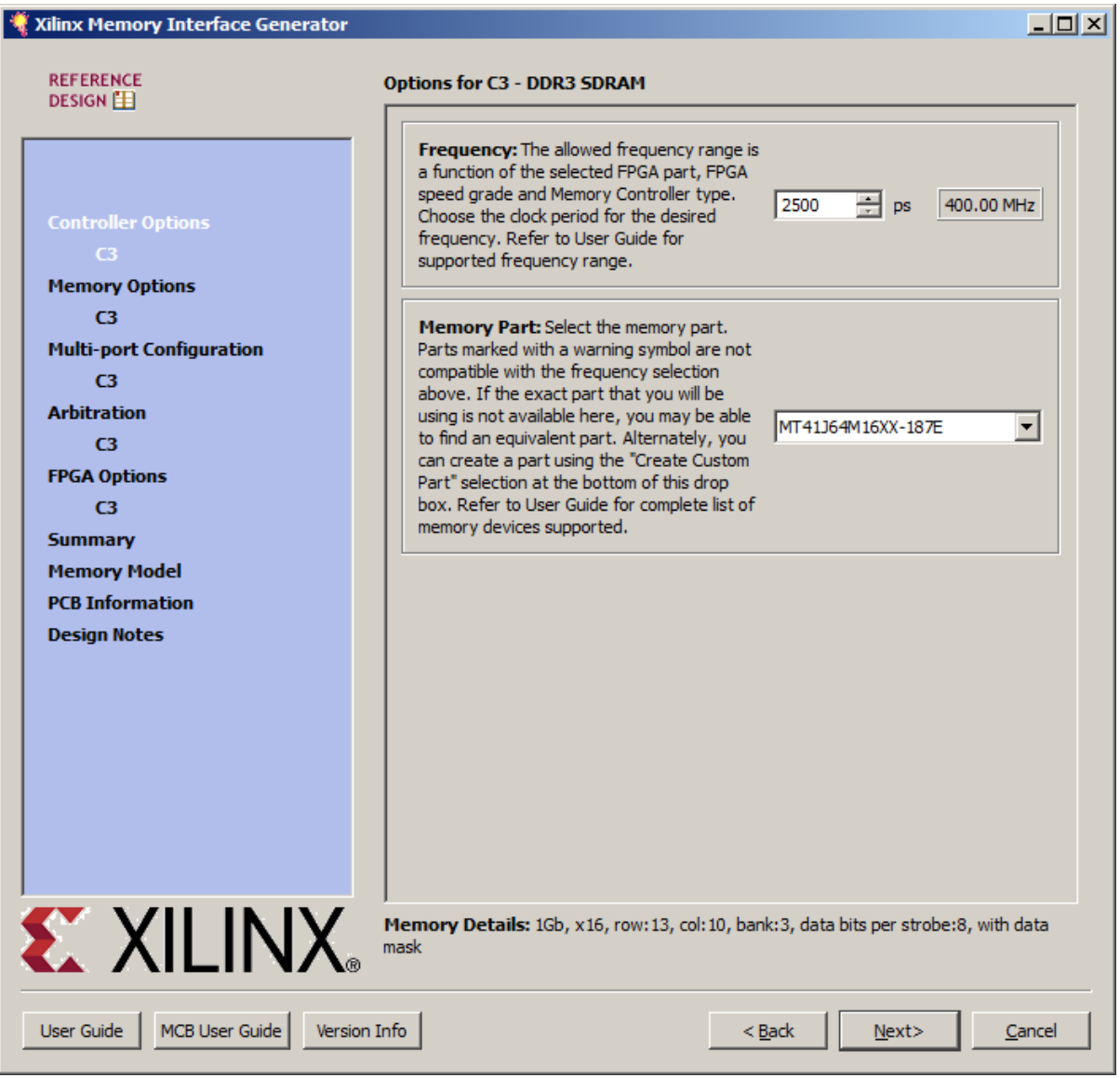
Generate MIG Example Design



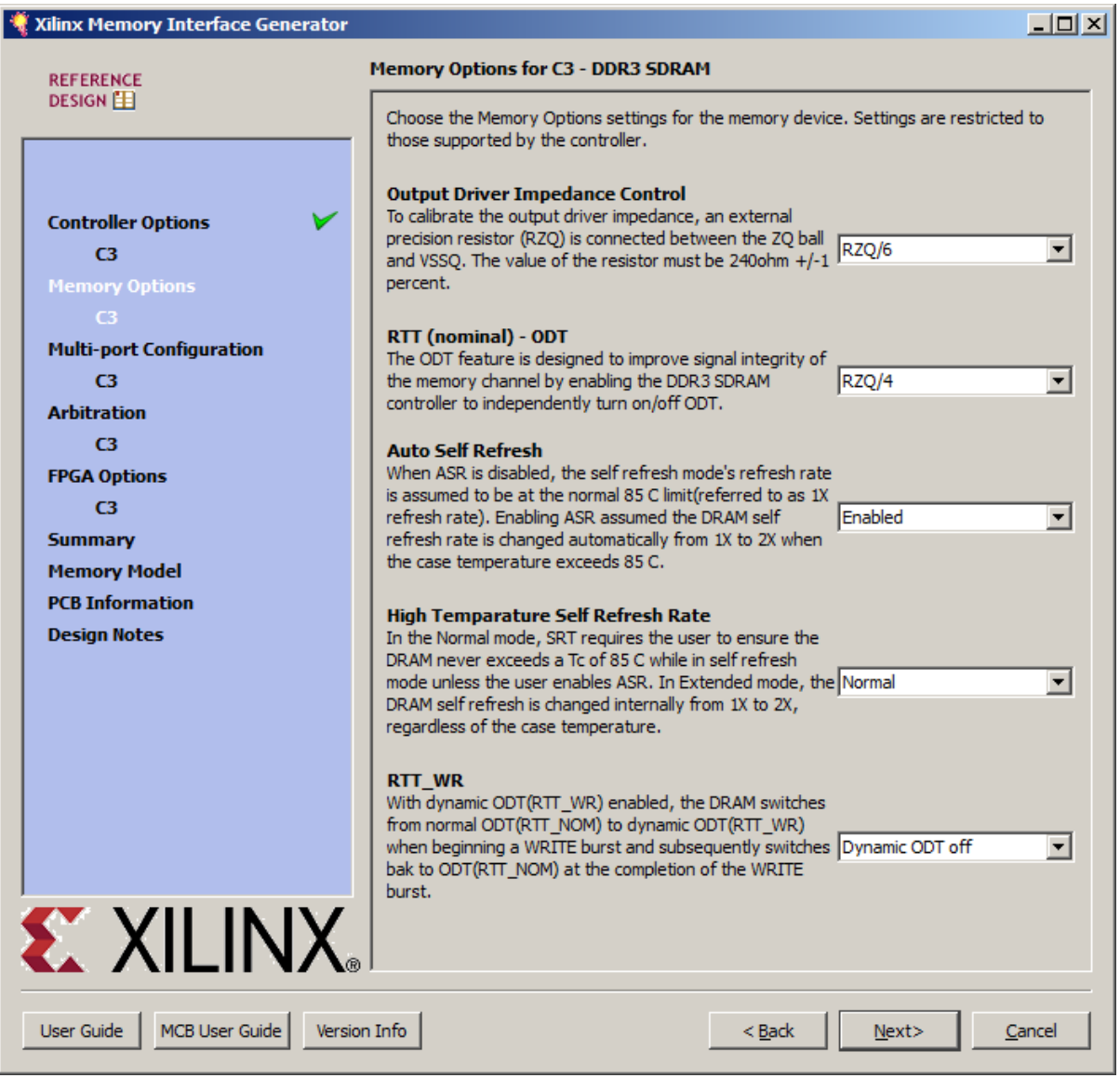
- **Select**
  - Bank 3 Middle MCB
- **Select Memory Type**
  - DDR3 SDRAM
  - Click Next

Generate MIG Example Design



- Set the Memory part to MT41J64M16XX-187E

Generate MIG Example Design



- **Leave this page as is**
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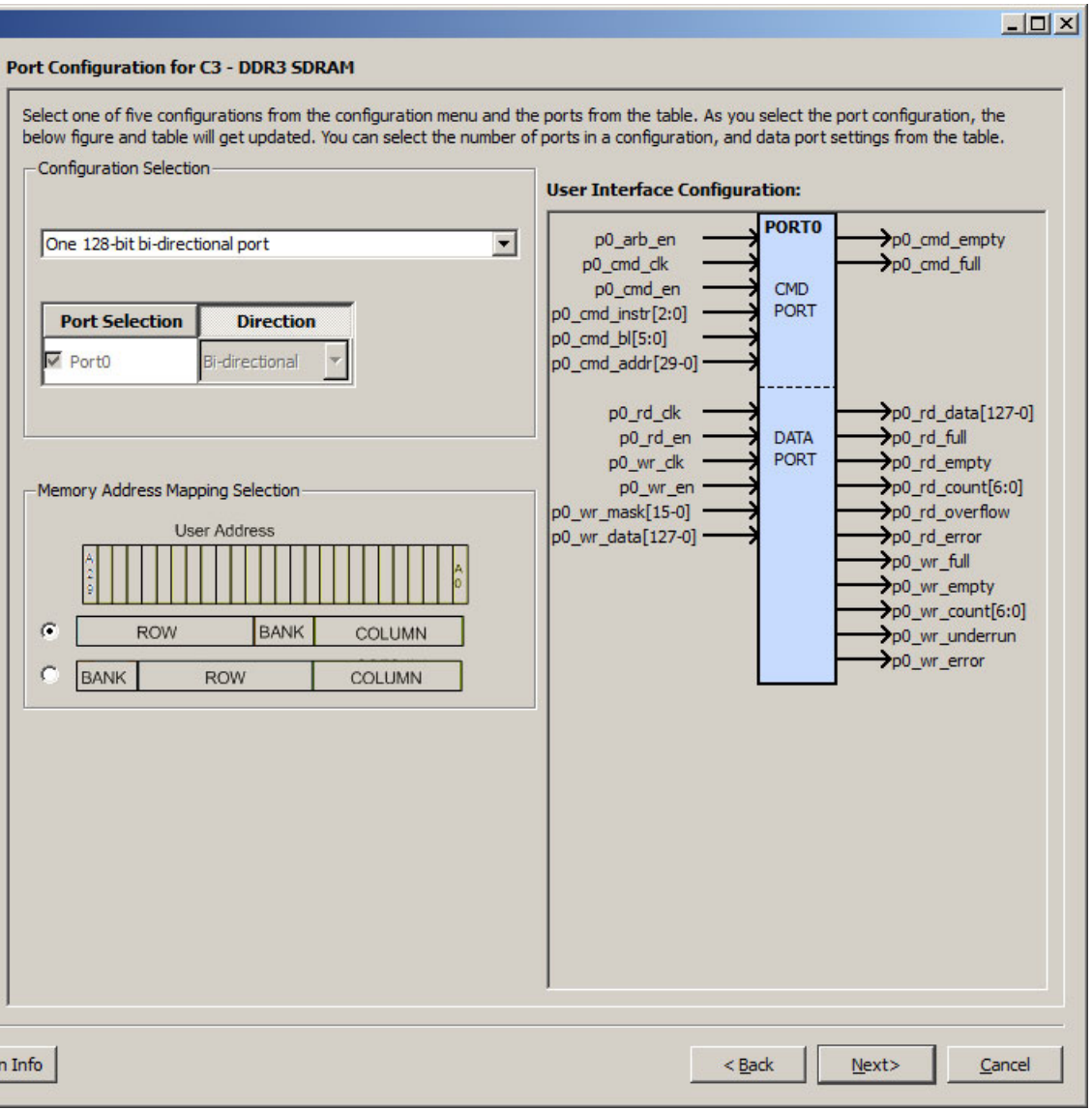
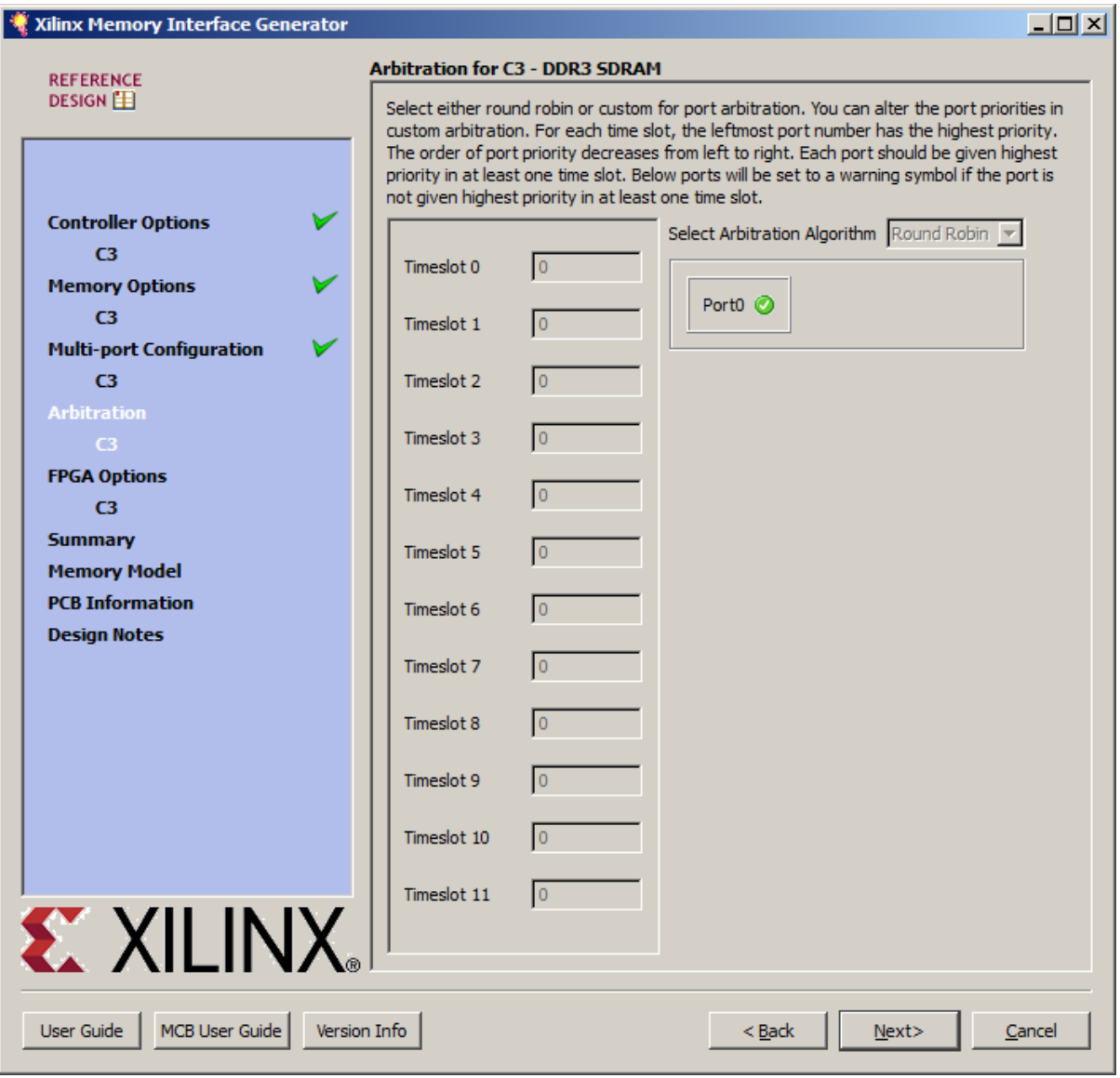
Generate MIG Example Design



- **Select**
  - One 128-bit bi-directional Port

Generate MIG Example Design



- **Leave this page as is**
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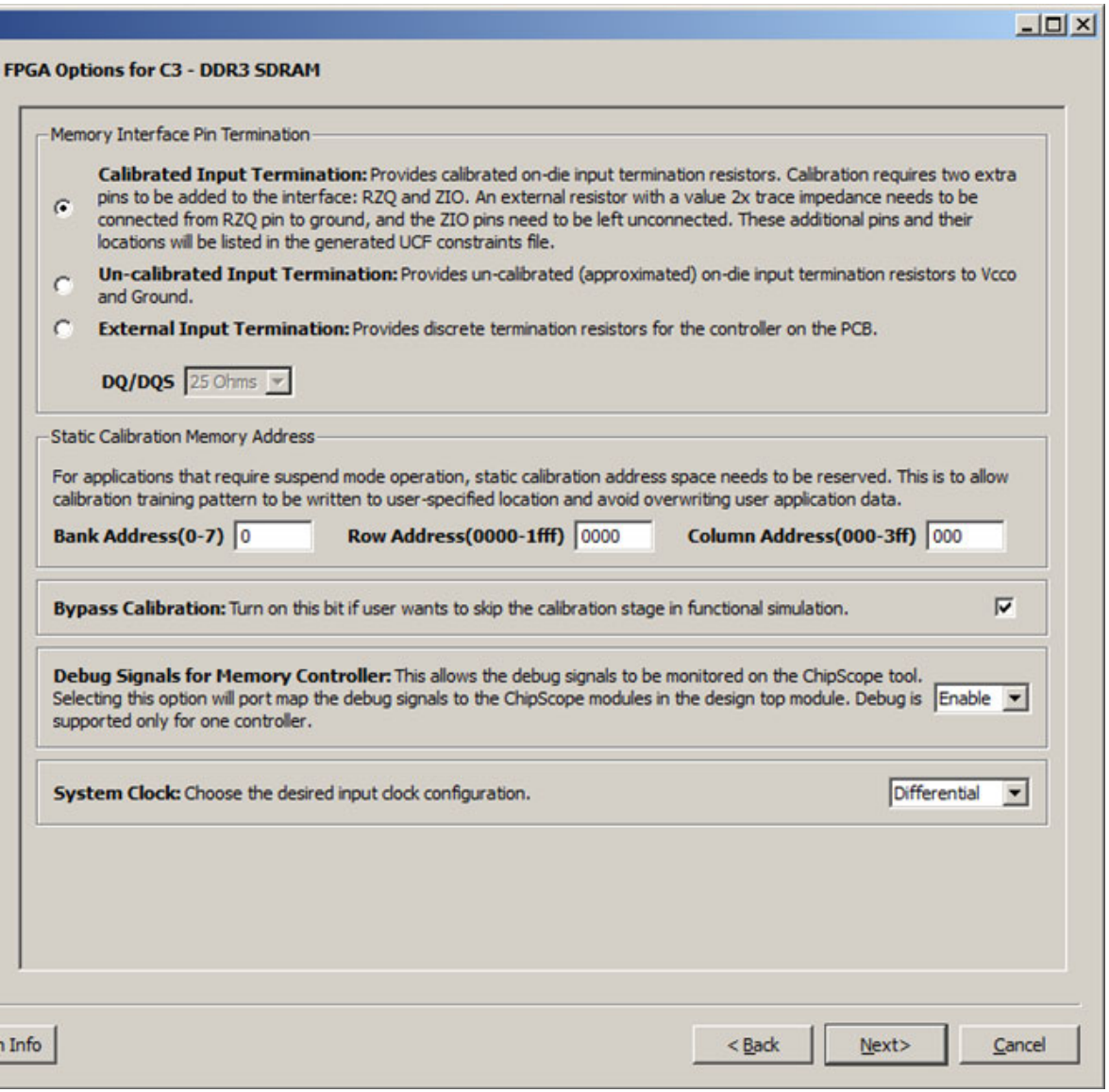
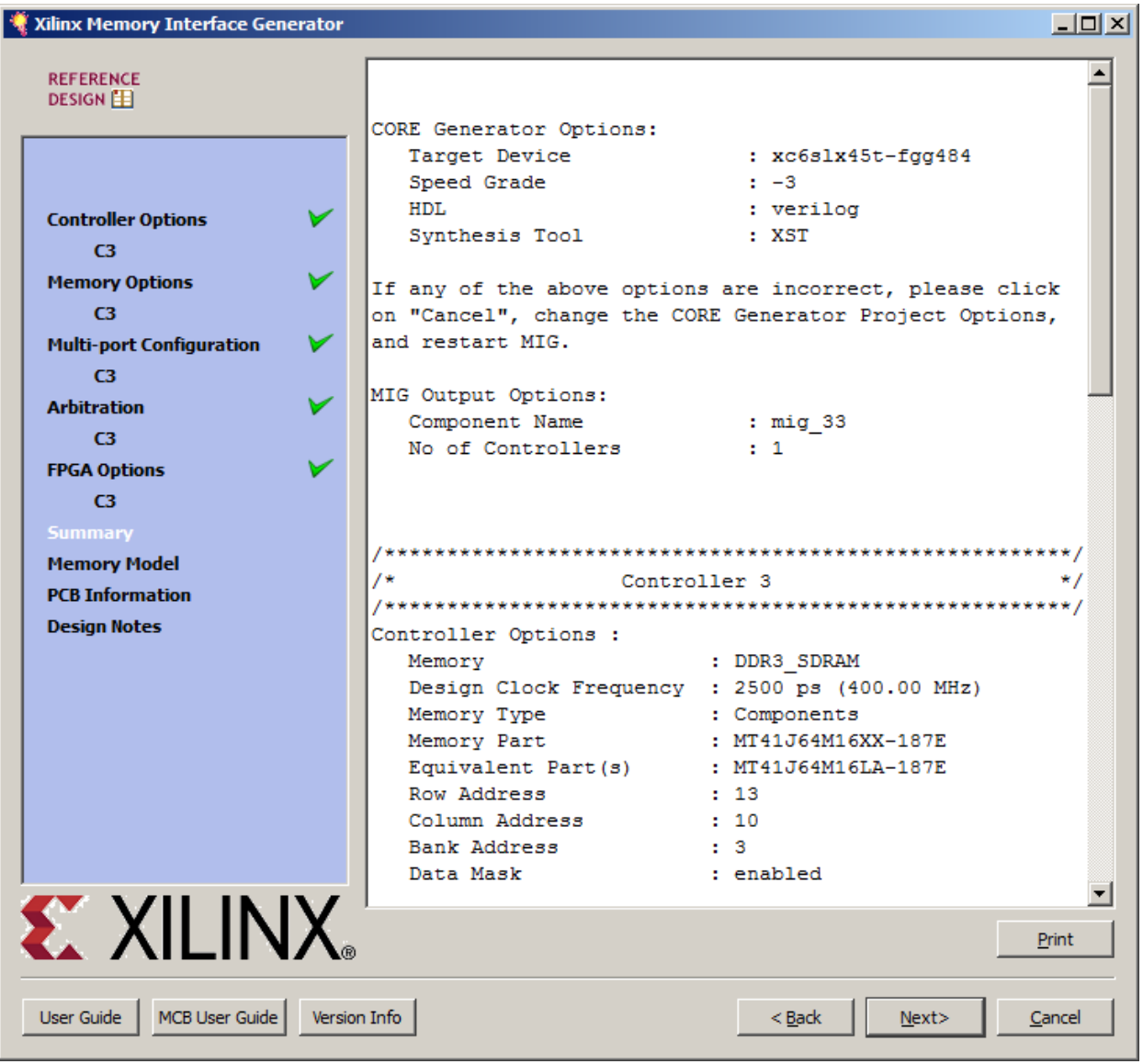
Generate MIG Example Design



- **Set DQ/DQS**
  - 50 Ohms
  - This sets the design to uncalibrated 50 Ohm termination on DQ/DQS inputs
- **Set Debug Signals**
  - Enable

Generate MIG Example Design



- **Leave this page as is**
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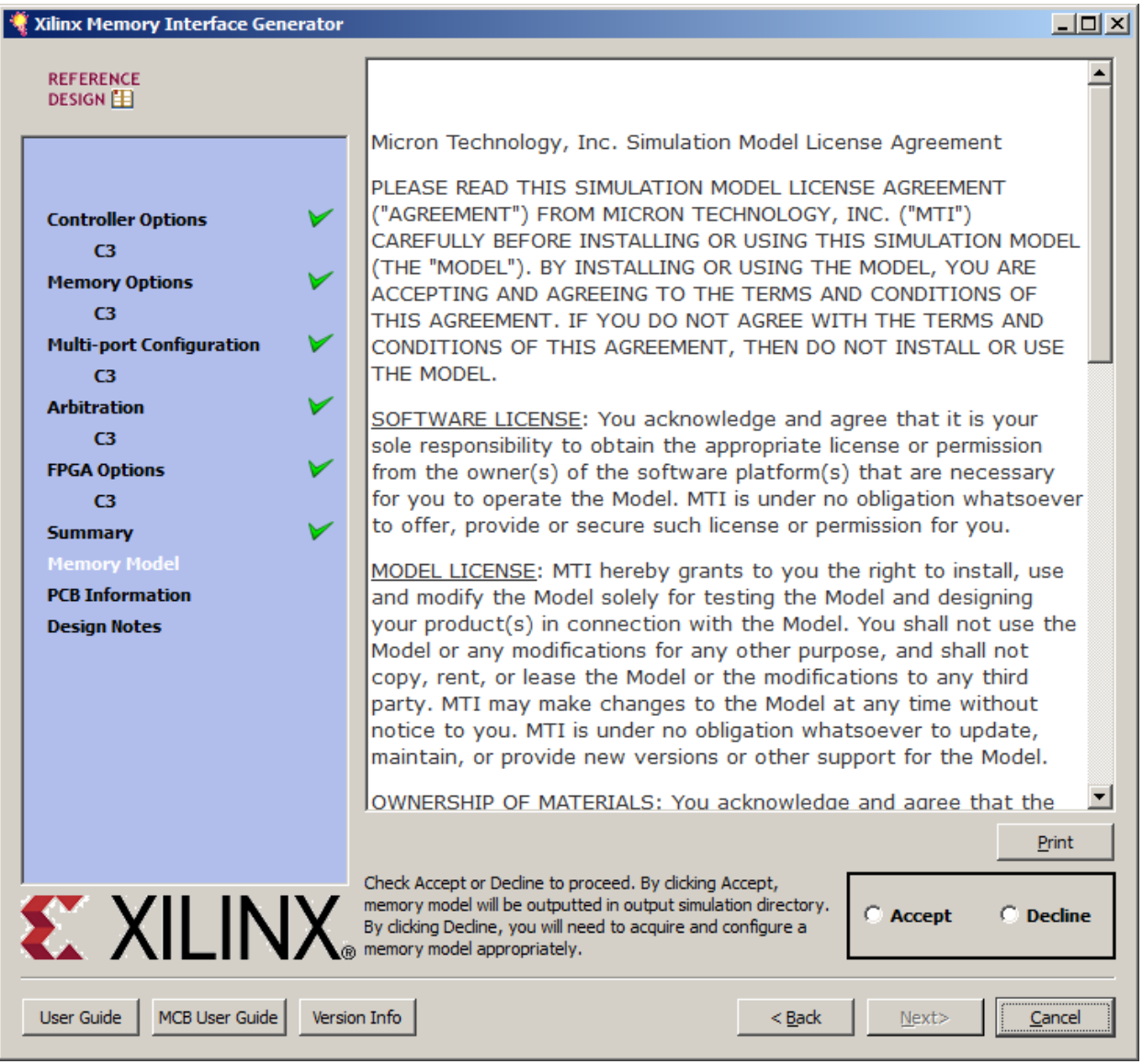
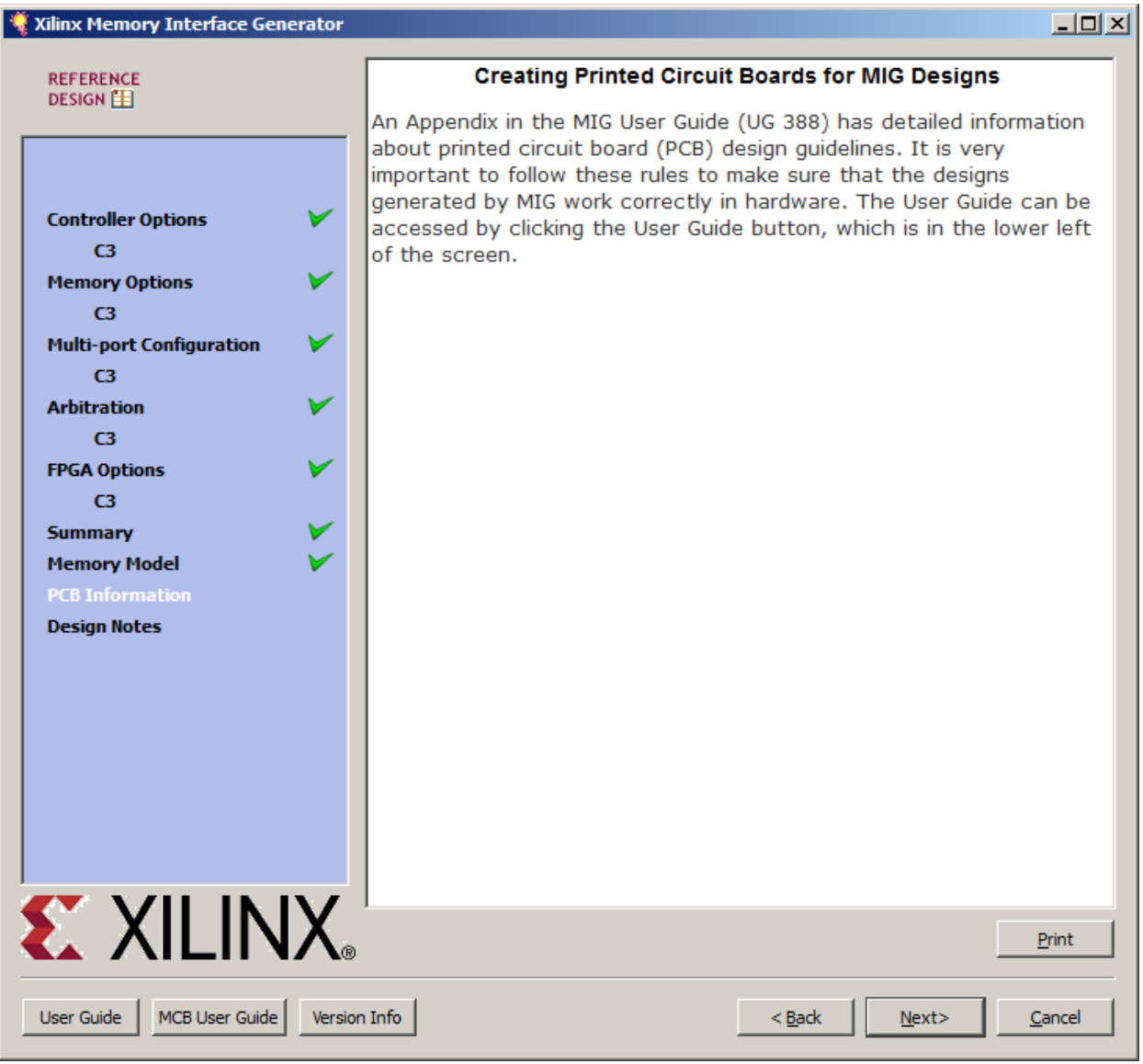
Generate MIG Example Design



- **Accept Simulation license, if desired**
  - Otherwise, Decline license
  - Click Next

Generate MIG Example Design



- **Leave this page as is**
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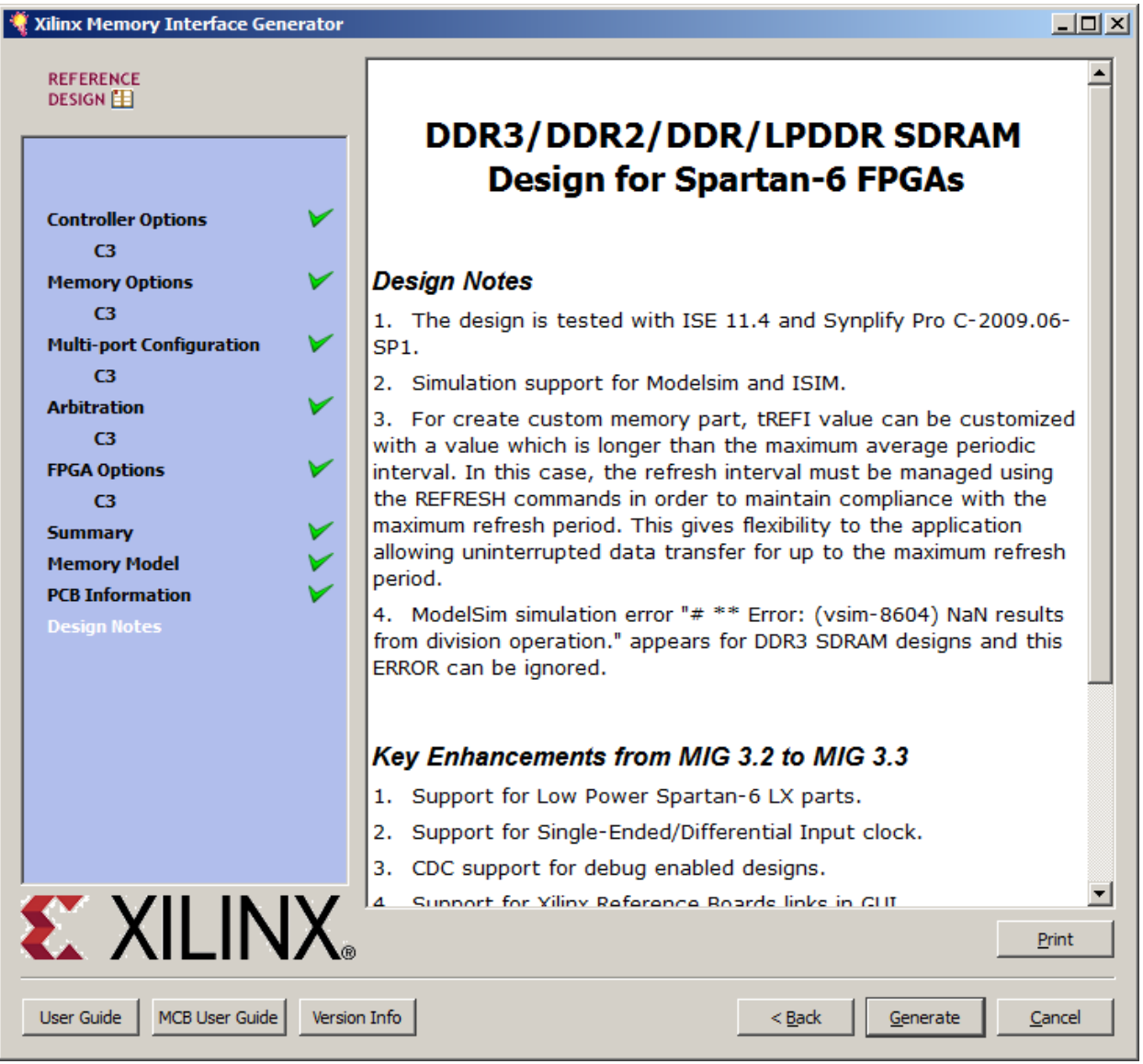
XILINX

Generate MIG Example Design



- Click Generate

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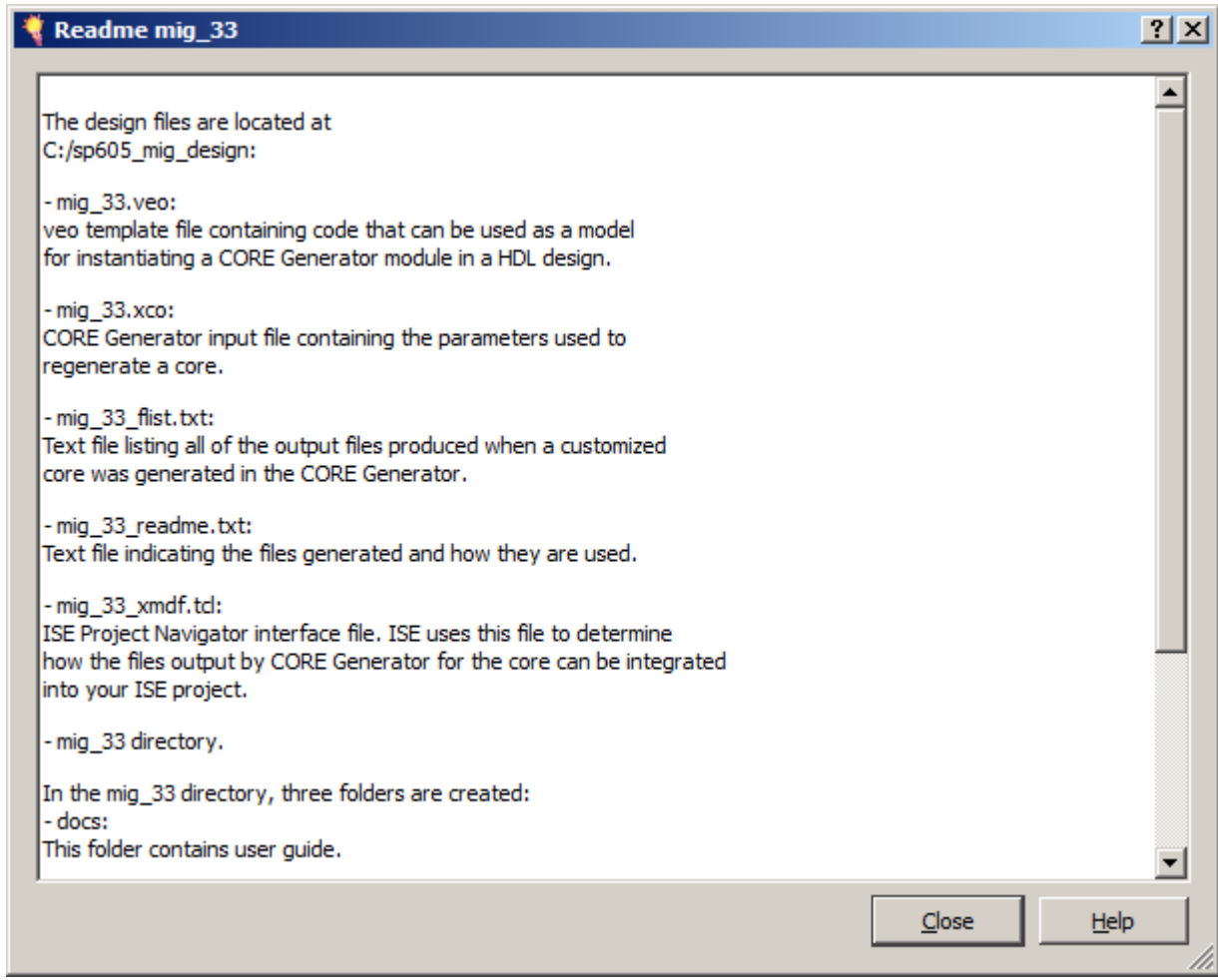
Generate MIG Example Design

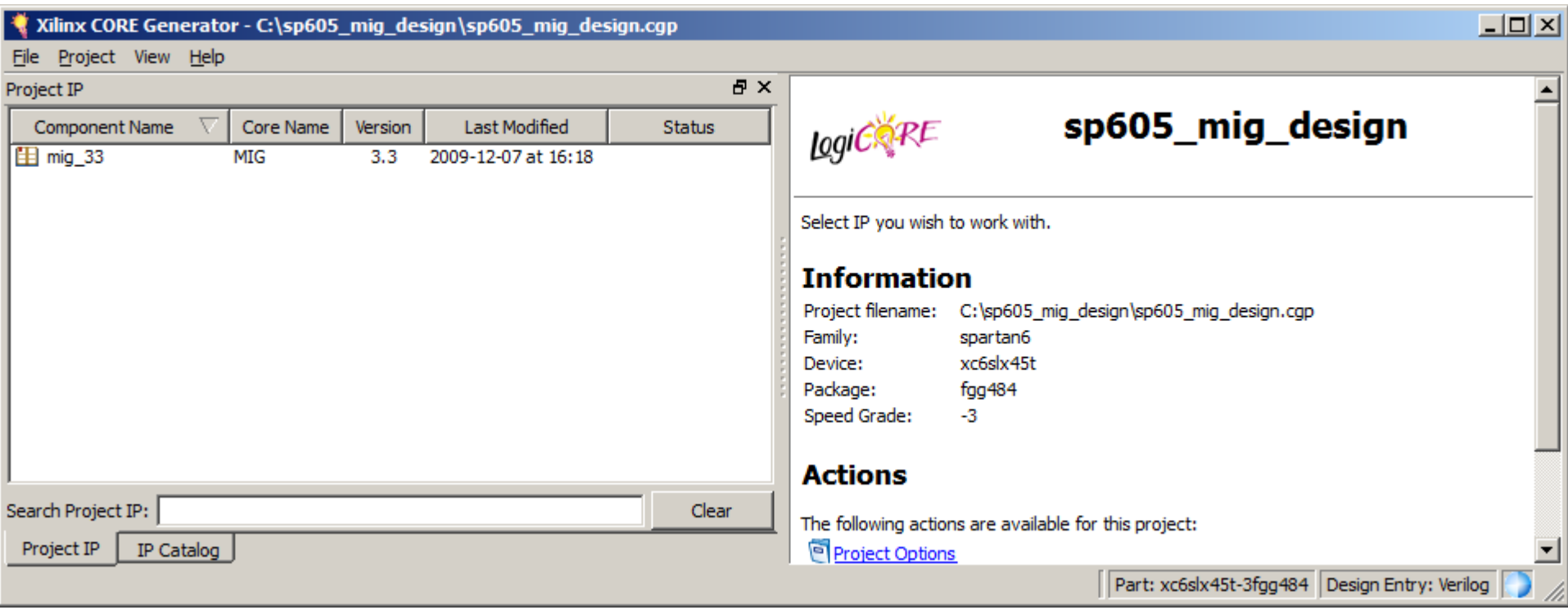
- After the MIG core finishes generating, click Close on the Datasheet window



Note: Presentation applies to the SP605

Generate MIG Example Design

- MIG design appears in Project IP



Note: Presentation applies to the SP605

Modifications to Example Design

- **RDF0029 includes**
  - ChipScope Project File, UCF, Verilog Files, and pre-built Example Design files
- **Modifications to RTL Files for SP605 Example Design**
  - Added GPIO outputs for visual status indicators with heartbeat clock
    - GPIO LED 3 = Calibration done
    - GPIO LED 2 = PLL locked
    - GPIO LED 1 = Error
    - GPIO LED 0 = Heartbeat (blinking)
  - Change CLKFBOUT_MULT to "4" to generate proper clocks:
    - MCB block runs at 800 MHz
    - Traffic Generator runs at 50 MHz
    - Soft calibration clock runs at 100 MHz

Note: Presentation applies to the SP605

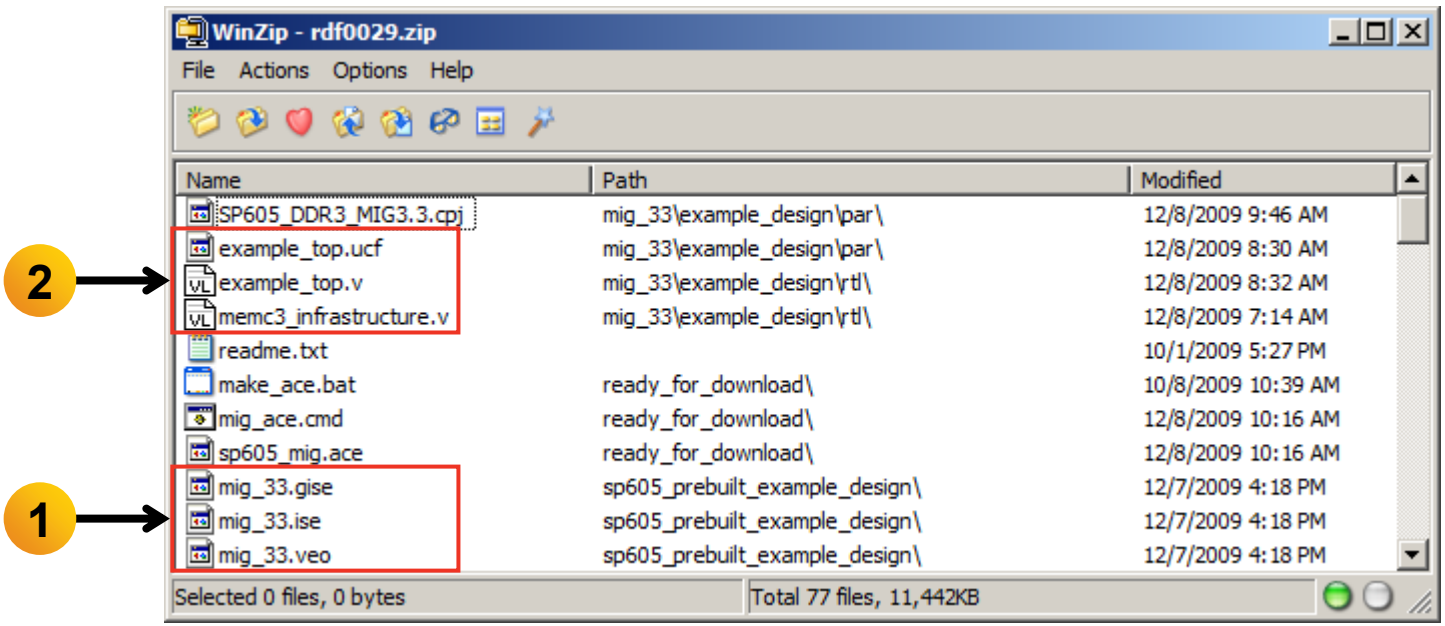
Modifications to Example Design

- **Updates to UCF file specifically required for SP605 board:**
  - Changed LOC of 200MHz differential sys_clk inputs
  - Changed LOC of sys_rst_n input to SP605 CPU_RESET switch
  - Added LOC for GPIO LED signals (2.5V bank voltage)
  - Double sys_clk_ibufg period constraint from 2.5ns to 5ns

Note: Presentation applies to the SP605

Modifications to Example Design

- **Unzip the rdf0029.zip file to your C:\sp605_mig_design directory**
  - This adds modifications to the example design
  - A fully pre-built SP605 example design is included in the zip file (1)
    - Use the included bitstream to run MIG with ChipScope
    - Run **ise_flow.bat** in <design directory>\sp605_pre-built_example_design\mig_33\example_design\par to recompile the pre-built example design



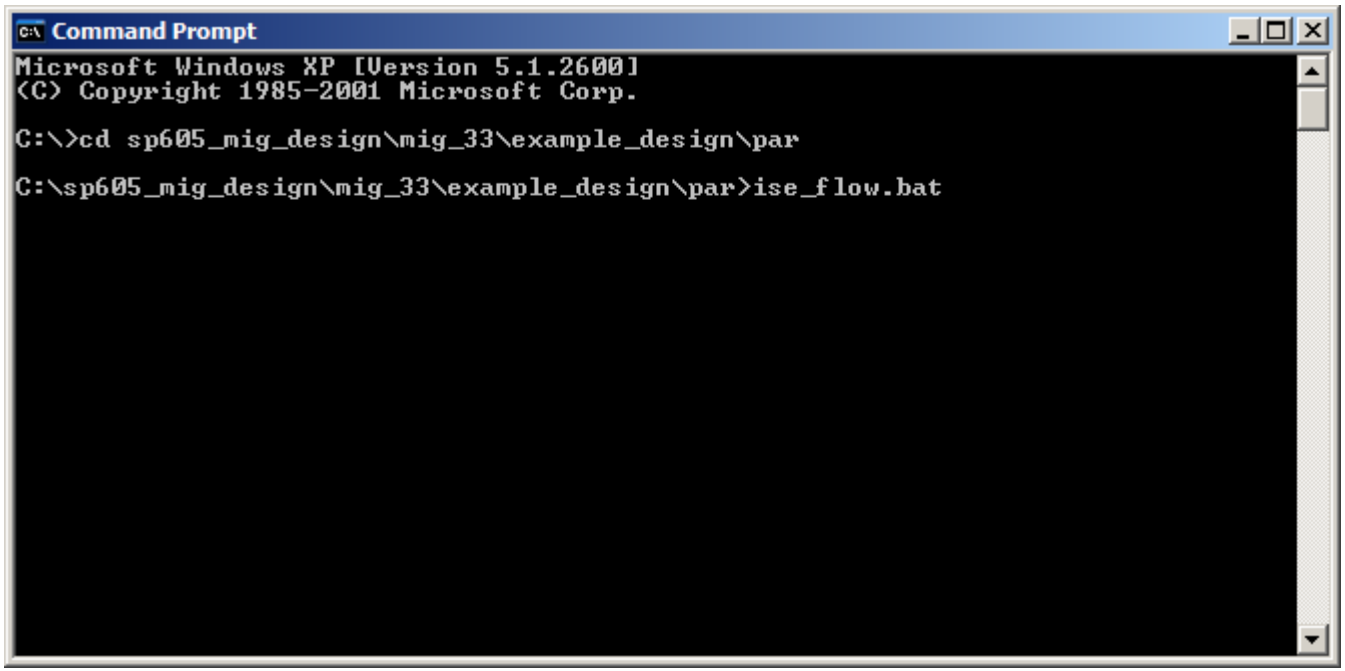
Note: Overwrites Core Generator output files with SP605 specific files (2)

Compile Example Design

- Start a windows command shell and enter these commands:

  cd sp605_mig_design\mig_33\example_design\par

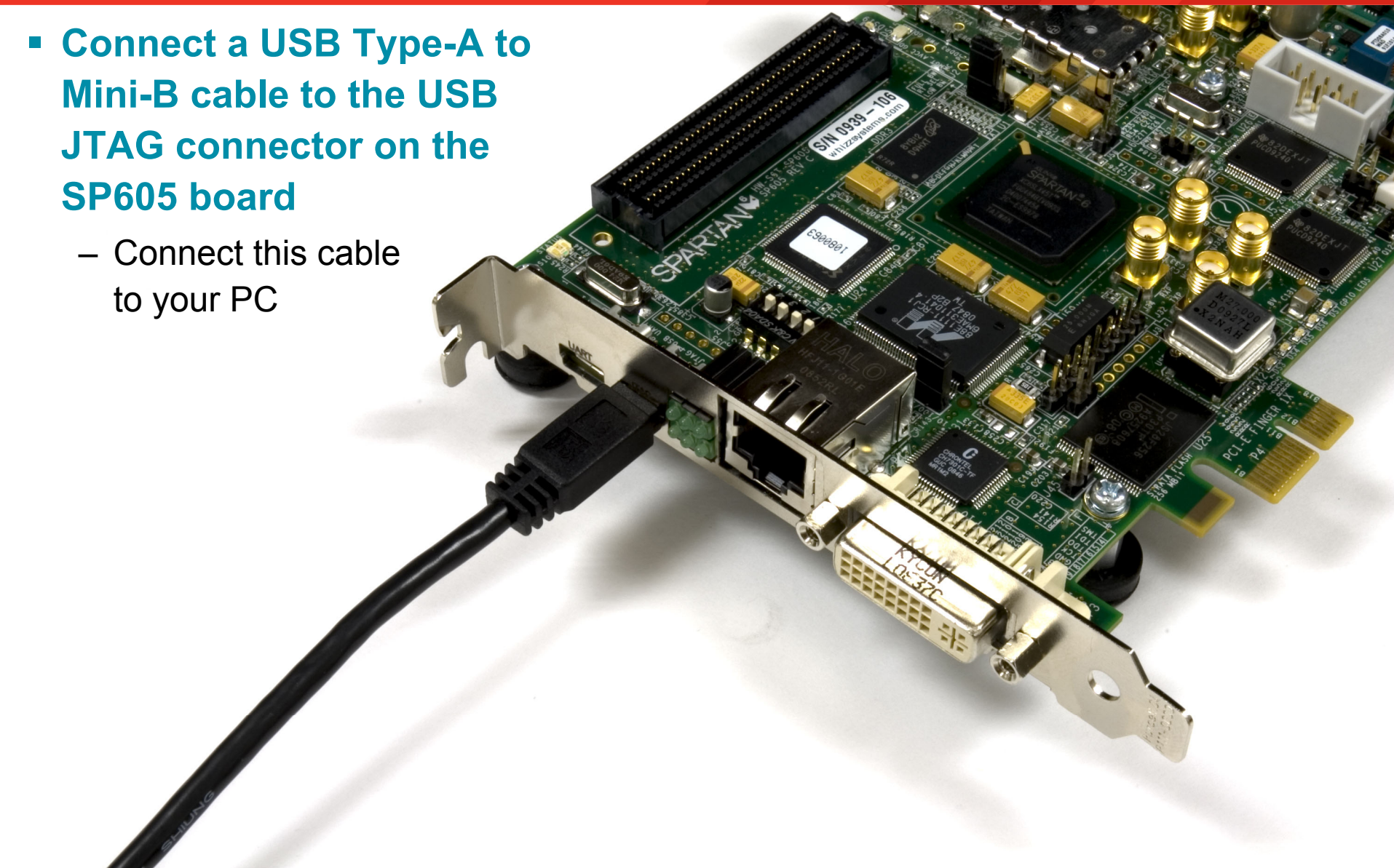
  ise_flow.bat



Note: Presentation applies to the SP605

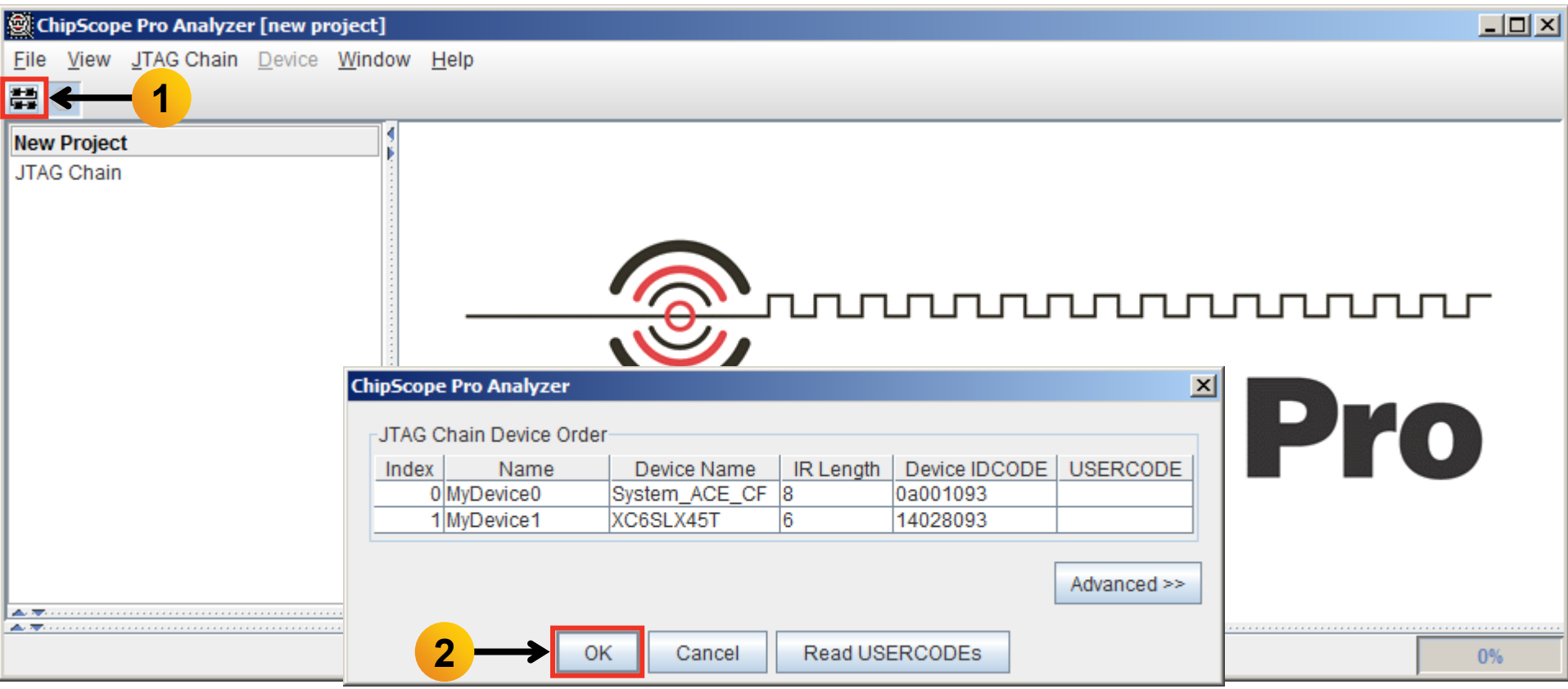
Setup for the SP605 MIG Designs

- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the SP605 board**
  - Connect this cable to your PC



Running the SP605 MIG Design

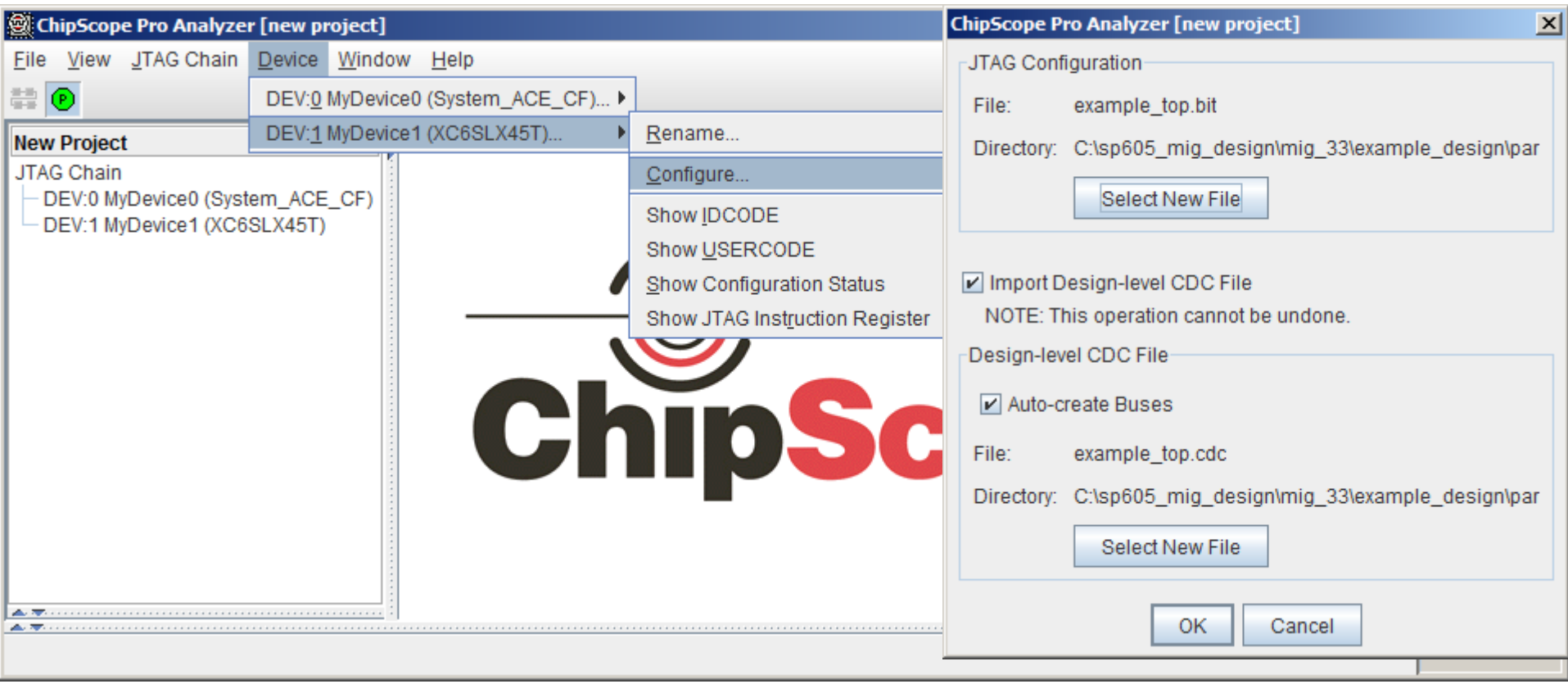
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the SP605

Running the SP605 MIG Design

- Select Device → DEV:1 MyDevice1 (XC6SLX45T) → Configure…
- Select <Design Path >\mig_33\example_design\par\example_top.bit



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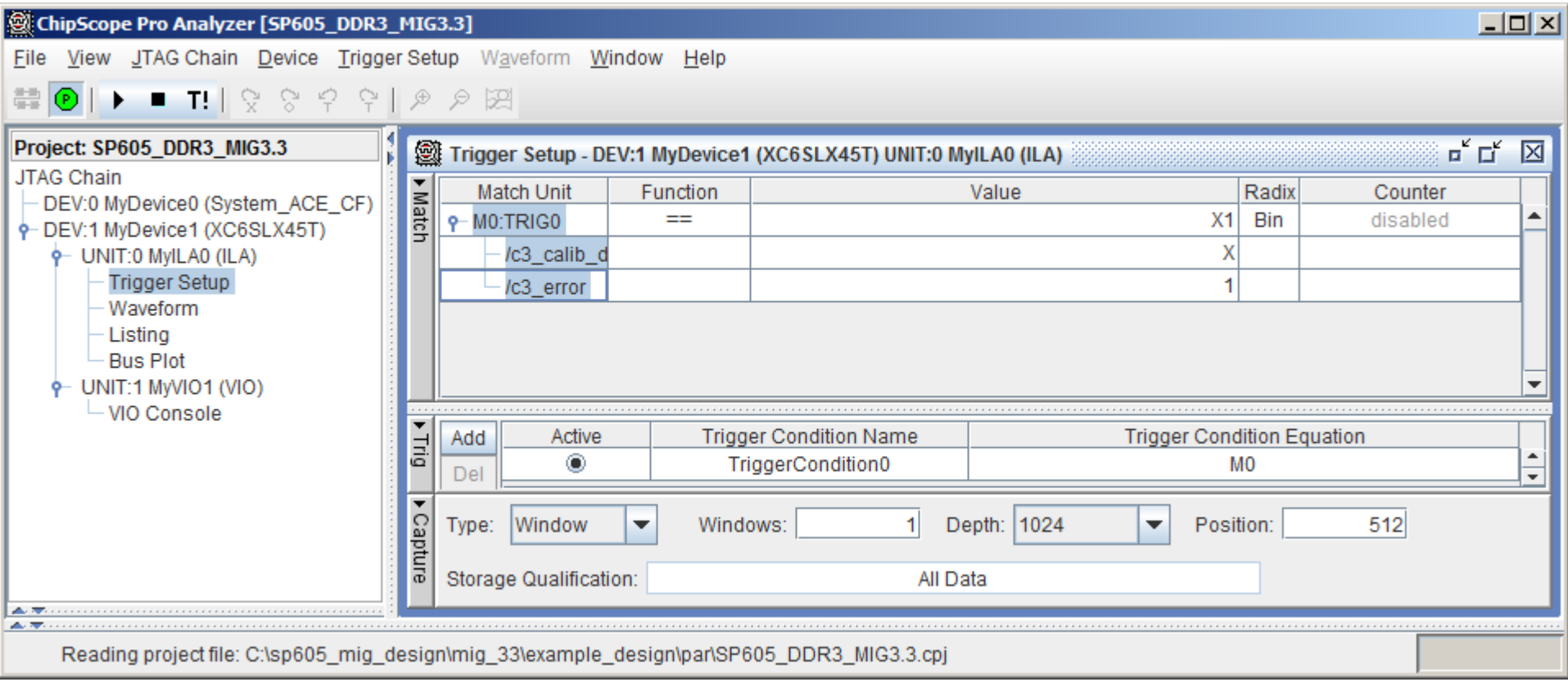
ChipScope Pro Setup

- Select File → Open Project…
- Select <Design Path>\mig_33\example_design\par\SP605_DDR3_MIG3.3.cpj

Note: Presentation applies to the SP605

Run MIG Example Design

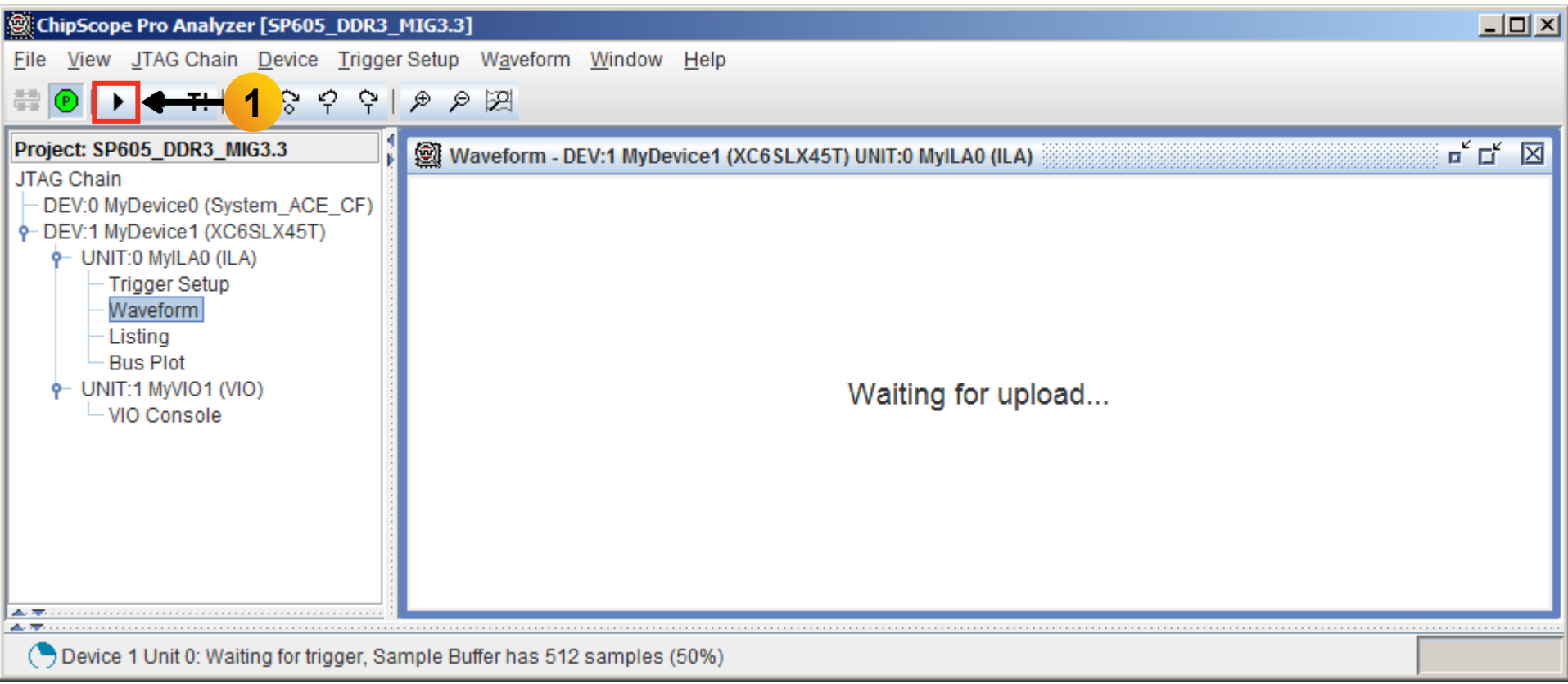
- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1



Note: Presentation applies to the SP605

Run MIG Example Design

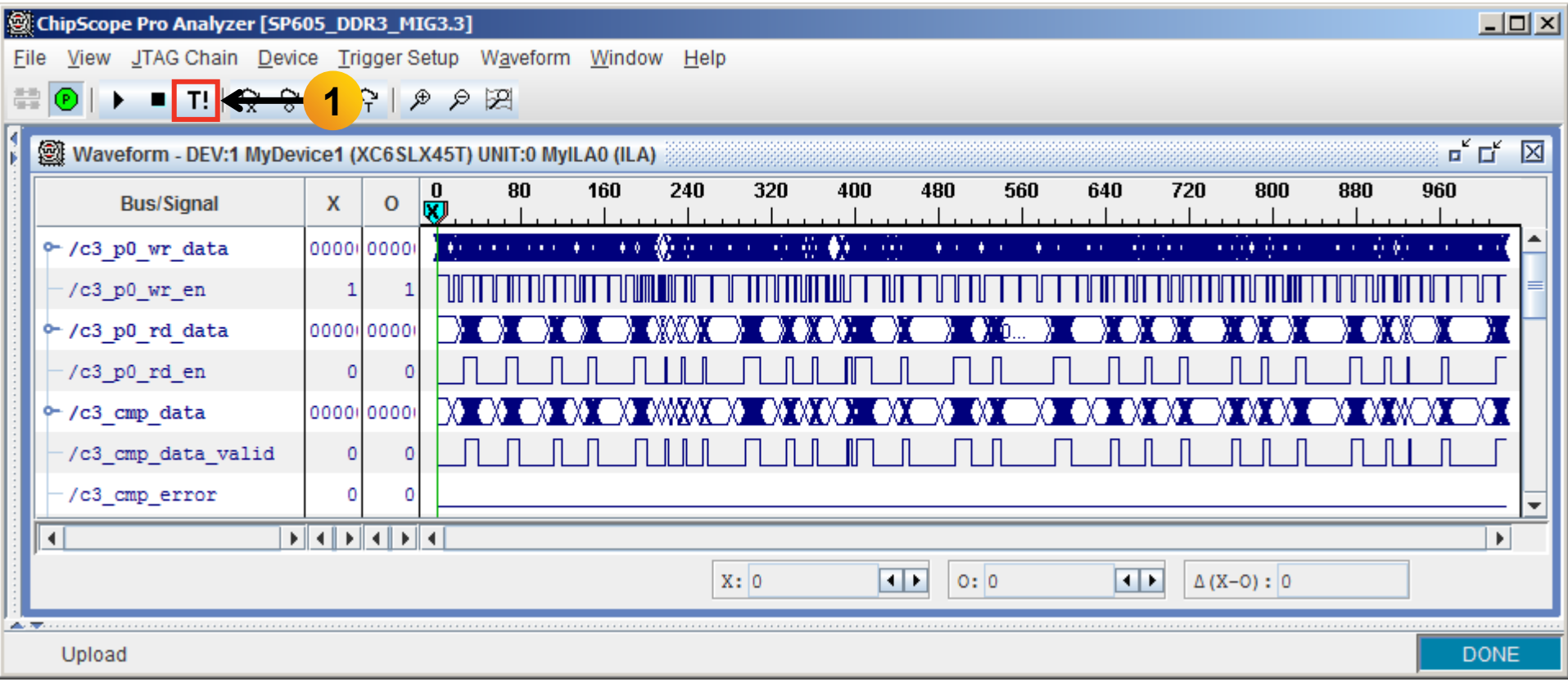
- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger



Note: Presentation applies to the SP605

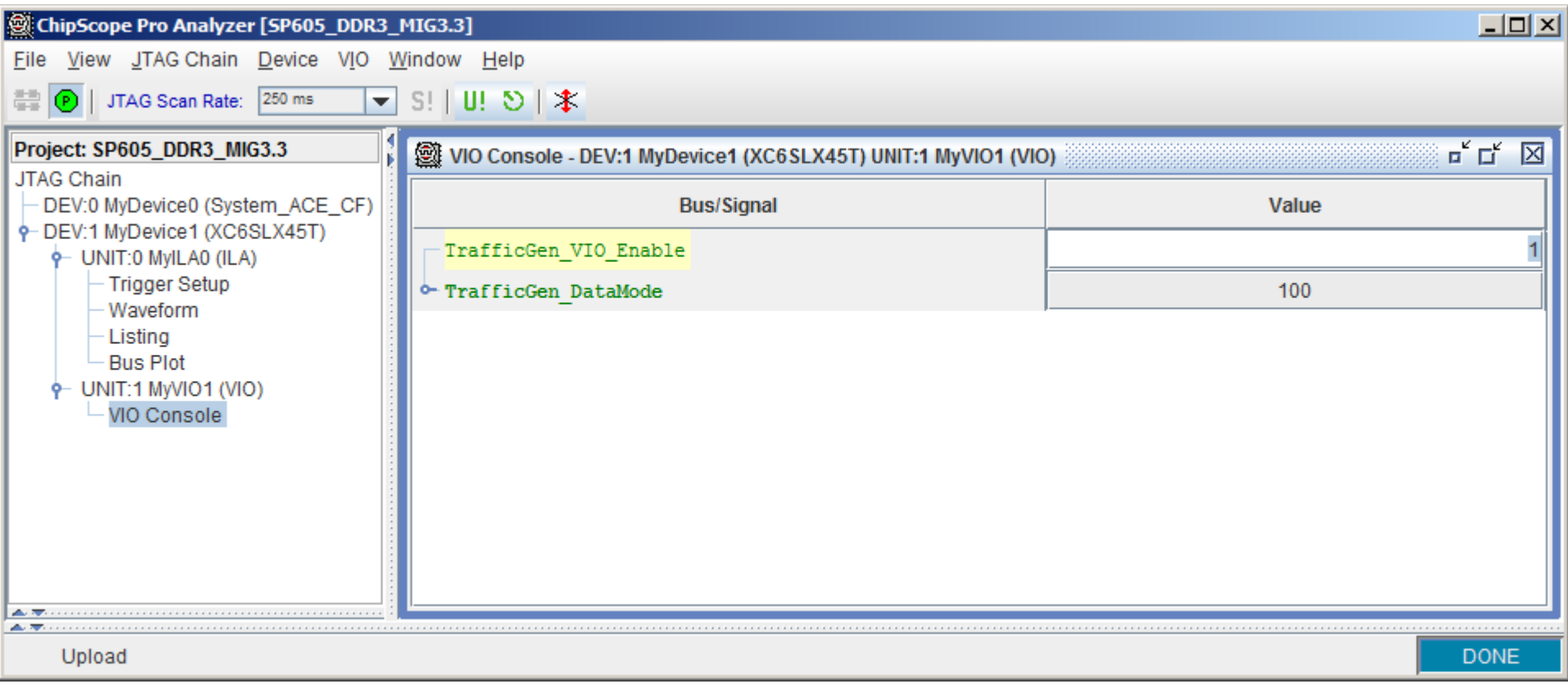
Run MIG Example Design

- The Example Design should run error free (no trigger on error)
- To force a trigger, click the T! button (1)



Adjust Data Pattern using VIO Console

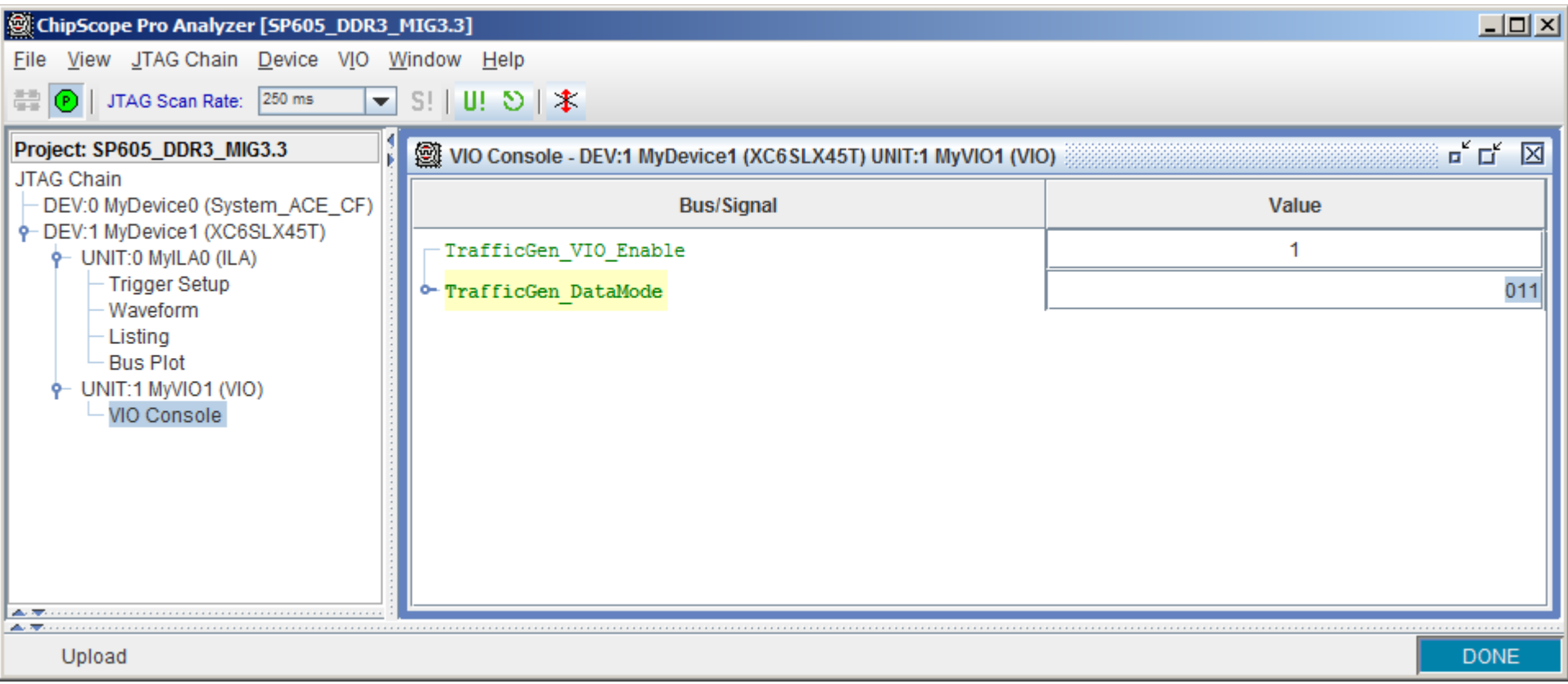
- Select VIO Console
- Set TrafficGen_VIO_Enable to 1



Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

- Set TrafficGen_DataMode to "011" for HAMMER_DATA_MODE



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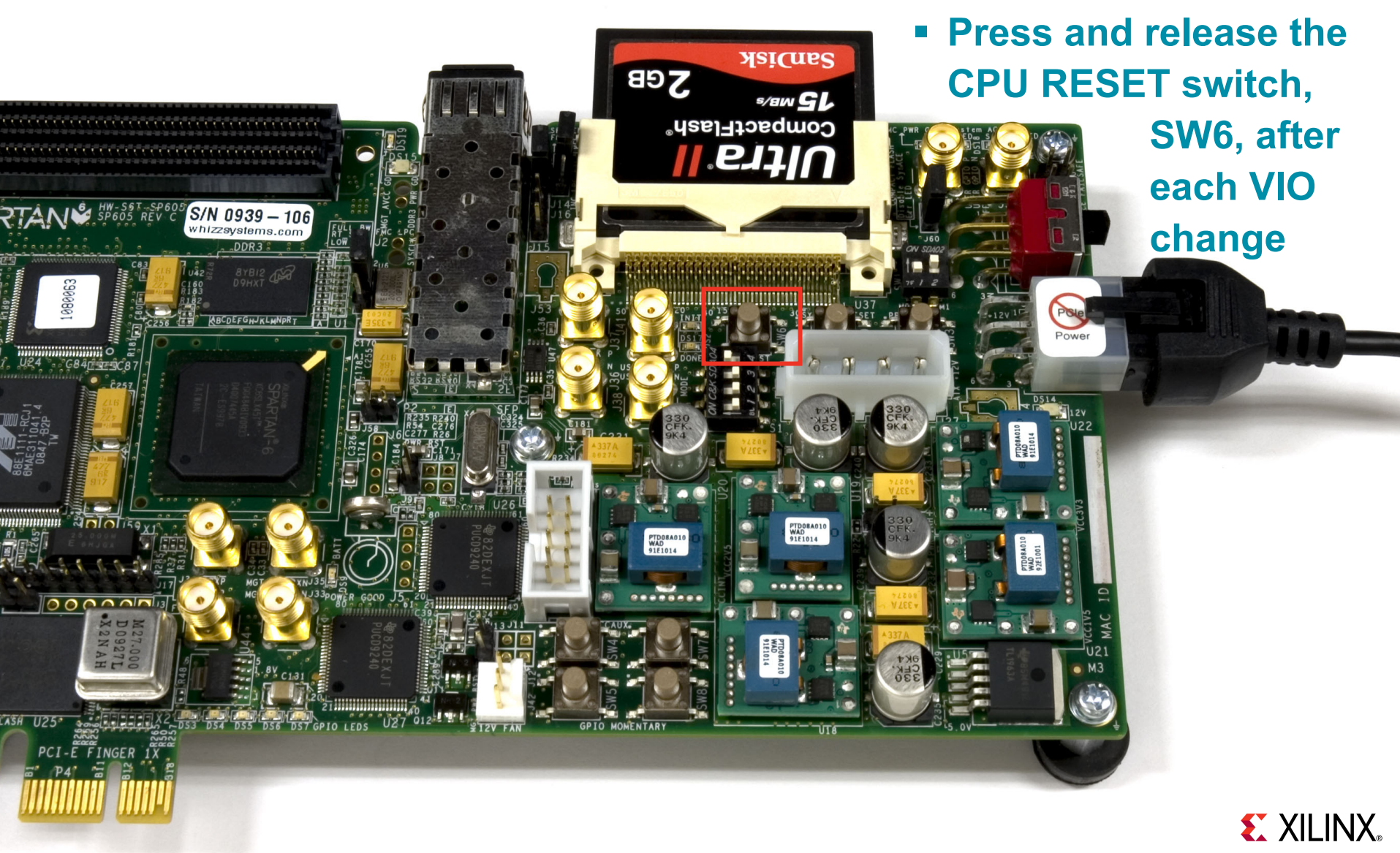
Adjust Data Pattern using VIO Console



- Press and release the CPU RESET switch, SW6, after each VIO change

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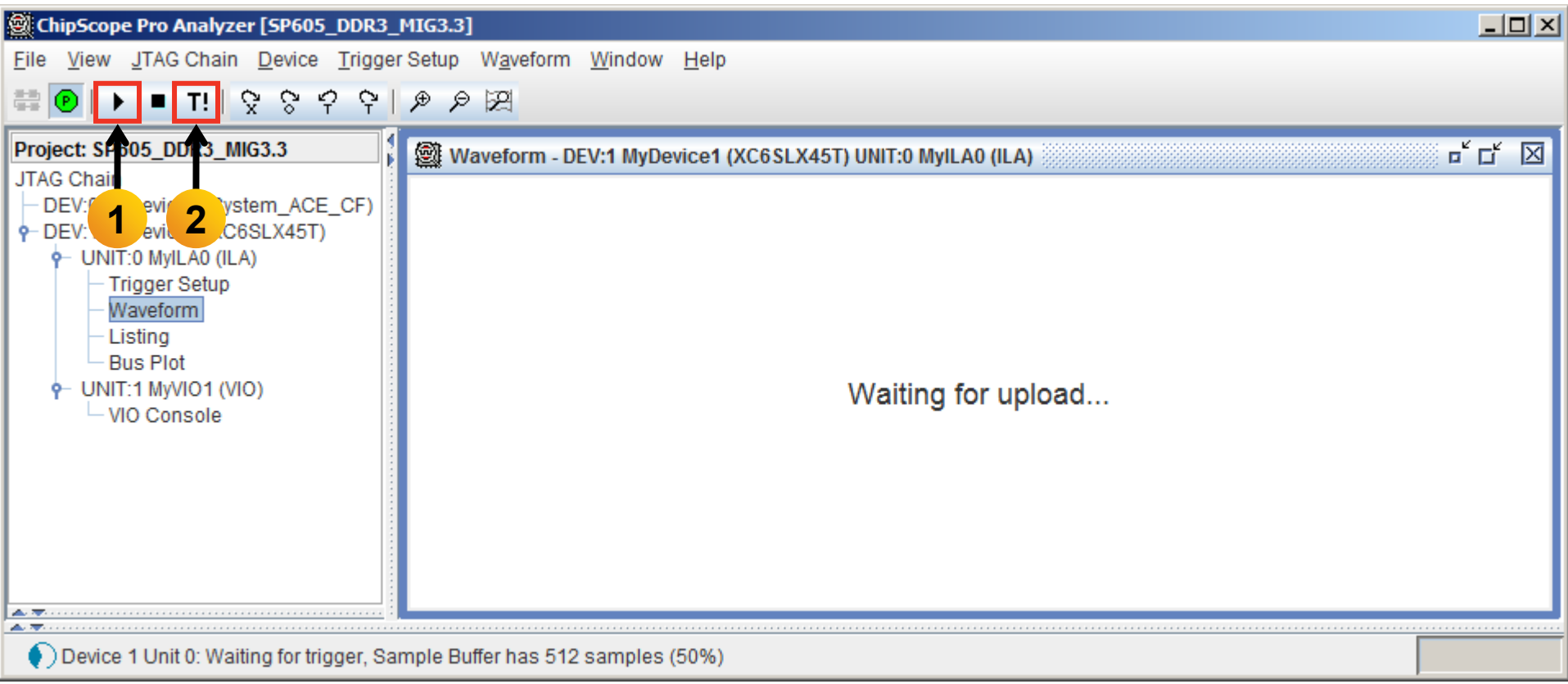
Run MIG Example Design

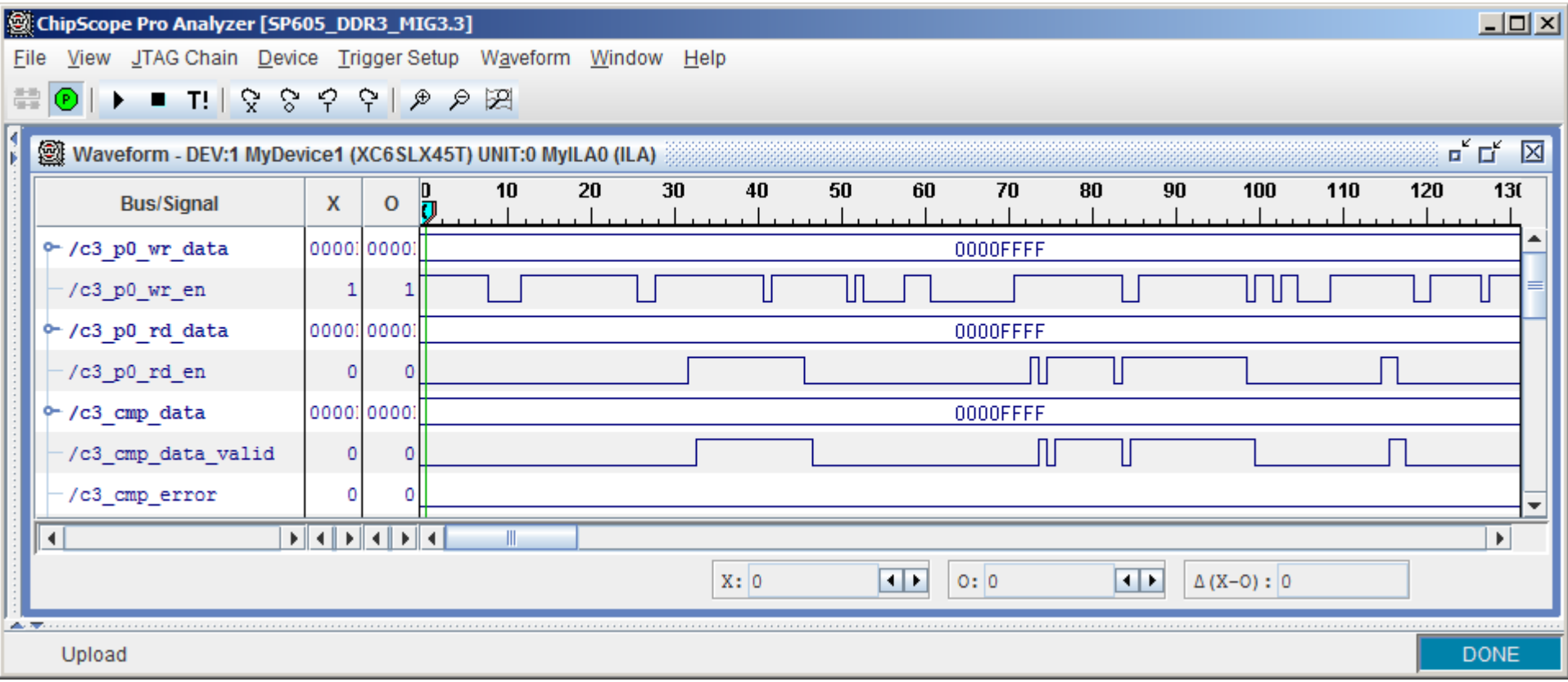
- Click on Waveform; click the Arm Trigger button (1)
- Force a trigger by clicking the T! button (2)



Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

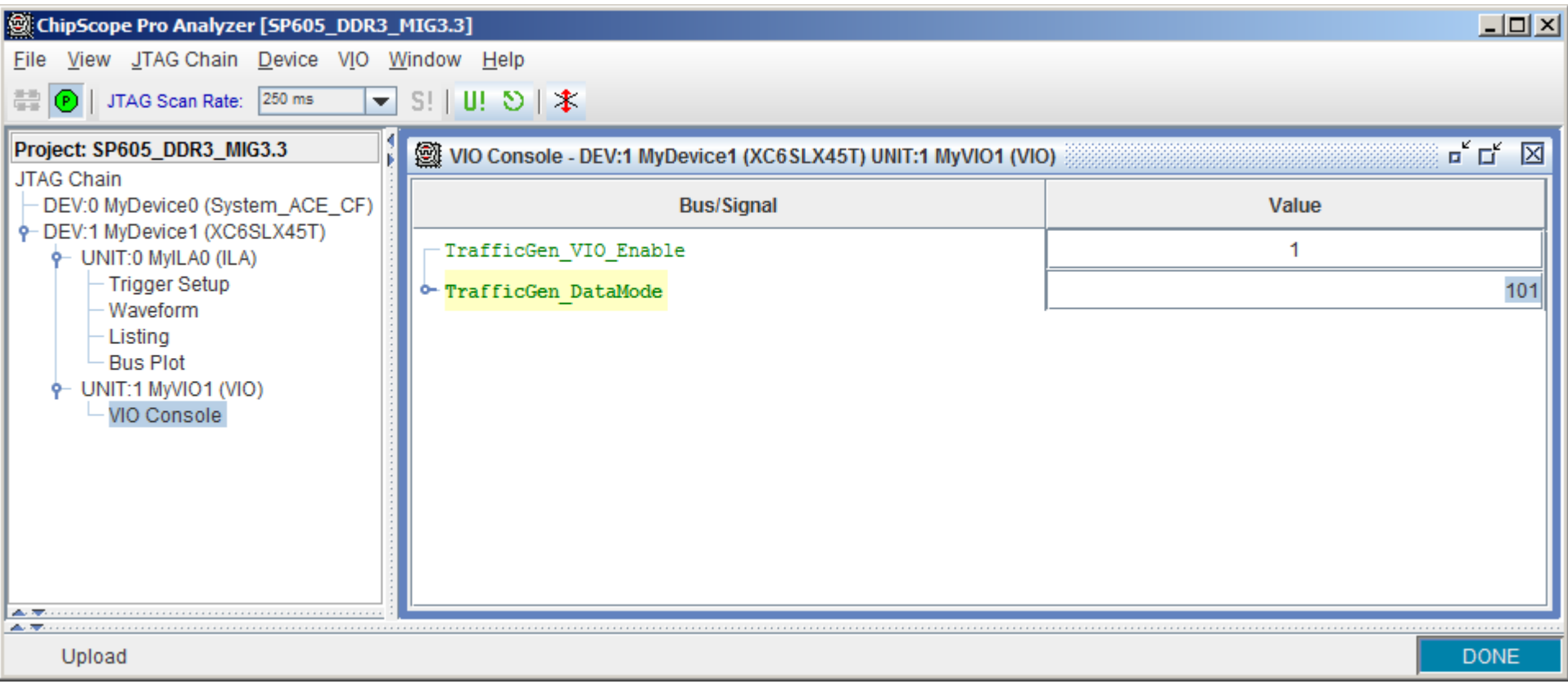
- **Hammer Data Mode**
  - 16 bit DQ data bus changes all bits on each cycle, “hammering” the bus
  - Read data compared with ‘expected’ data and error generated on mismatch



Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

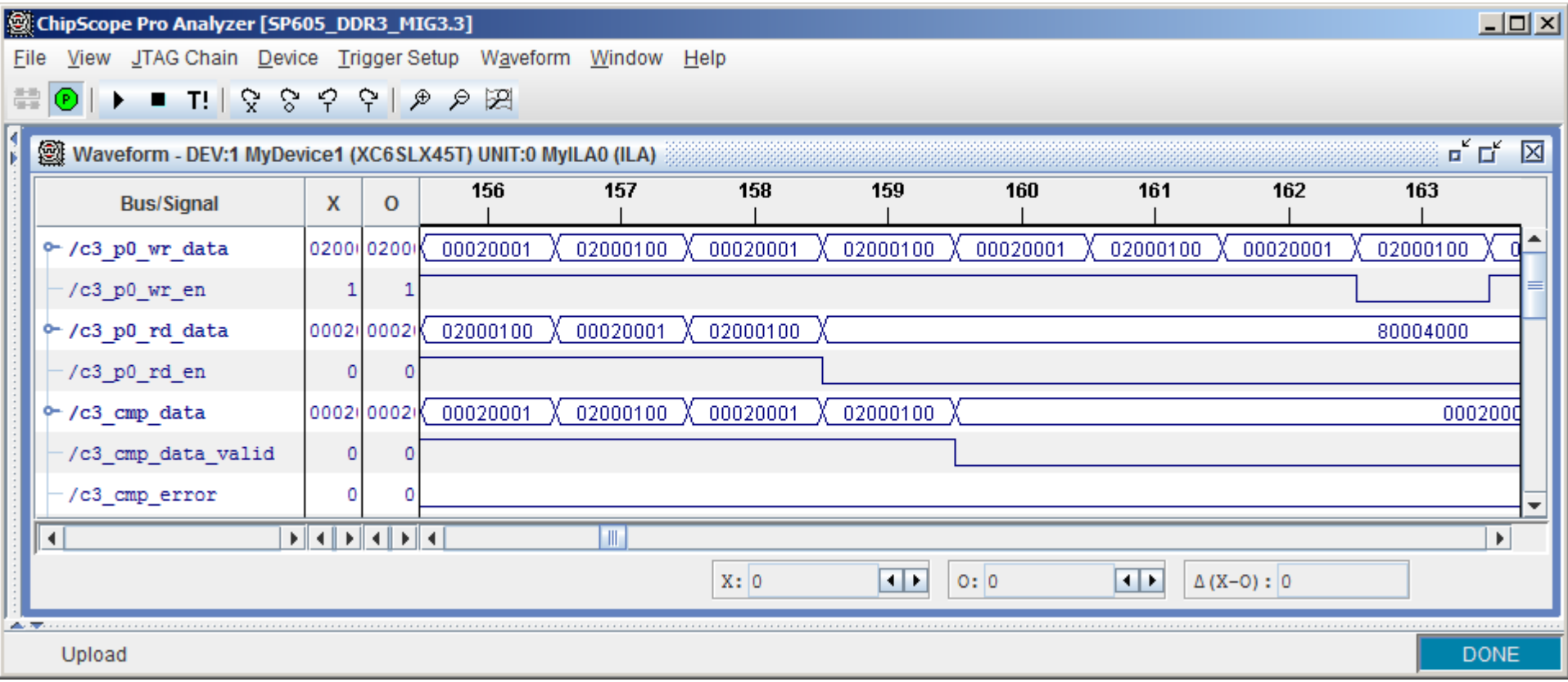
- Set TrafficGen_DataMode to "101" for WALKING1_DATA_MODE
- Push CPU Reset, click Arm Trigger button, click T! button



Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

- **Walking 1s Data Mode**



Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

- See UG388 for more details on the available data patterns
  - `ADDR_DATA_MODE = 3'b010;`
  - `HAMMER_DATA_MODE = 3'b011;`
  - `NEIGHBOR_DATA_MODE = 3'b100;`
  - `WALKING1_DATA_MODE = 3'b101;`
  - `WALKING0_DATA_MODE = 3'b110;`
  - `PRBS_DATA_MODE = 3'b111;`

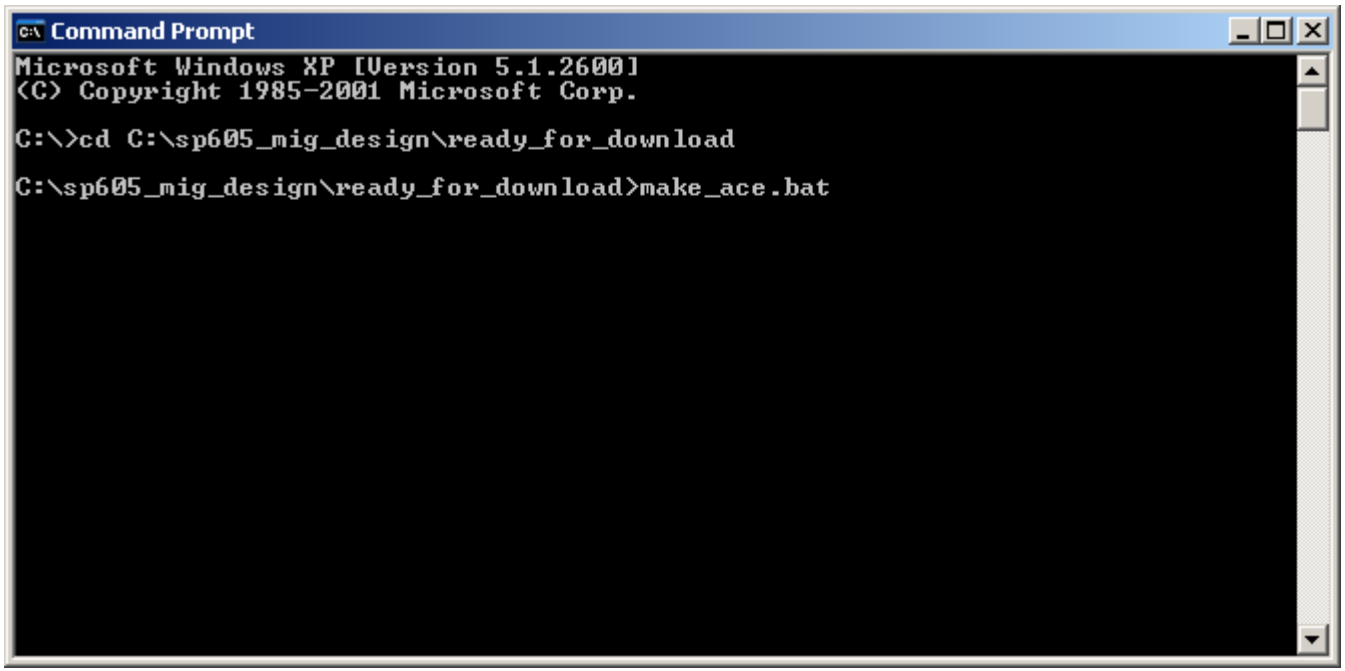
Note: Presentation applies to the SP605

Generate MIG ACE File (Optional)

- **Type these commands in a windows command shell:**

  cd C:\sp605_mig_design\ready_for_download

  make_ace.bat



Note: Presentation applies to the SP605

References

References

- **Spartan-6**
  - Spartan-6 FPGA Memory Controller – UG388
    http://www.xilinx.com/support/documentation/user_guides/ug388.pdf
- **ChipScope Pro**
  - ChipScope Pro Software and Cores User Guide
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/chipscope_pro_sw_cores_ug029.pdf

Documentation

Documentation

- **Spartan-6**
  - Spartan-6 FPGA Family
    http://www.xilinx.com/products/spartan6/index.htm
- **SP605 Documentation**
  - Spartan-6 FPGA SP605 Evaluation Kit
    http://www.xilinx.com/products/devkits/EK-S6-SP605-G.htm
  - SP605 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug526.pdf
  - SP605 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug527.pdf