

SP605 MIG Design Creation

December 2009

Overview

- **Spartan-6 Memory Controller Block**
- **Xilinx SP605 Board**
- **Software Requirements**
- **SP605 Setup**
- **Generate MIG Core**
- **Modifications to Example Design**
- **Compile Example Design**
- **ChipScope Pro Setup**
- **Run MIG**
- **References**

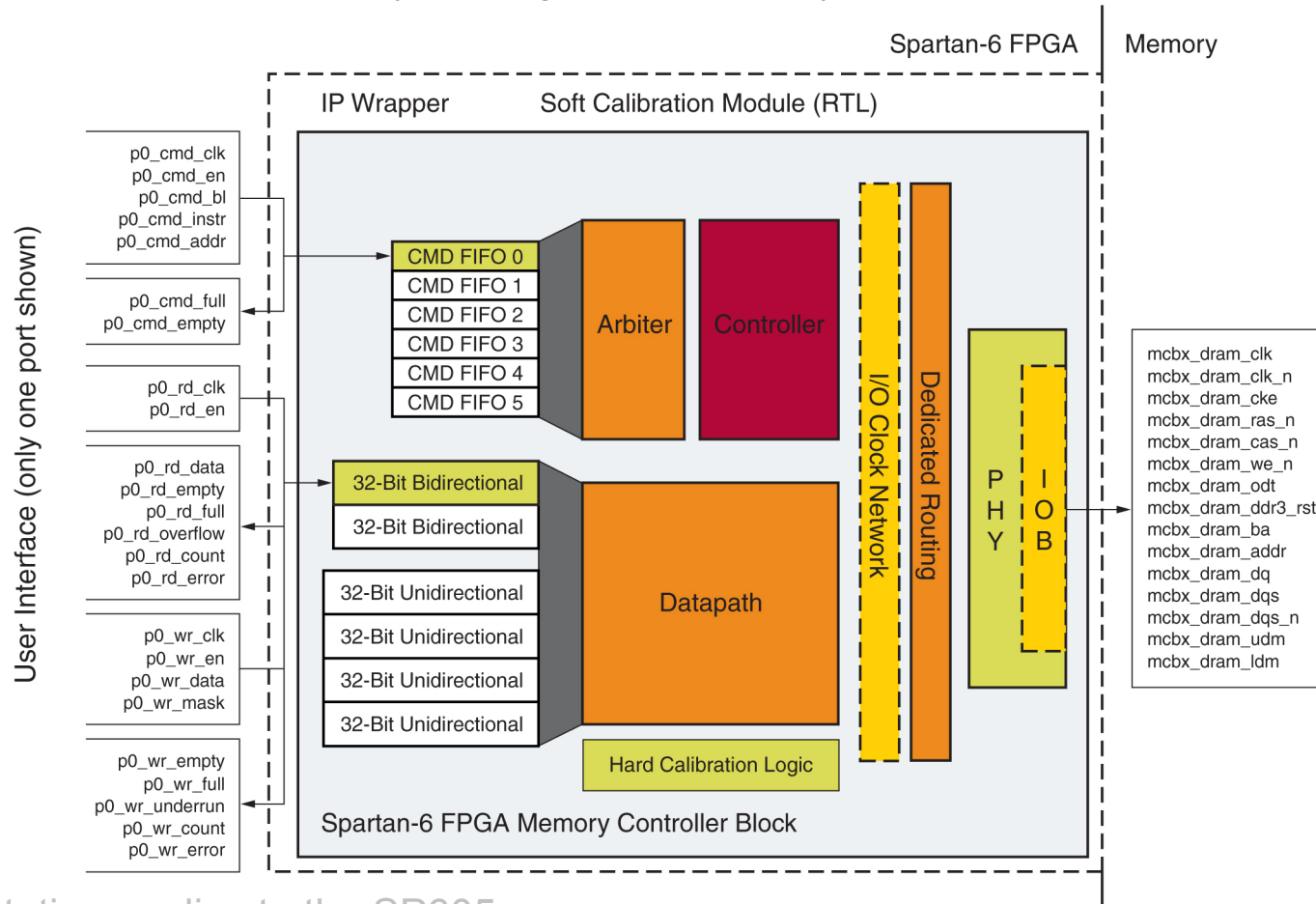
Note: This presentation applies to the SP605

Spartan-6 Memory Controller Block

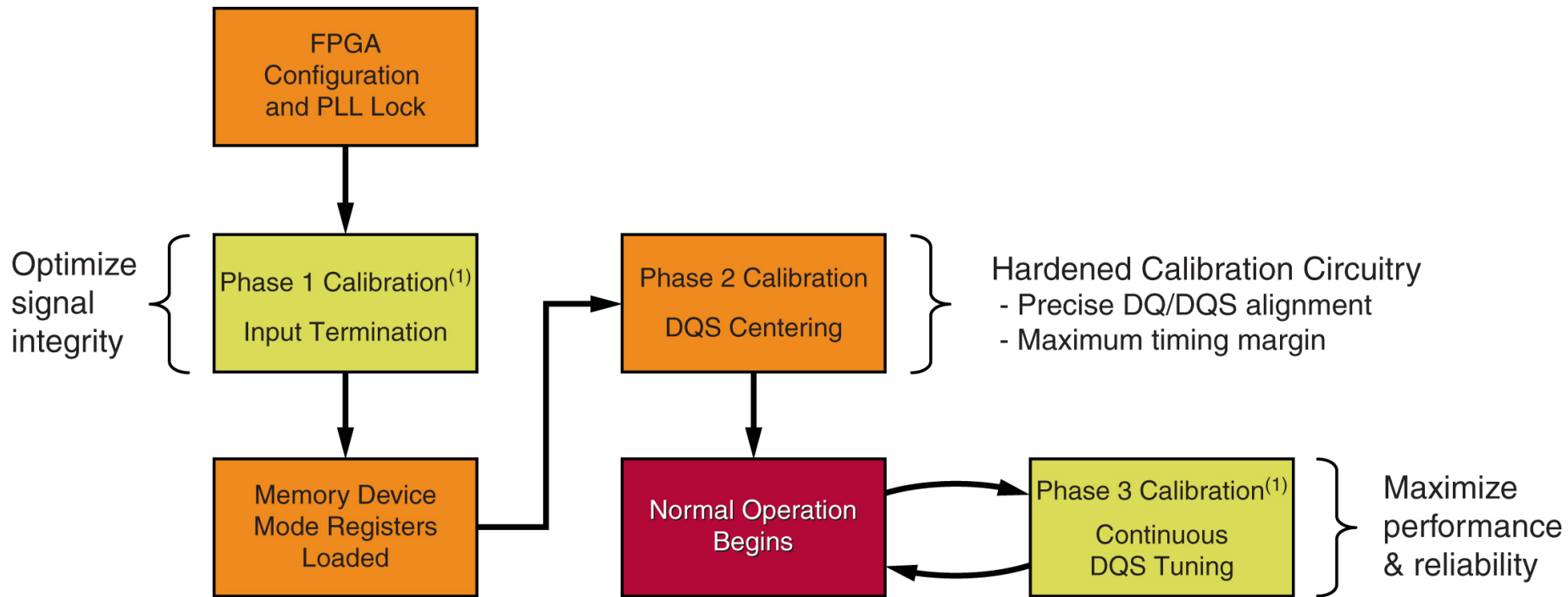
- **Dedicated Memory Controller Blocks (MCB) for Simplified DRAM interfaces**
 - Up to 4 MCB cores in a single Spartan-6 device
 - Embedded controller and physical (PHY) interface
 - Supports 4-bit, 8-bit, or 16-bit single component memory
 - Memory densities up to 4 Gbit
- **Performance up to 800 Mb/s (400 MHz double data rate)**
- **Configurable dedicated Multi-port user interface to FPGA logic**
 - 1 to 6 ports per MCB depending on configuration
 - Internal 32-, 64-, or 128-bit data bus options

MCB Block Diagram

- **Simple User Interface abstracts away complexity of memory transactions**
- **MIG / EDK wrapper delivers complete interface solution**
 - Internal block assembly and signal connectivity is made transparent to the user



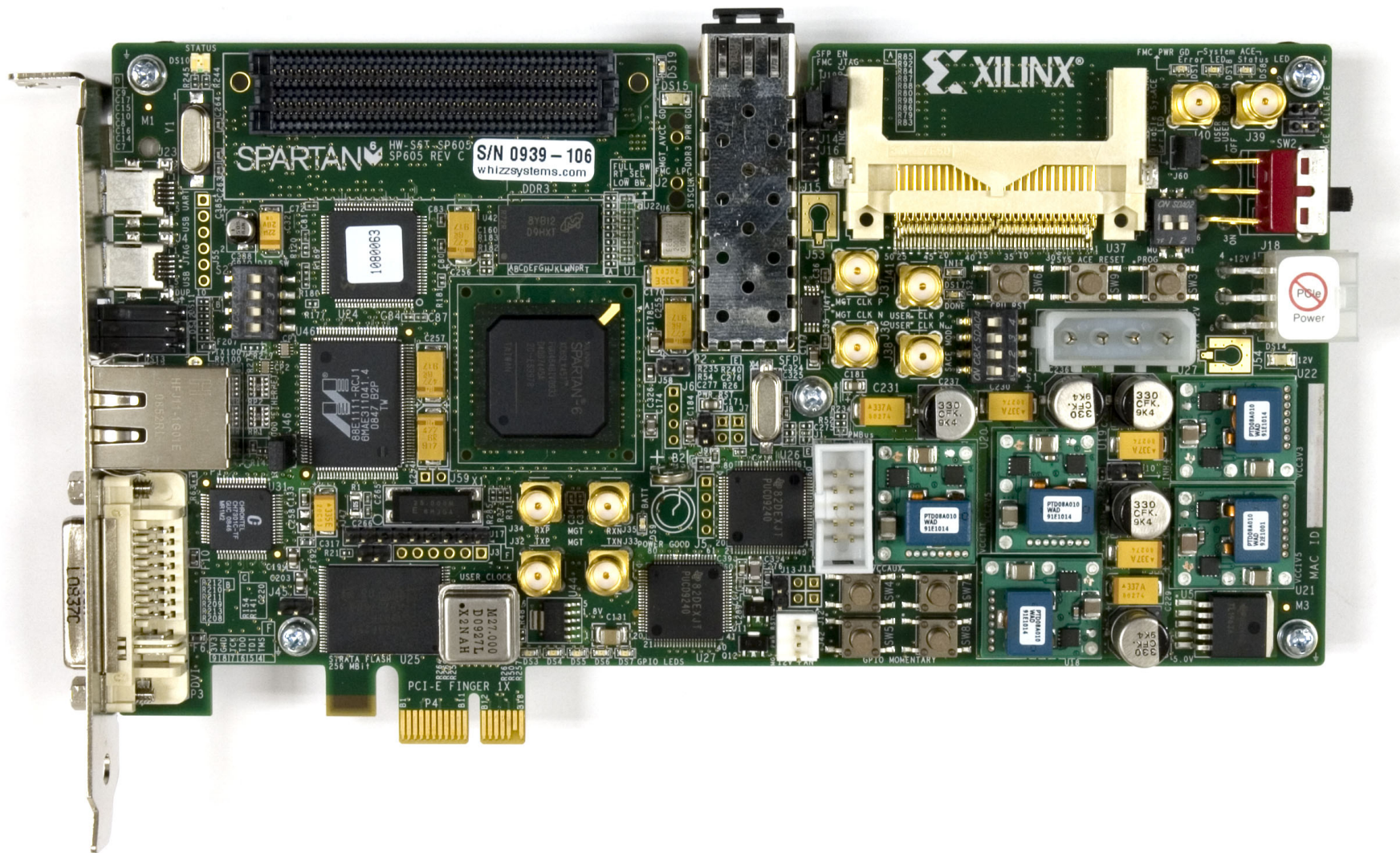
Memory Controller Block Startup



1. Phase 1 & 3 of calibration are controlled by a **soft module** – enabled by MIG or EDK

Automatic memory configuration and controller calibration

Xilinx SP605 Board



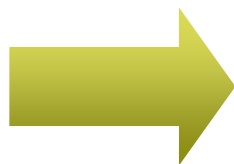
ISE Software Requirement

- Xilinx ISE 11.4 software



ChipScope Pro Software Requirement

- Xilinx ChipScope Pro 11.4 software

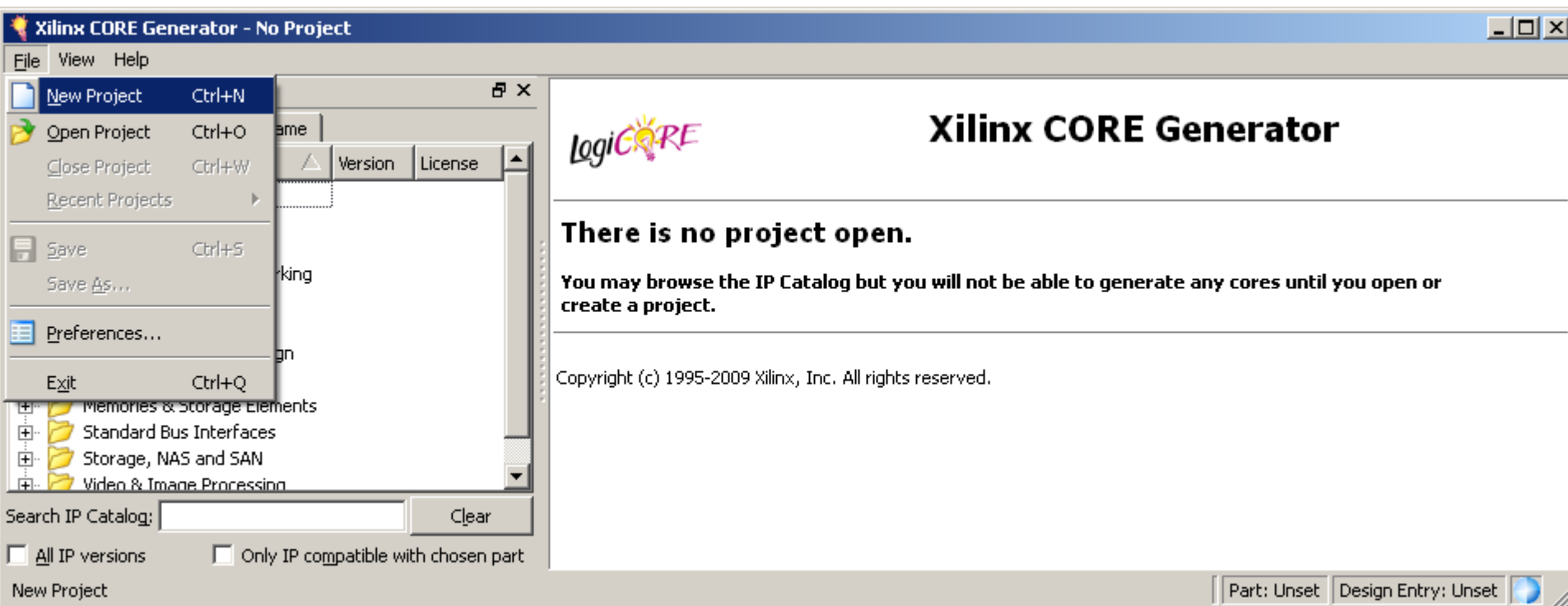


Generate MIG Example Design

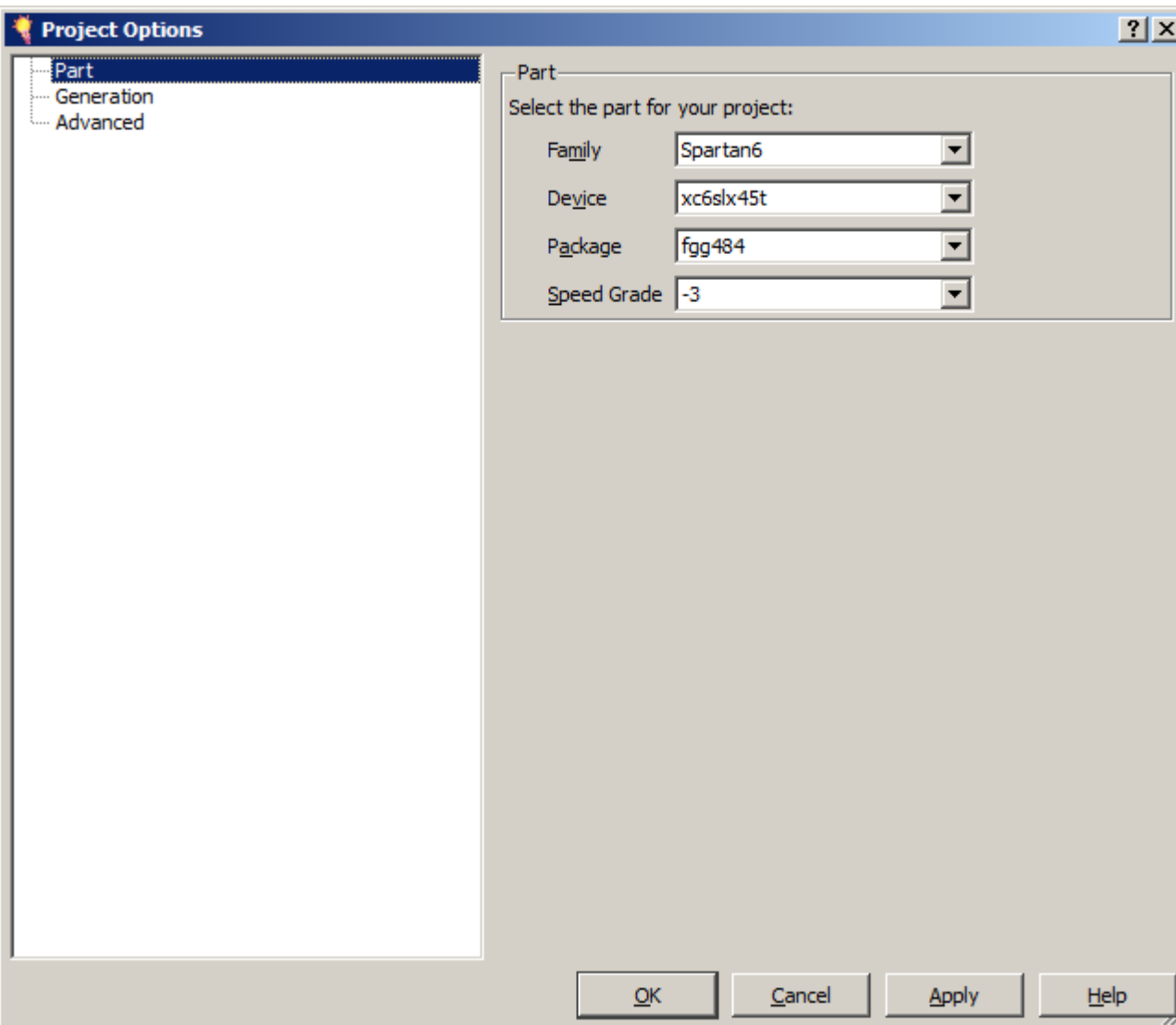
- **Open the CORE Generator**

**Start → All Programs → Xilinx ISE Design Suite 11 →
ISE → Accessories → CORE Generator**

- **Create a new project; select File → New Project**



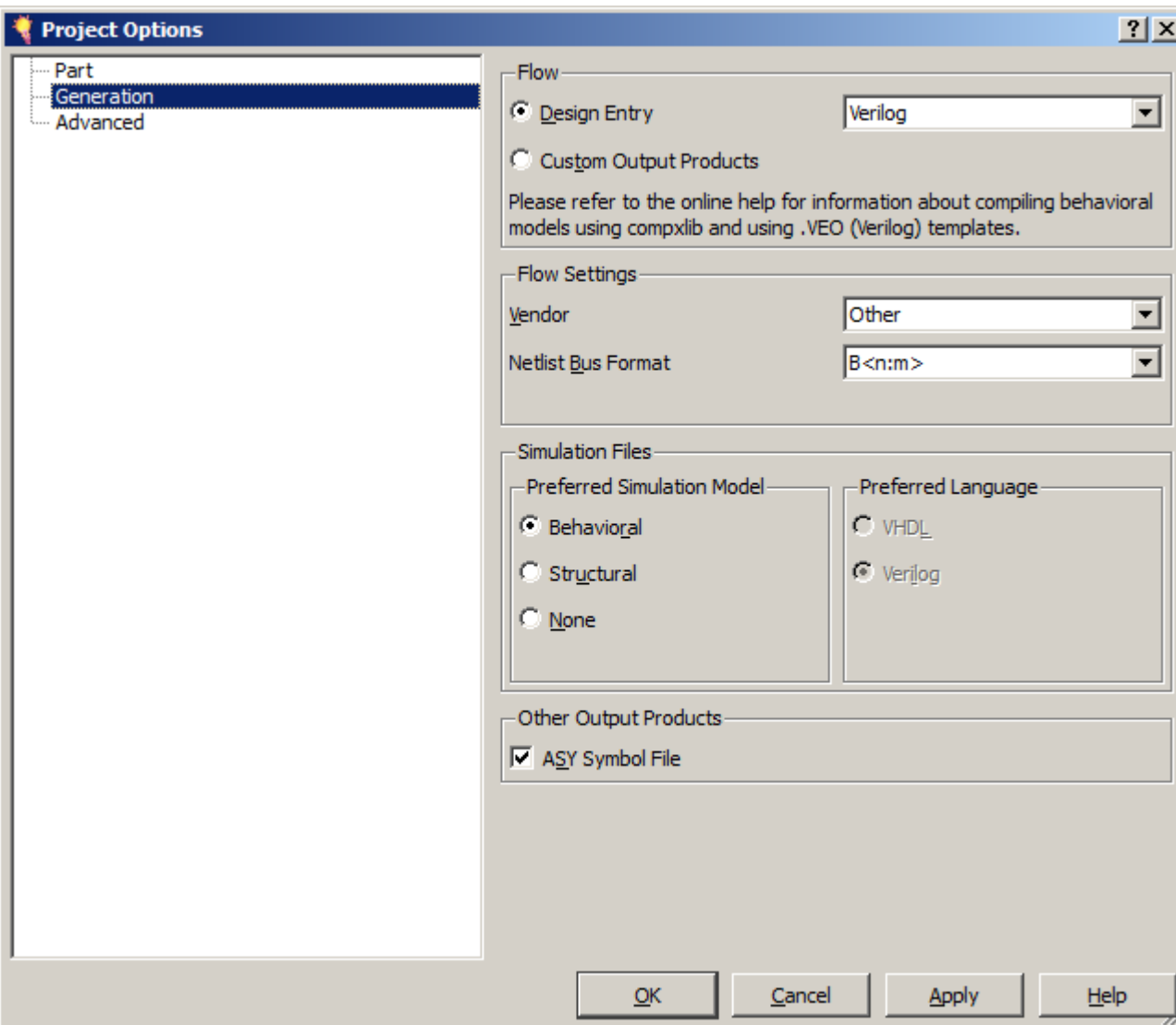
Generate MIG Example Design



- Create a project directory:
sp605_mig_design
- Name the project:
sp605_mig_design.cgp
- Set the Part (as shipped on the SP605):
 - Family: Spartan6
 - Device: xc6slx45t
 - Package: fgg484
 - Speed Grade: -3

Note: Presentation applies to the SP605

Generate MIG Example Design

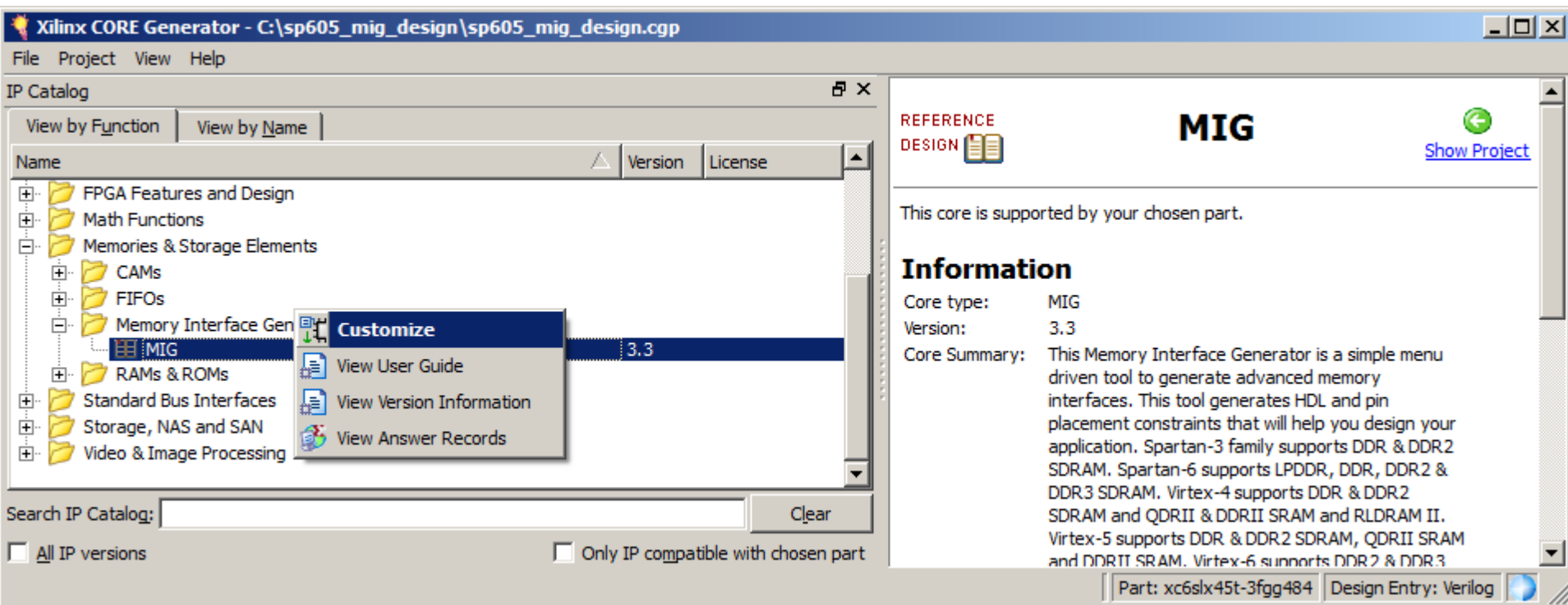


- Select Generation
- Set the Design Entry to Verilog
- Click OK

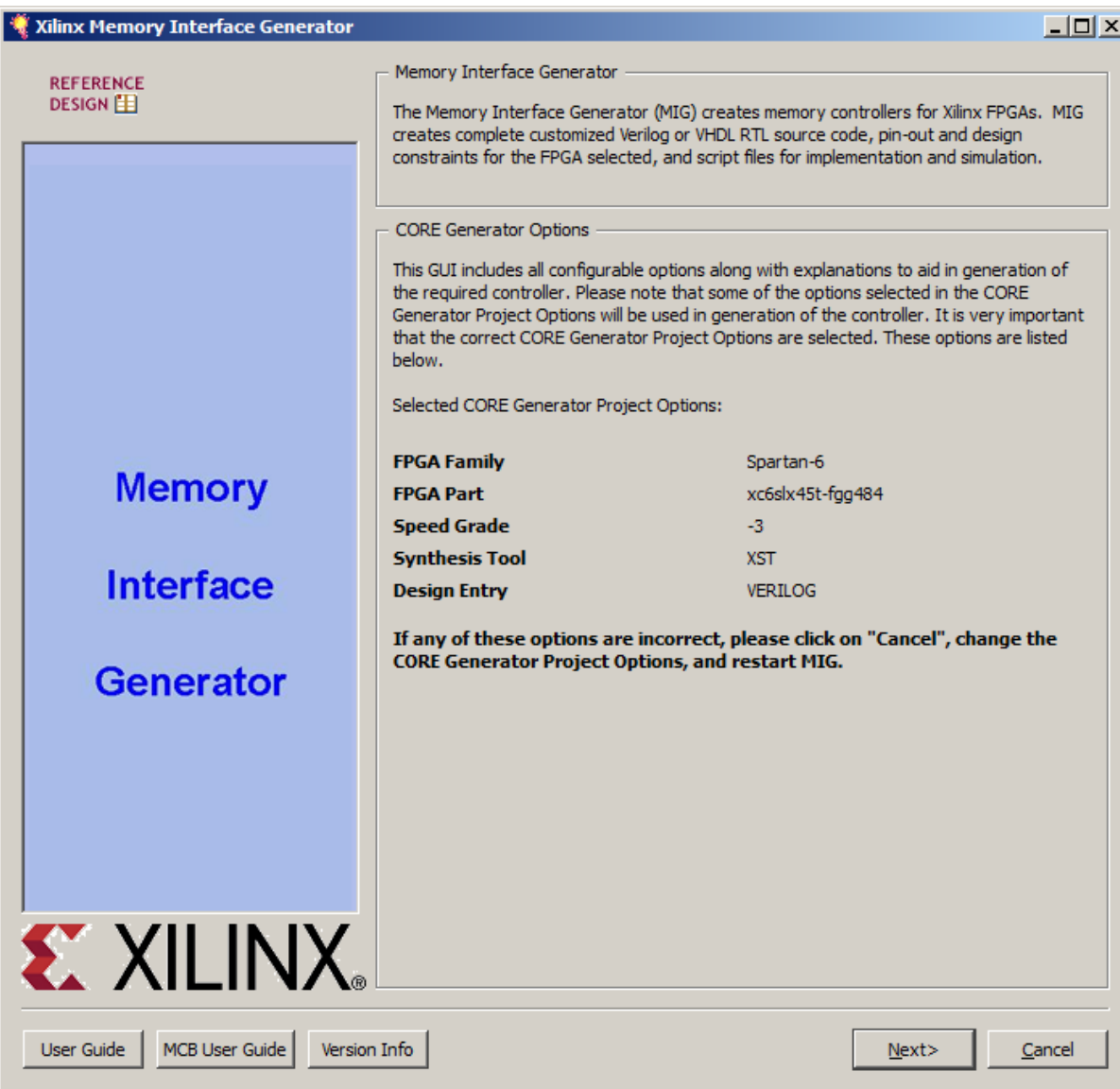
Note: Presentation applies to the SP605

Generate MIG Example Design

- Right click on MIG Version 3.3
 - Select **Customize**

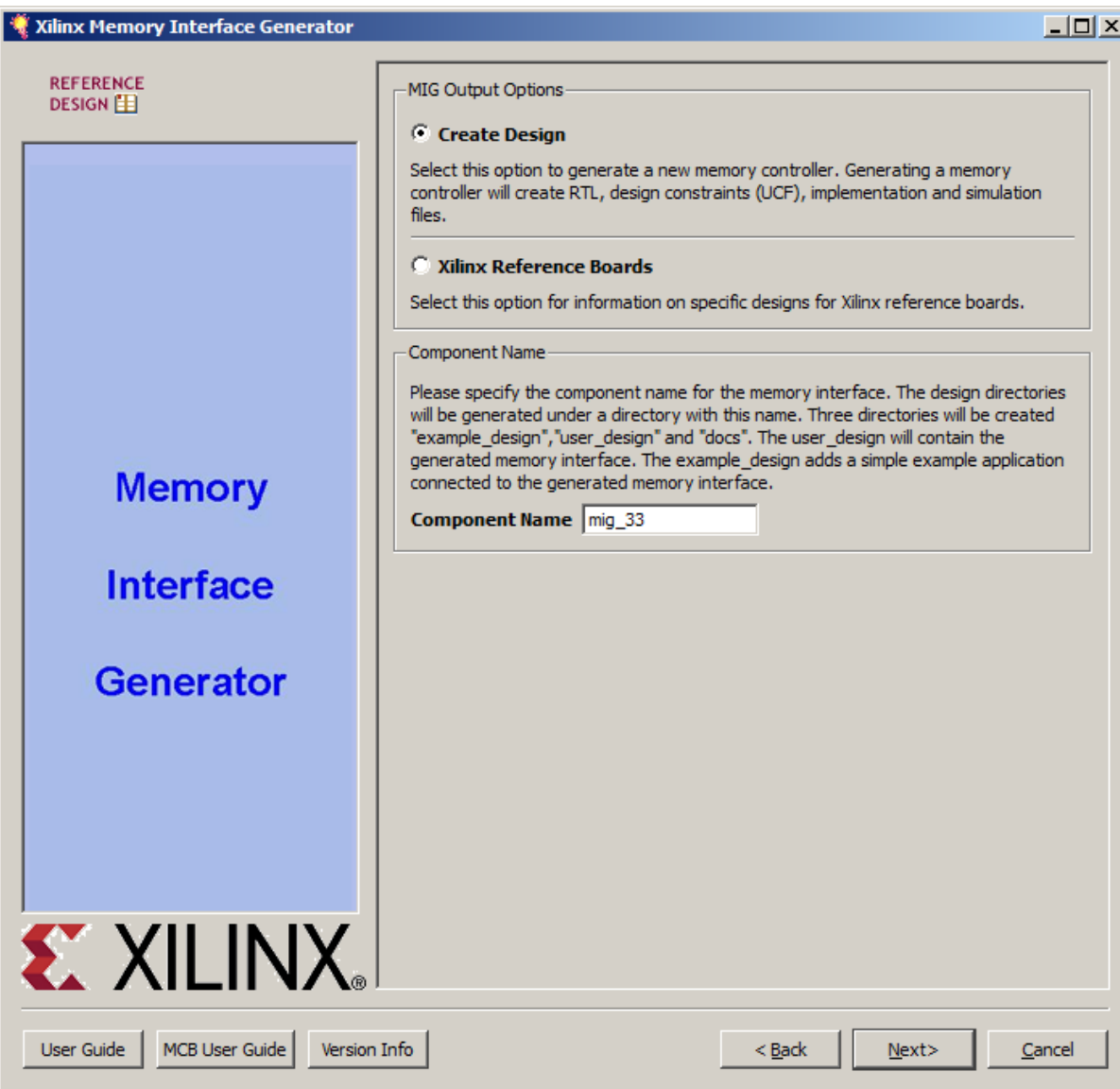


Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design

Memory Selection

Select the memory interface type from the Memory Type selection box provided for each bank. Hardware verified devices are listed in the User Guide.

The MCB in Bank 3 (marked with an asterisk below) has fewer multi-purpose IO pins and is therefore the preferred location for designs with a single controller. The other MCB locations have more multi-purpose pins. Check your design to make sure there are no conflicts with MCB interface pins.

	Bank 0	
<div>Memory Type DDR3 SDRAM</div>	<div>(C3) Mid MCB Bank 3 *</div> <div>xc6slx45t-fgg484</div>	<div>(C1) Mid MCB Bank 1</div> <div>Memory Type none</div>
	Bank 2	

[n Info](#) [< Back](#) [Next >](#) [Cancel](#)

- **Select**
 - Bank 3 Middle MCB
- **Select Memory Type**
 - DDR3 SDRAM
 - Click Next

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Controller Options
C3

Memory Options
C3

Multi-port Configuration
C3

Arbitration
C3

FPGA Options
C3

Summary

Memory Model

PCB Information

Design Notes

Options for C3 - DDR3 SDRAM

Frequency: The allowed frequency range is a function of the selected FPGA part, FPGA speed grade and Memory Controller type. Choose the clock period for the desired frequency. Refer to User Guide for supported frequency range.

2500 ps 400.00 MHz

Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. If the exact part that you will be using is not available here, you may be able to find an equivalent part. Alternately, you can create a part using the "Create Custom Part" selection at the bottom of this drop box. Refer to User Guide for complete list of memory devices supported.

MT41J64M16XX-187E

Memory Details: 1Gb, x16, row:13, col:10, bank:3, data bits per strobe:8, with data mask

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User Guide MCB User Guide Version Info < Back Next > Cancel

- Set the Memory part to MT41J64M16XX-187E

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Controller Options ✓

C3

Memory Options

C3

Multi-port Configuration

C3

Arbitration

C3

FPGA Options

C3

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Design Notes

Memory Options for C3 - DDR3 SDRAM

Choose the Memory Options settings for the memory device. Settings are restricted to those supported by the controller.

Output Driver Impedance Control
To calibrate the output driver impedance, an external precision resistor (RZQ) is connected between the ZQ ball and VSSQ. The value of the resistor must be 240ohm +/-1 percent.

RZQ/6

RTT (nominal) - ODT
The ODT feature is designed to improve signal integrity of the memory channel by enabling the DDR3 SDRAM controller to independently turn on/off ODT.

RZQ/4

Auto Self Refresh
When ASR is disabled, the self refresh mode's refresh rate is assumed to be at the normal 85 C limit(referred to as 1X refresh rate). Enabling ASR assumed the DRAM self refresh rate is changed automatically from 1X to 2X when the case temperature exceeds 85 C.

Enabled

High Temperature Self Refresh Rate
In the Normal mode, SRT requires the user to ensure the DRAM never exceeds a Tc of 85 C while in self refresh mode unless the user enables ASR. In Extended mode, the DRAM self refresh is changed internally from 1X to 2X, regardless of the case temperature.

Normal

RTT_WR
With dynamic ODT(RTT_WR) enabled, the DRAM switches from normal ODT(RTT_NOM) to dynamic ODT(RTT_WR) when beginning a WRITE burst and subsequently switches bak to ODT(RTT_NOM) at the completion of the WRITE burst.

Dynamic ODT off

User Guide MCB User Guide Version Info < Back Next > Cancel

- Leave this page as is
 - Click Next

Generate MIG Example Design

Port Configuration for C3 - DDR3 SDRAM

Select one of five configurations from the configuration menu and the ports from the table. As you select the port configuration, the below figure and table will get updated. You can select the number of ports in a configuration, and data port settings from the table.

Configuration Selection

One 128-bit bi-directional port

Port Selection	Direction
<input checked="" type="checkbox"/> Port0	Bi-directional

Memory Address Mapping Selection

User Address

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

☒ ROW BANK COLUMN

☐ BANK ROW COLUMN

User Interface Configuration:

PORT0	
p0_arb_en	→ p0_cmd_empty
p0_cmd_clk	→ p0_cmd_full
p0_cmd_en	
p0_cmd_instr[2:0]	
p0_cmd_bl[5:0]	
p0_cmd_addr[29:0]	

p0_rd_clk	→ p0_rd_data[127:0]
p0_rd_en	→ p0_rd_full
p0_wr_clk	→ p0_rd_empty
p0_wr_en	→ p0_rd_count[6:0]
p0_wr_mask[15:0]	→ p0_rd_overflow
p0_wr_data[127:0]	→ p0_rd_error
	→ p0_wr_full
	→ p0_wr_empty
	→ p0_wr_count[6:0]
	→ p0_wr_underrun
	→ p0_wr_error

< Back Next> Cancel

■ Select

- One 128-bit bi-directional Port

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Controller Options ✓
C3

Memory Options ✓
C3

Multi-port Configuration ✓
C3

Arbitration
C3

FPGA Options
C3

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Arbitration for C3 - DDR3 SDRAM

Select either round robin or custom for port arbitration. You can alter the port priorities in custom arbitration. For each time slot, the leftmost port number has the highest priority. The order of port priority decreases from left to right. Each port should be given highest priority in at least one time slot. Below ports will be set to a warning symbol if the port is not given highest priority in at least one time slot.

Select Arbitration Algorithm: Round Robin

Timeslot 0	0
Timeslot 1	0
Timeslot 2	0
Timeslot 3	0
Timeslot 4	0
Timeslot 5	0
Timeslot 6	0
Timeslot 7	0
Timeslot 8	0
Timeslot 9	0
Timeslot 10	0
Timeslot 11	0

Port0 ✓

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User Guide MCB User Guide Version Info < Back Next> Cancel

- Leave this page as is
 - Click Next

Generate MIG Example Design

FPGA Options for C3 - DDR3 SDRAM

Memory Interface Pin Termination

☒ **Calibrated Input Termination:** Provides calibrated on-die input termination resistors. Calibration requires two extra pins to be added to the interface: RZQ and ZIO. An external resistor with a value 2x trace impedance needs to be connected from RZQ pin to ground, and the ZIO pins need to be left unconnected. These additional pins and their locations will be listed in the generated UCF constraints file.

☐ **Un-calibrated Input Termination:** Provides un-calibrated (approximated) on-die input termination resistors to Vcco and Ground.

☐ **External Input Termination:** Provides discrete termination resistors for the controller on the PCB.

DQ/DQS

Static Calibration Memory Address

For applications that require suspend mode operation, static calibration address space needs to be reserved. This is to allow calibration training pattern to be written to user-specified location and avoid overwriting user application data.

Bank Address(0-7) Row Address(0000-1fff) Column Address(000-3ff)

Bypass Calibration: Turn on this bit if user wants to skip the calibration stage in functional simulation. ☒

Debug Signals for Memory Controller: This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. Debug is

System Clock: Choose the desired input clock configuration.

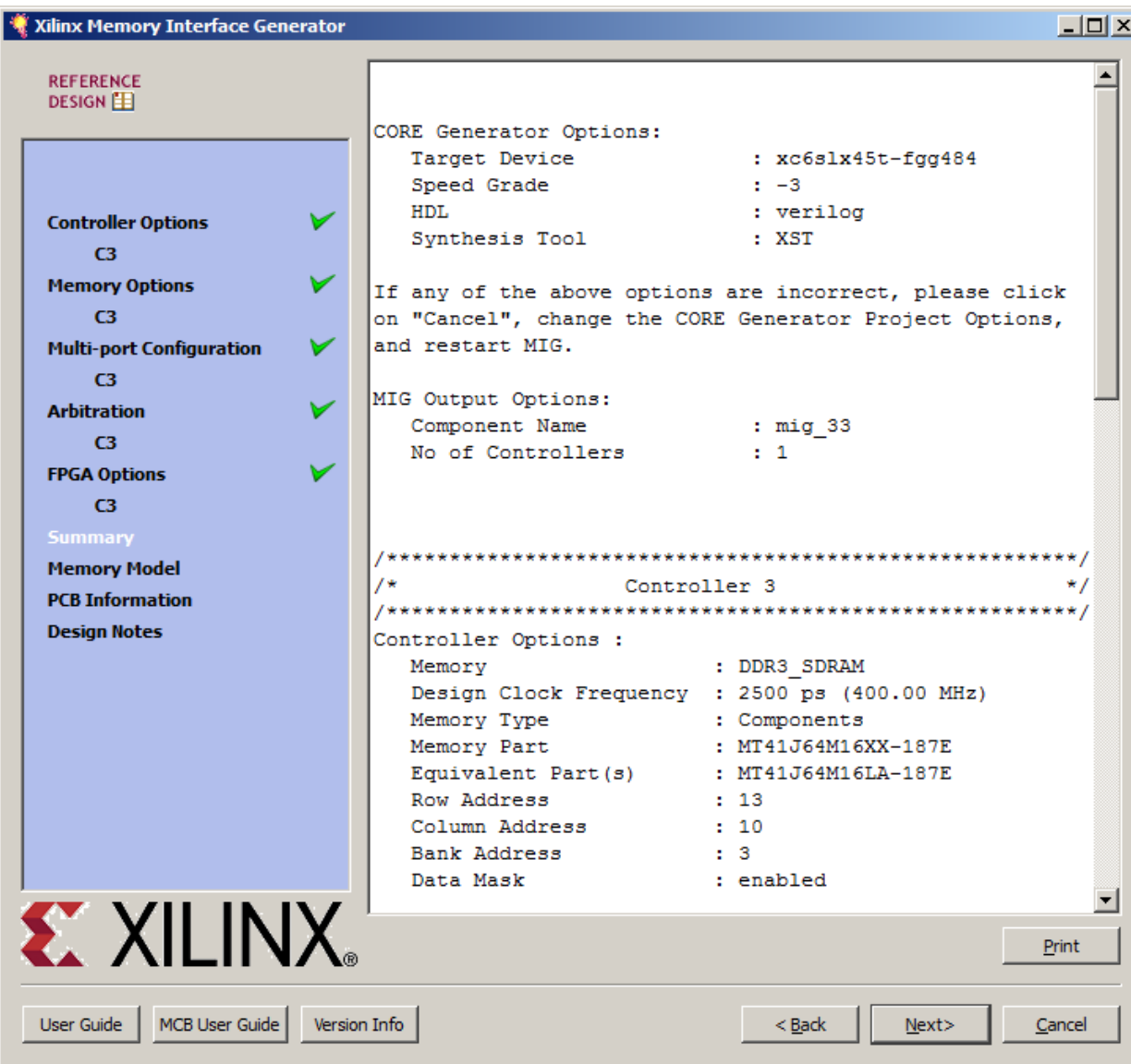
■ Set DQ/DQS

- 50 Ohms
- This sets the design to uncalibrated 50 Ohm termination on DQ/DQS inputs

■ Set Debug Signals

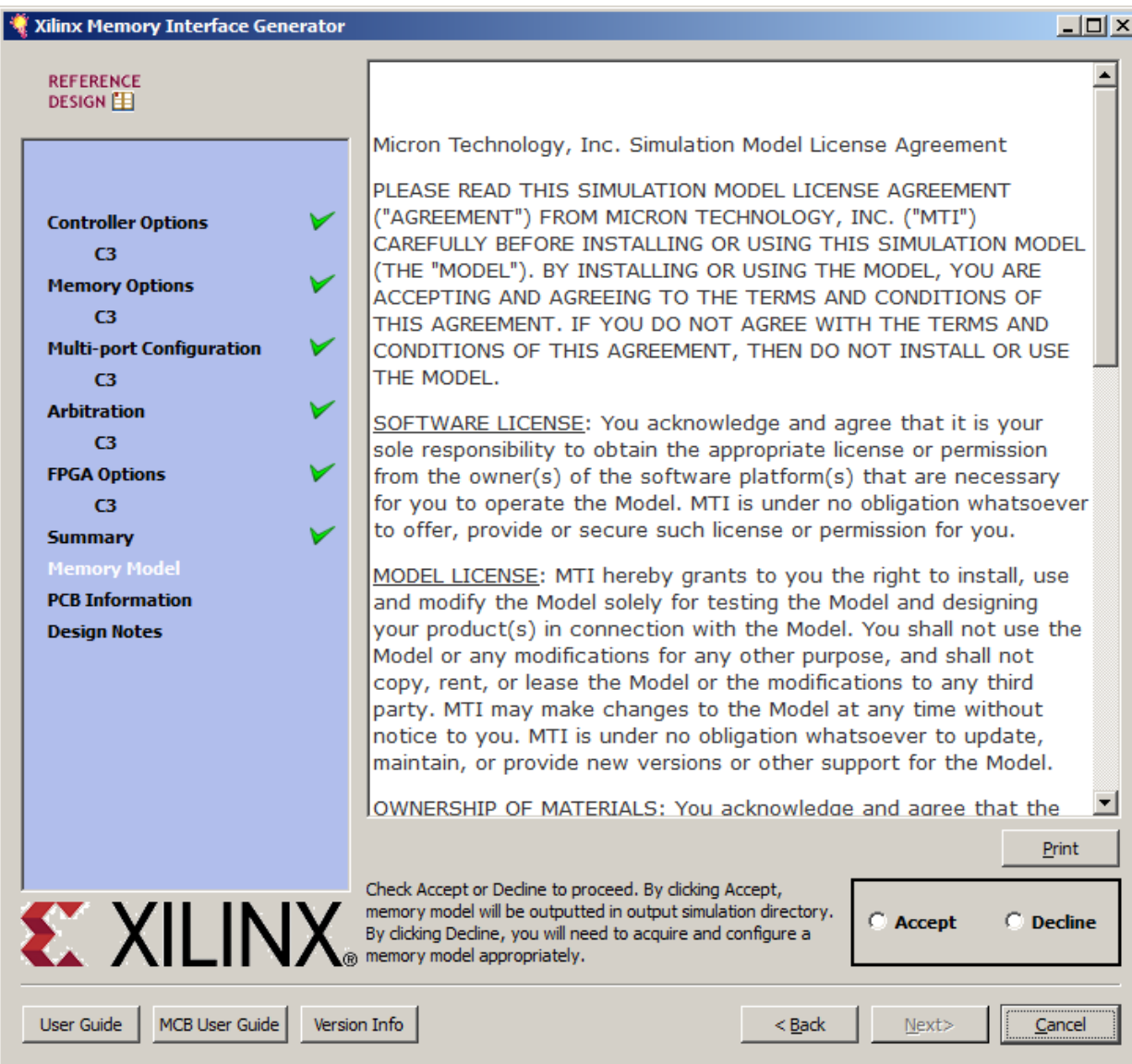
- Enable

Generate MIG Example Design



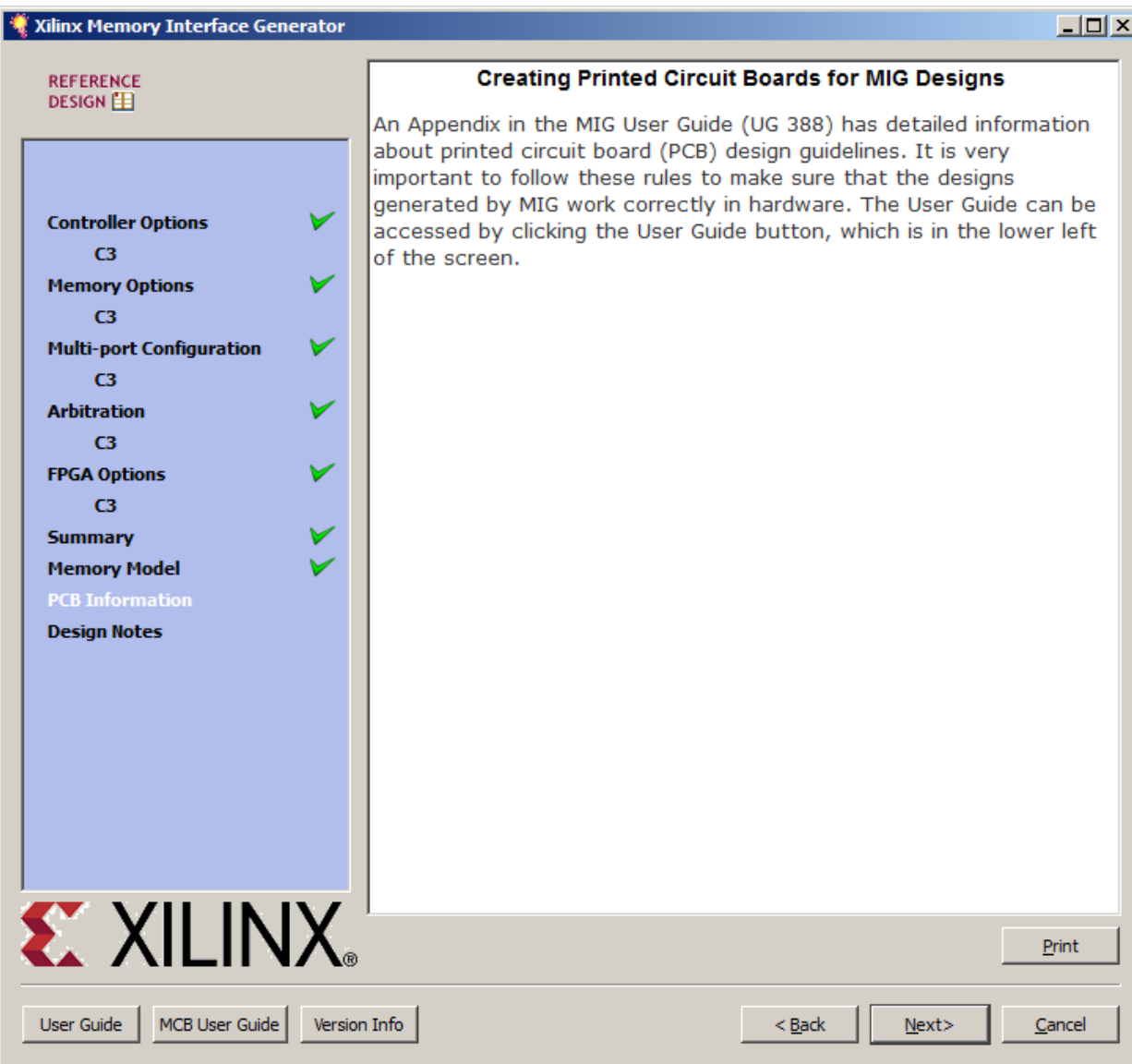
- Leave this page as is
 - Click Next

Generate MIG Example Design



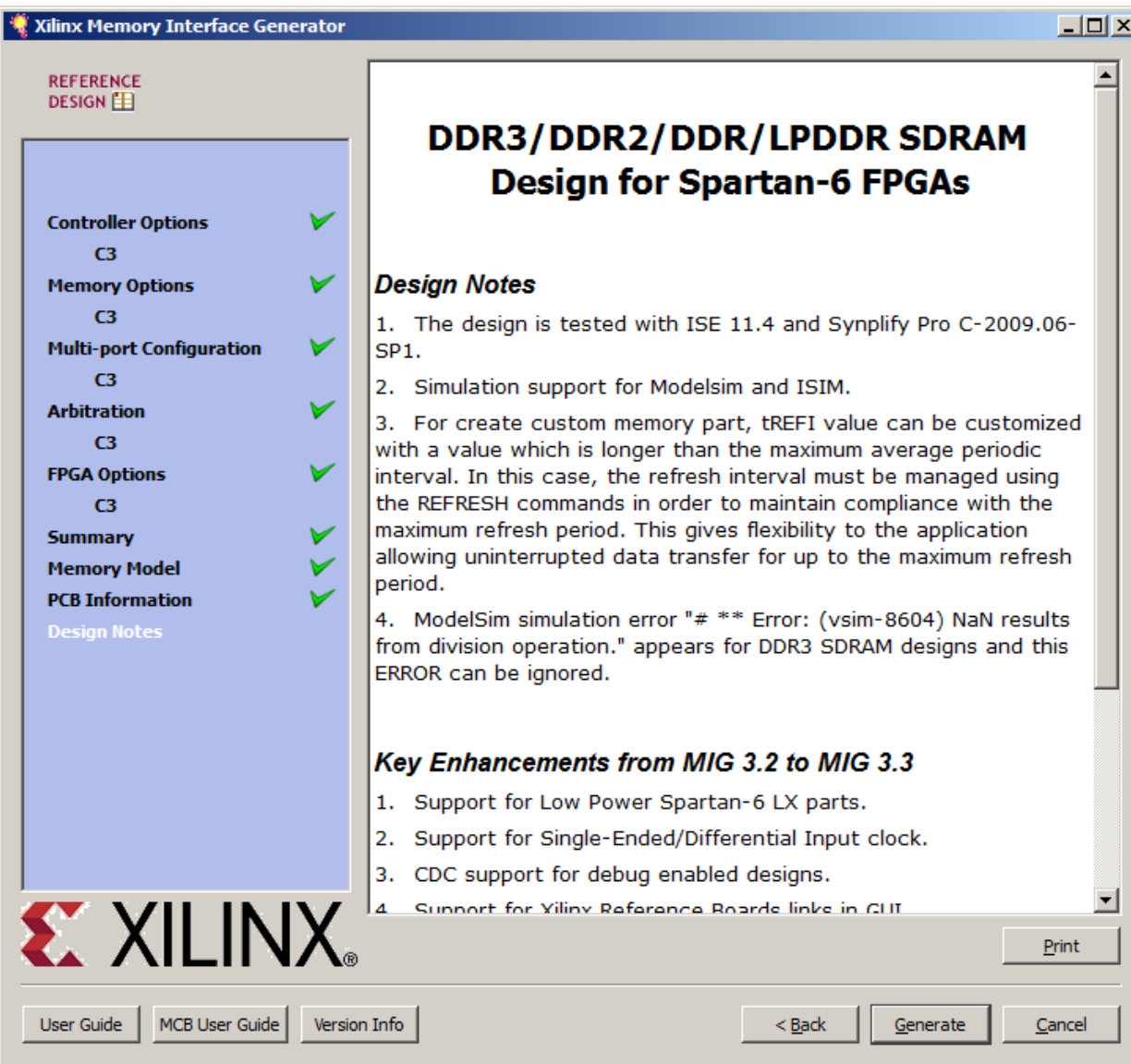
- **Accept Simulation license, if desired**
 - Otherwise, Decline license
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

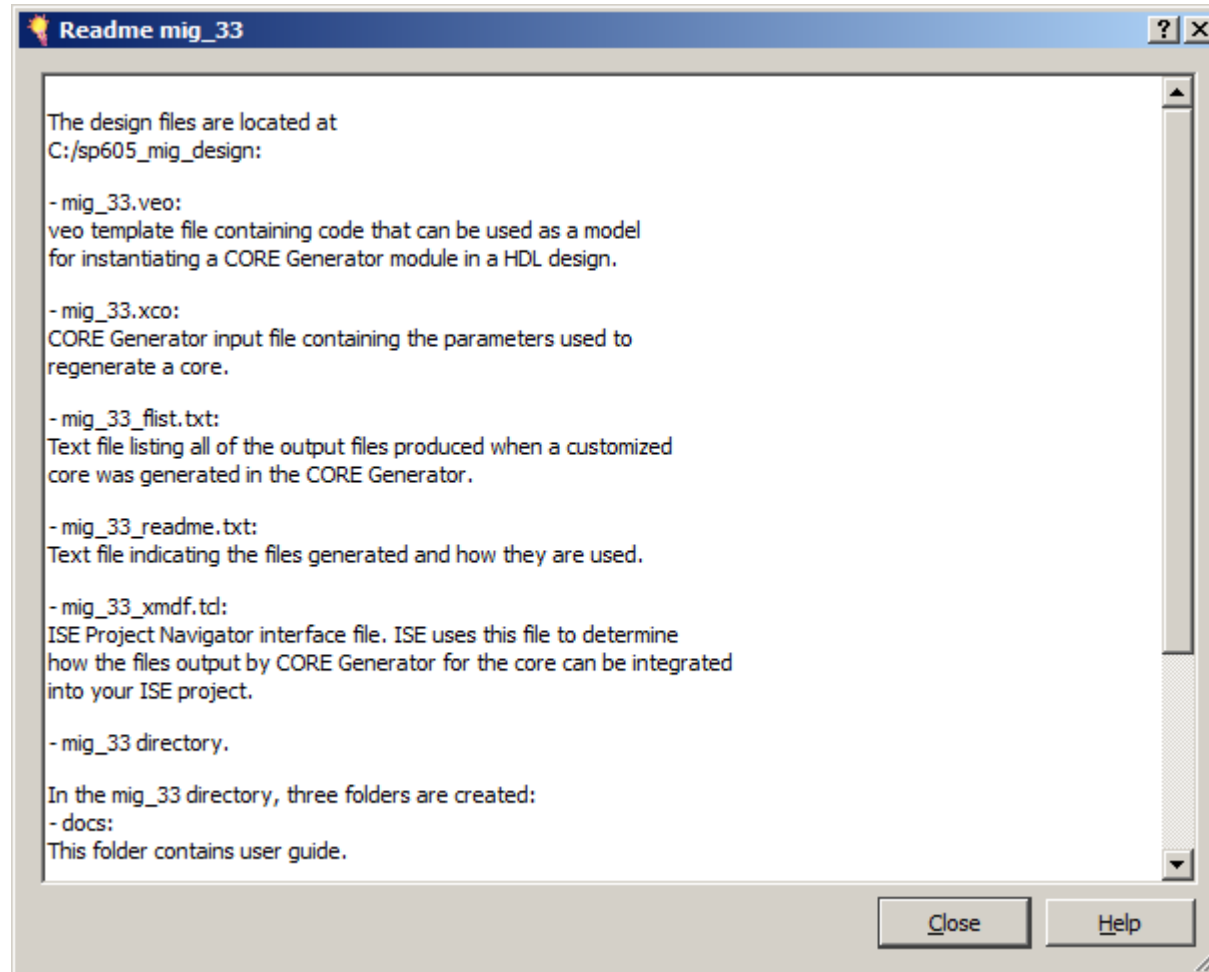
Generate MIG Example Design



■ Click Generate

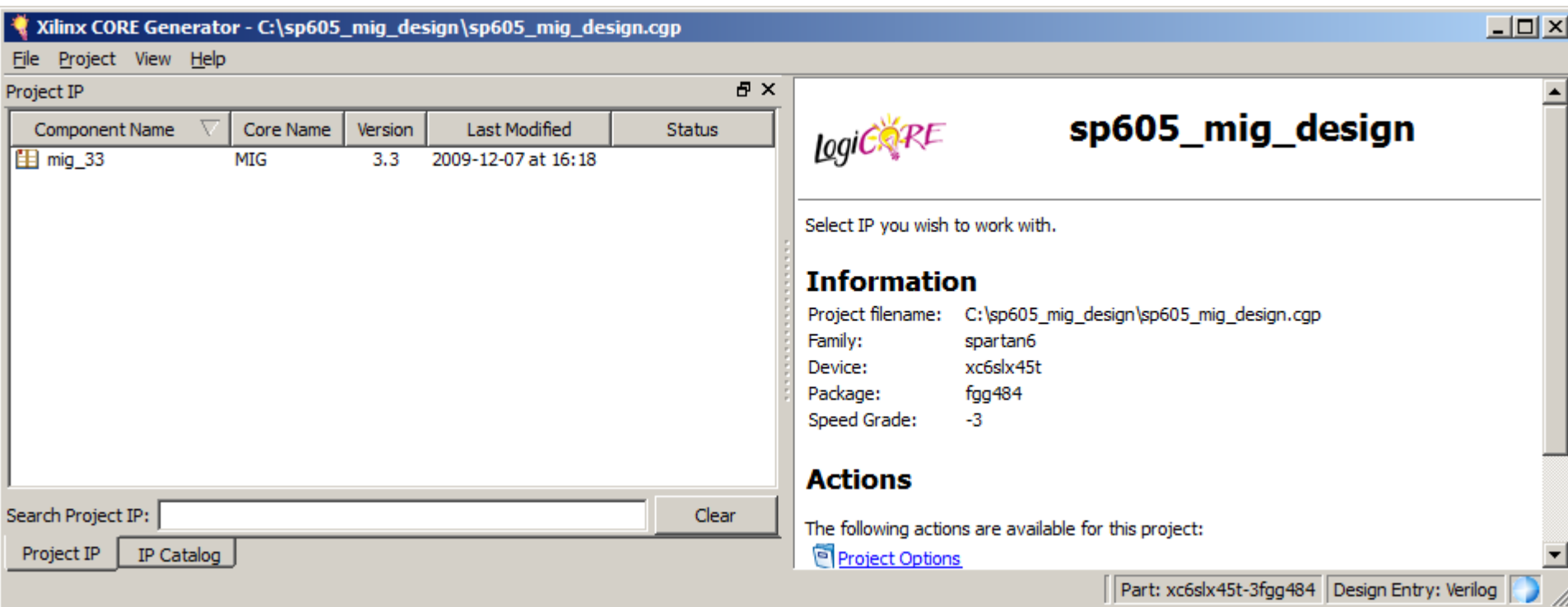
Generate MIG Example Design

- After the MIG core finishes generating, click Close on the Datasheet window



Generate MIG Example Design

- MIG design appears in Project IP



Modifications to Example Design

▪ RDF0029 includes

- ChipScope Project File, UCF, Verilog Files, and pre-built Example Design files

▪ Modifications to RTL Files for SP605 Example Design

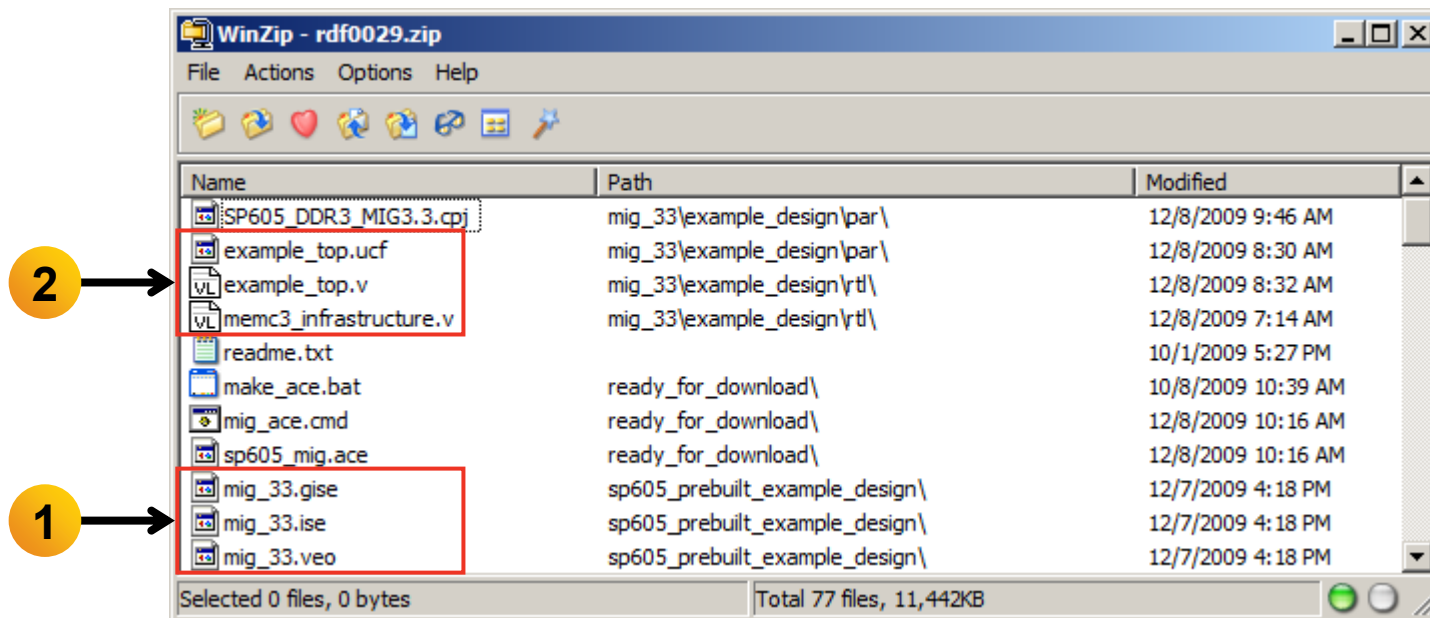
- Added GPIO outputs for visual status indicators with heartbeat clock
 - GPIO LED 3 = Calibration done
 - GPIO LED 2 = PLL locked
 - GPIO LED 1 = Error
 - GPIO LED 0 = Heartbeat (blinking)
- Change CLKFBOUT_MULT to "4" to generate proper clocks:
 - MCB block runs at 800 MHz
 - Traffic Generator runs at 50 MHz
 - Soft calibration clock runs at 100 MHz

Modifications to Example Design

- **Updates to UCF file specifically required for SP605 board:**
 - Changed LOC of 200MHz differential sys_clk inputs
 - Changed LOC of sys_rst_n input to SP605 CPU_RESET switch
 - Added LOC for GPIO LED signals (2.5V bank voltage)
 - Double sys_clk_ibufg period constraint from 2.5ns to 5ns

Modifications to Example Design

- **Unzip the rdf0029.zip file to your C:\sp605_mig_design directory**
 - This adds modifications to the example design
 - A fully pre-built SP605 example design is included in the zip file (1)
 - Use the included bitstream to [run MIG with ChipScope](#)
 - Run **ise_flow.bat** in <design directory>\sp605_pre-built_example_design\mig_33\example_design\par to recompile the pre-built example design

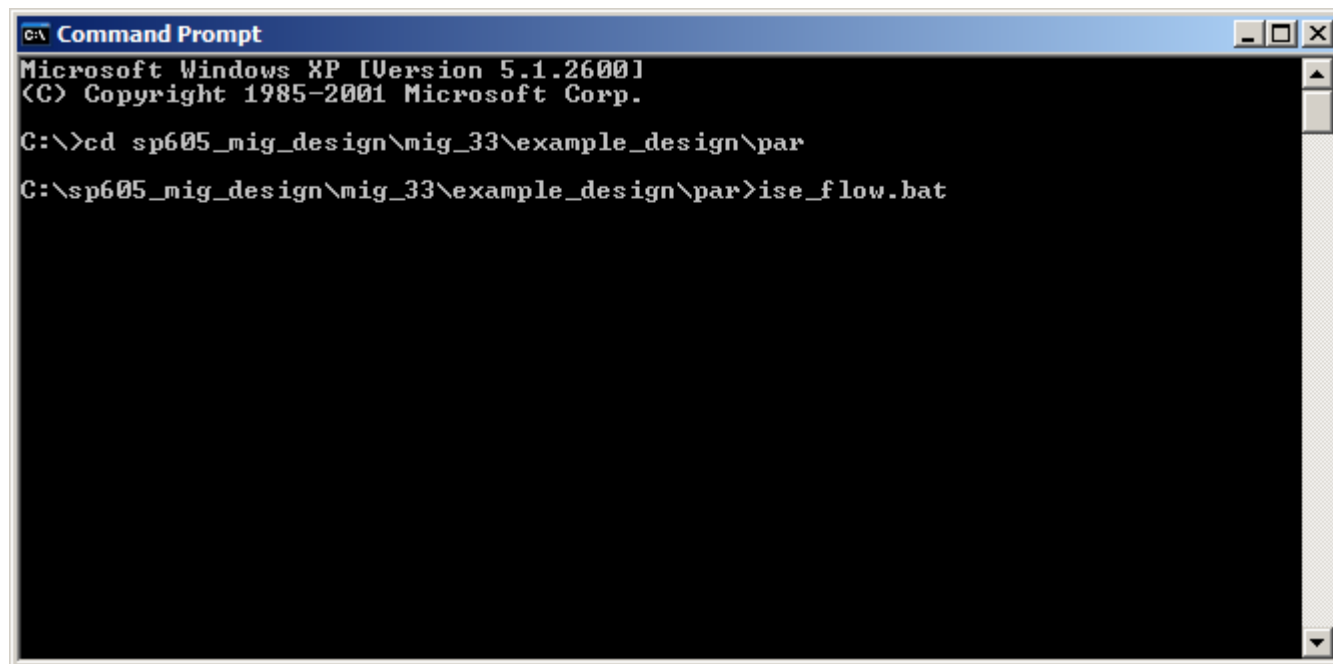


Note: Overwrites Core Generator output files with SP605 specific files (2)

Compile Example Design

- Start a windows command shell and enter these commands:

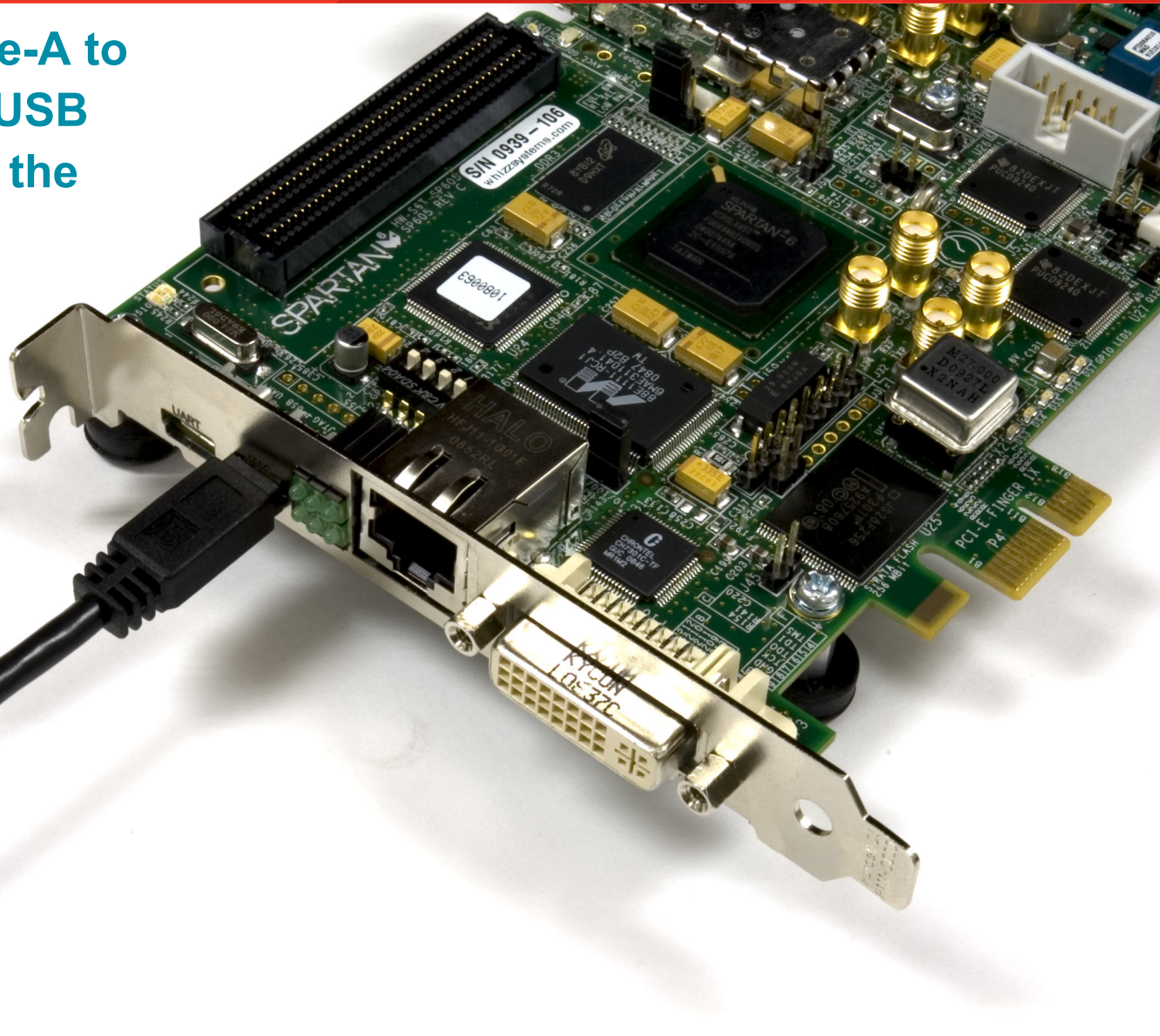
```
cd sp605_mig_design\mig_33\example_design\par  
ise_flow.bat
```



```
Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd sp605_mig_design\mig_33\example_design\par  
C:\sp605_mig_design\mig_33\example_design\par>ise_flow.bat
```

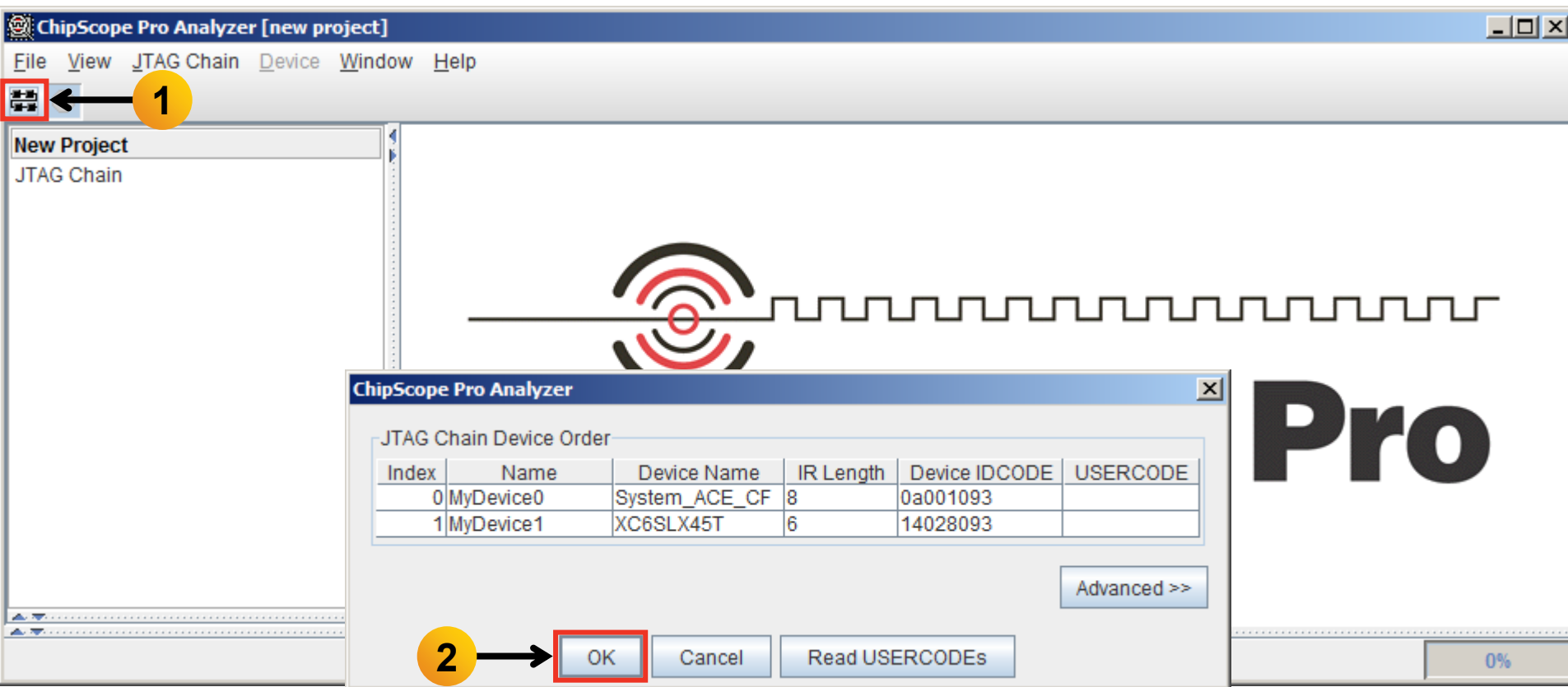
Setup for the SP605 MIG Designs

- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the SP605 board**
 - Connect this cable to your PC



Running the SP605 MIG Design

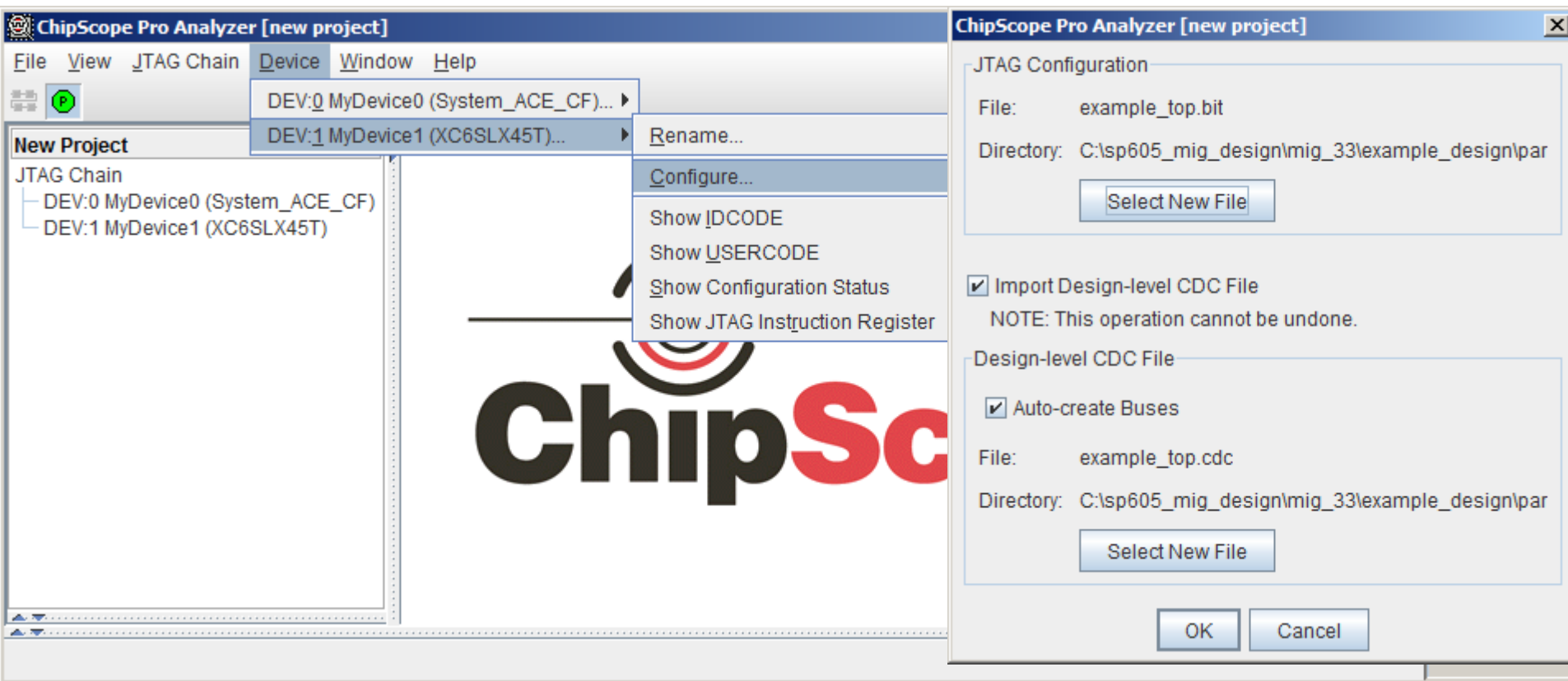
- Open ChipScope Pro and click on the Open Cable Button (1)
- Click OK (2)



Note: Presentation applies to the SP605

Running the SP605 MIG Design

- Select Device → DEV:1 MyDevice1 (XC6SLX45T) → Configure...
- Select <Design Path >\mig_33\example_design\par\example_top.bit



ChipScope Pro Setup

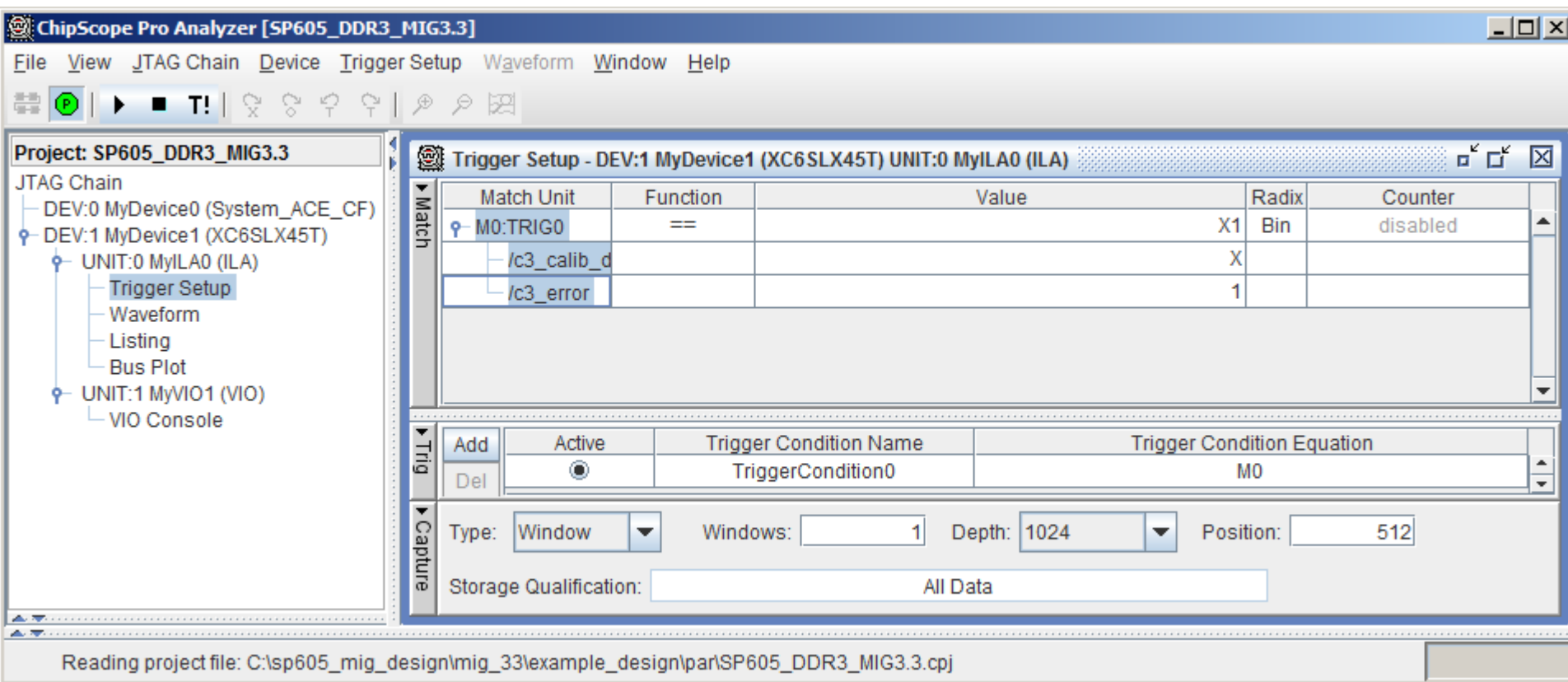
- **Select File → Open Project...**
- **Select <Design Path>\mig_33\example_design\par\SP605_DDR3_MIG3.3.cpj**



Note: Presentation applies to the SP605

Run MIG Example Design

- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1



ChipScope Pro Analyzer [SP605_DDR3_MIG3.3]

File View JTAG Chain Device Trigger Setup Waveform Window Help

Project: SP605_DDR3_MIG3.3

JTAG Chain

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6SLX45T)
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - VIO Console

Trigger Setup - DEV:1 MyDevice1 (XC6SLX45T) UNIT:0 MyILA0 (ILA)

Match Unit	Function	Value	Radix	Counter
M0:TRIG0	==		X1	Bin
/c3_calib_d			X	
/c3_error			1	

Trig

Add	Active	Trigger Condition Name	Trigger Condition Equation
Del	<input checked="" type="radio"/>	TriggerCondition0	M0

Capture

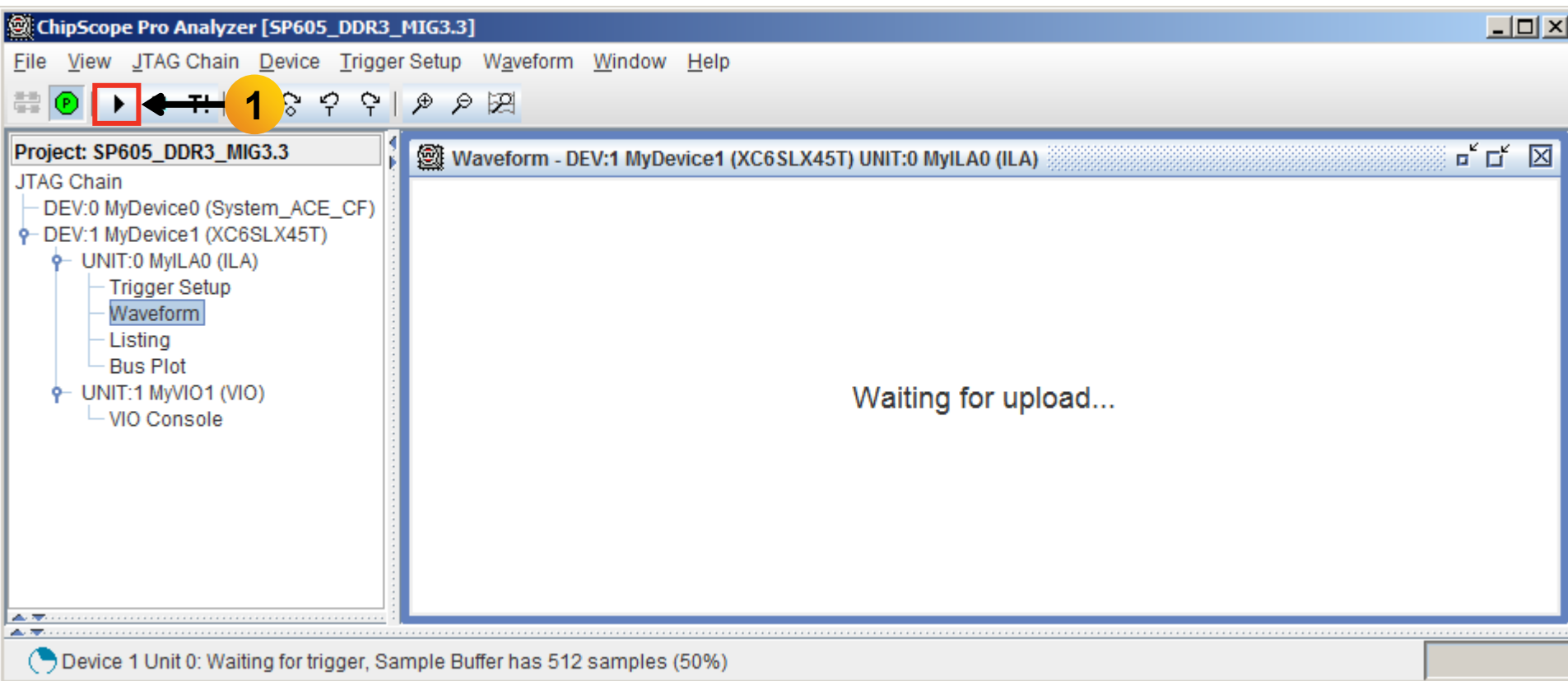
Type: Window Windows: 1 Depth: 1024 Position: 512

Storage Qualification: All Data

Reading project file: C:\sp605_mig_design\mig_33\example_design\par\SP605_DDR3_MIG3.3.cpj

Run MIG Example Design

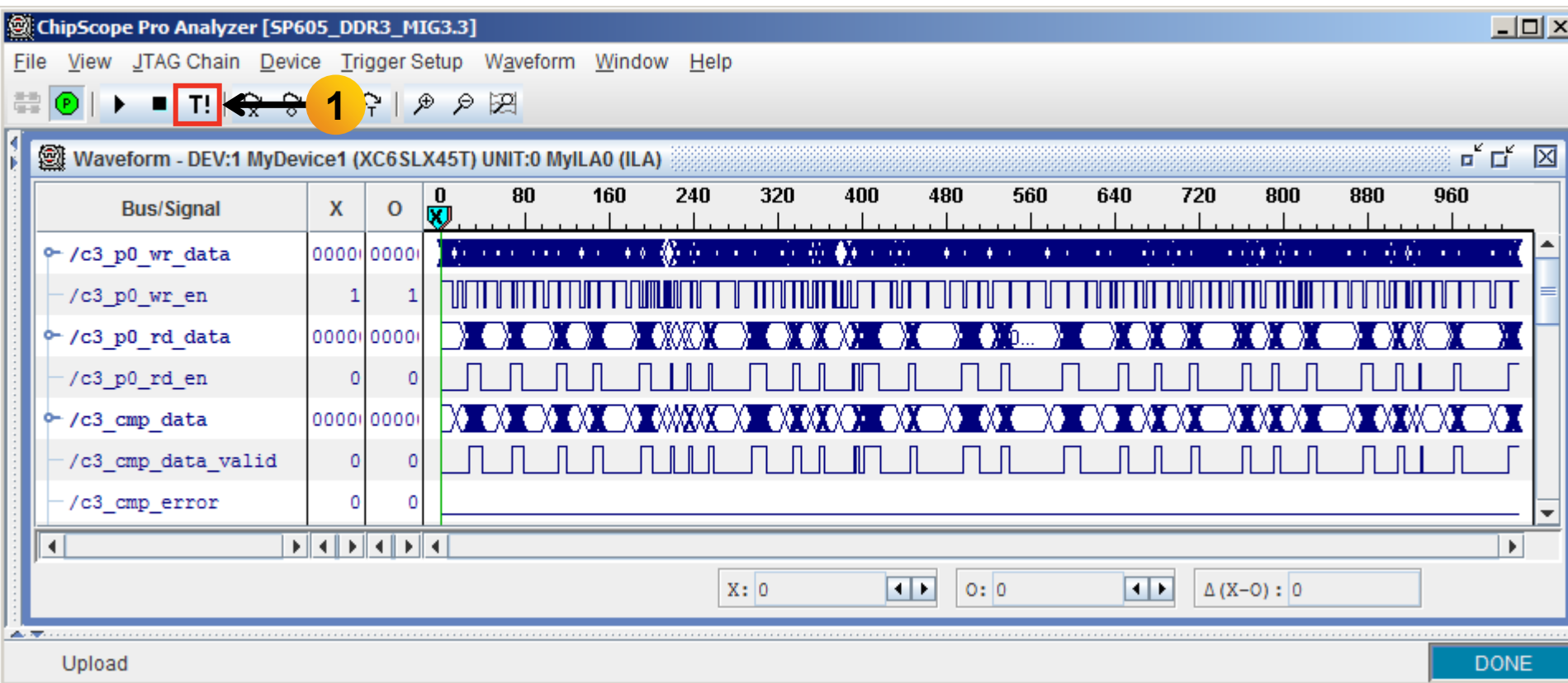
- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger



Note: Presentation applies to the SP605

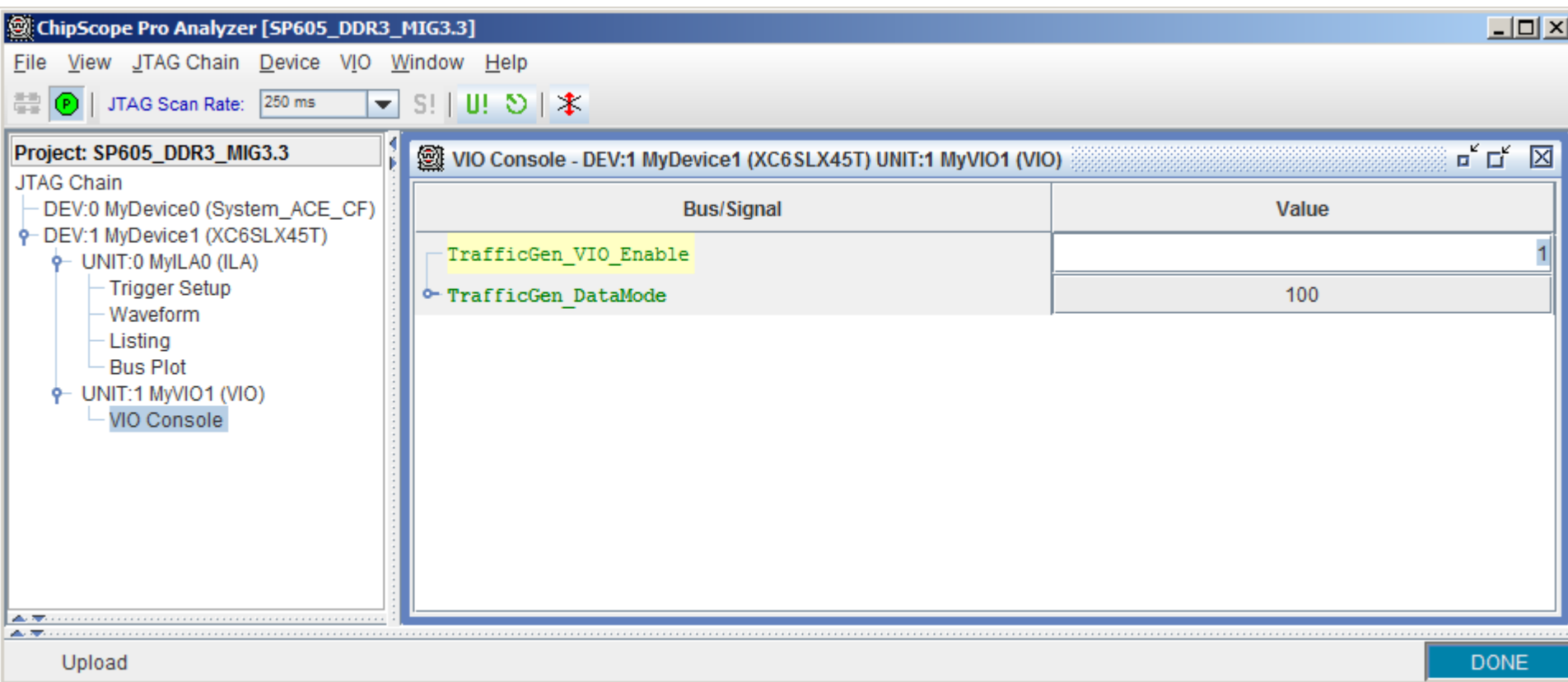
Run MIG Example Design

- The Example Design should run error free (no trigger on error)
- To force a trigger, click the T! button (1)



Adjust Data Pattern using VIO Console

- Select VIO Console
- Set TrafficGen_VIO_Enable to 1



The screenshot displays the ChipScope Pro Analyzer interface for project SP605_DDR3_MIG3.3. The left pane shows the JTAG Chain with the following structure:

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6SLX45T)
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - VIO Console

The right pane, titled "VIO Console - DEV:1 MyDevice1 (XC6SLX45T) UNIT:1 MyVIO1 (VIO)", contains a table with the following data:

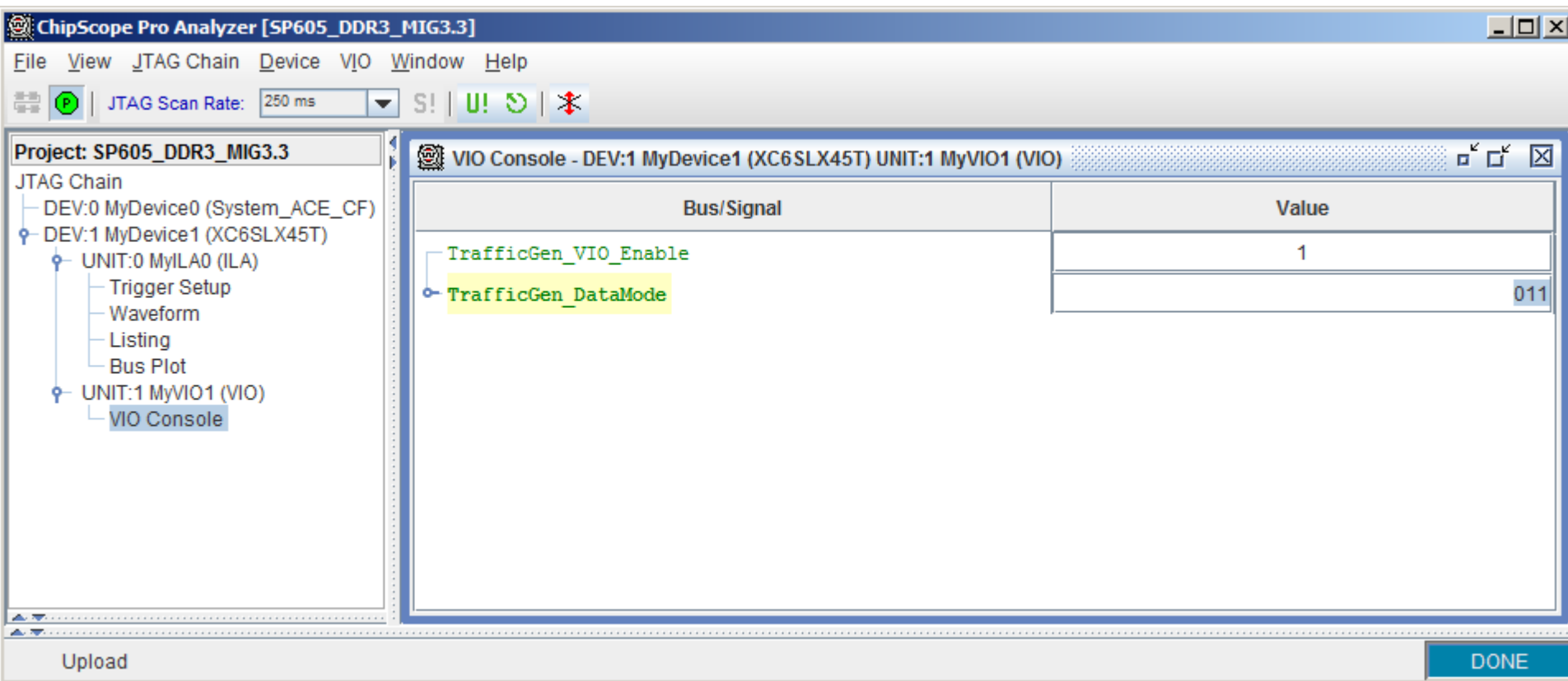
Bus/Signal	Value
TrafficGen_VIO_Enable	1
TrafficGen_DataMode	100

The "Upload" button is visible at the bottom left, and the "DONE" button is at the bottom right.

Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

- Set TrafficGen_DataMode to "011" for HAMMER_DATA_MODE



The screenshot displays the ChipScope Pro Analyzer interface for project SP605_DDR3_MIG3.3. The left pane shows the JTAG Chain with the following structure:

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6SLX45T)
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - VIO Console

The right pane shows the VIO Console window for DEV:1 MyDevice1 (XC6SLX45T) UNIT:1 MyVIO1 (VIO). It contains a table with the following data:

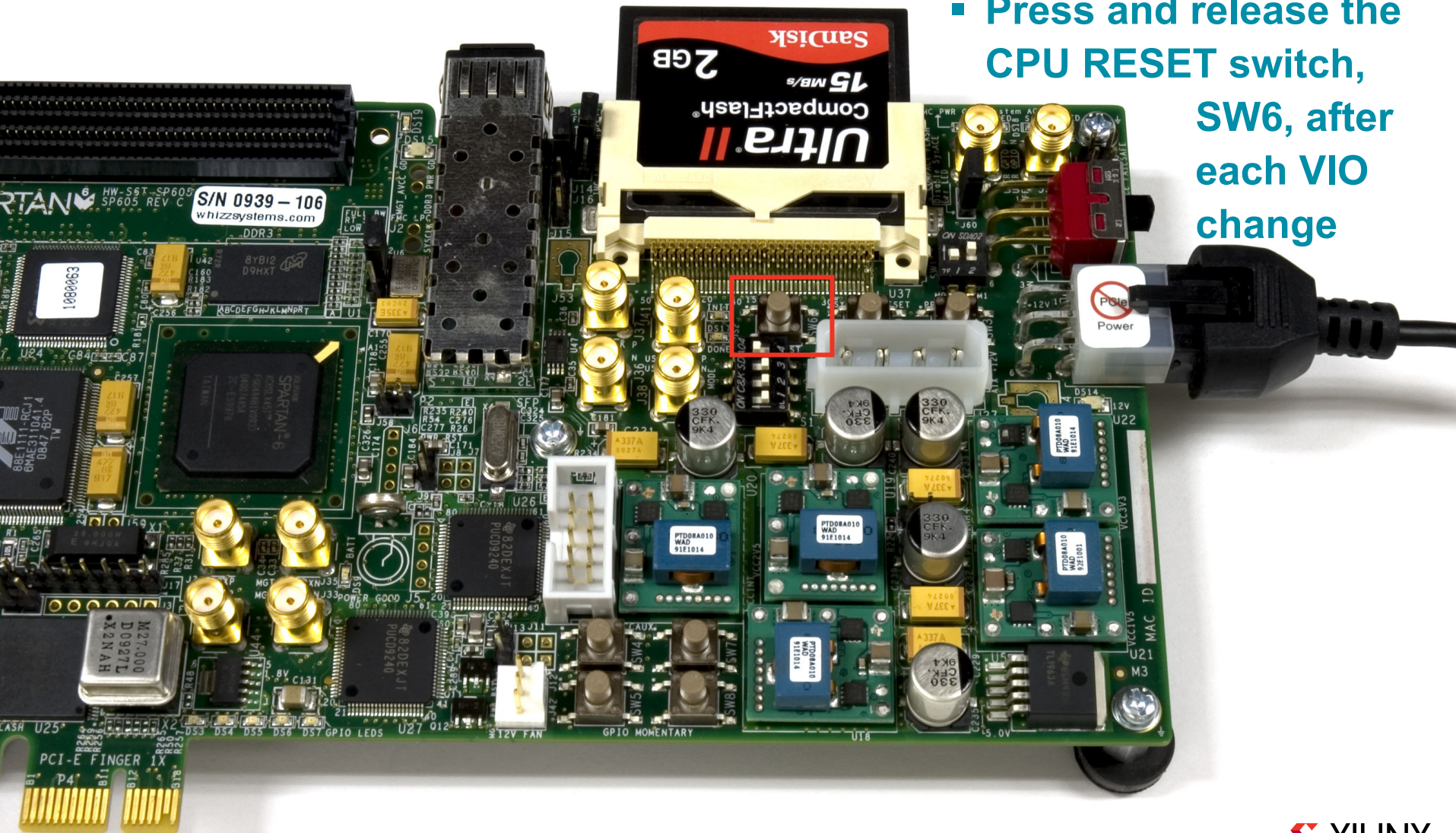
Bus/Signal	Value
TrafficGen_VIO_Enable	1
TrafficGen_DataMode	011

The 'TrafficGen_DataMode' signal is highlighted in yellow. At the bottom of the interface, there is an 'Upload' button on the left and a 'DONE' button on the right.

Note: Presentation applies to the SP605

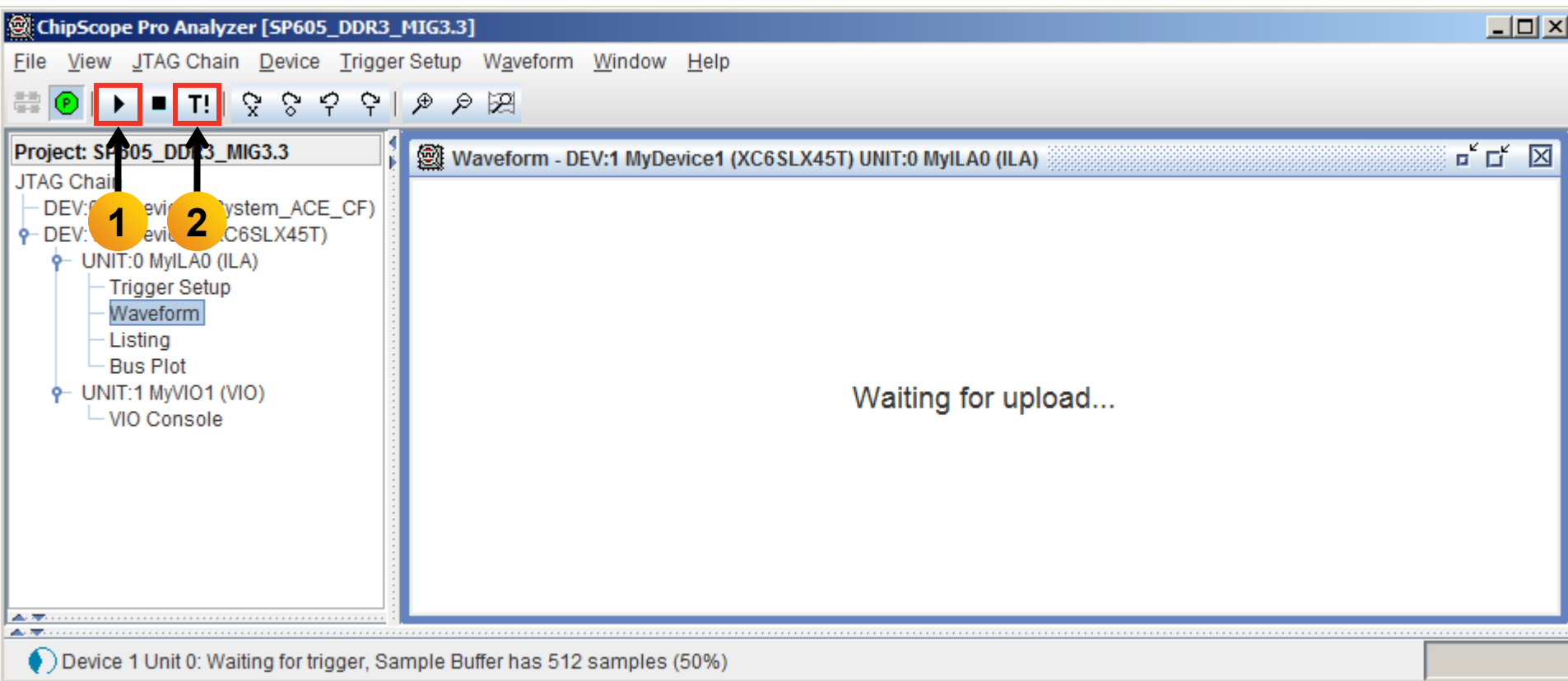
Adjust Data Pattern using VIO Console

- Press and release the CPU RESET switch, SW6, after each VIO change



Run MIG Example Design

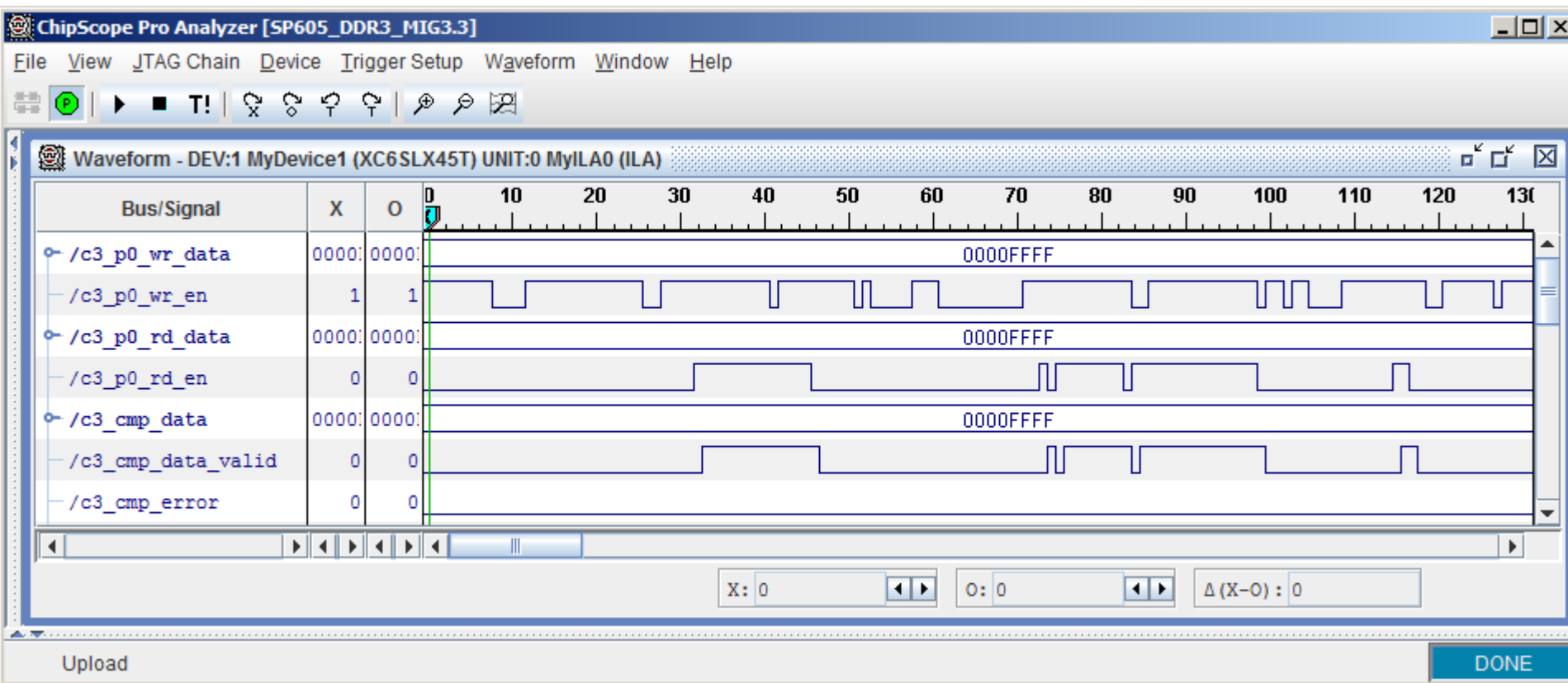
- Click on Waveform; click the Arm Trigger button (1)
- Force a trigger by clicking the T! button (2)



Adjust Data Pattern using VIO Console

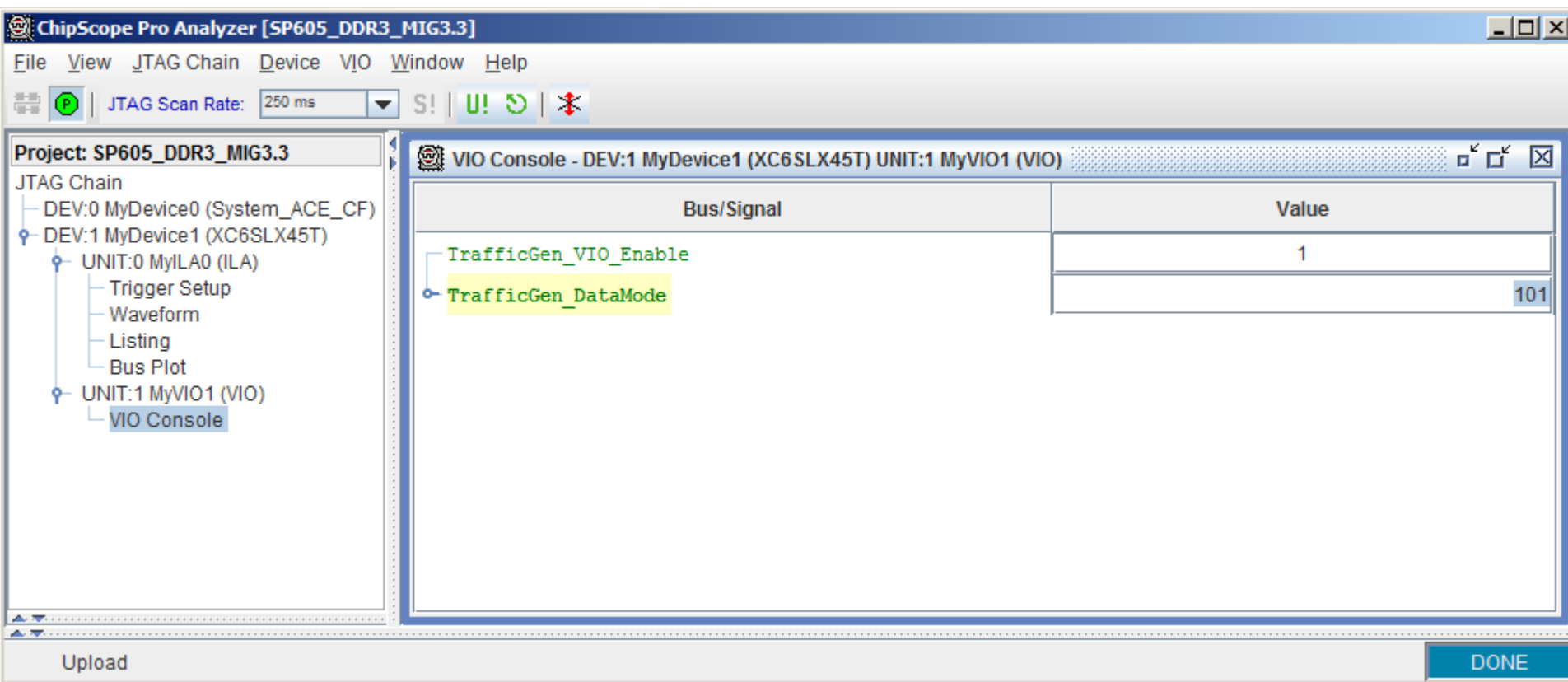
▪ Hammer Data Mode

- 16 bit DQ data bus changes all bits on each cycle, “hammering” the bus
- Read data compared with ‘expected’ data and error generated on mismatch



Adjust Data Pattern using VIO Console

- Set TrafficGen_DataMode to "101" for WALKING1_DATA_MODE
- Push CPU Reset, click Arm Trigger button, click T! button



The screenshot shows the ChipScope Pro Analyzer interface for project SP605_DDR3_MIG3.3. The VIO Console window is open, displaying a table with two rows of data:

Bus/Signal	Value
TrafficGen_VIO_Enable	1
TrafficGen_DataMode	101

The VIO Console window title is "VIO Console - DEV:1 MyDevice1 (XC6SLX45T) UNIT:1 MyVIO1 (VIO)". The left sidebar shows the JTAG Chain with the following structure:

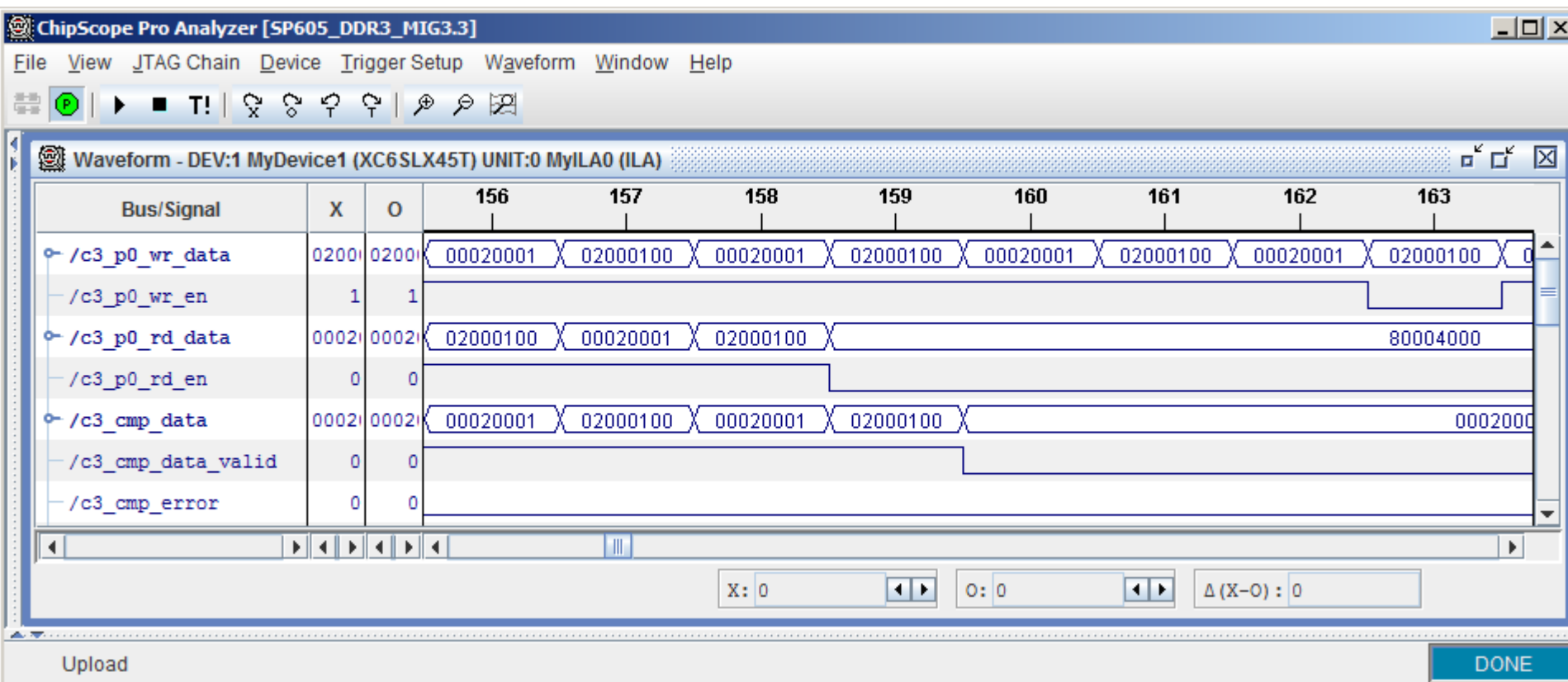
- Project: SP605_DDR3_MIG3.3
 - JTAG Chain
 - DEV:0 MyDevice0 (System_ACE_CF)
 - DEV:1 MyDevice1 (XC6SLX45T)
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - VIO Console

The bottom of the interface has an "Upload" button and a "DONE" button.

Note: Presentation applies to the SP605

Adjust Data Pattern using VIO Console

- Walking 1s Data Mode



Adjust Data Pattern using VIO Console

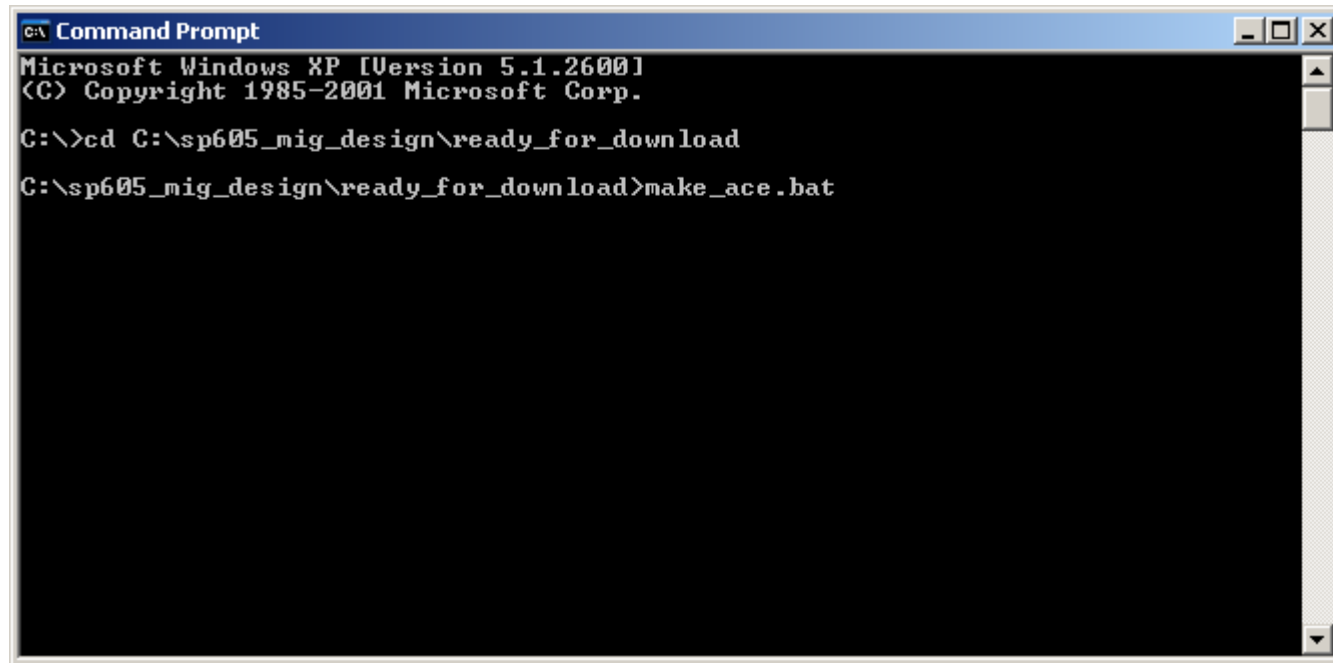
- See [UG388](#) for more details on the available data patterns

– ADDR_DATA_MODE	=	3'b010;
– HAMMER_DATA_MODE	=	3'b011;
– NEIGHBOR_DATA_MODE	=	3'b100;
– WALKING1_DATA_MODE	=	3'b101;
– WALKING0_DATA_MODE	=	3'b110;
– PRBS_DATA_MODE	=	3'b111;

Generate MIG ACE File (Optional)

- Type these commands in a windows command shell:

```
cd C:\sp605_mig_design\ready_for_download  
make_ace.bat
```



A screenshot of a Windows Command Prompt window. The title bar reads "C:\ Command Prompt". The window content shows the following text: "Microsoft Windows XP [Version 5.1.2600] (C) Copyright 1985-2001 Microsoft Corp." followed by a prompt "C:\>". The user has entered "cd C:\sp605_mig_design\ready_for_download" and the prompt has moved to the new directory. The user has then entered "make_ace.bat" and the command has been executed, with no output visible.

```
C:\>cd C:\sp605_mig_design\ready_for_download  
C:\sp605_mig_design\ready_for_download>make_ace.bat
```

References

References

- **Spartan-6**

- Spartan-6 FPGA Memory Controller – UG388

- http://www.xilinx.com/support/documentation/user_guides/ug388.pdf

- **ChipScope Pro**

- ChipScope Pro Software and Cores User Guide

- http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/chipscope_pro_sw_cores_ug029.pdf

Documentation

Documentation

- **Spartan-6**

- Spartan-6 FPGA Family

- <http://www.xilinx.com/products/spartan6/index.htm>

- **SP605 Documentation**

- Spartan-6 FPGA SP605 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-S6-SP605-G.htm>

- SP605 Hardware User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug526.pdf

- SP605 Reference Design User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug527.pdf