

SP605 Built-In Self Test Flash Application

December 2009

Overview

- **Xilinx SP605 Board**
- **Software Requirements**
- **SP605 Setup**
- **SP605 BIST (Built-In Self Test)**
- **Compile SP605 BIST Design**
- **Program SP605 BPI**
- **References**

Note: This presentation applies to the SP605

SP605 BIST Design Description

▪ Description

- The Built-In System Test (BIST) application uses an EDK MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

▪ Reference Design IP

- EDK IP: MicroBlaze, plb_v46, lmb_v10, mdm, lmb_bram_if_cntlr, bram_block, xps_bram_if_cntlr, xps_uart16550, xps_gpio, clock_generator, mpmc, proc_sys_reset, xps_intc, xps_timer, xps_iic, xps_mch_emc, xps_spi, util_io_mux, util_bus_split, xps_ethernetlite
 - [Embedded System Tools Reference Guide](#) (UG111)
 - http://www.xilinx.com/ise/embedded/edk_ip.htm

▪ Reference Design Source

- rdf0045.zip

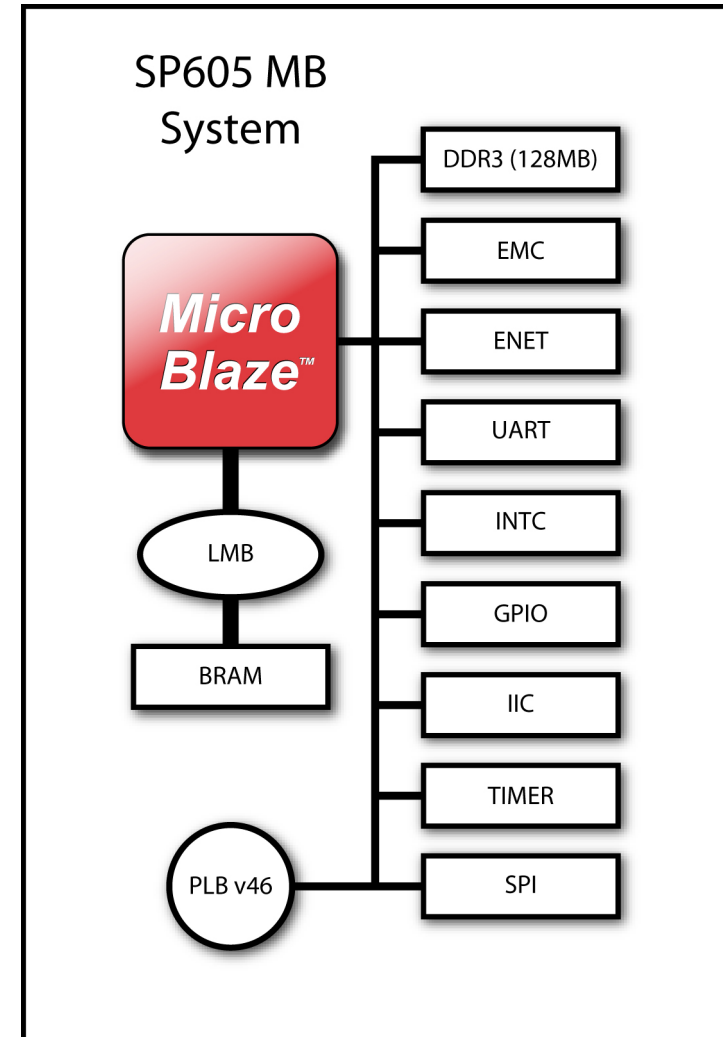
Embedded Processor Design

- **The provided embedded reference design is supported “as is”**
 - Please refer to the click through license agreement
- **Embedded reference design has been verified on the SP605 Evaluation Kit**
 - Design consists of Early Access IP
 - Design may change in subsequent releases
- **The reference design will allow users to:**
 - Re-build and verify functionality on the SP605 evaluation kit

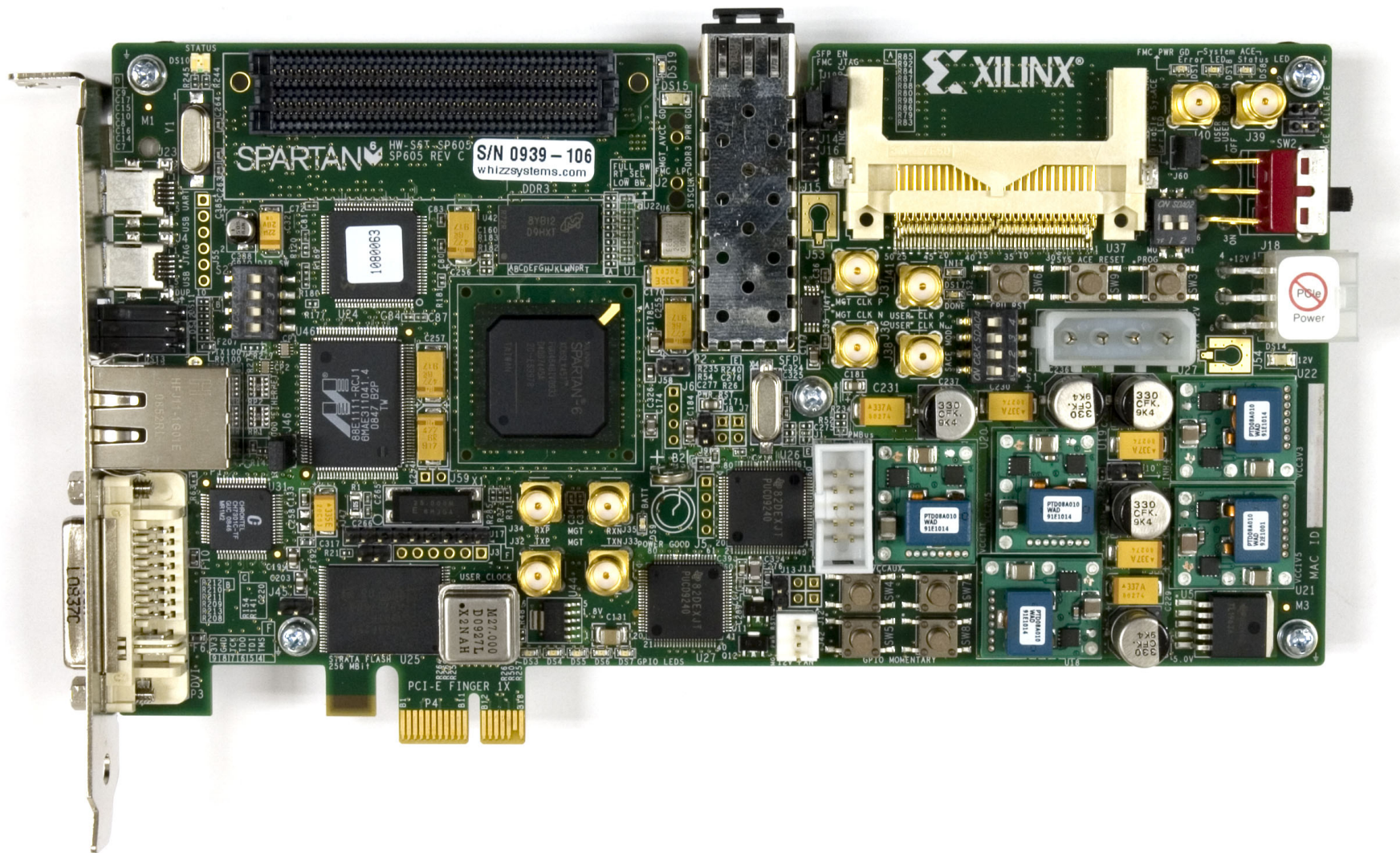
SP605 MicroBlaze Hardware

▪ The SP605 MicroBlaze Design Hardware includes:

- DDR3 Interface (128 MB)
- BRAM
- External Memory Controller (EMC)
 - Flash Memory
- Networking
- UART
- Interrupt Controller
- GPIO (HDR Pins, IIC, LEDs)
- PLB Arbiter
- SPI



Xilinx SP605 Board



ISE Software Requirement

- Xilinx ISE 11.4 software



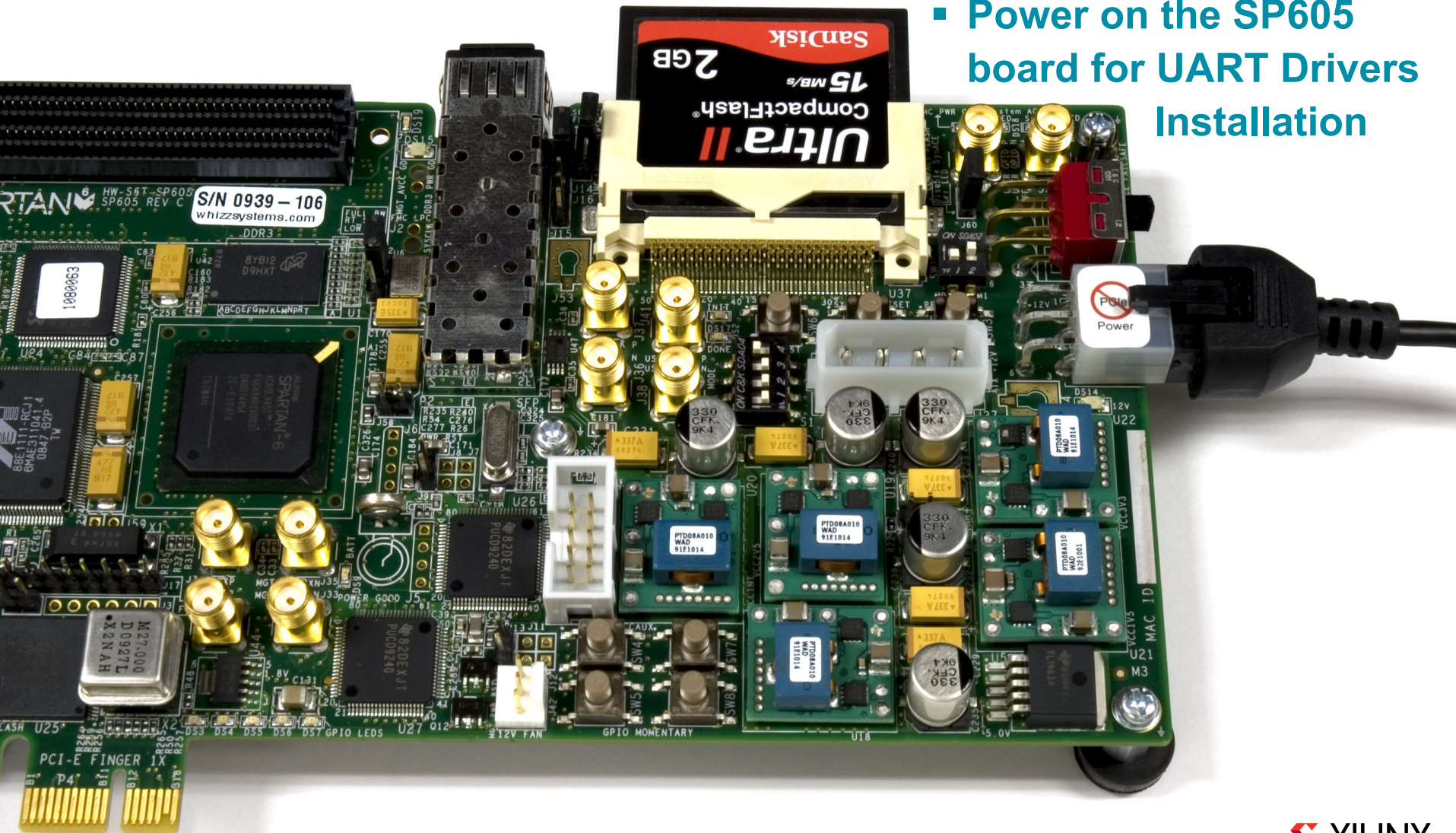
EDK Software Requirement

- Xilinx EDK 11.4 software



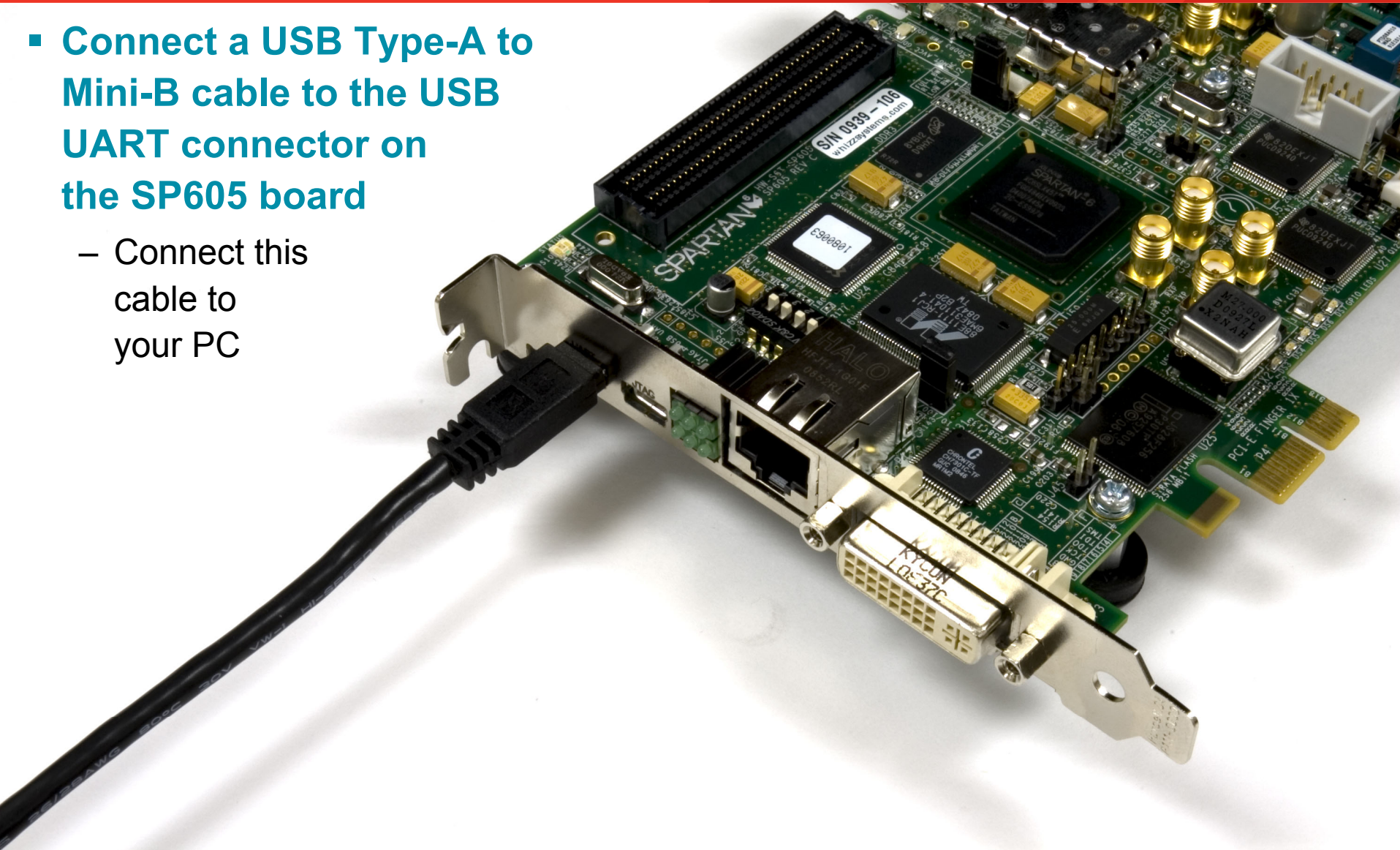
SP605 Setup

- Power on the SP605 board for UART Drivers Installation



Setup for the SP605 IBERT Designs

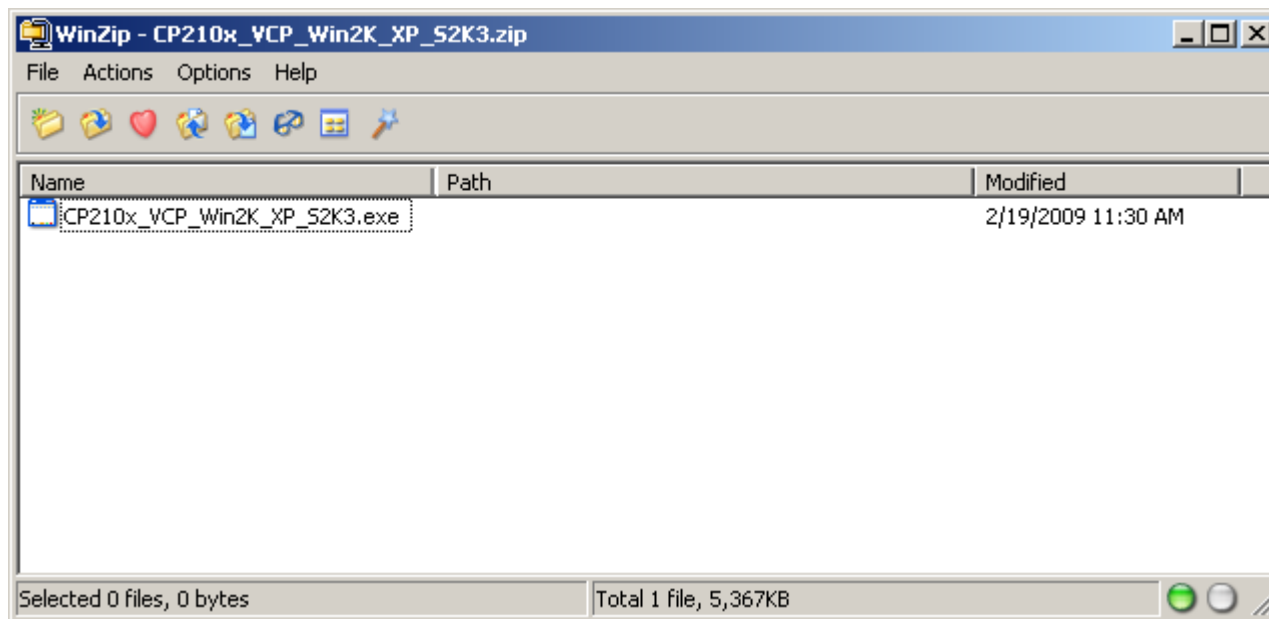
- **Connect a USB Type-A to Mini-B cable to the USB UART connector on the SP605 board**
 - Connect this cable to your PC



SP605 Setup

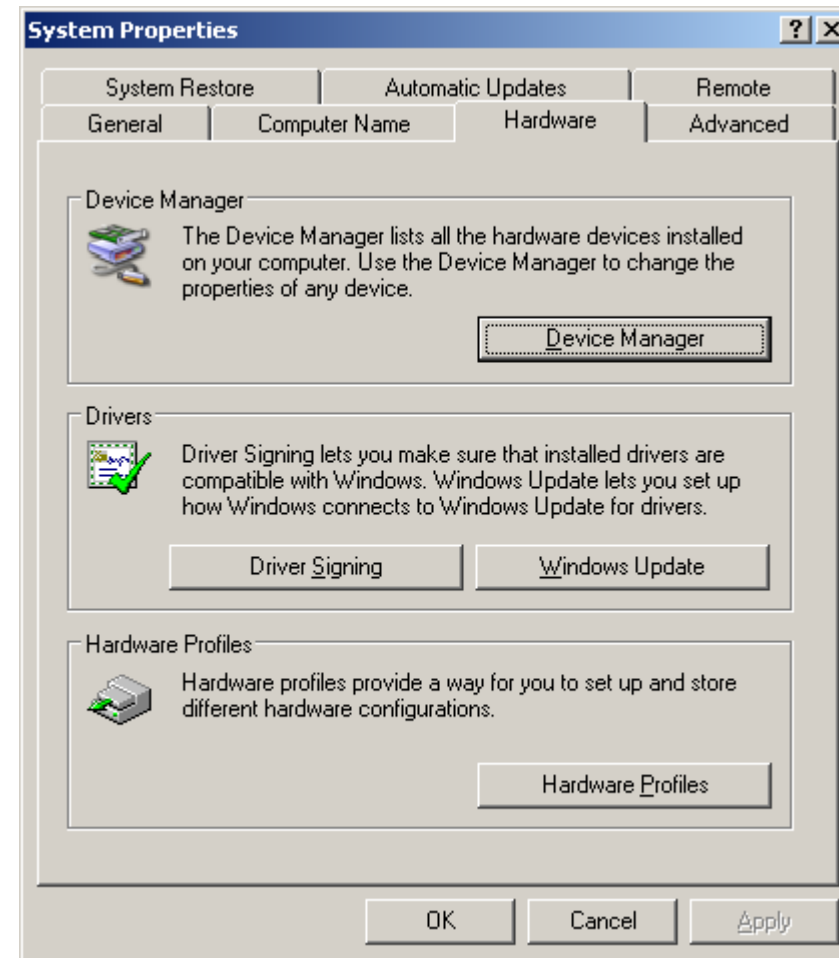
■ Install USB UART Drivers

- https://www.silabs.com/Support Documents/Software/CP210x_VCP_Win2K_XP_S2K3.zip



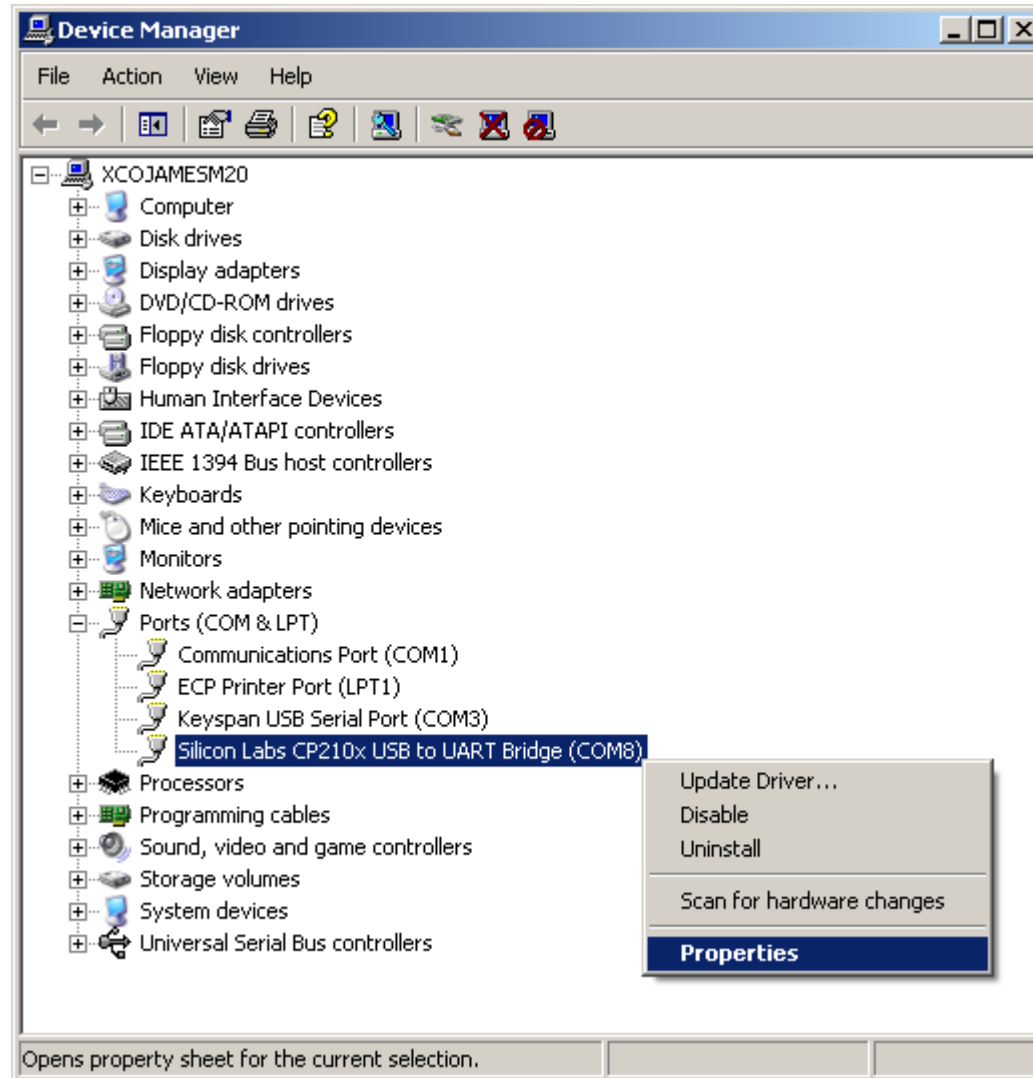
SP605 Setup

- **Right-click on My Computer and select Properties**
 - Select the Hardware tab
 - Click on Device Manager



SP605 Setup

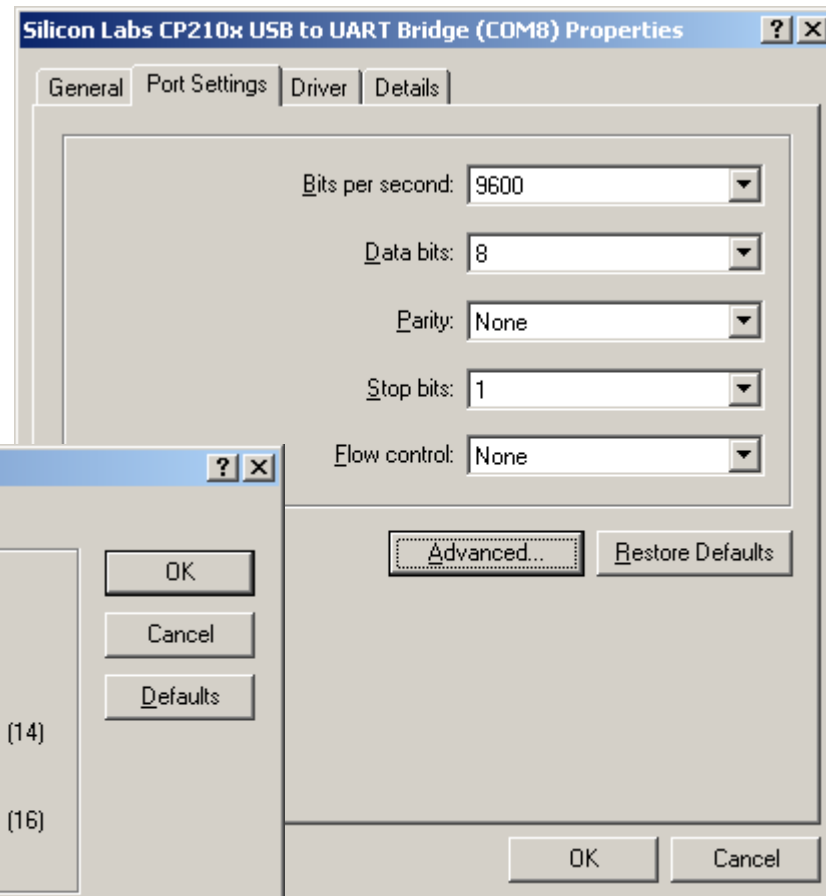
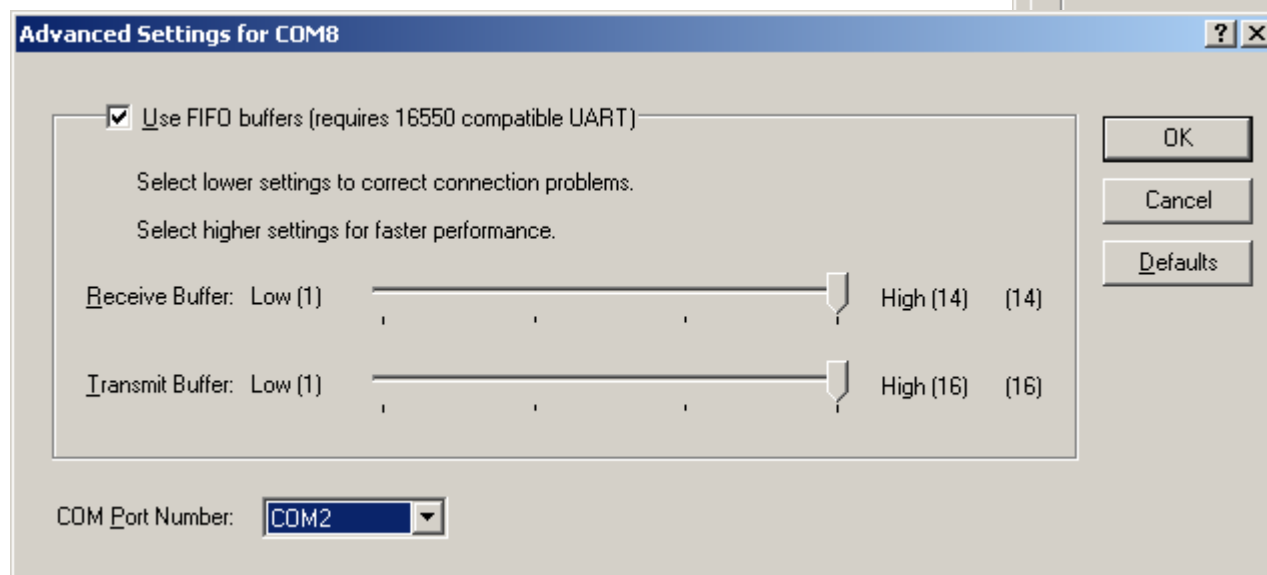
- **Expand the Ports Hardware**
 - Right-click on **Silicon Labs CP210x USB to UART Bridge** and select **Properties**



SP605 Setup

■ Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



SP605 Setup

- Insert SP605 Evaluation Kit CompactFlash



SP605 Setup



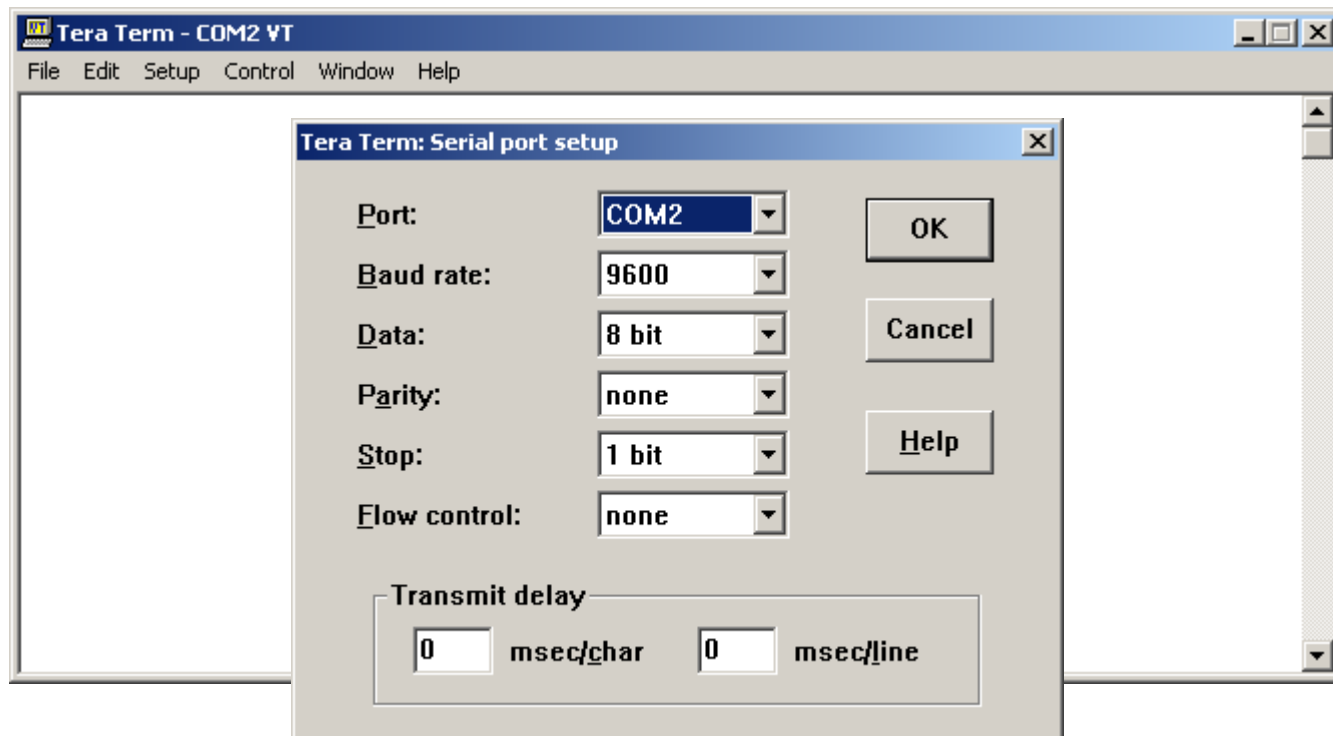
■ Set the mode pins for System ACE

- M0 = 0
- M1 = 1

- Set the System ACE SW1 to 0001 as shown

SP605 BIST Setup

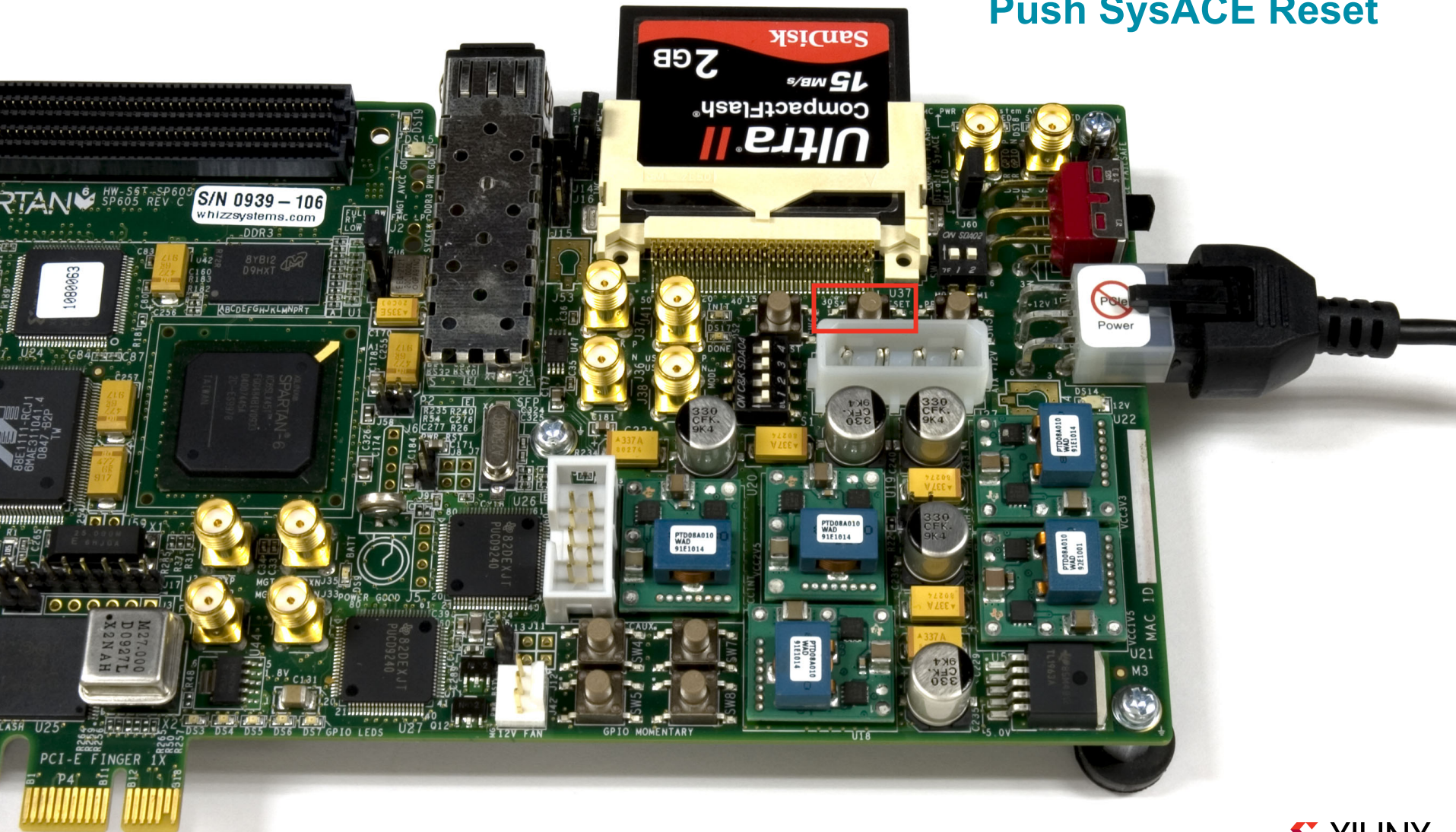
- Board Power must be on before starting Tera Term
- Start the Terminal Program
 - Select your USB Com Port
 - Set the baud to 9600



Note: Tera Term may need to be restarted if board power is cycled

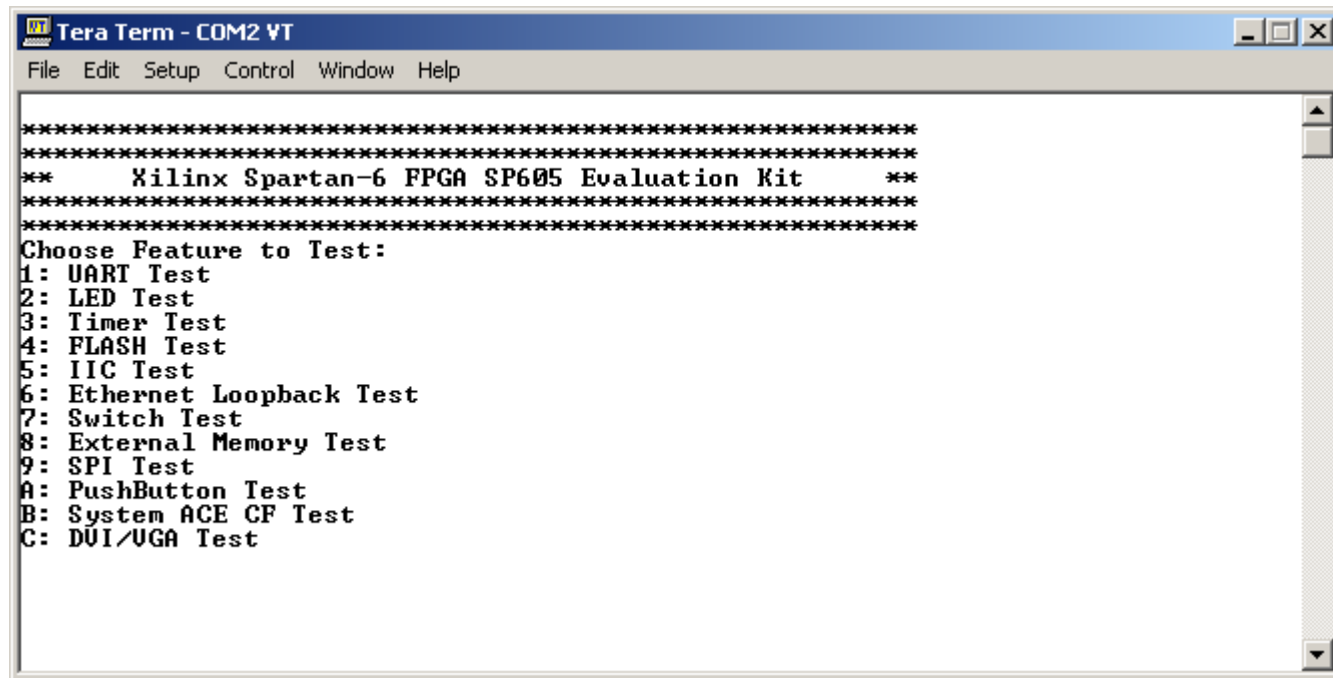
SP605 BIST

Push SysACE Reset



SP605 BIST

- Insert SP605 Evaluation Kit CompactFlash into the SP605
- Push SysACE Reset and view initial BIST screen
 - Type “1” to start the UART Test

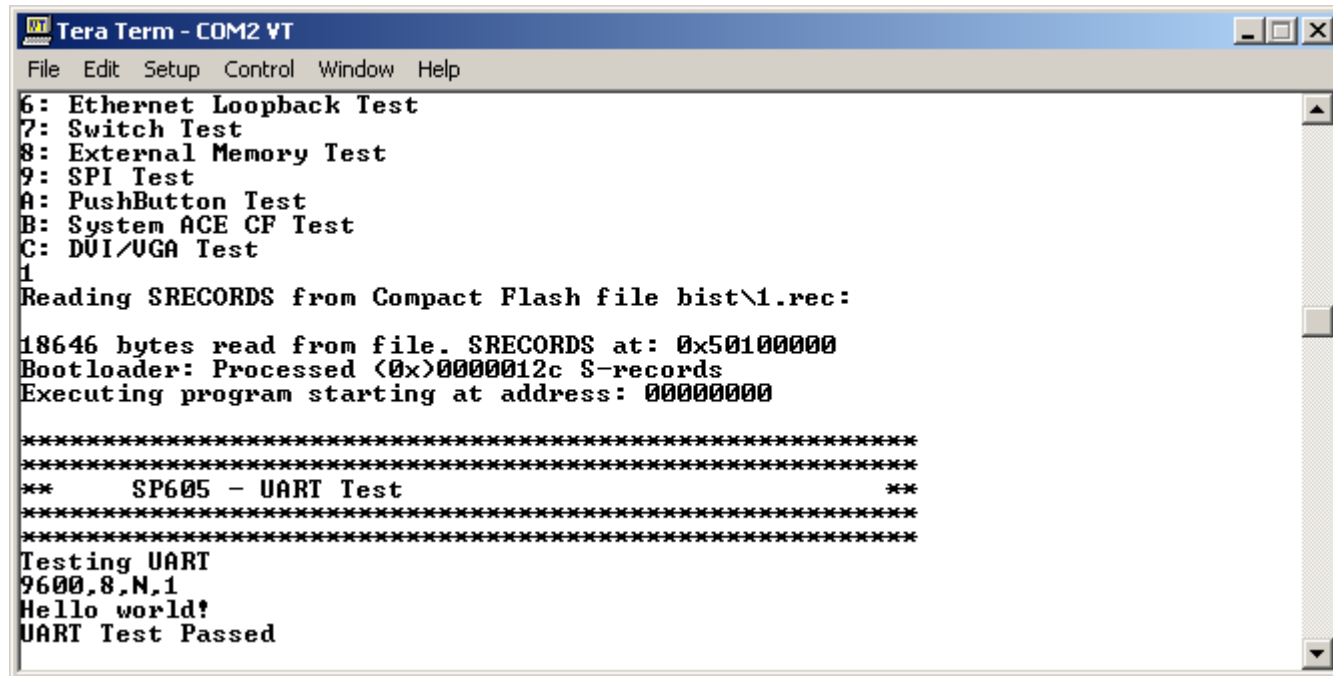


```
Tera Term - COM2 VT
File Edit Setup Control Window Help

*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
```

SP605 BIST

- UART Test completed



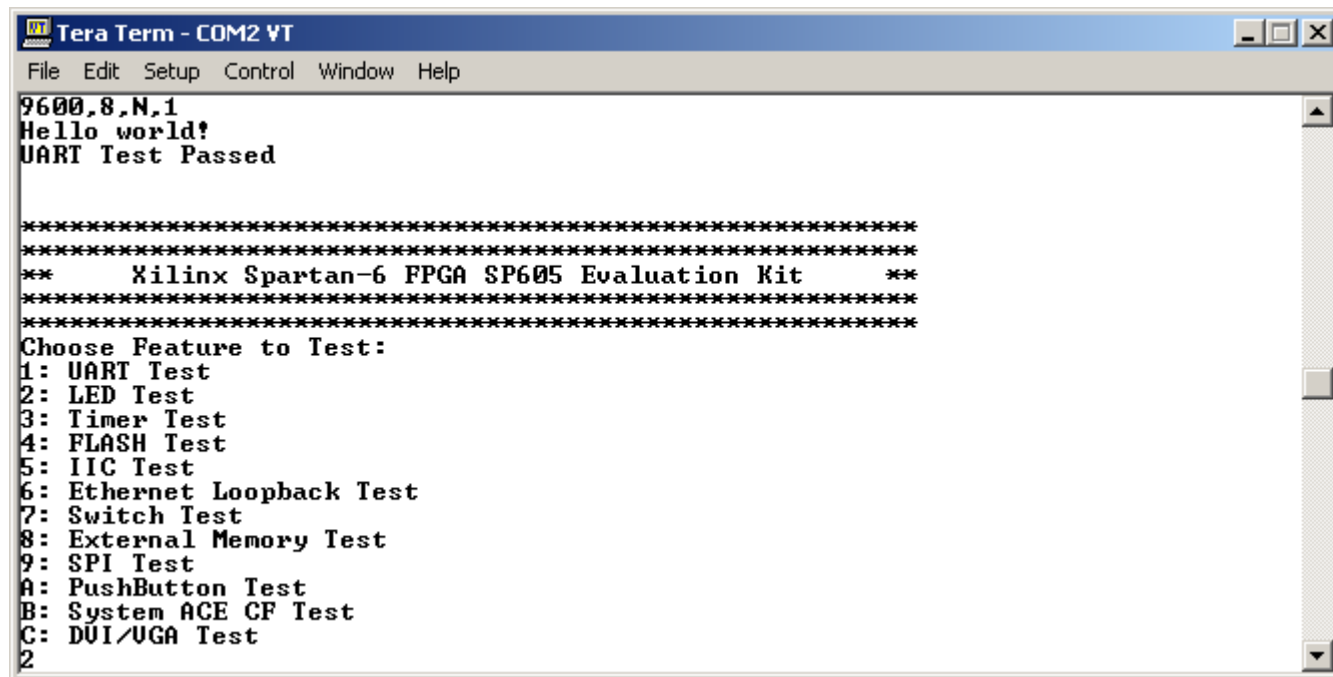
The screenshot shows a Tera Term window titled "Tera Term - COM2 VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main text area displays the following output:

```
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
1
Reading SRECORDS from Compact Flash file bist\1.rec:
18646 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)0000012c S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - UART Test      **
*****
*****
Testing UART
9600,8,N,1
Hello world!
UART Test Passed
```

SP605 BIST

- Output returns to initial menu after UART Test completes
 - Type 2 to begin LED Test

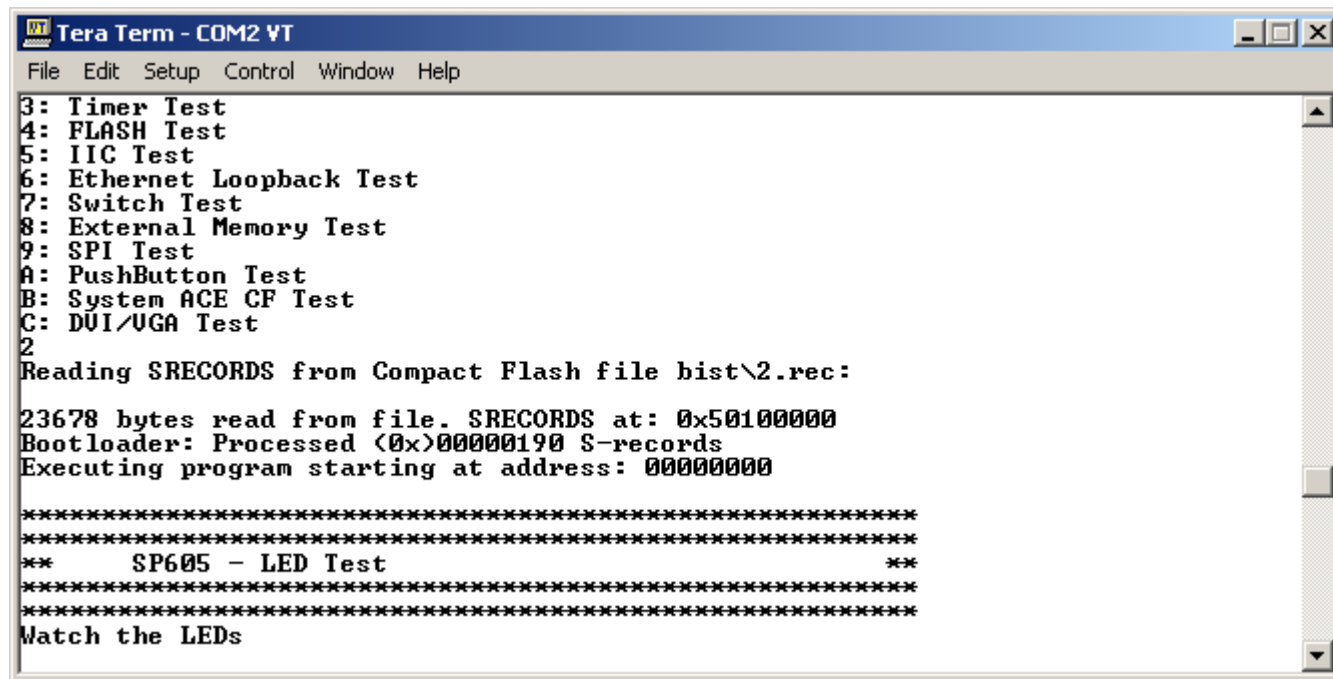


```
Tera Term - COM2 VT
File Edit Setup Control Window Help
9600,8,N,1
Hello world!
UART Test Passed

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
2
```

SP605 BIST

- **View Walking 1's pattern on GPIO LEDs**
 - Sequence repeats six times
- **LED Test completed**
 - Type **3** to begin Timer Test

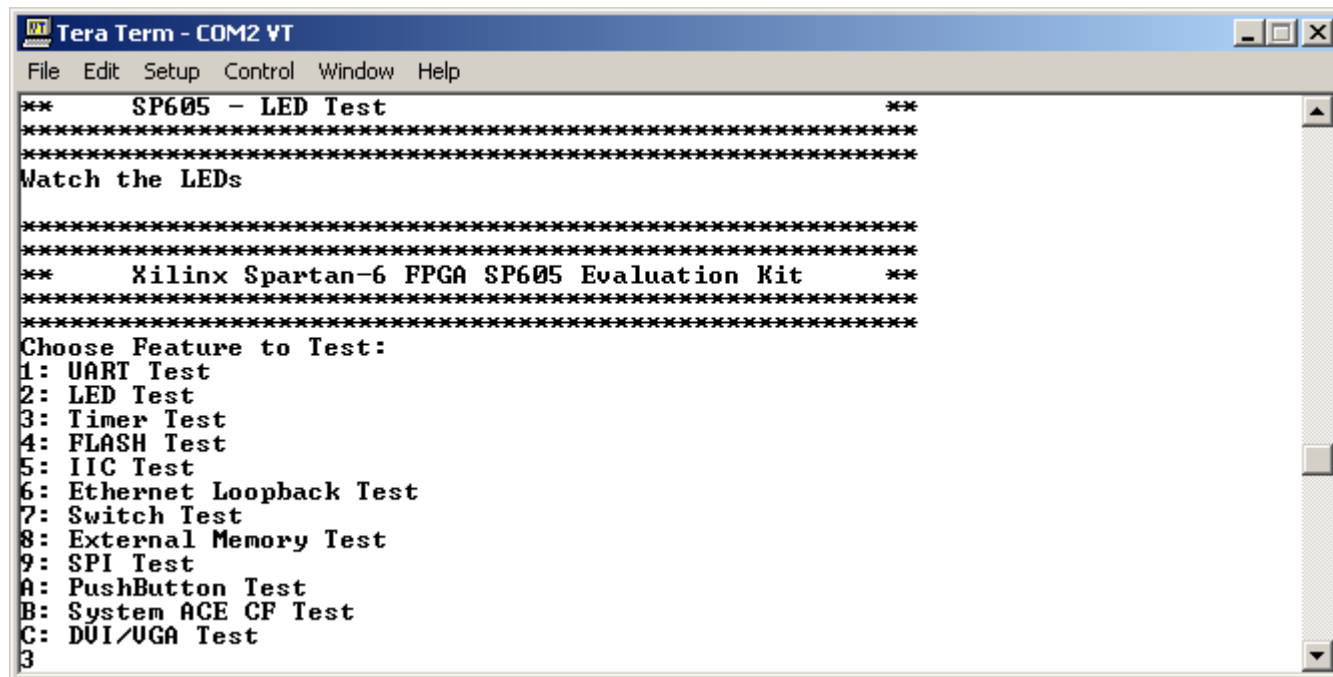


```
Tera Term - COM2 VT
File Edit Setup Control Window Help
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
2
Reading SRECORDS from Compact Flash file bist\2.rec:
23678 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000190 S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - LED Test      **
*****
*****
Watch the LEDs
```


SP605 BIST

- **Output returns to initial menu after LED Test completes**
 - Type **3** to begin Timer Test

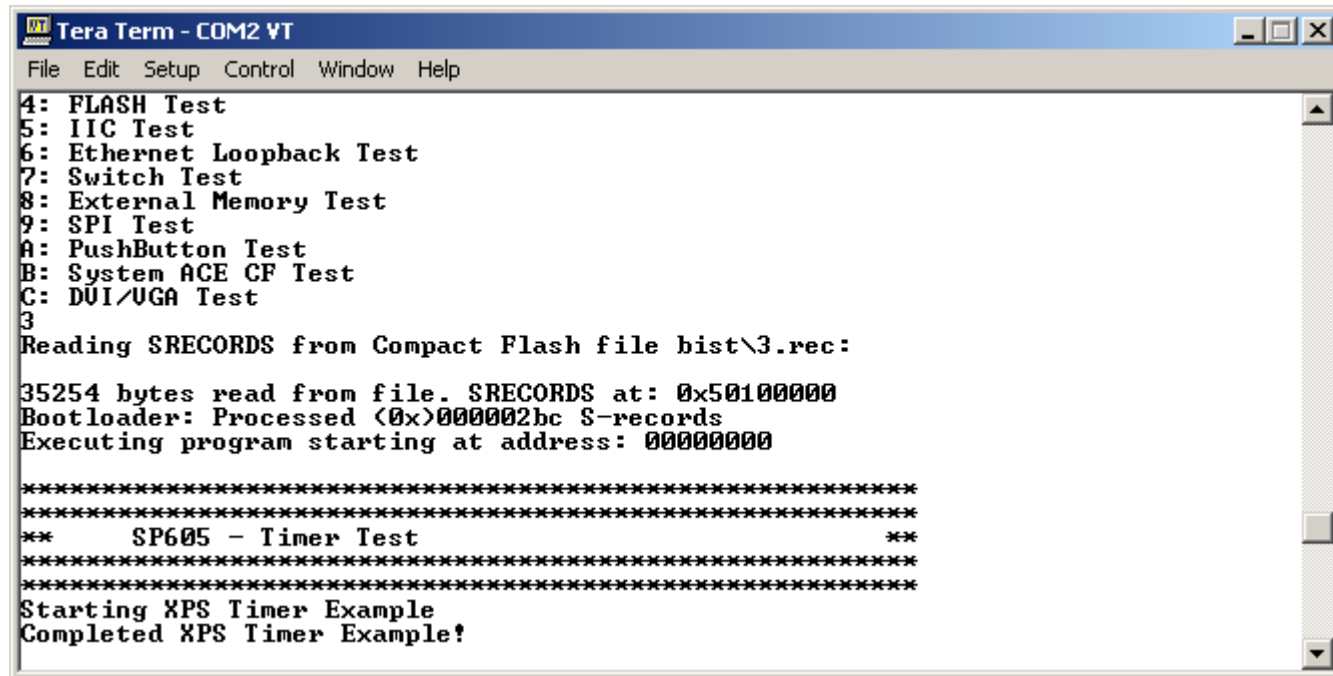


```
Tera Term - COM2 VT
File Edit Setup Control Window Help
**      SP605 - LED Test      **
*****
*****
Match the LEDs

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
3
```

SP605 BIST

- Timer Test completed



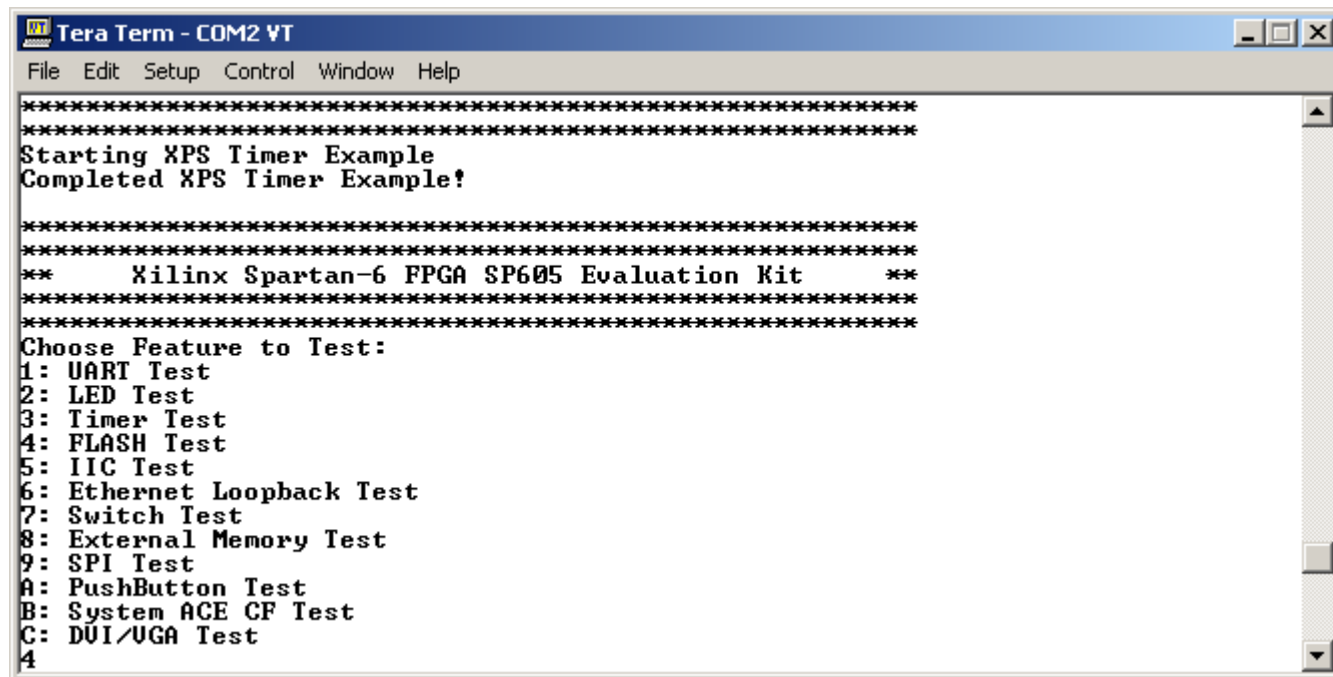
The screenshot shows a terminal window titled "Tera Term - COM2 VT" with a menu bar (File, Edit, Setup, Control, Window, Help). The text output is as follows:

```
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
3
Reading SRECORDS from Compact Flash file bist\3.rec:
35254 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000002bc S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - Timer Test      **
*****
*****
Starting XPS Timer Example
Completed XPS Timer Example!
```

SP605 BIST

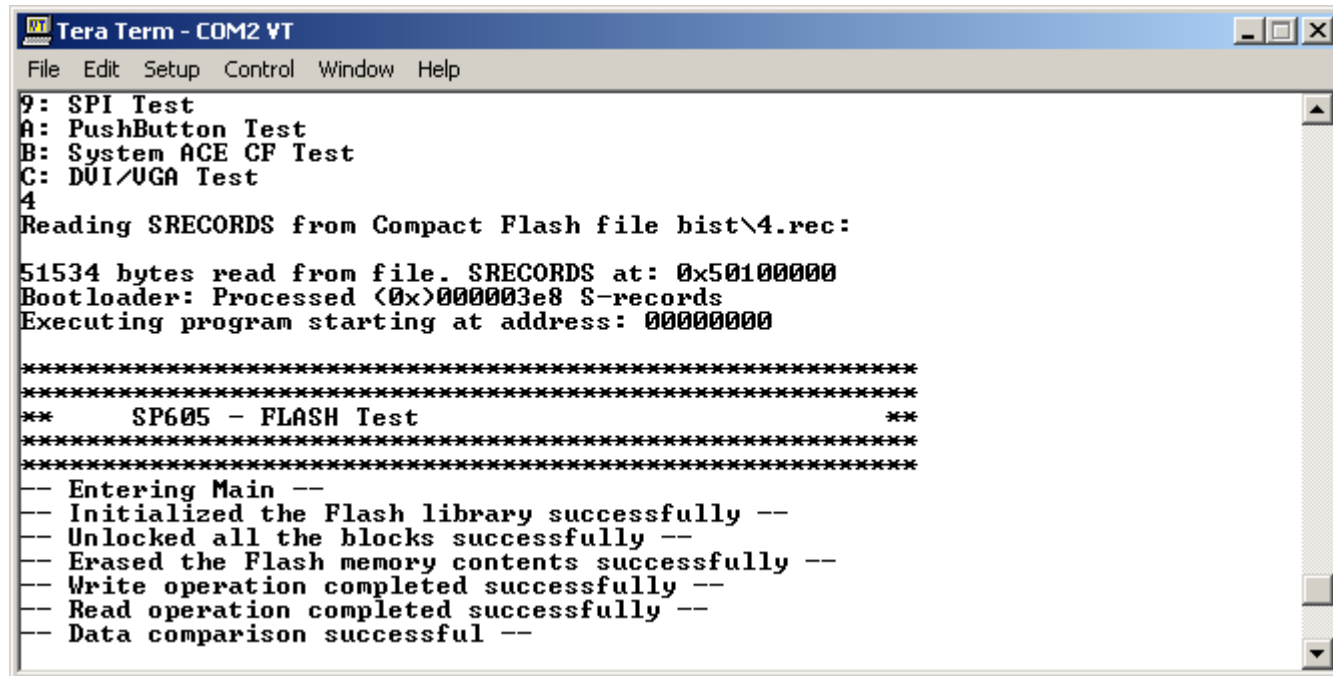
- Output returns to initial menu after Timer Test completes
 - Type 4 to begin Flash test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
*****
Starting XPS Timer Example
Completed XPS Timer Example!
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
4
```

SP605 BIST

- Flash Test completed



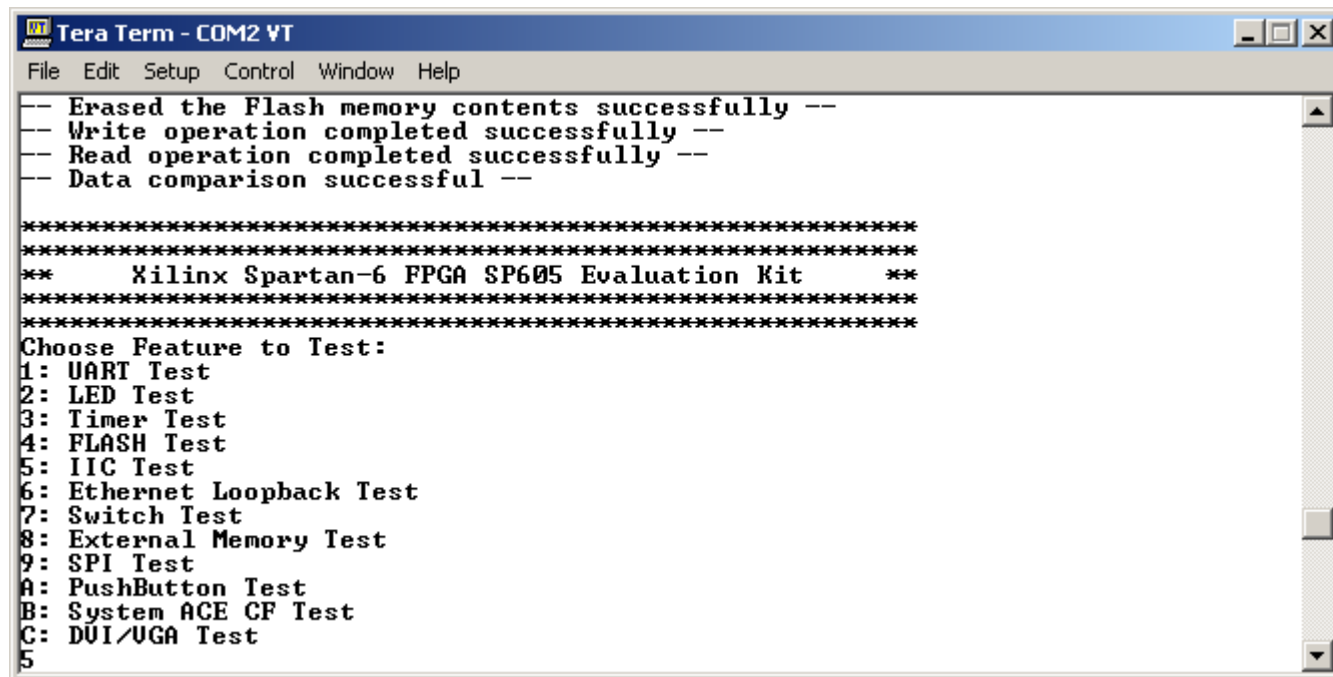
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
4
Reading SRECORDS from Compact Flash file bist\4.rec:

51534 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)0000003e8 S-records
Executing program starting at address: 00000000

*****
**      SP605 - FLASH Test      **
*****
-- Entering Main --
-- Initialized the Flash library successfully --
-- Unlocked all the blocks successfully --
-- Erased the Flash memory contents successfully --
-- Write operation completed successfully --
-- Read operation completed successfully --
-- Data comparison successful --
```

SP605 BIST

- Output returns to initial menu after Flash Test completes
 - Type **5** to begin IIC EEPROM Test

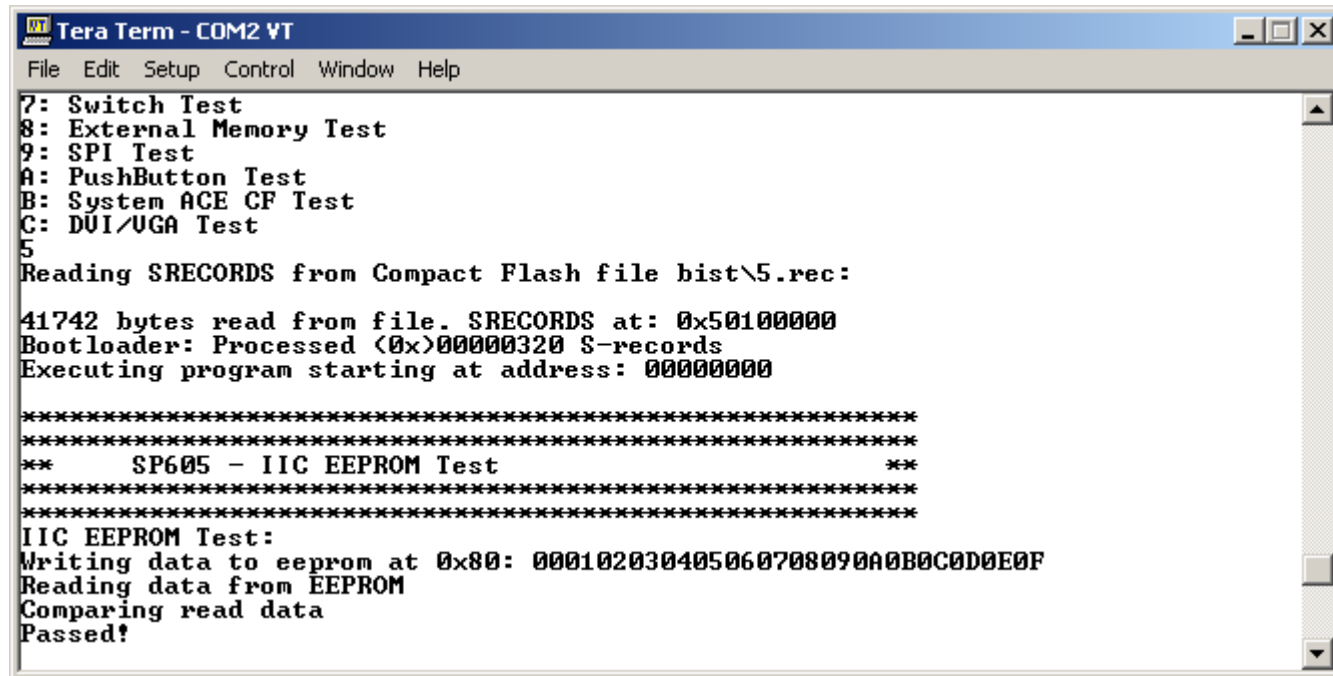


```
Tera Term - COM2 VT
File Edit Setup Control Window Help
-- Erased the Flash memory contents successfully --
-- Write operation completed successfully --
-- Read operation completed successfully --
-- Data comparison successful --

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
5
```

SP605 BIST

- IIC EEPROM Test completed



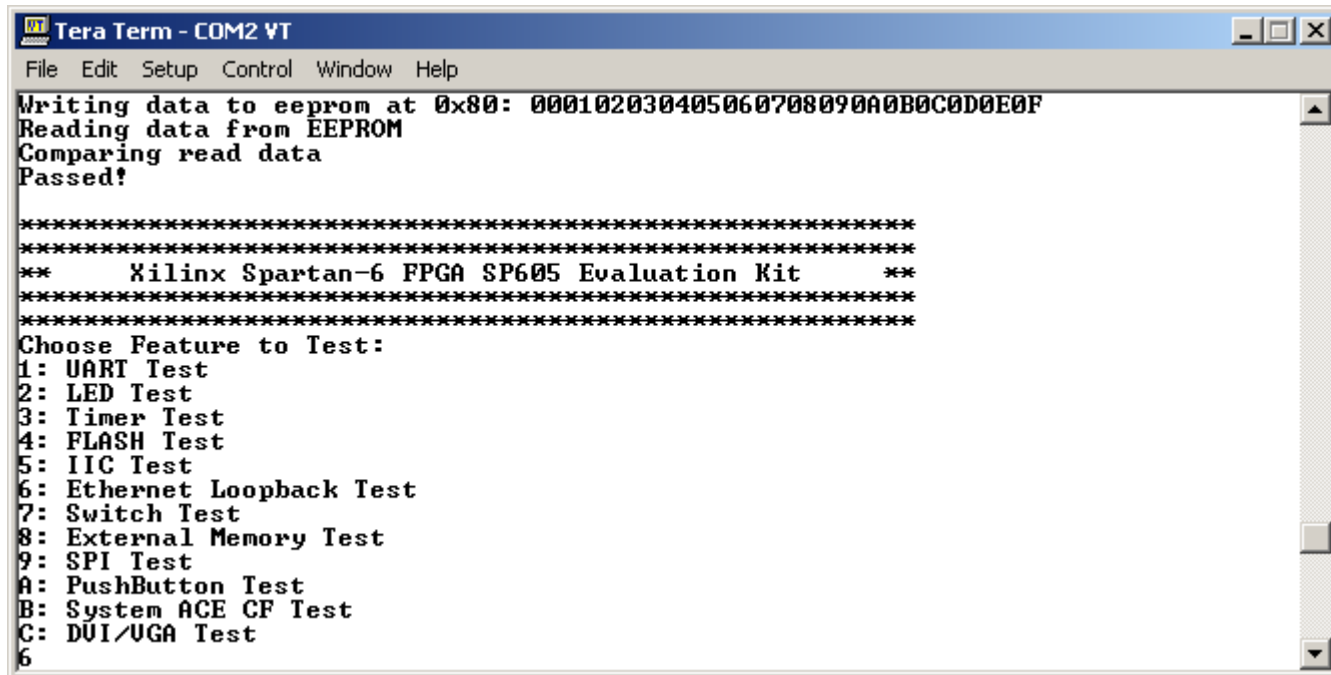
The screenshot shows a terminal window titled "Tera Term - COM2 VT" with a menu bar (File, Edit, Setup, Control, Window, Help). The terminal output displays a list of tests: 7: Switch Test, 8: External Memory Test, 9: SPI Test, A: PushButton Test, B: System ACE CF Test, and C: DVI/UGA Test. It then shows the execution of S-records from a Compact Flash file, followed by the "SP605 - IIC EEPROM Test" section. This section reports writing data to EEPROM at address 0x80, reading the data back, and comparing it, resulting in a "Passed!" status.

```
Tera Term - COM2 VT
File Edit Setup Control Window Help
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
5
Reading SRECORDS from Compact Flash file bist\5.rec:
41742 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - IIC EEPROM Test      **
*****
*****
IIC EEPROM Test:
Writing data to eeprom at 0x80: 000102030405060708090A0B0C0D0E0F
Reading data from EEPROM
Comparing read data
Passed!
```

SP605 BIST

- **Output returns to initial menu after IIC EEPROM Test completes**
 - Type **6** to begin Ethernet Loopback Test
 - PHY is put into internal loopback mode



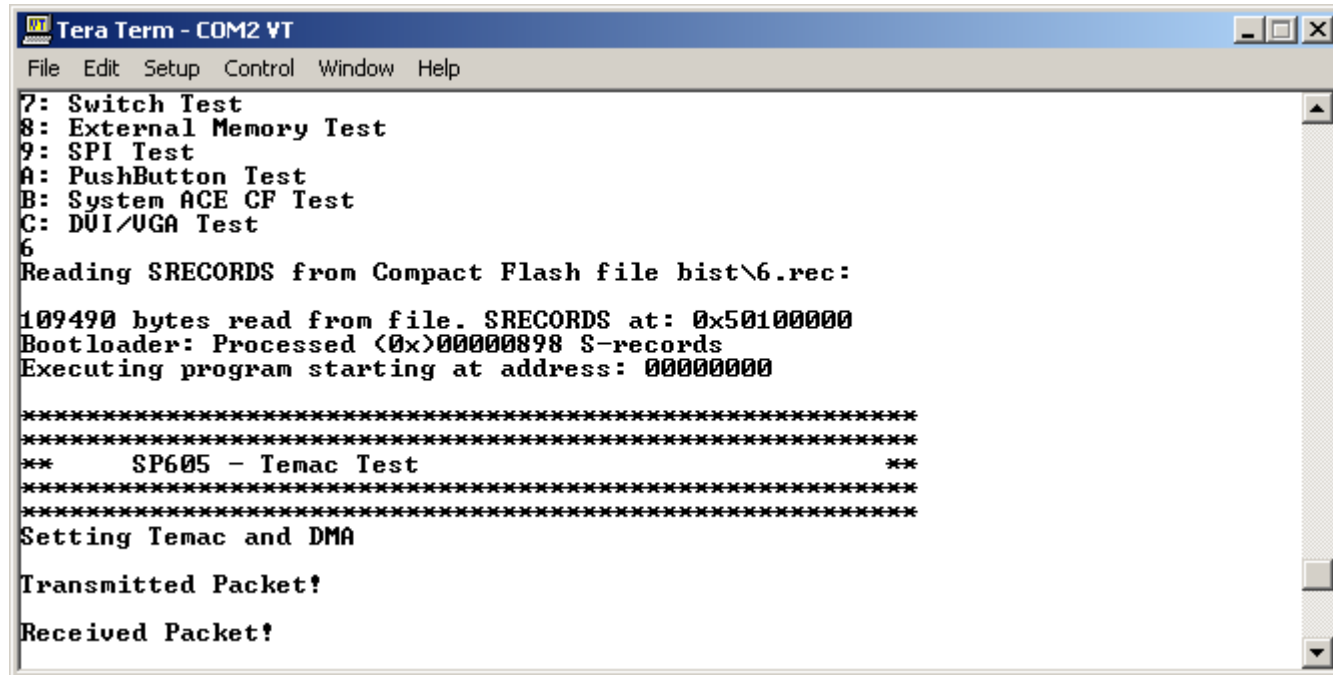
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
Writing data to eeprom at 0x80: 000102030405060708090A0B0C0D0E0F
Reading data from EEPROM
Comparing read data
Passed!

*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****

Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
6
```


SP605 BIST

- Ethernet Loopback Test completed



The screenshot shows a Tera Term window titled "Tera Term - COM2 VT" with a menu bar (File, Edit, Setup, Control, Window, Help). The terminal output displays a list of tests: 7: Switch Test, 8: External Memory Test, 9: SPI Test, A: PushButton Test, B: System ACE CF Test, and C: DVI/UGA Test. It then shows the execution of a BIST test from a Compact Flash file, reading 109490 bytes and processing 0x00000898 S-records. The test results for the SP605 - Temac Test are shown, indicating that the Ethernet Loopback Test was completed successfully.

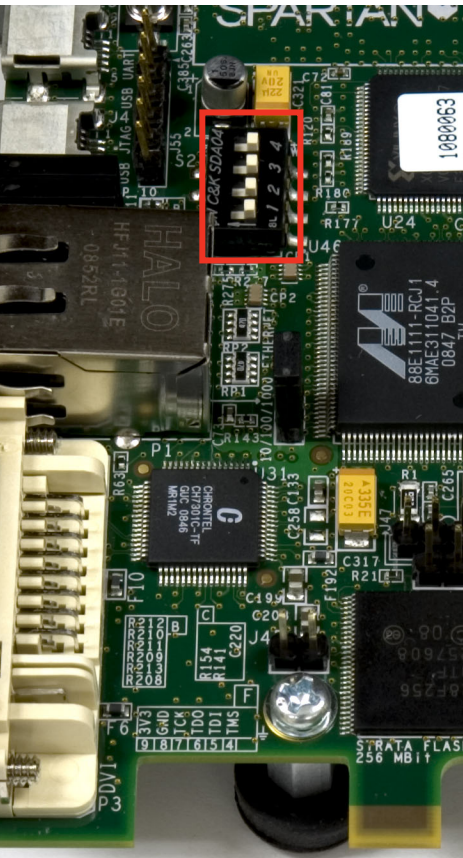
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
6
Reading SRECORDS from Compact Flash file bist\6.rec:
109490 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000898 S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - Temac Test      **
*****
*****
Setting Temac and DMA
Transmitted Packet!
Received Packet!
```

SP605 BIST

- Output returns to initial menu after Ethernet Loopback Test completes

- Set 4-position GPIO DIP Switch (S2)
- Type 7 to begin GPIO Switch Test
 - Reads switch settings



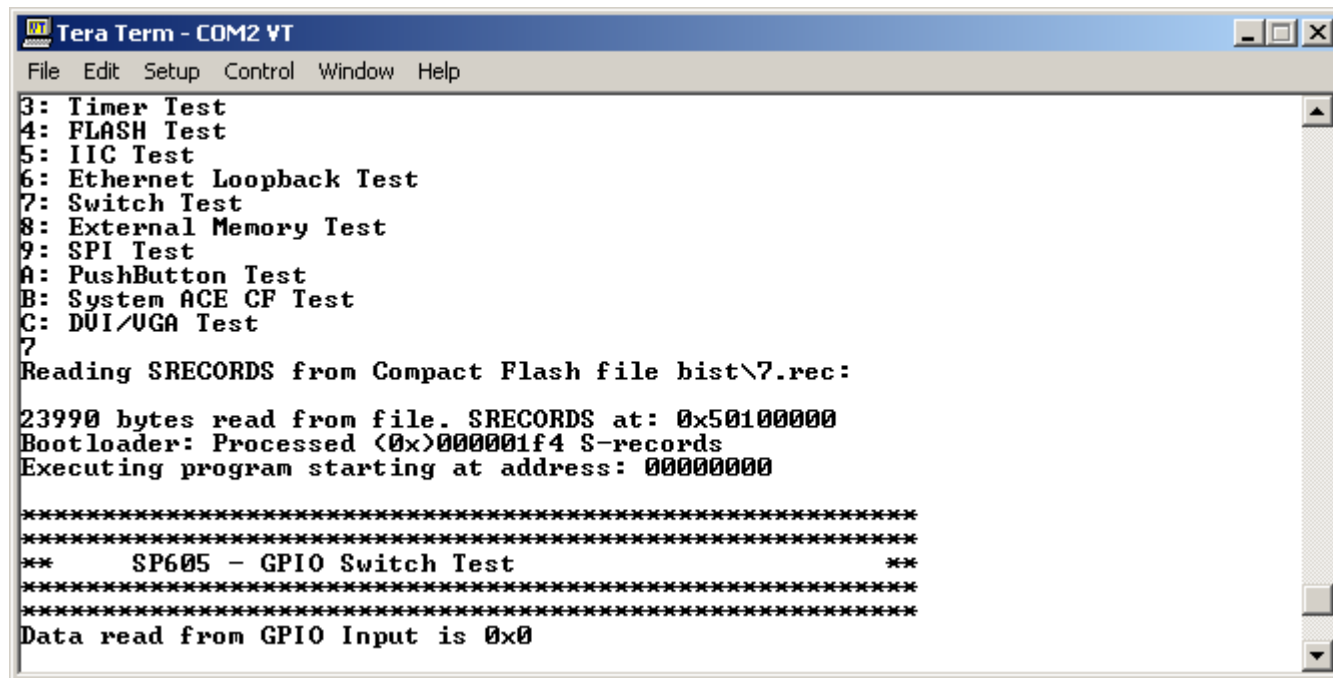
```
Tera Term - COM2 VT
File Edit Setup Control Window Help

Transmitted Packet?
Received Packet?

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
7
```

SP605 BIST

- GPIO Switch Test completed



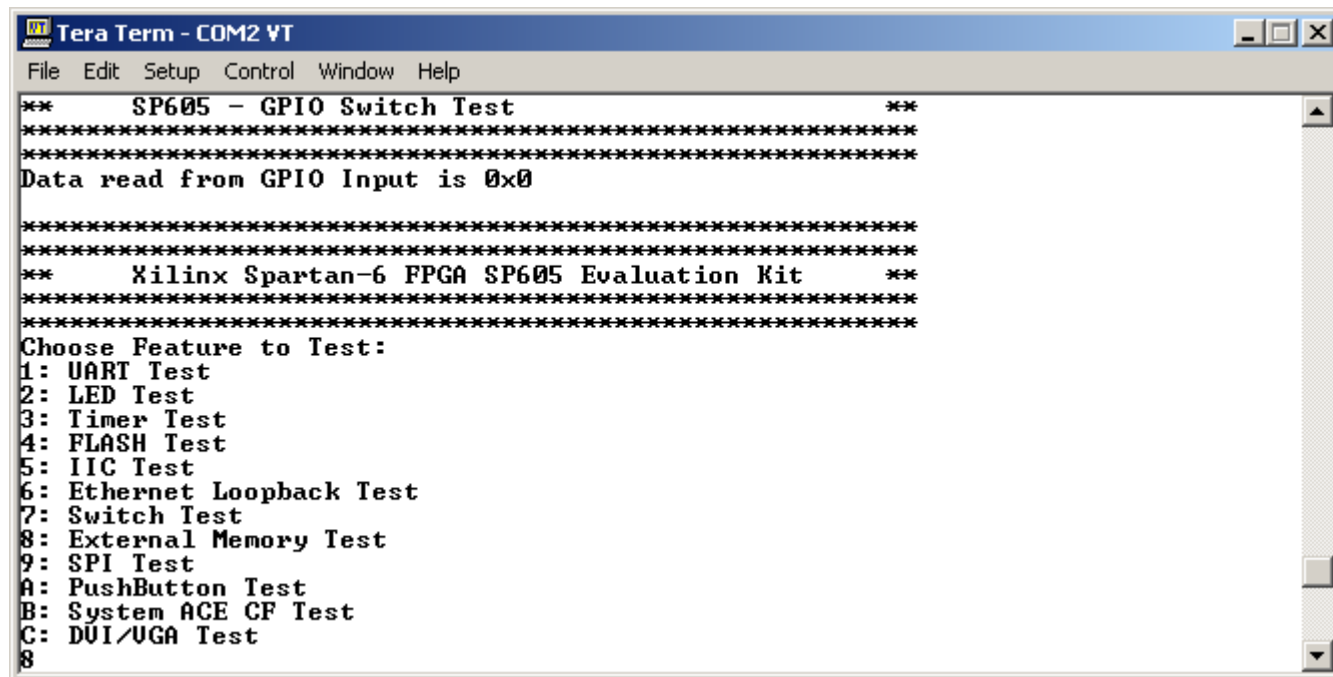
The screenshot shows a Tera Term window titled "Tera Term - COM2 VT" with a menu bar (File, Edit, Setup, Control, Window, Help). The terminal output lists various tests: 3: Timer Test, 4: FLASH Test, 5: IIC Test, 6: Ethernet Loopback Test, 7: Switch Test, 8: External Memory Test, 9: SPI Test, A: PushButton Test, B: System ACE CF Test, and C: DVI/UGA Test. Below this, it shows "Reading SRECORDS from Compact Flash file bist\7.rec:", "23990 bytes read from file. SRECORDS at: 0x50100000", "Bootloader: Processed (0x)000001f4 S-records", and "Executing program starting at address: 00000000". A separator of asterisks follows, then "** SP605 - GPIO Switch Test **", another separator, and finally "Data read from GPIO Input is 0x0".

```
Tera Term - COM2 VT
File Edit Setup Control Window Help
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
?
Reading SRECORDS from Compact Flash file bist\7.rec:
23990 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000001f4 S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - GPIO Switch Test      **
*****
*****
Data read from GPIO Input is 0x0
```

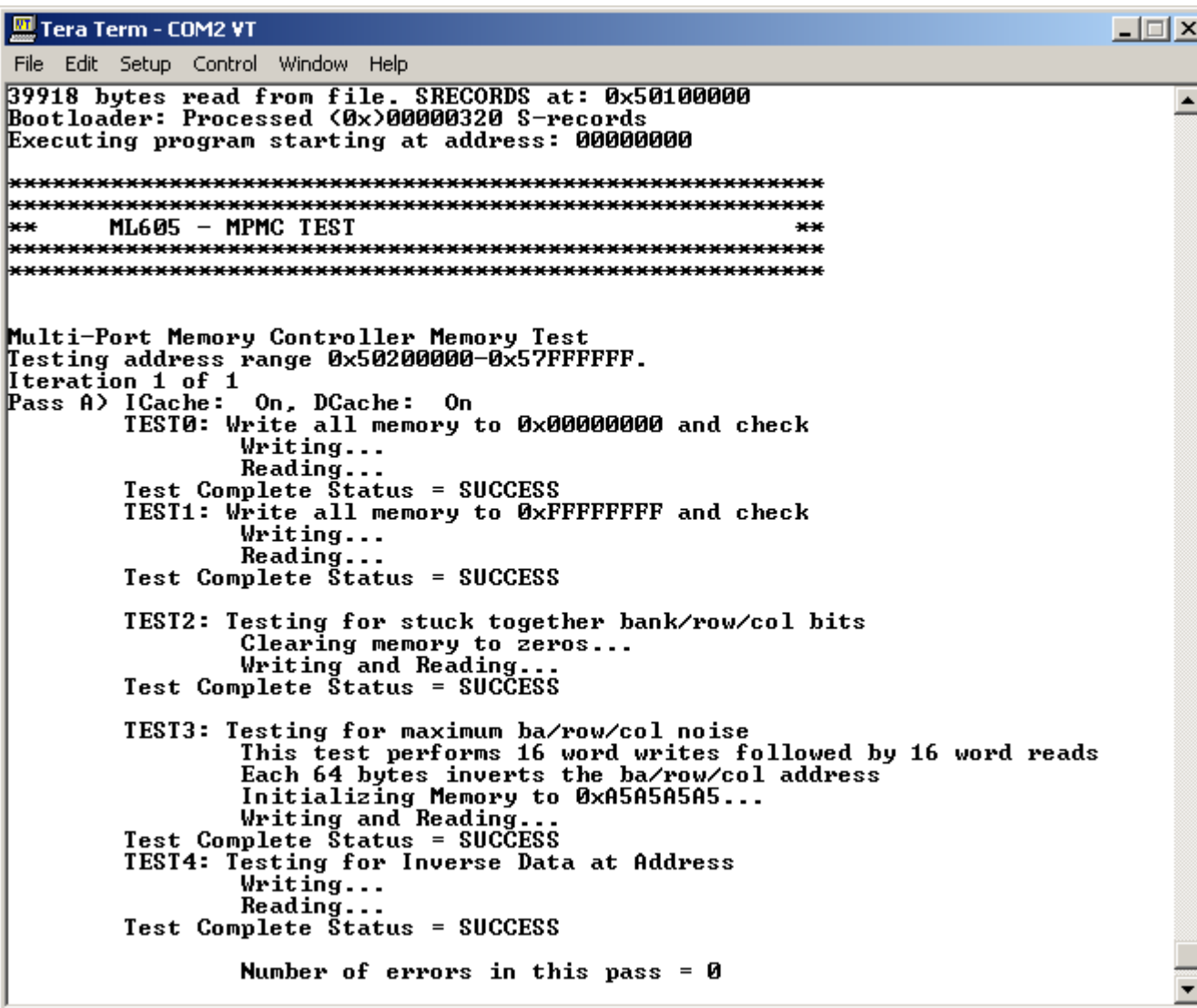
SP605 BIST

- Output returns to initial menu after GPIO Switch Test completes
 - Type 8 to begin External Memory Test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
**      SP605 - GPIO Switch Test      **
*****
*****
Data read from GPIO Input is 0x0
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
8
```

SP605 BIST



```
Tera Term - COM2 VT
File Edit Setup Control Window Help

39918 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      ML605 - MPMC TEST      **
*****
*****

Multi-Port Memory Controller Memory Test
Testing address range 0x50200000-0x57FFFFFF.
Iteration 1 of 1
Pass A) ICache: On, DCache: On
  TEST0: Write all memory to 0x00000000 and check
        Writing...
        Reading...
  Test Complete Status = SUCCESS
  TEST1: Write all memory to 0xFFFFFFFF and check
        Writing...
        Reading...
  Test Complete Status = SUCCESS

  TEST2: Testing for stuck together bank/row/col bits
        Clearing memory to zeros...
        Writing and Reading...
  Test Complete Status = SUCCESS

  TEST3: Testing for maximum ba/row/col noise
        This test performs 16 word writes followed by 16 word reads
        Each 64 bytes inverts the ba/row/col address
        Initializing Memory to 0xA5A5A5A5...
        Writing and Reading...
  Test Complete Status = SUCCESS
  TEST4: Testing for Inverse Data at Address
        Writing...
        Reading...
  Test Complete Status = SUCCESS

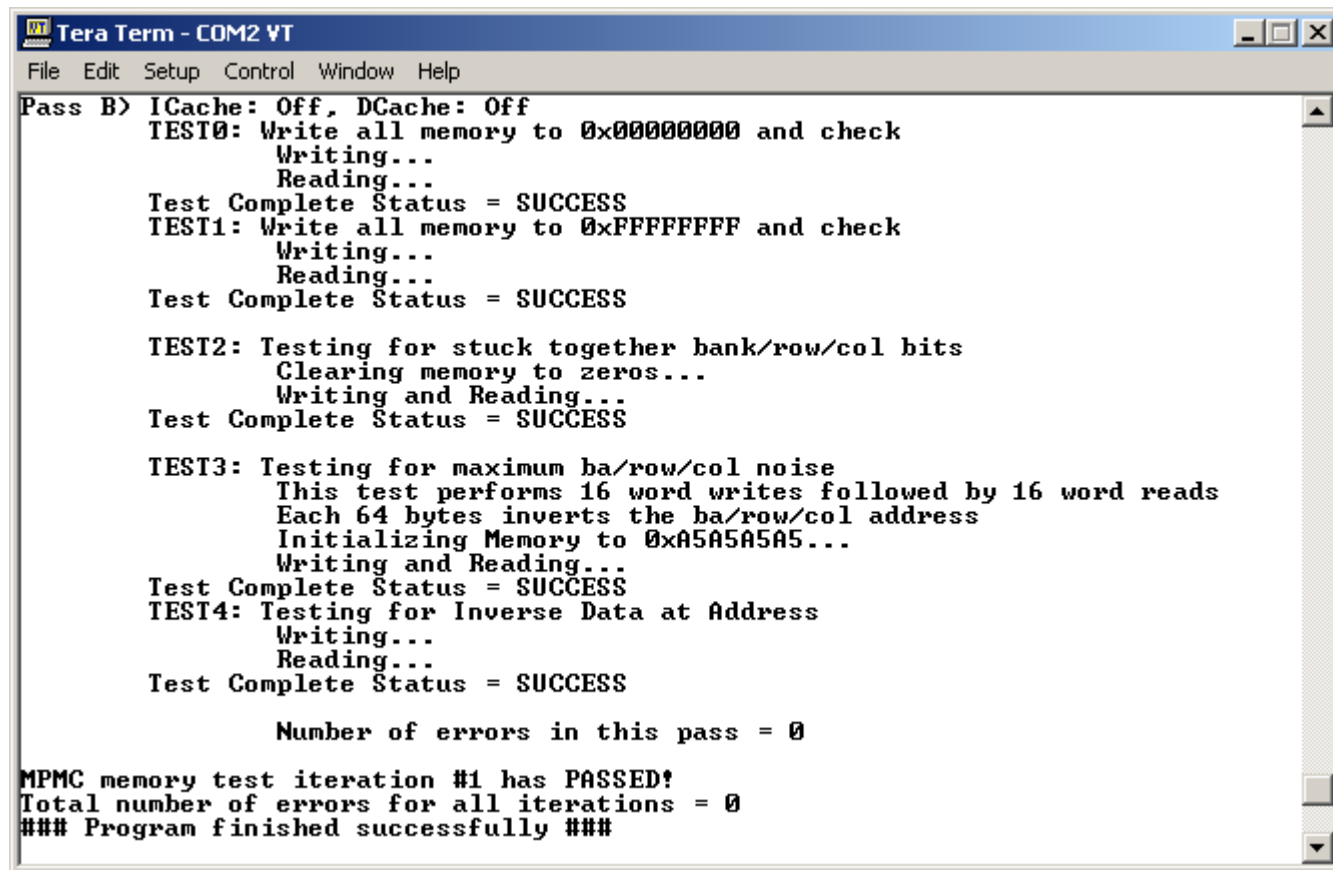
        Number of errors in this pass = 0
```

- External Memory Test running with caches on

Note: External Memory Test takes about 20 minutes

SP605 BIST

- Second part of External Memory test (caches off)



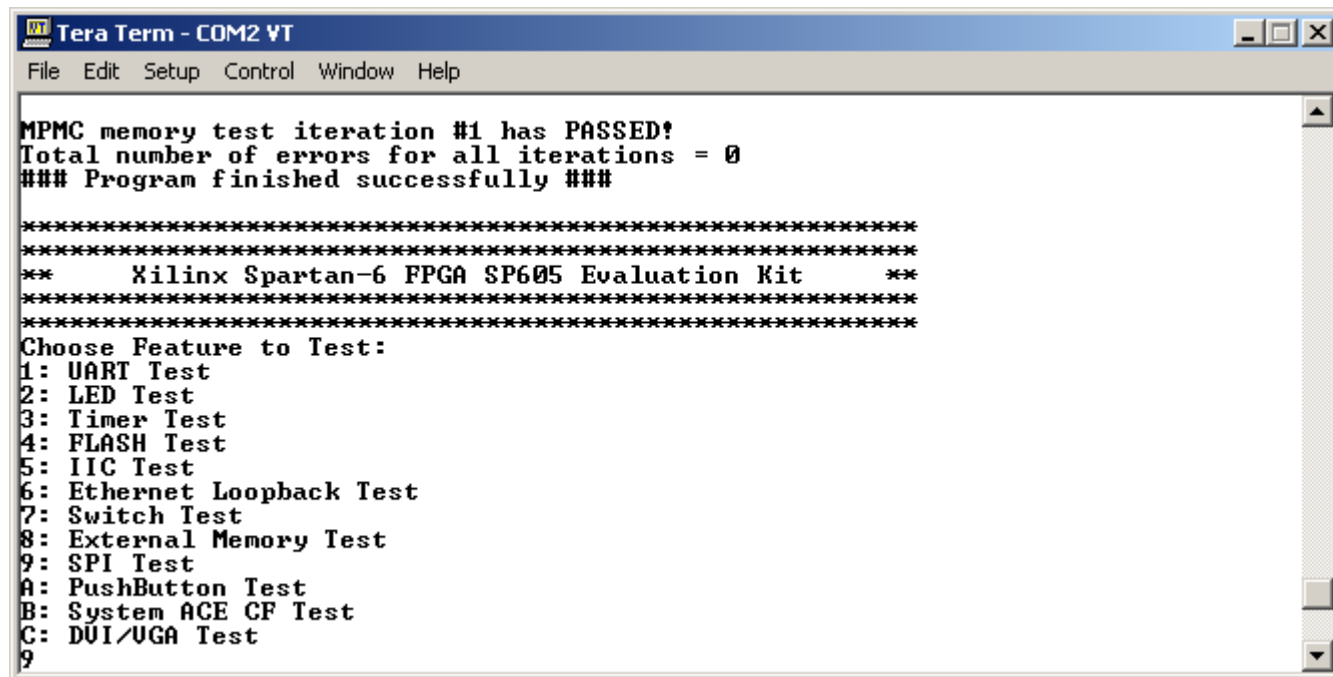
```
Tera Term - COM2 VT
File Edit Setup Control Window Help
Pass B> ICache: Off, DCache: Off
TEST0: Write all memory to 0x00000000 and check
        Writing...
        Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
        Writing...
        Reading...
Test Complete Status = SUCCESS
TEST2: Testing for stuck together bank/row/col bits
        Clearing memory to zeros...
        Writing and Reading...
Test Complete Status = SUCCESS
TEST3: Testing for maximum ba/row/col noise
        This test performs 16 word writes followed by 16 word reads
        Each 64 bytes inverts the ba/row/col address
        Initializing Memory to 0xA5A5A5A5...
        Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
        Writing...
        Reading...
Test Complete Status = SUCCESS

        Number of errors in this pass = 0

MPMC memory test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###
```

SP605 BIST

- Output returns to initial menu after External Memory test completes
 - Type **9** to begin SPI Test



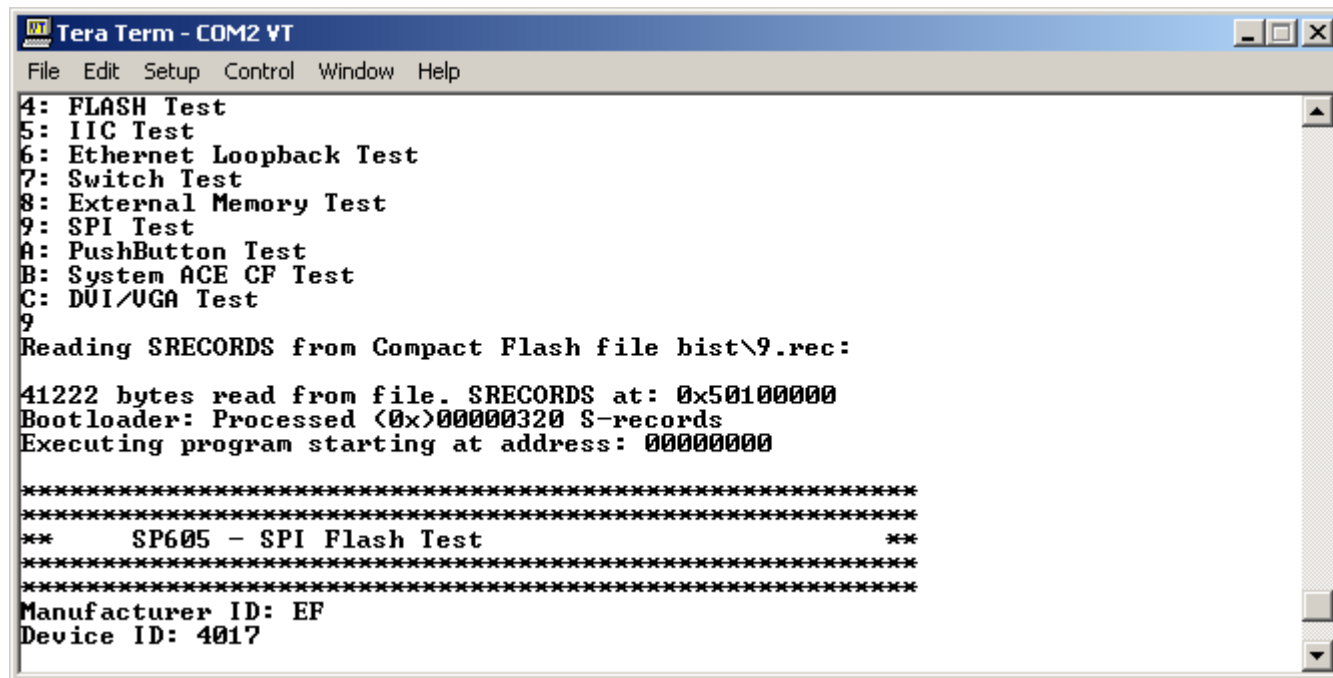
```
Tera Term - COM2 VT
File Edit Setup Control Window Help

MPMC memory test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ###

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
9
```


SP605 BIST

- SPI Test completed



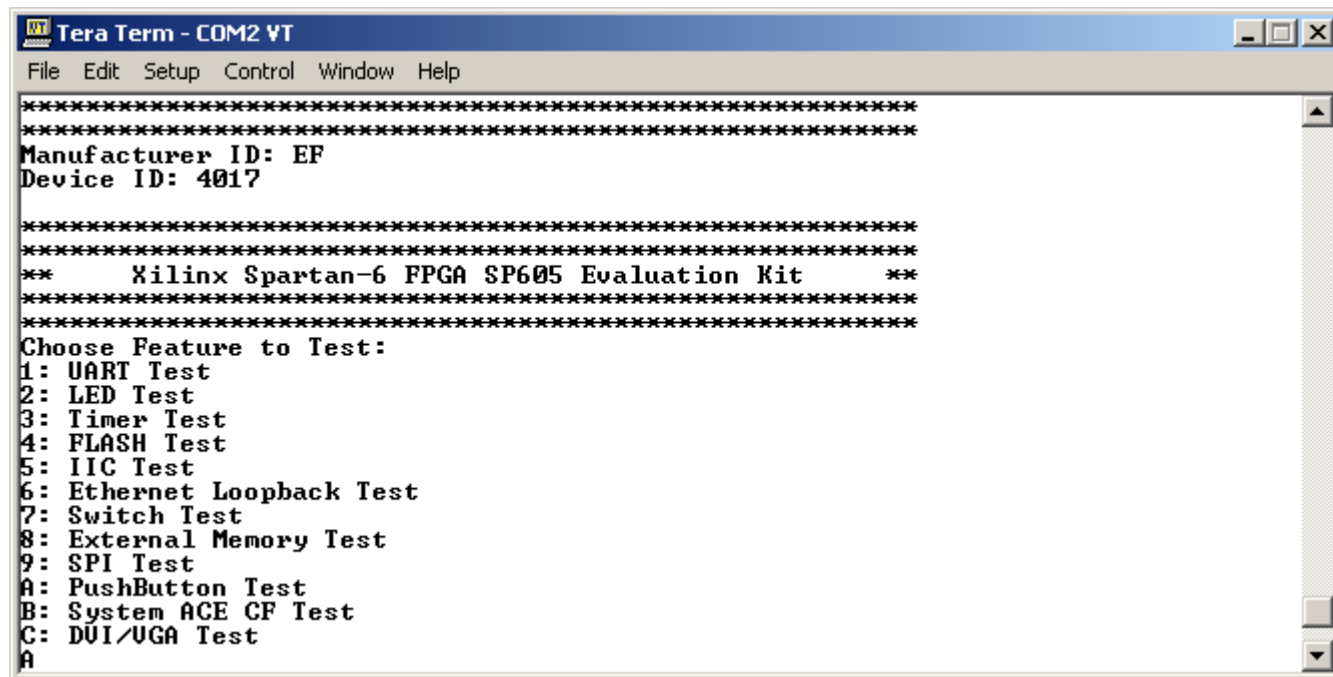
The screenshot shows a terminal window titled "Tera Term - COM2 VT" with a menu bar (File, Edit, Setup, Control, Window, Help). The text output is as follows:

```
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
9
Reading SRECORDS from Compact Flash file bist\9.rec:
41222 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000320 S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - SPI Flash Test      **
*****
*****
Manufacturer ID: EF
Device ID: 4017
```

SP605 BIST

- **Output returns to initial menu after SPI Test completes**
 - Type **A** to begin PushButton Test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
*****
*****
Manufacturer ID: EF
Device ID: 4017
*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
A
```

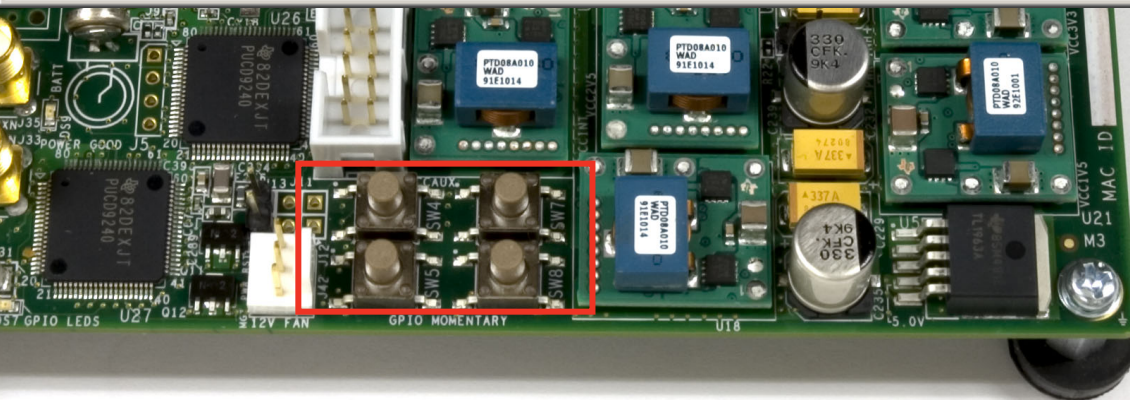
SP605 BIST

```
Tera Term - COM2 VT
File Edit Setup Control Window Help

A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
A
Reading SRECORDS from Compact Flash file bist\A.rec:
18558 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)0000012c S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - Button Test      **
*****
*****
Press SW4 Button & see if LED0 <DS3> glows
Press SW7 Button & see if LED1 <DS4> glows
Press SW5 Button & see if LED2 <DS5> glows
Press SW8 Button & see if all the 4 LEDs glow
```

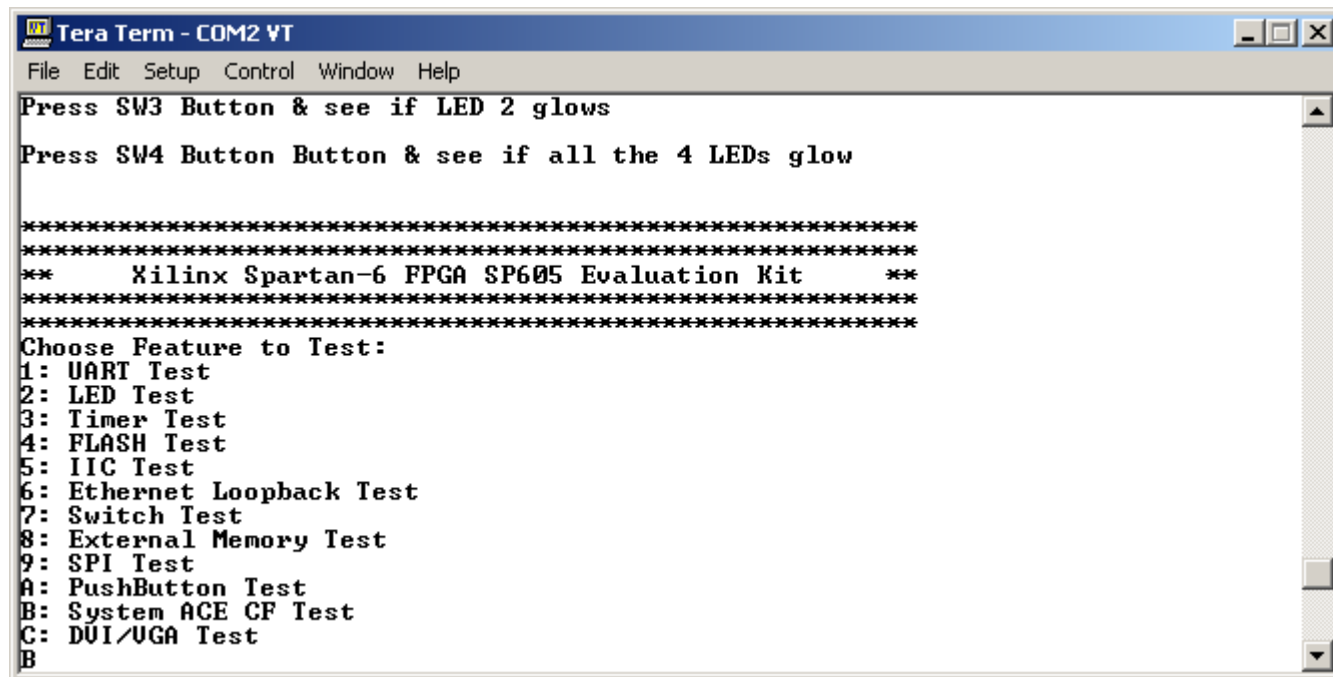
- Push the Buttons in the order requested



Note: Presentation applies to the SP605

SP605 BIST

- **Output returns to initial menu after PushButton Test completes**
 - Type **B** to begin System ACE CF Test



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
Press SW3 Button & see if LED 2 glows
Press SW4 Button Button & see if all the 4 LEDs glow

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/UGA Test
B
```

SP605 BIST

```
Tera Term - COM2 VT
File Edit Setup Control Window Help
73382 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)000005dc S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - Sysace Test      **
*****
*****

This program attempts to access the CF card's file system
to perform file I/O operations.

Please insert a CF card with the contents of the directory
<ref design install dir>/sw/standalone/testfatfs/required_files/
copied into a directory named test on that CF card.

Warning: This program will attempt to create a file and directory
on the CF card.

File I/O Test Program running.
Reading file : a:\test\test.txt
This is a test file.
          0123456789
                abcdefghijklmnopqrstuvwxyz

Total bytes read = 60

Reading file : a:\test\xflow.log
dummy log file

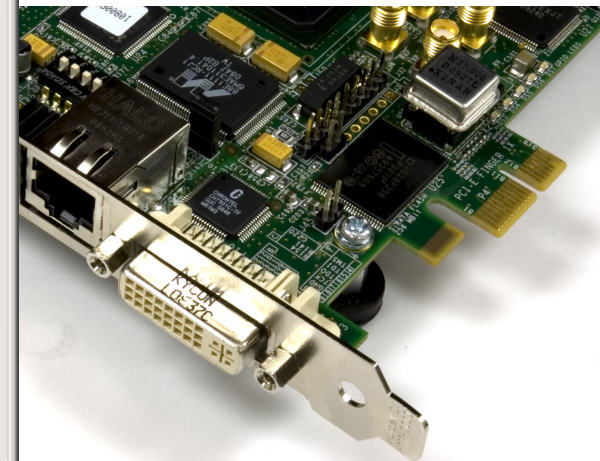
Total bytes read = 16
Reading file : a:\test\xilfatfs.pdf
Total bytes read = 59885
Failed to open a:\test\noexist.c: check if file present
Total bytes read = 0

read done
Writing file contents.

# of bytes written: 38
write done
executing mkdir talica..
mkdir success
```

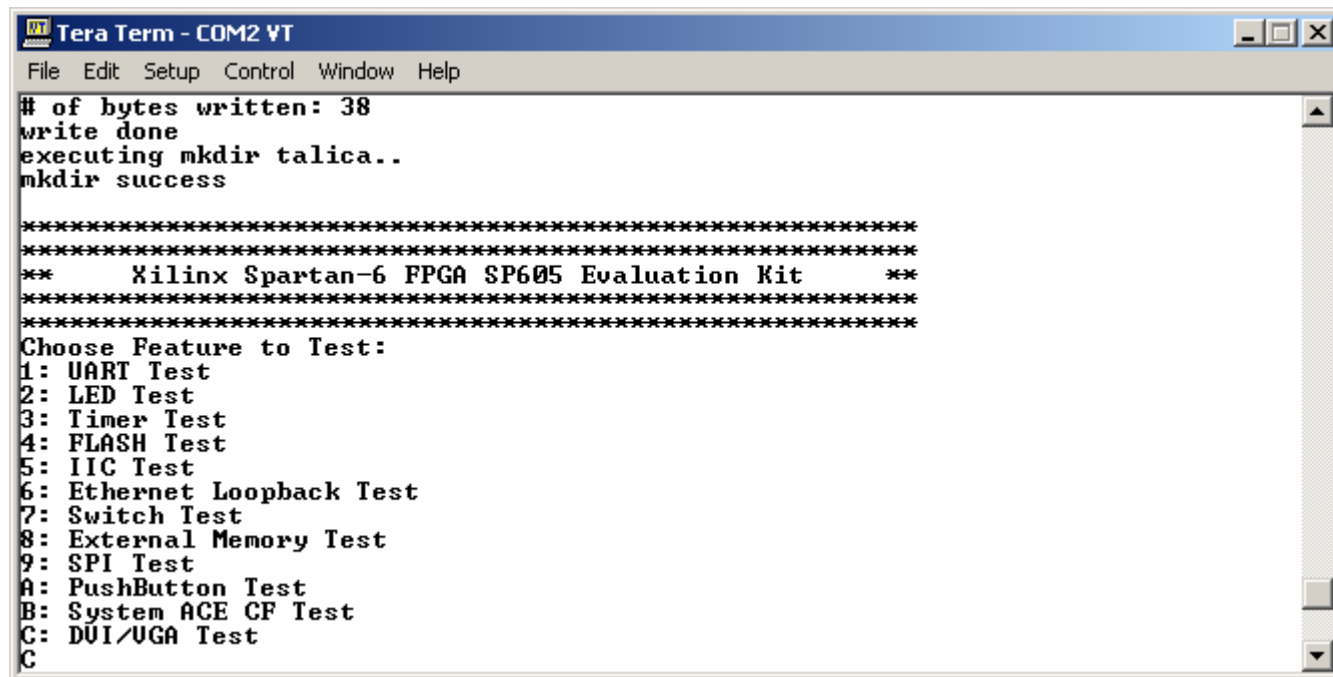
■ System ACE CF Test completed

- Connect a DVI Monitor to the SP605 board



SP605 BIST

- Output returns to initial menu after System ACE CF Test completes
 - Type **C** to begin DVI/VGA Test

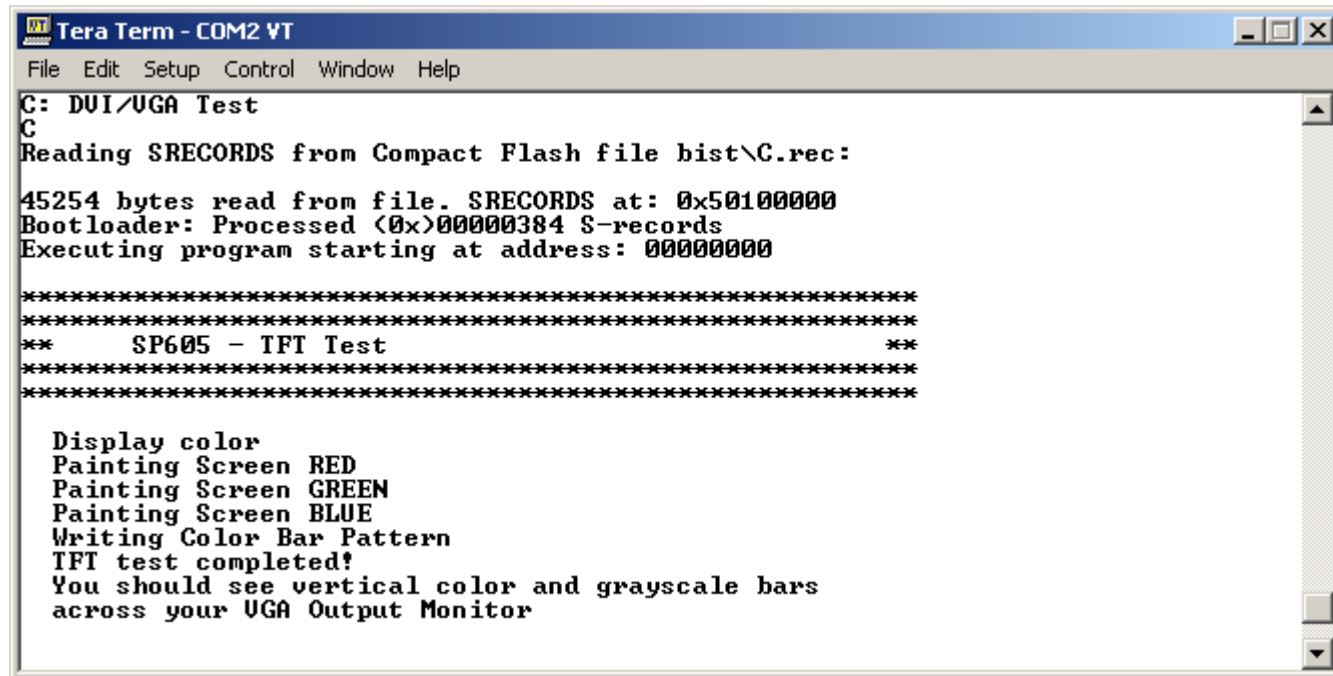


```
Tera Term - COM2 VT
File Edit Setup Control Window Help
# of bytes written: 38
write done
executing mkdir talica..
mkdir success

*****
*****
**      Xilinx Spartan-6 FPGA SP605 Evaluation Kit      **
*****
*****
Choose Feature to Test:
1: UART Test
2: LED Test
3: Timer Test
4: FLASH Test
5: IIC Test
6: Ethernet Loopback Test
7: Switch Test
8: External Memory Test
9: SPI Test
A: PushButton Test
B: System ACE CF Test
C: DVI/VGA Test
C
```

SP605 BIST

- DVI/VGA Test completed



```
Tera Term - COM2 VT
File Edit Setup Control Window Help
C: DVI/VGA Test
C
Reading SRECORDS from Compact Flash file bist\C.rec:
45254 bytes read from file. SRECORDS at: 0x50100000
Bootloader: Processed (0x)00000384 S-records
Executing program starting at address: 00000000

*****
*****
**      SP605 - TFT Test      **
*****
*****

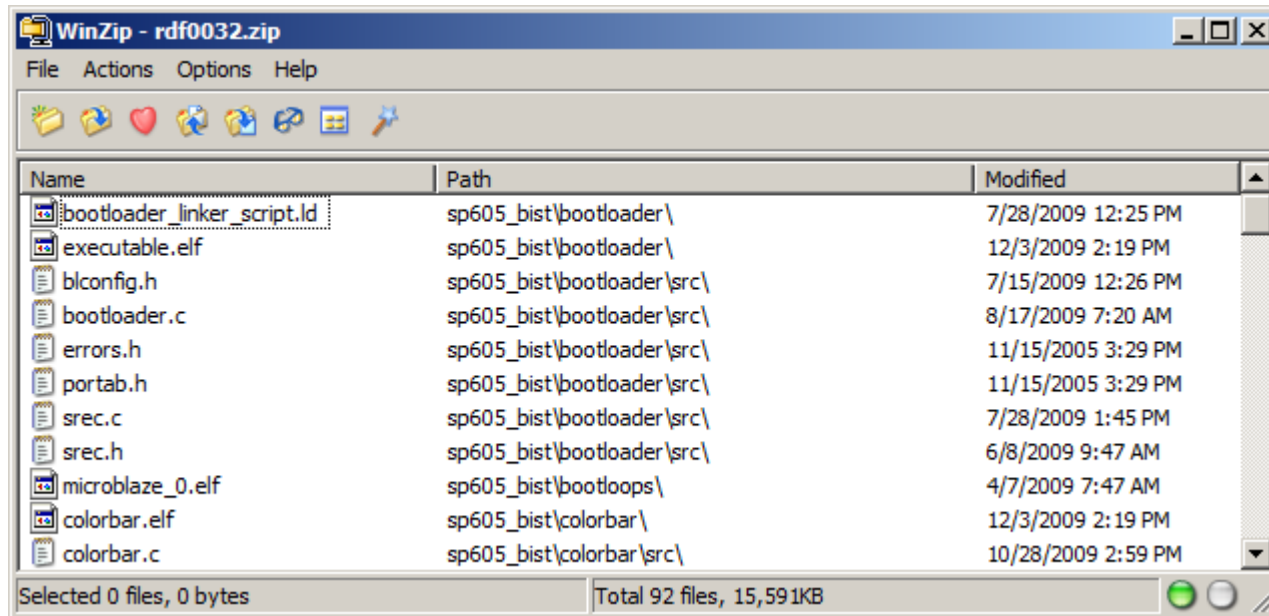
Display color
Painting Screen RED
Painting Screen GREEN
Painting Screen BLUE
Writing Color Bar Pattern
TFT test completed!
You should see vertical color and grayscale bars
across your UGA Output Monitor
```

Compile SP605 BIST Design

Compile SP605 BIST Design

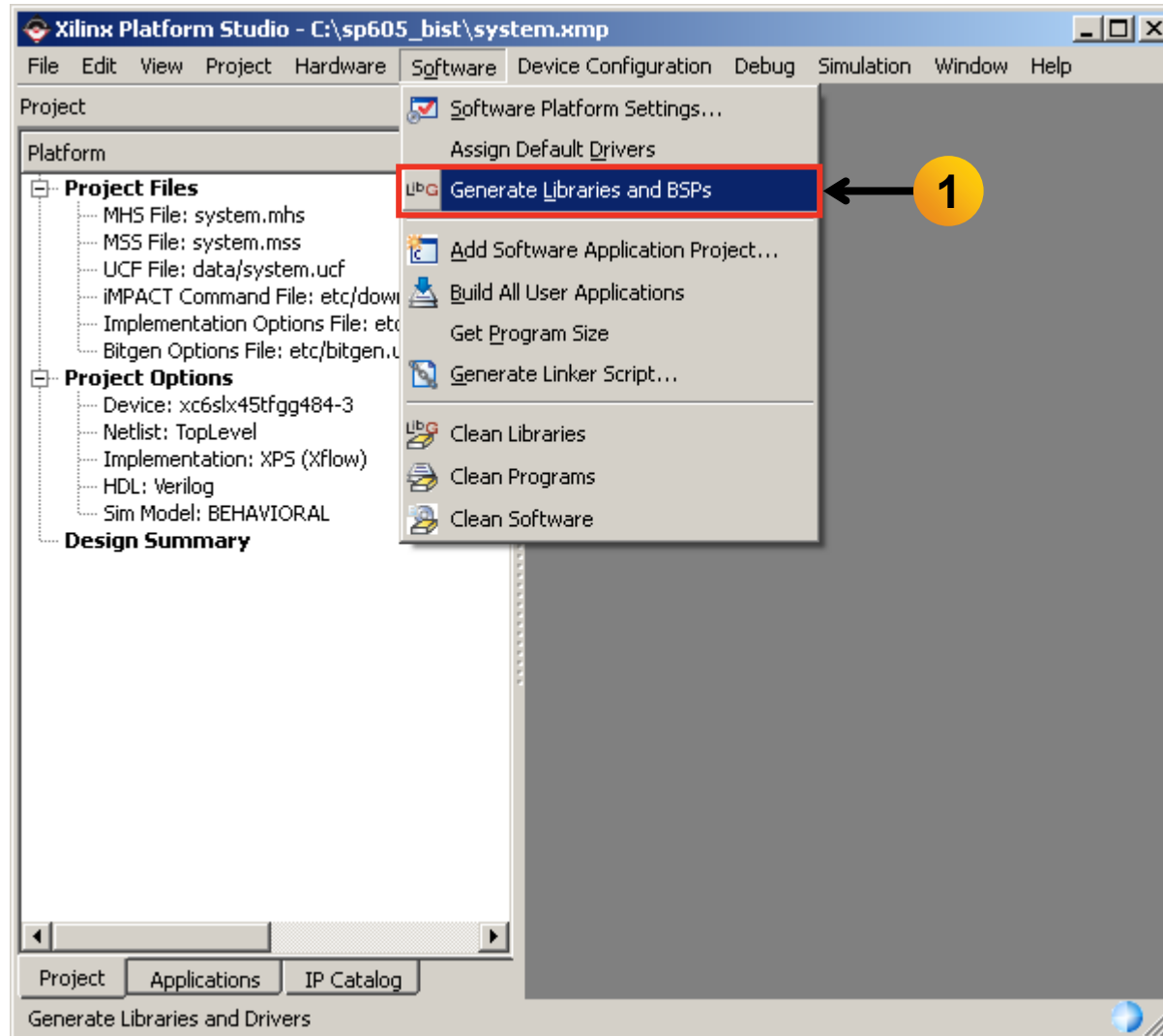
- Unzip the rdf0032.zip file

- <https://secure.xilinx.com/webreg/clickthrough.do?cid=140333>



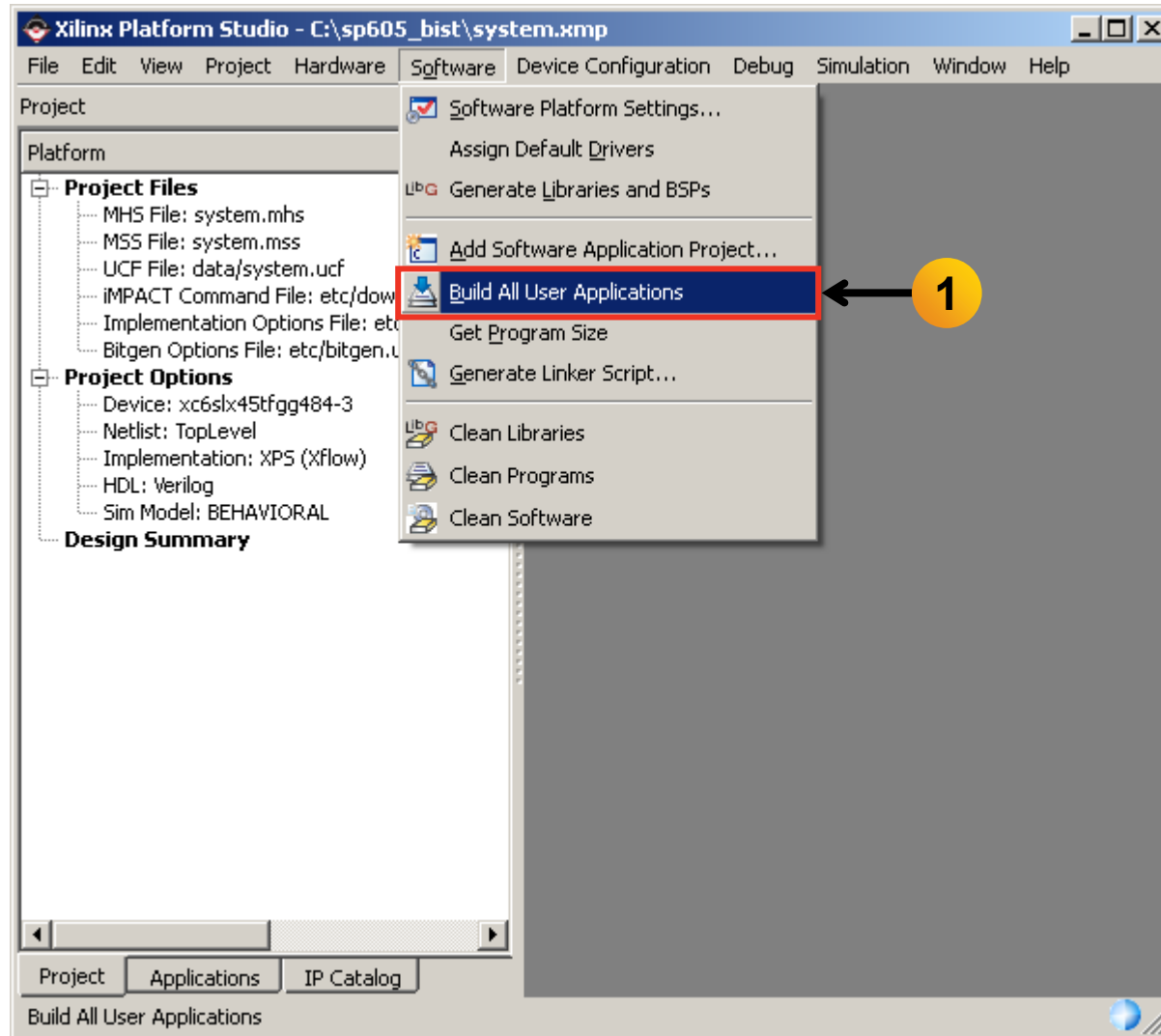
Compile SP605 BIST Design

- The BIST Design can be compiled with EDK
- Open XPS project <design path>\system.xmp
- Generate the libraries needed to create the bitstream
 - Select **Software** → **Generate Libraries and BSPs** (1)



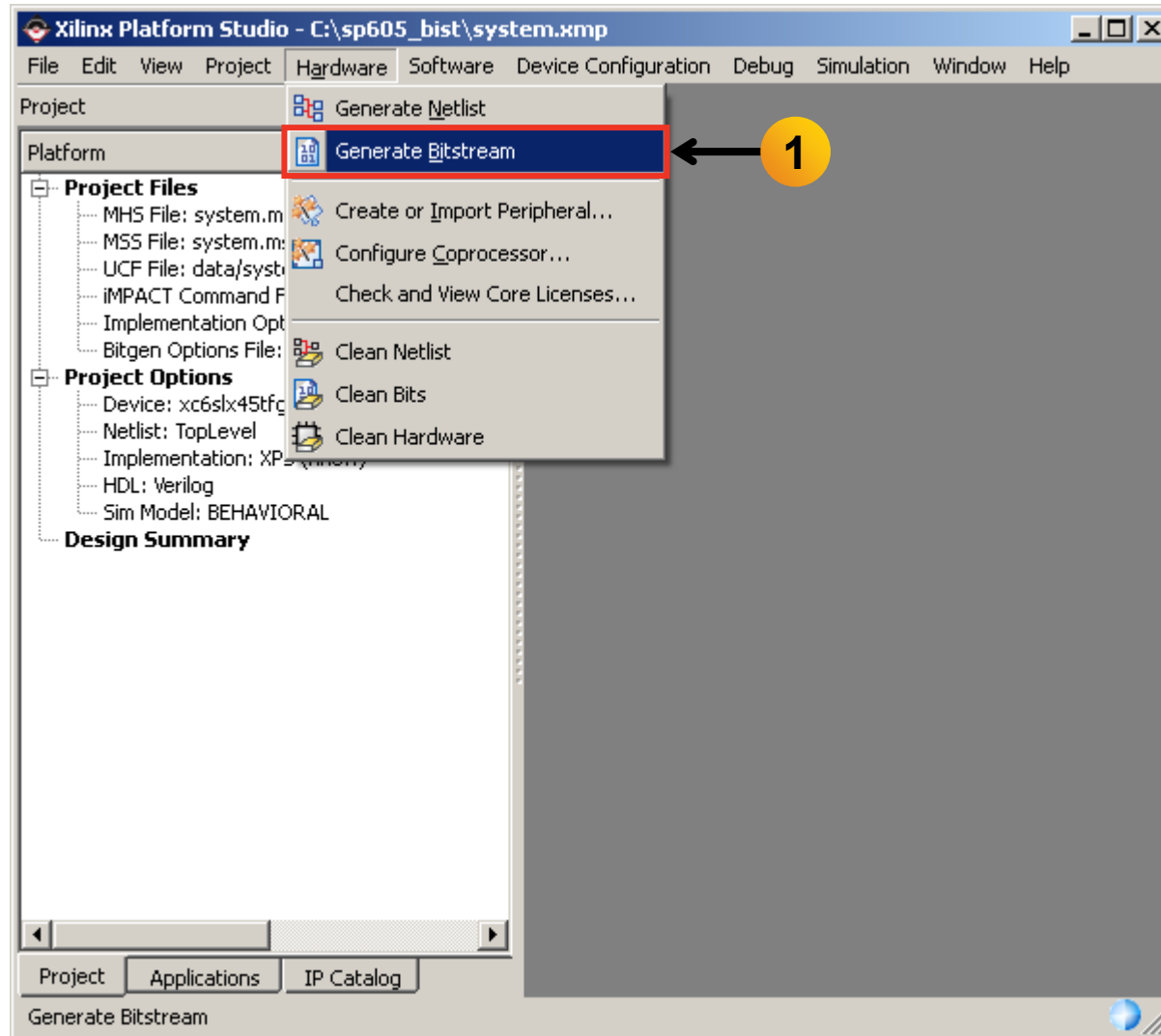
Compile SP605 BIST Design

- **Compile the Software Applications and create the application ELF files**
 - Select **Software** → **Build All User Applications** (1)



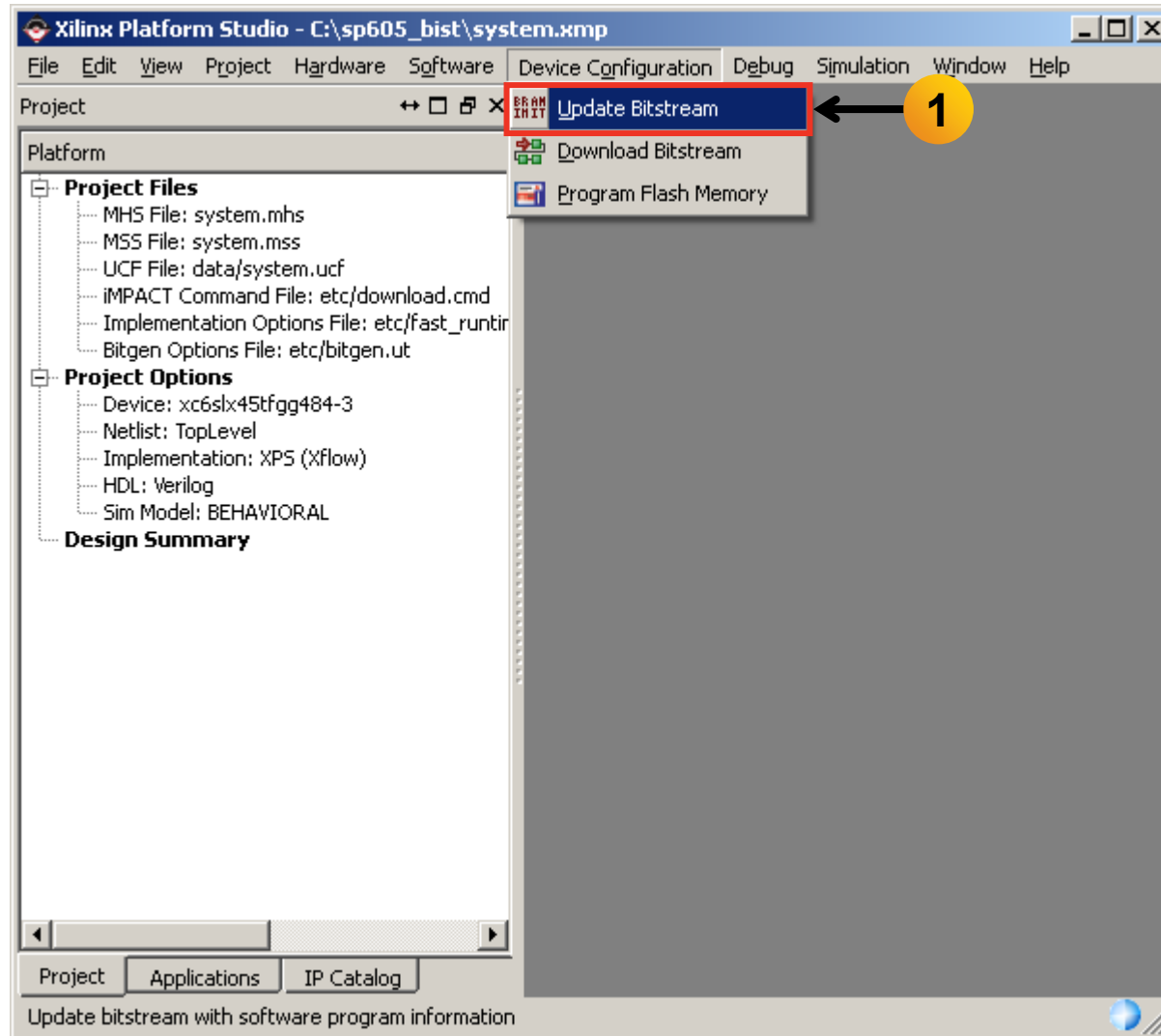
Compile SP605 BIST Design

- Create the hardware design, system.bit, located in <project directory>/implementation
 - Select Hardware → **Generate Bitstream** (1)



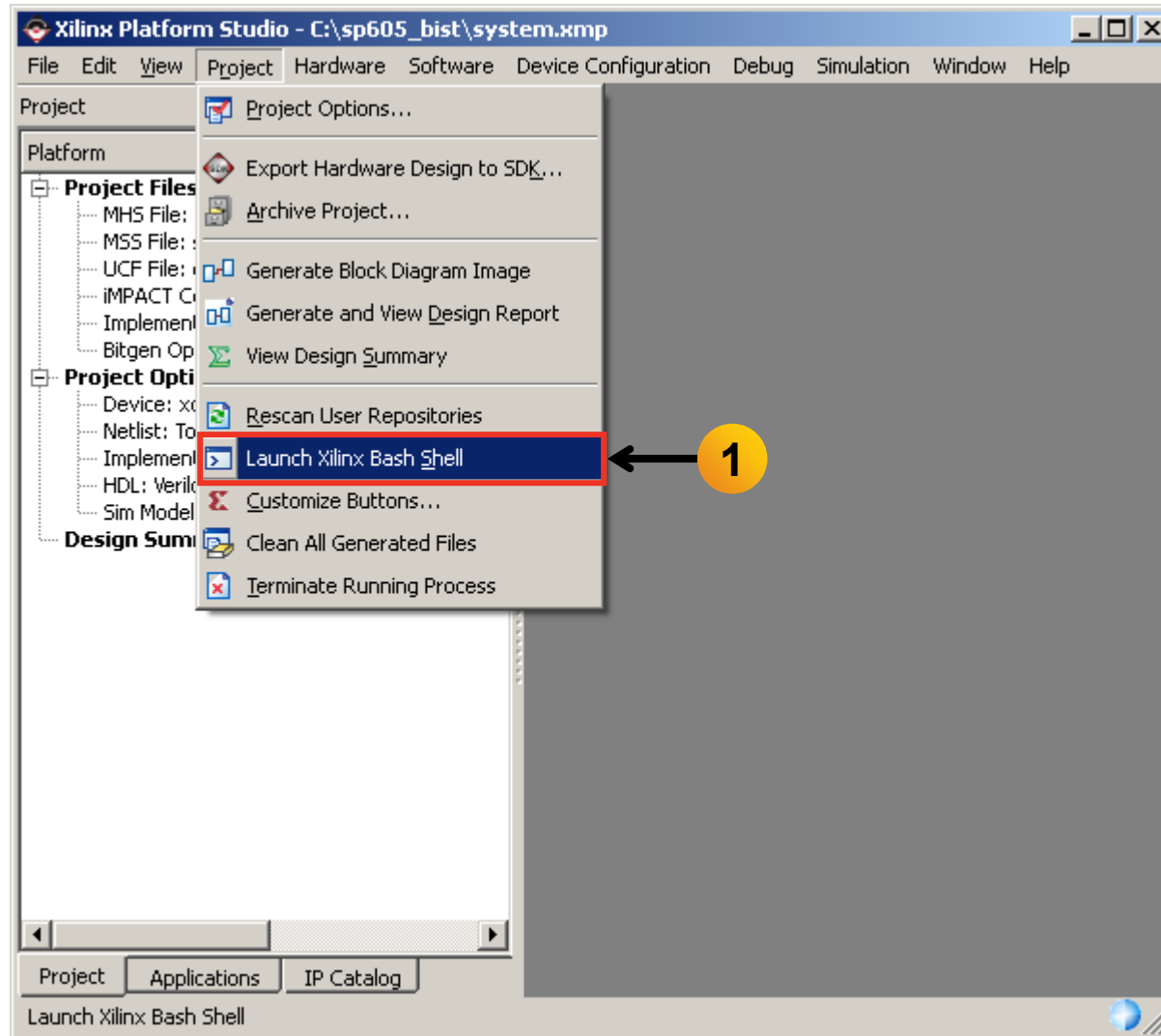
Compile SP605 BIST Design

- **Init memory with the Bootloader Application ELF**
 - Update the bitstream (download.bit) with the bootloader ELF (executable.elf)
 - Select **Device Configuration** → **Update Bitstream** (1)



Generate SP605 BIST Design CompactFlash

- **Convert the ELF files to S-record format and create ACE file**
 - Select **Project** → **Launch Xilinx Bash Shell** (1)



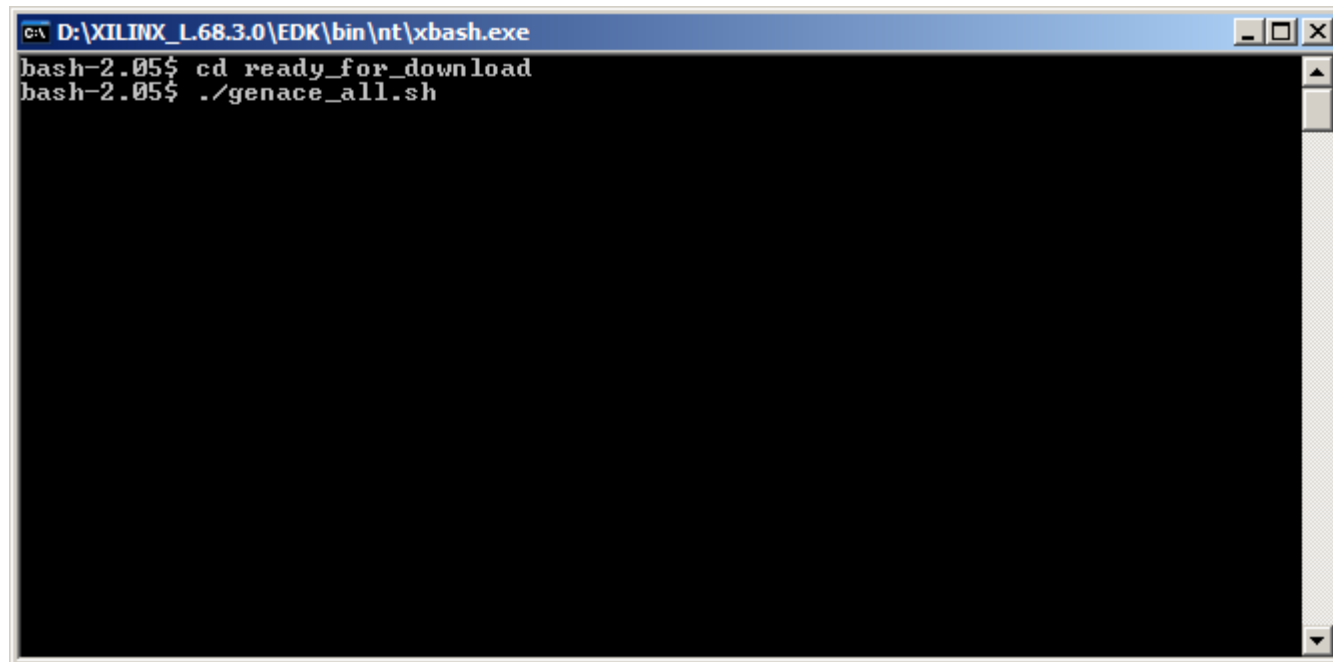
Generate SP605 BIST Design CompactFlash

- **Generate the S Records and ACE file**

- `cd ready_for_download`

- `./genace_all.sh`

- Copy the contents of **ready_for_download/cf_image** to your CompactFlash



```
C:\XILINX_L.68.3.0\EDK\bin\nt\xbash.exe
bash-2.05$ cd ready_for_download
bash-2.05$ ./genace_all.sh
```

References

References

- **EDK Documentation**

- Embedded System Tools Reference Guide

- http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/est_rm.pdf

- **System ACE CF**

- System ACE CompactFlash Solution

- http://www.xilinx.com/support/documentation/boards_and_kits/ug080.pdf

- **Spartan-6 Configuration**

- Spartan-6 FPGA Configuration User Guide

- http://www.xilinx.com/support/documentation/user_guides/ug380.pdf

Documentation

Documentation

- **Spartan-6**

- Spartan-6 FPGA Family

- <http://www.xilinx.com/products/spartan6/index.htm>

- **SP605 Documentation**

- Spartan-6 FPGA SP605 Evaluation Kit

- <http://www.xilinx.com/products/devkits/EK-S6-SP605-G.htm>

- SP605 Hardware User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug526.pdf

- SP605 Reference Design User Guide

- http://www.xilinx.com/support/documentation/boards_and_kits/ug527.pdf