Disclaimer:

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Trace length from the resistor pins to the FPGA pins MGTRREF and MGTVTTRCAL must be equal in length.

Power, GND, and Dedicated Banks

Title: Power, GND, and Dedicated Banks

PCB P/N: 0431534
SCH P/N: 0381305
PCB P/N: 0431534

XILINX

Sheet Size: B
Sheet 7 of 35
Rev: 04
Drawn By: WF
VCCOB3 remote sense pair connects from here back to (10)
Jumper to include FMC in JTAG chain.
The VIO voltage must match the appropriate bank IO voltage.
IIC Address = 0x76
SP605 EVALUATION PLATFORM

System ACE CF

Title: SYSTEM ACE CF
Created By: D.P. Date: 3-17-2010 9:23
Printed: 3-24-2010 Rev: 04
Sheet Size: B

Sheet 20 of 35

SCH P/N:  0381305
PCB P/N:  0431534

Part No. 1
LEVEL-SHD
SCHEM-TQFP144

U17

W701=71KΩ±5% R113

U37

SysACE Failsafe Mode Jumpers

FPGA & CPU Combined

Pushbutton
Silkscreen:

SYSACE_CFGMODEPIN
4.75K
1%
SYSACE_CFGADDR0
OUT
SYSACE_STAT_LED
1
SYSACE_TDI
SYSACE_CFGADDR2
20
200
Rev:

200
=sys

SP605 EVALUATION PLATFORM

U17

U17

System ACE CF

Title: SYSTEM ACE CF
Created By: D.P. Date: 3-17-2010 9:23
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Sheet Size: B

Sheet 20 of 35

SCH P/N:  0381305
PCB P/N:  0431534

Part No. 1
LEVEL-SHD
SCHEM-TQFP144

U17

W701=71KΩ±5% R113

U37

SysACE Failsafe Mode Jumpers

FPGA & CPU Combined

Pushbutton
Silkscreen:
PTD08A010W 10A Max. Power Channel
PMBus Address is calculated as follows:

\[ \text{PMBus Address} = 12 \times \text{Value(ADDRSEN1)} + \text{Value(ADDRSEN0)} \]

Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k

Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127

AGND should be a copper island underneath the 9240 and every associated module

VCCxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA

SP605 EVALUATION PLATFORM
TI UCD9240 Power System

FPGA UCD9240 PMBus Controller
NOTE: EMBEDDED VERSION

PART_NUMBER=CY7C68013A

 dateFormat: 9-24-2009_15:56

USB TYPE B

USB MINI_B

SHLD1

SHLD2

SHLD3

USBHDR_TMS_R

NOTE: J1 DOES NOT NEED TO BE POPULATED DURING PRODUCTION, BUT THE

MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH
The Embedded USB JTAG Download circuit on this page is for reference only! This circuit should not be designed into an end customer product or solution. Xilinx will not provide support on this embedded USB JTAG Download circuit.

- **Test P/N:** TSS0123
- **ART P/N:** 1280473
- **SCH P/N:** 0381305

**I2C EEPROM**

<table>
<thead>
<tr>
<th>Vendor ID</th>
<th>Product ID</th>
<th>Data Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x004B4</td>
<td>0x8613</td>
<td></td>
</tr>
<tr>
<td>0x03FD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XILINX</td>
<td>EMBEDDED</td>
<td></td>
</tr>
</tbody>
</table>

**DEFAULT PID/VID EEPROM**

- **Low Power Boot Conditions**
- **Power-On Reset**
- **Electronic Serial Number**

**PCB P/N:** 0431534

**Notes:**
- Produces 5ms Power-On Reset
- Status LEDs (Option A)
- JTAG Connector (Option B)
- Electromagnetic Number

**Last Revision:** 9-24-2009_15:00