

ZC702 EVALUATION PLATFORM HW-Z7-ZC702

(XC7Z020-CLG484)

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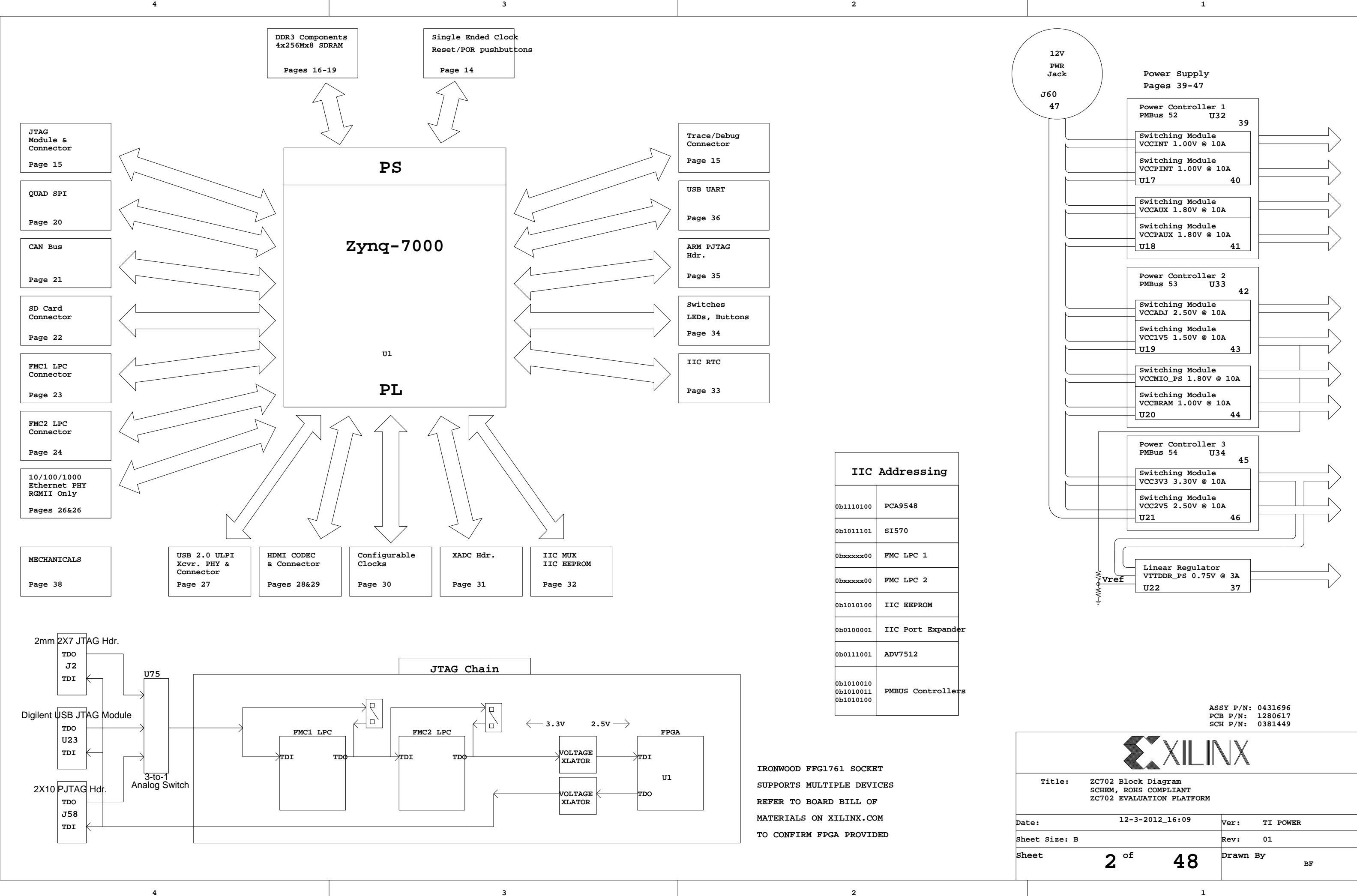
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Title:		ASSY P/N: 0431696 SCHEM, ROHS COMPLIANT PCB P/N: 1280617 ZC702 EVALUATION PLATFORM SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
Sheet	1 of 48	Drawn By	BF



IRONWOOD FFG1761 SOCKET
SUPPORTS MULTIPLE DEVICES
REFER TO BOARD BILL OF
MATERIALS ON XILINX.COM
TO CONFIRM FPGA PROVIDED

SOC_IRON_CL484

BANK 13
XC7Z020CLG484

VADJ

AA10	VCCO_13_AA10
AB3	VCCO_13_AB3
T5	VCCO_13_T5
U8	VCCO_13_U8
V11	VCCO_13_V11
W4	VCCO_13_W4
Y7	VCCO_13_Y7

IO_0_13_R7	
IO_L1P_T0_13_V10	
IO_L1N_T0_13_V9	
IO_L2P_T0_13_V8	
IO_L2N_T0_13_W8	
IO_L3P_T0_DQS_13_W11	
IO_L3N_T0_DQS_13_W10	
IO_L4P_T0_13_V12	
IO_L4N_T0_13_W12	
IO_L5P_T0_13_U12	
IO_L5N_T0_13_U11	
IO_L6P_T0_13_U10	
IO_L6N_T0_VREF_13_U9	
IO_L7P_T1_13_AA12	
IO_L7N_T1_13_AB12	
IO_L8P_T1_13_AA11	
IO_L8N_T1_13_AB11	
IO_L9P_T1_DQS_13_AB10	
IO_L9N_T1_DQS_13_AB9	
IO_L10P_T1_13_Y11	
IO_L10N_T1_13_Y10	
IO_L11P_T1_SRCC_13_AA9	
IO_L11N_T1_SRCC_13_AA8	
IO_L12P_T1_MRCC_13_Y9	
IO_L12N_T1_MRCC_13_Y8	
IO_L13P_T2_MRCC_13_Y6	
IO_L13N_T2_MRCC_13_Y5	
IO_L14P_T2_SRCC_13_AA7	
IO_L14N_T2_SRCC_13_AA6	
IO_L15P_T2_DQS_13_AB2	
IO_L15N_T2_DQS_13_AB1	
IO_L16P_T2_13_AB5	
IO_L16N_T2_13_AB4	
IO_L17P_T2_13_AB7	
IO_L17N_T2_13_AB6	
IO_L18P_T2_13_Y4	
IO_L18N_T2_13_AA4	
IO_L19P_T3_13_R6	
IO_L19N_T3_VREF_13_T6	
IO_L20P_T3_13_T4	
IO_L20N_T3_13_U4	
IO_L21P_T3_DQS_13_V5	
IO_L21N_T3_DQS_13_V4	
IO_L22P_T3_13_U6	
IO_L22N_T3_13_U5	
IO_L23P_T3_13_V7	
IO_L23N_T3_13_W7	
IO_L24P_T3_13_W6	
IO_L24N_T3_13_W5	
IO_25_13_U7	

R7	PL_PJTAG_TDO	R	■	35
V10	PL_PJTAG_TCK			
V9	PL_PJTAG_TMS			
V8	PL_PJTAG_TDI			
W8	IIC_SDA_MAIN_LS			
W11	IIC_SCL_MAIN_LS			
W10	PMOD2_1_LS			
V12	FMC2_LPC_LA23_P			
W12	FMC2_LPC_LA23_N			
U12	FMC2_LPC_LA26_P			
U11	FMC2_LPC_LA26_N			
U10	FMC2_LPC_LA22_P			
U9	FMC2_LPC_LA22_N			
AA12	FMC2_LPC_LA25_P			
AB12	FMC2_LPC_LA25_N			
AA11	FMC2_LPC_LA29_P			
AB11	FMC2_LPC_LA29_N			
AB10	FMC2_LPC_LA31_P			
AB9	FMC2_LPC_LA31_N			
Y11	FMC2_LPC_LA33_P			
Y10	FMC2_LPC_LA33_N			
AA9	FMC2_LPC_LA18_CC_P			
AA8	FMC2_LPC_LA18_CC_N			
Y9	USRCLK_P			
Y8	USRCLK_N			
Y6	FMC2_LPC_CLK1_M2C_P			
Y5	FMC2_LPC_CLK1_M2C_N			
AA7	FMC2_LPC_LA17_CC_P			
AA6	FMC2_LPC_LA17_CC_N			
AB2	FMC2_LPC_LA27_P			
AB1	FMC2_LPC_LA27_N			
AB5	FMC2_LPC_LA28_P			
AB4	FMC2_LPC_LA28_N			
AB7	FMC2_LPC_LA30_P			
AB6	FMC2_LPC_LA30_N			
Y4	FMC2_LPC_LA32_P			
AA4	FMC2_LPC_LA32_N			
R6	FMC2_LPC_LA19_P			
T6	FMC2_LPC_LA19_N			
T4	FMC2_LPC_LA20_P			
U4	FMC2_LPC_LA20_N			
V5	FMC2_LPC_LA21_P			
V4	FMC2_LPC_LA21_N			
U6	FMC2_LPC_LA24_P			
U5	FMC2_LPC_LA24_N			
V7	PMOD2_0_LS			
W7	GPIO_DIP_SW1			
W6	GPIO_DIP_SW0			
W5	PMOD1_3_LS			
U7	IIC_RTC_IRQ_1_B			



PL_PJTAG_TDO

U1

SOC_IRON_CL484

Zynq Bank 13



Title: Zynq Bank 13 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
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SOC_IRON_CL484

BANK 33
XC7Z020CLG484

VADJ

AA20	VCCO_33_AA20
AB13	VCCO_33_AB13
U18	VCCO_33_U18
V21	VCCO_33_V21
W14	VCCO_33_W14
Y17	VCCO_33_Y17

IO_0_33_U19	IO_L1P_T0_33_T21	IO_L1N_T0_33_U21	IO_L2P_T0_33_T22	IO_L2N_T0_33_U22	IO_L3P_T0_DQS_33_V22	IO_L3N_T0_DQS_33_W22	IO_L4P_T0_33_W20	IO_L4N_T0_33_W21	IO_L5P_T0_33_U20	IO_L5N_T0_33_V20	IO_L6P_T0_33_V18	IO_L6N_T0_VREF_33_V19	IO_L7P_T1_33_AA22	IO_L7N_T1_33_AB22	IO_L8P_T1_33_AA21	IO_L8N_T1_33_AB21	IO_L9P_T1_DQS_33_Y20	IO_L9N_T1_DQS_33_Y21	IO_L10P_T1_33_AB19	IO_L10N_T1_33_AB20	IO_L11P_T1_SRCC_33_Y19	IO_L11N_T1_SRCC_33_AA19	IO_L12P_T1_MRCC_33_Y18	IO_L12N_T1_MRCC_33_AA18	IO_L13P_T2_MRCC_33_W17	IO_L13N_T2_MRCC_33_W18	IO_L14P_T2_SRCC_33_W16	IO_L14N_T2_SRCC_33_Y16	IO_L15P_T2_DQS_33_U15	IO_L15N_T2_DQS_33_U16	IO_L16P_T2_33_U17	IO_L16N_T2_33_V17	IO_L17P_T2_33_AA17	IO_L17N_T2_33_AB17	IO_L18P_T2_33_AA16	IO_L18N_T2_33_AB16	IO_L19P_T3_33_V14	IO_L19N_T3_VREF_33_V15	IO_L20P_T3_33_V13	IO_L20N_T3_33_W13	IO_L21P_T3_DQS_33_W15	IO_L21N_T3_DQS_33_Y15	IO_L22P_T3_33_Y14	IO_L22N_T3_33_AA14	IO_L23P_T3_33_Y13	IO_L23N_T3_33_AA13	IO_L24P_T3_33_AB14	IO_L24N_T3_33_AB15	IO_25_33_U14
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U19	HDMI R D12	■	29
T21	FMC2 LPC LA07 P	■	24
U21	FMC2 LPC LA07 N	■	24
T22	FMC2 LPC LA14 P	■	24
U22	FMC2 LPC LA14 N	■	24
V22	FMC2 LPC LA13 P	■	24
W22	FMC2 LPC LA13 N	■	24
W20	HDMI R D9	■	29
W21	HDMI R D8	■	29
U20	HDMI R D7	■	29
V20	HDMI R D6	■	29
V18	HDMI R D5	■	29
V19	HDMI R D4	■	29
AA22	HDMI R D3	■	29
AB22	HDMI R D2	■	29
AA21	HDMI R D1	■	29
AB21	HDMI R D0	■	29
Y20	FMC2 LPC LA10 P	■	24
Y21	FMC2 LPC LA10 N	■	24
AB19	FMC2 LPC LA05 P	■	24
AB20	FMC2 LPC LA05 N	■	24
Y19	FMC2 LPC LA00 CC P	■	24
AA19	FMC2 LPC LA00 CC N	■	24
Y18	FMC2 LPC CLK0 M2C P	■	24
AA18	FMC2 LPC CLK0 M2C N	■	24
W17	PMOD1_2 LS	■	35
W18	HDMI R D10	■	29
W16	FMC2 LPC LA01 CC P	■	24
Y16	FMC2 LPC LA01 CC N	■	24
U15	FMC2 LPC LA09 P	■	24
U16	FMC2 LPC LA09 N	■	24
U17	FMC2 LPC LA06 P	■	24
V17	FMC2 LPC LA06 N	■	24
AA17	FMC2 LPC LA08 P	■	24
AB17	FMC2 LPC LA08 N	■	24
AA16	FMC2 LPC LA03 P	■	24
AB16	FMC2 LPC LA03 N	■	24
V14	FMC2 LPC LA02 P	■	24
V15	FMC2 LPC LA02 N	■	24
V13	FMC2 LPC LA04 P	■	24
W13	FMC2 LPC LA04 N	■	24
W15	FMC2 LPC LA12 P	■	24
Y15	FMC2 LPC LA12 N	■	24
Y14	FMC2 LPC LA11 P	■	24
AA14	FMC2 LPC LA11 N	■	24
Y13	FMC2 LPC LA15 P	■	24
AA13	FMC2 LPC LA15 N	■	24
AB14	FMC2 LPC LA16 P	■	24
AB15	FMC2 LPC LA16 N	■	24
U14	HDMI INT	■	28

U1

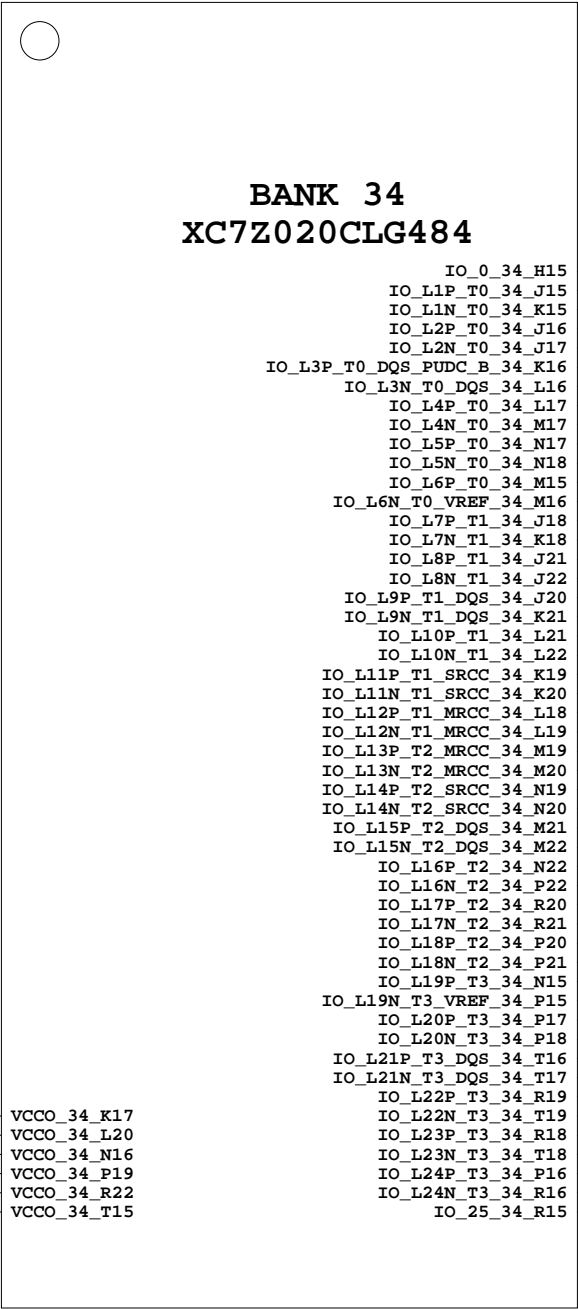
SOC_IRON_CL484

Zynq Bank 33



Title: Zynq Bank 33 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date: 12-3-2012_16:09	Ver: TI POWER		
Sheet Size: B		Rev: 01	
Sheet 5 of 48	Drawn By BF		

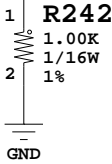
SOC_IRON_CL484



U1

SOC_IRON_CL484

H15	HDMI_R_VSYNC	29
J15	FMC1_LPC_LA07_P	23
K15	FMC1_LPC_LA07_N	23
J16	FMC1_LPC_LA14_P	23
J17	FMC1_LPC_LA14_N	23
K16		
L16	HDMI_R_CLK	29
L17	FMC1_LPC_LA10_P	23
M17	FMC1_LPC_LA10_N	23
N17	FMC1_LPC_LA05_P	23
N18	FMC1_LPC_LA05_N	23
M15	FMC1_LPC_LA09_P	23
M16	FMC1_LPC_LA09_N	23
J18	FMC1_LPC_LA06_P	23
K18	FMC1_LPC_LA06_N	23
J21	FMC1_LPC_LA08_P	23
J22	FMC1_LPC_LA08_N	23
J20	FMC1_LPC_LA03_P	23
K21	FMC1_LPC_LA03_N	23
L21	FMC1_LPC_LA02_P	23
L22	FMC1_LPC_LA02_N	23
K19	FMC1_LPC_LA00_CC_P	23
K20	FMC1_LPC_LA00_CC_N	23
L18	FMC1_LPC_CLK0_M2C_P	23
L19	FMC1_LPC_CLK0_M2C_N	23
M19	FMC1_LPC_CLK1_M2C_P	23
M20	FMC1_LPC_CLK1_M2C_N	23
N19	FMC1_LPC_LA01_CC_P	23
N20	FMC1_LPC_LA01_CC_N	23
M21	FMC1_LPC_LA04_P	23
M22	FMC1_LPC_LA04_N	23
N22	FMC1_LPC_LA12_P	23
P22	FMC1_LPC_LA12_N	23
R20	FMC1_LPC_LA11_P	23
R21	FMC1_LPC_LA11_N	23
P20	FMC1_LPC_LA15_P	23
P21	FMC1_LPC_LA15_N	23
N15	FMC1_LPC_LA16_P	23
P15	FMC1_LPC_LA16_N	23
P17	PMOD2_3_LS	34
P18	PMOD2_2_LS	34
T16	HDMI_R_D15	29
T17	HDMI_R_D14	29
R19	HDMI_R_D13	29
T19	HDMI_R_D11	29
R18	HDMI_R_HSYNC	29
T18	HDMI_R_DE	29
P16	FMC1_LPC_LA13_P	23
R16	FMC1_LPC_LA13_N	23
R15	HDMI_R_SPDIF	29



Zynq Bank 34

Title:		ASSY P/N: 0431696	
		PCB P/N: 1280617	
		SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
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SOC_IRON_CL484

BANK 35
XC7Z020CLG484

VADJ

A20	VCCO_35_A20
C16	VCCO_35_C16
D19	VCCO_35_D19
E22	VCCO_35_E22
F15	VCCO_35_F15
G18	VCCO_35_G18
H21	VCCO_35_H21


IO_0_35_H17	
IO_L1P_T0_AD0P_35_F16	
IO_L1N_T0_AD0N_35_E16	
IO_L2P_T0_AD8P_35_D16	
IO_L2N_T0_AD8N_35_D17	
IO_L3P_T0_DQS_AD1P_35_E15	
IO_L3N_T0_DQS_AD1N_35_D15	
IO_L4P_T0_35_G15	
IO_L4N_T0_35_G16	
IO_L5P_T0_AD9P_35_F18	
IO_L5N_T0_AD9N_35_E18	
IO_L6P_T0_35_G17	
IO_L6N_T0_VREF_35_F17	
IO_L7P_T1_AD2P_35_C15	
IO_L7N_T1_AD2N_35_B15	
IO_L8P_T1_AD10P_35_B16	
IO_L8N_T1_AD10N_35_B17	
IO_L9P_T1_DQS_AD3P_35_A16	
IO_L9N_T1_DQS_AD3N_35_A17	
IO_L10P_T1_AD11P_35_A18	
IO_L10N_T1_AD11N_35_A19	
IO_L11P_T1_SRCC_35_C17	
IO_L11N_T1_SRCC_35_C18	
IO_L12P_T1_MRCC_35_D18	
IO_L12N_T1_MRCC_35_C19	
IO_L13P_T2_MRCC_35_B19	
IO_L13N_T2_MRCC_35_B20	
IO_L14P_T2_AD4P_SRCC_35_D20	
IO_L14N_T2_AD4N_SRCC_35_C20	
IO_L15P_T2_DQS_AD12P_35_A21	
IO_L15N_T2_DQS_AD12N_35_A22	
IO_L16P_T2_35_D22	
IO_L16N_T2_35_C22	
IO_L17P_T2_AD5P_35_E21	
IO_L17N_T2_AD5N_35_D21	
IO_L18P_T2_AD13P_35_B21	
IO_L18N_T2_AD13N_35_B22	
IO_L19P_T3_35_H19	
IO_L19N_T3_VREF_35_H20	
IO_L20P_T3_AD6P_35_G19	
IO_L20N_T3_AD6N_35_F19	
IO_L21P_T3_DQS_AD14P_35_E19	
IO_L21N_T3_DQS_AD14N_35_E20	
IO_L22P_T3_AD7P_35_G20	
IO_L22N_T3_AD7N_35_G21	
IO_L23P_T3_35_F21	
IO_L23N_T3_35_F22	
IO_L24P_T3_AD15P_35_H22	
IO_L24N_T3_AD15N_35_G22	
IO_25_35_H18	

H17	XADC_GPIO_0	31
F16	XADC_VAUX0P_R	31
E16	XADC_VAUX0N_R	31
D16	XADC_VAUX8P_R	31
D17	XADC_VAUX8N_R	31
E15	PMOD1_0_LS	31
D15	PMOD1_1_LS	35
G15	FMCI_LPC_LA23_P	23
G16	FMCI_LPC_LA23_N	23
F18	FMCI_LPC_LA26_P	23
E18	FMCI_LPC_LA26_N	23
G17	FMCI_LPC_LA22_P	23
F17	FMCI_LPC_LA22_N	23
C15	FMCI_LPC_LA25_P	23
B15	FMCI_LPC_LA25_N	23
B16	FMCI_LPC_LA29_P	23
B17	FMCI_LPC_LA29_N	23
A16	FMCI_LPC_LA31_P	23
A17	FMCI_LPC_LA31_N	23
A18	FMCI_LPC_LA33_P	23
A19	FMCI_LPC_LA33_N	23
C17	FMCI_LPC_LA27_P	23
C18	FMCI_LPC_LA27_N	23
D18	SYSCLK_P	30
C19	SYSCLK_N	30
B19	FMCI_LPC_LA17_CC_P	23
B20	FMCI_LPC_LA17_CC_N	23
D20	FMCI_LPC_LA18_CC_P	23
C20	FMCI_LPC_LA18_CC_N	23
A21	FMCI_LPC_LA24_P	23
A22	FMCI_LPC_LA24_N	23
D22	FMCI_LPC_LA28_P	23
C22	FMCI_LPC_LA28_N	23
E21	FMCI_LPC_LA30_P	23
D21	FMCI_LPC_LA30_N	23
B21	FMCI_LPC_LA32_P	23
B22	FMCI_LPC_LA32_N	23
H19	FMC_C2M_PG_LS	34
H20	HDMI_SPDIF_OUT_LS	34
G19	GPIO_SW_N	34
F19	GPIO_SW_S	34
E19	FMCI_LPC_LA19_P	23
E20	FMCI_LPC_LA19_N	23
G20	FMCI_LPC_LA20_P	23
G21	FMCI_LPC_LA20_N	23
F21	FMCI_LPC_LA21_P	23
F22	FMCI_LPC_LA21_N	23
H22	XADC_GPIO_1	31
G22	XADC_GPIO_2	31
H18	XADC_GPIO_3	31

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SOC_IRON_CL484

Zynq Bank 35

			
Title:		Zynq Bank 35 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
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SOC_IRON_CL484

BANK 500
XC7Z020CLG484

PS_CLK_500_F7	F7	PS_CLK	30
PS_POR_B_500_B5	B5	PS_POR_B	14,25,27
PS_MIO15_500_E6	E6	SDIO_SDWP	22
PS_MIO14_500_B6	B6	PS_DIP_SW0	8
PS_MIO13_500_A6	A6	IIC_MUX_RESET_B_LS	34
PS_MIO12_500_C5	C5	PS_DIP_SW1	8
PS_MIO11_500_B4	B4	PHY_RESET_B_AND	25
PS_MIO10_500_G7	G7	PS_LED1	8
PS_MIO9_500_C4	C4	CAN_STB_B_LS	21
PS_MIO8_500_E5	E5	PS_MIO8_LED0	8,14
PS_MIO7_500_D5	D5	USB_RESET_B_AND	14,27
PS_MIO6_500_A4	A4	QSPI_CLK	14,20
PS_MIO5_500_A3	A3	QSPI_IO3	14,20
PS_MIO4_500_E4	E4	QSPI_IO2	14,20
PS_MIO3_500_F6	F6	QSPI_IO1	14,20
PS_MIO2_500_A2	A2	QSPI_IO0	14,20
PS_MIO1_500_A1	A1	QSPI_CS_B	20
PS_MIO0_500_G6	G6	SDIO_SDDET	22

U1

SOC_IRON_CL484

VCC1V8

B3 VCCO_MIO0_500_B3
C6 VCCO_MIO0_500_C6

VCC1V8

Pushbutton
TL3301EF100QG

1 P1 P2 2

SW13

R413
4.7K
1/10W
5%

GND

VCC1V8

Pushbutton
TL3301EF100QG

1 P1 P2 2

SW14

R414
4.7K
1/10W
5%

GND

VCC1V8

SDA02H1SBD

SW15

VCC3V3

D523
LED-GRN-SMT

R416
1%
1/10W
261

Q21

NDS331N
460MW

GND

PS_LED1

SOC_IRON_CL484

BANK 501
XC7Z020CLG484

PS_MIO_VREF_501_F8	F8	PHY_TXD0	25
PS_MIO17_501_E9	E9	PHY_TXD2	25
PS_MIO19_501_E10	E10	PHY_TX_CTRL	25
PS_MIO21_501_F11	F11	PHY_RXD0	25
PS_MIO23_501_E11	E11	PHY_RXD2	25
PS_MIO25_501_F12	F12	PHY_RX_CTRL	25
PS_MIO27_501_D7	D7	PHY_RX_CTRL	25
PS_MIO29_501_E8	E8	USB_DIR	27
PS_MIO31_501_F9	F9	USB_NXT	27
PS_MIO33_501_G13	G13	USB_DATA1	27
PS_MIO35_501_F14	F14	USB_DATA3	27
PS_MIO38_501_F13	F13	USB_DATA6	27
PS_MIO40_501_E14	E14	SDIO_CLK_LS	22
PS_MIO42_501_D8	D8	SDIO_DAT0_LS	22
PS_MIO44_501_E13	E13	SDIO_DAT2_LS	22
PS_MIO46_501_D12	D12	CAN_RXD_LS	21
PS_MIO48_501_D11	D11	USB_UART_RX	36
PS_MIO50_501_D13	D13	PS_SCL_MAIN	32
PS_MIO52_501_D10	D10	PHY_MDC	25
PS_SRST_B_501_C9	C9	PS_SRST_B	25
PS_MIO16_501_D6	D6	PHY_TX_CLK	25
PS_MIO18_501_A7	A7	PHY_TXD1	25
PS_MIO20_501_A8	A8	PHY_TXD3	25
PS_MIO22_501_A14	A14	PHY_RX_CLK	25
PS_MIO24_501_B7	B7	PHY_RXD1	25
PS_MIO26_501_A13	A13	PHY_RXD3	25
PS_MIO28_501_A12	A12	USB_DATA4	27
PS_MIO30_501_A11	A11	USB_STP	27
PS_MIO32_501_C7	C7	USB_DATA0	27
PS_MIO34_501_B12	B12	USB_DATA2	27
PS_MIO36_501_A9	A9	USB_CLKOUT	27
PS_MIO37_501_B14	B14	USB_DATA5	27
PS_MIO39_501_C13	C13	USB_DATA7	27
PS_MIO41_501_C8	C8	SDIO_CMD_LS	22
PS_MIO43_501_B11	B11	SDIO_DAT1_LS	22
PS_MIO45_501_B9	B9	SDIO_CD_DAT3_LS	22
PS_MIO47_501_B10	B10	CAN_TXD_LS	21
PS_MIO49_501_C14	C14	USB_UART_TX	36
PS_MIO51_501_C10	C10	PS_SDA_MAIN	32
PS_MIO53_501_C12	C12	PHY_MDIO	25

U1

SOC_IRON_CL484

VCC1V8

A10 VCCO_MIO1_501_A10
B13 VCCO_MIO1_501_B13
D9 VCCO_MIO1_501_D9
E12 VCCO_MIO1_501_E12

VCC3V3

D512
LED-GRN-SMT

R393
1%
1/10W
261

Q11

NDS331N
460MW

GND

PS_MIO8_LED0

R243
1.00K
1/16W
1%

R244
1.00K
1/16W
1%

VCC1V8

C192
0.01UF
25V
X7R

14

GND

Zynq Banks 500, 501



Title: Zynq Banks 500, 501
SCHEM, ROHS COMPLIANT
ZC702 EVALUATION PLATFORM

ASSY P/N: 0431696
PCB P/N: 1280617
SCH P/N: 0381449

Date: 12-3-2012_16:09 Ver: TI POWER

Sheet Size: B Rev: 01

Sheet 8 of 48 Drawn By BF

SOC_IRON_CL484

BANK 502
XC7Z020CLG484

PS_DDR_DRST_B_502_F3	F3	PS_DDR3_RESET_B	16,17,18,19
PS_DDR_DQ0_502_D1	D1	PS_DDR3_DQ3	16
PS_DDR_DQ1_502_C3	C3	PS_DDR3_DQ1	16
PS_DDR_DQ2_502_B2	B2	PS_DDR3_DQ6	16
PS_DDR_DQ3_502_D3	D3	PS_DDR3_DQ7	16
PS_DDR_DM0_502_B1	B1	PS_DDR3_DM0	16
PS_DDR_DQS_P0_502_C2	C2	PS_DDR3_DQS0_P	16
PS_DDR_DQS_N0_502_D2	D2	PS_DDR3_DQS0_N	16
PS_DDR_DQ4_502_E3	E3	PS_DDR3_DQ0	16
PS_DDR_DQ5_502_E1	E1	PS_DDR3_DQ5	16
PS_DDR_DQ6_502_F2	F2	PS_DDR3_DQ2	16
PS_DDR_DQ7_502_F1	F1	PS_DDR3_DQ4	16
PS_DDR_DQ8_502_G2	G2	PS_DDR3_DQ8	17
PS_DDR_DQ9_502_G1	G1	PS_DDR3_DQ10	17
PS_DDR_DQ10_502_L1	L1	PS_DDR3_DQ9	17
PS_DDR_DQ11_502_L2	L2	PS_DDR3_DQ13	17
PS_DDR_DM1_502_H3	H3	PS_DDR3_DM1	17
PS_DDR_DQS_P1_502_H2	H2	PS_DDR3_DQS1_P	17
PS_DDR_DQS_N1_502_J2	J2	PS_DDR3_DQS1_N	17
PS_DDR_DQ12_502_L3	L3	PS_DDR3_DQ12	17
PS_DDR_DQ13_502_K1	K1	PS_DDR3_DQ11	17
PS_DDR_DQ14_502_J1	J1	PS_DDR3_DQ14	17
PS_DDR_DQ15_502_K3	K3	PS_DDR3_DQ15	17
PS_DDR_A14_502_G4	G4	PS_DDR3_A14	17,18,19
PS_DDR_A13_502_F4	F4	PS_DDR3_A13	17,18,19
PS_DDR_A12_502_H4	H4	PS_DDR3_A12	17,18,19
PS_DDR_A11_502_G5	G5	PS_DDR3_A11	17,18,19
PS_DDR_A10_502_J3	J3	PS_DDR3_A10	17,18,19
PS_DDR_A9_502_H5	H5	PS_DDR3_A9	17,18,19
PS_DDR_A8_502_J5	J5	PS_DDR3_A8	17,18,19
PS_DDR_A7_502_J6	J6	PS_DDR3_A7	17,18,19
PS_DDR_A6_502_J7	J7	PS_DDR3_A6	17,18,19
PS_DDR_A5_502_K5	K5	PS_DDR3_A5	17,18,19
PS_DDR_A4_502_K6	K6	PS_DDR3_A4	17,18,19
PS_DDR_A3_502_L4	L4	PS_DDR3_A3	17,18,19
PS_DDR_VRN_502_M7	M7	PS_VRN	9
PS_DDR_VRP_502_N7	N7	PS_VRP	9
PS_DDR_CKP_502_N4	N4	PS_DDR3_CLK_P	17,18,19
PS_DDR_CKN_502_N5	N5	PS_DDR3_CLK_N	17,18,19
PS_DDR_A2_502_K4	K4	PS_DDR3_A2	17,18,19
PS_DDR_A1_502_M5	M5	PS_DDR3_A1	17,18,19
PS_DDR_A0_502_M4	M4	PS_DDR3_A0	17,18,19
PS_DDR_BA2_502_M6	M6	PS_DDR3_BA2	17,18,19
PS_DDR_BA1_502_L6	L6	PS_DDR3_BA1	17,18,19
PS_DDR_BA0_502_L7	L7	PS_DDR3_BA0	17,18,19
PS_DDR_ODT_502_P5	P5	PS_DDR3_ODT	16,17,18,19
PS_DDR_CS_B_502_P6	P6	PS_DDR3_CS_B	16,17,18,19
PS_DDR_CKE_502_V3	V3	PS_DDR3_CKE	17,18,19
PS_DDR_WE_B_502_R4	R4	PS_DDR3_WE_B	17,18,19
PS_DDR_CAS_B_502_P3	P3	PS_DDR3_CAS_B	17,18,19
PS_DDR_RAS_B_502_R5	R5	PS_DDR3_RAS_B	17,18,19
PS_DDR_DQ16_502_M1	M1	PS_DDR3_DQ16	18
PS_DDR_DQ17_502_T3	T3	PS_DDR3_DQ17	18
PS_DDR_DQ18_502_N3	N3	PS_DDR3_DQ18	18
PS_DDR_DQ19_502_T1	T1	PS_DDR3_DQ19	18
PS_DDR_DM2_502_P1	P1	PS_DDR3_DM2	18
PS_DDR_DQS_P2_502_N2	N2	PS_DDR3_DQS2_P	18
PS_DDR_DQS_N2_502_P2	P2	PS_DDR3_DQS2_N	18
PS_DDR_DQ20_502_R3	R3	PS_DDR3_DQ20	18
PS_DDR_DQ21_502_T2	T2	PS_DDR3_DQ21	18
PS_DDR_DQ22_502_M2	M2	PS_DDR3_DQ22	18
PS_DDR_DQ23_502_R1	R1	PS_DDR3_DQ23	18
PS_DDR_DQ24_502_AA3	AA3	PS_DDR3_DQ27	19
PS_DDR_DQ25_502_U1	U1	PS_DDR3_DQ24	19
PS_DDR_DQ26_502_AA1	AA1	PS_DDR3_DQ25	19
PS_DDR_DQ27_502_U2	U2	PS_DDR3_DQ26	19
PS_DDR_DM3_502_AA2	AA2	PS_DDR3_DM3	19
PS_DDR_DQS_P3_502_V2	V2	PS_DDR3_DQS3_P	19
PS_DDR_DQS_N3_502_W2	W2	PS_DDR3_DQS3_N	19
PS_DDR_DQ28_502_W1	W1	PS_DDR3_DQ28	19
PS_DDR_DQ29_502_Y3	Y3	PS_DDR3_DQ29	19
PS_DDR_DQ30_502_W3	W3	PS_DDR3_DQ30	19
PS_DDR_DQ31_502_Y1	Y1	PS_DDR3_DQ31	19
PS_DDR_VREF0_502_H7	H7		
PS_DDR_VREF1_502_P7	P7		

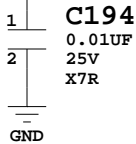
VCC1V5

E2	VCCO_DDR_502_E2
F5	VCCO_DDR_502_F5
H1	VCCO_DDR_502_H1
J4	VCCO_DDR_502_J4
K7	VCCO_DDR_502_K7
M3	VCCO_DDR_502_M3
N6	VCCO_DDR_502_N6
R2	VCCO_DDR_502_R2
V1	VCCO_DDR_502_V1

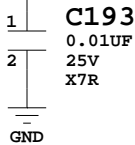
U1

SOC_IRON_CL484

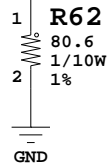
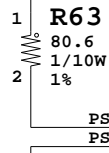
VTTVREF_PS



VTTVREF_PS



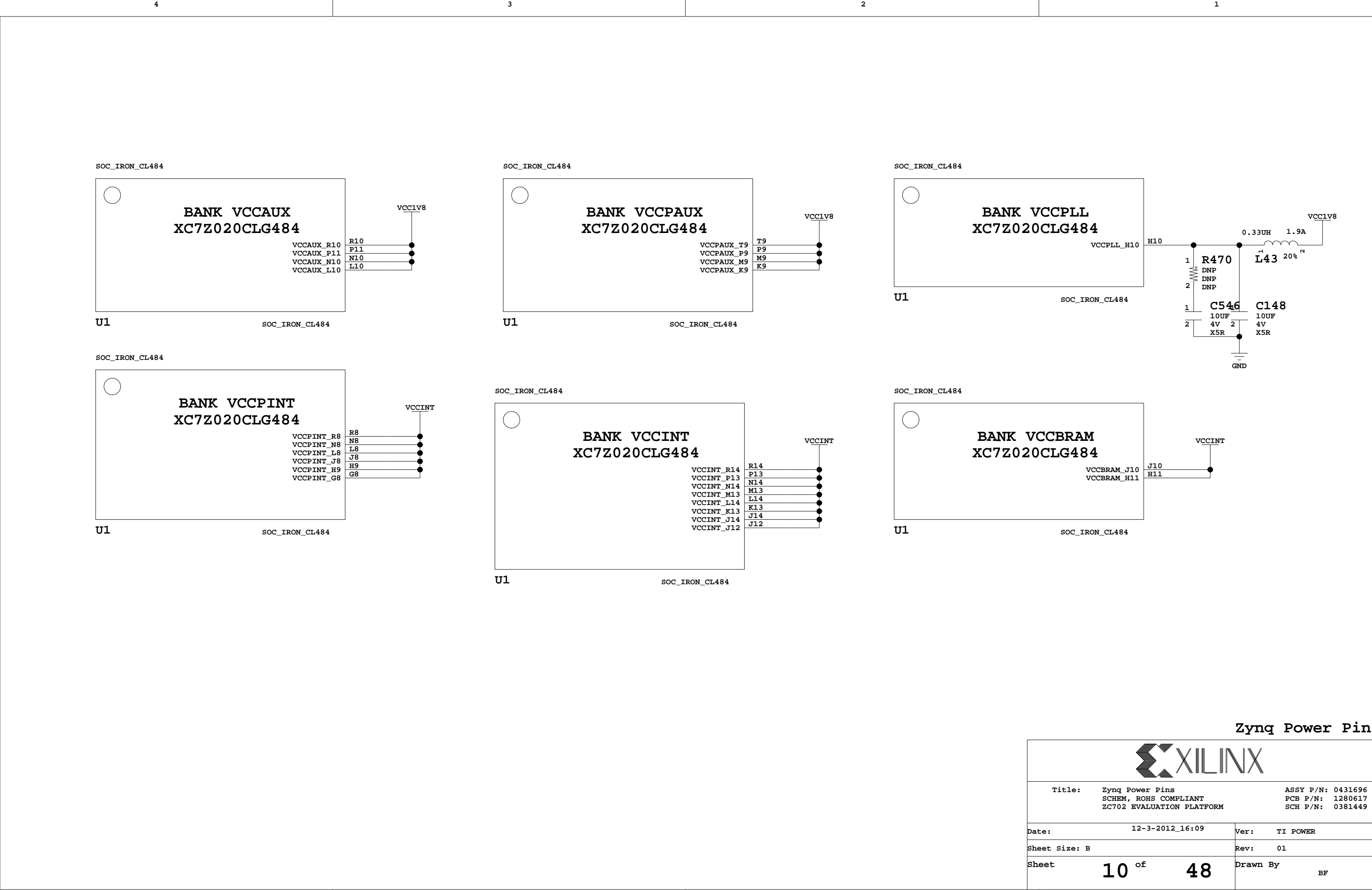
VCC1V5



Zynq Bank 502



Title: Zynq Bank 502 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
Sheet 9 of 48	Drawn By BF	



Zynq Power Pins

Title:		Zynq Power Pins SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
Sheet	10 of 48	Drawn By	BF

SOC_IRON_CL484



BANK GND
XC7Z020CLG484

- GND_Y22
- GND_Y12
- GND_Y2
- GND_W19
- GND_W9
- GND_V16
- GND_V6
- GND_U13
- GND_U3
- GND_T20
- GND_R17
- GND_R13
- GND_R11
- GND_R9
- GND_P14
- GND_P12
- GND_P10
- GND_P8
- GND_P4
- GND_N21
- GND_N13
- GND_N9
- GND_N1
- GND_M18
- GND_M14
- GND_M10
- GND_M8
- GND_L15
- GND_L13
- GND_L9
- GND_L5
- GND_K22
- GND_K14
- GND_K10
- GND_K8
- GND_K2
- GND_J19
- GND_J13
- GND_J11
- GND_J9
- GND_H16
- GND_H14
- GND_H12
- GND_H8
- GND_H6
- GND_G3
- GND_F20
- GND_F10
- GND_E17
- GND_E7
- GND_D14
- GND_D4
- GND_C21
- GND_C11
- GND_C1
- GND_B18
- GND_B8
- GND_AB18
- GND_AB8
- GND_AA15
- GND_AA5
- GND_A15
- GND_A5

- Y22
- Y12
- Y2
- W19
- W9
- V16
- V6
- U13
- U3
- T20
- R17
- R13
- R11
- R9
- P14
- P12
- P10
- P8
- P4
- N21
- N13
- N9
- N1
- M18
- M14
- M10
- M8
- L15
- L13
- L9
- L5
- K22
- K14
- K10
- K8
- K2
- J19
- J13
- J11
- J9
- H16
- H14
- H12
- H8
- H6
- G3
- F20
- F10
- E17
- E7
- D14
- D4
- C21
- C11
- C1
- B18
- B8
- AB18
- AB8
- AA15
- AA5
- A15
- A5

GND

U1

SOC_IRON_CL484

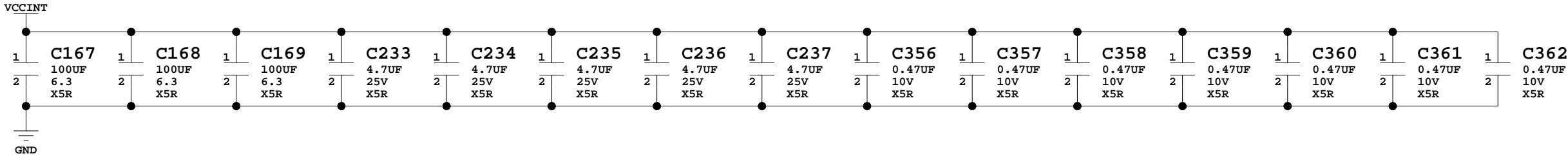
Zynq GND



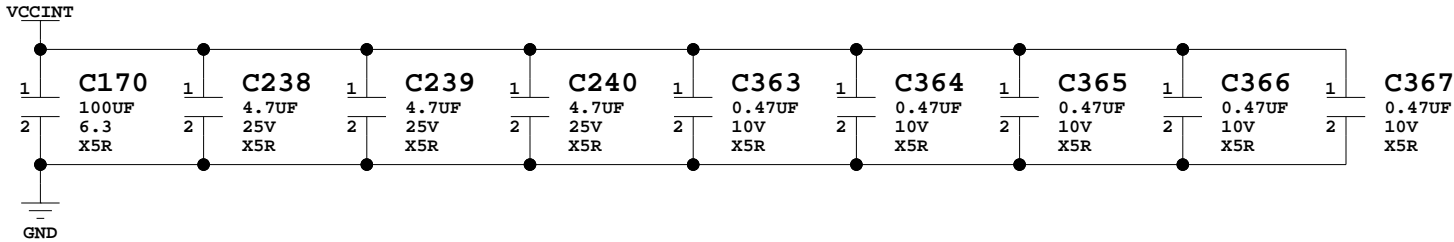
Title: Zynq GND SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
Sheet	11 of 48	Drawn By	BF

BYPASS CAPACITORS

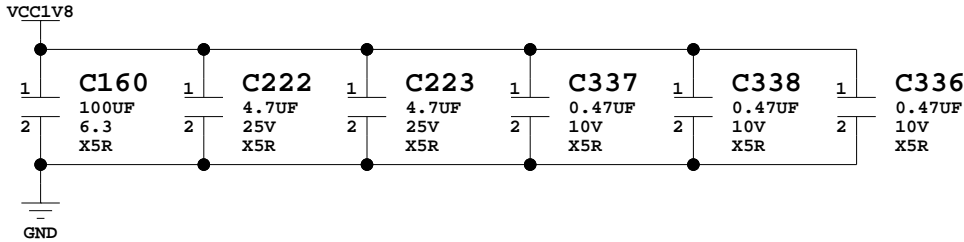
VCCINT_PL 100uF (3), 4.7uF (5), 0.47uF (7)



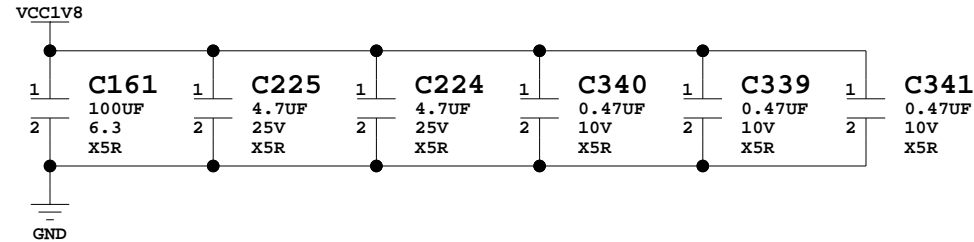
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



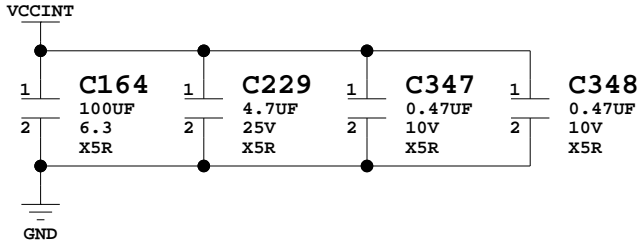
VCCAUX 100uF (1), 4.7uF (2), 0.47uF (3)



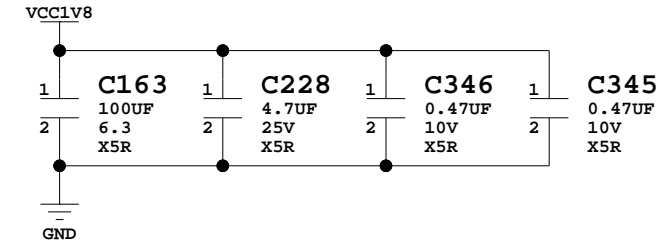
VCCPAUX 100uF (1), 4.7uF (2), 0.47uF (3)



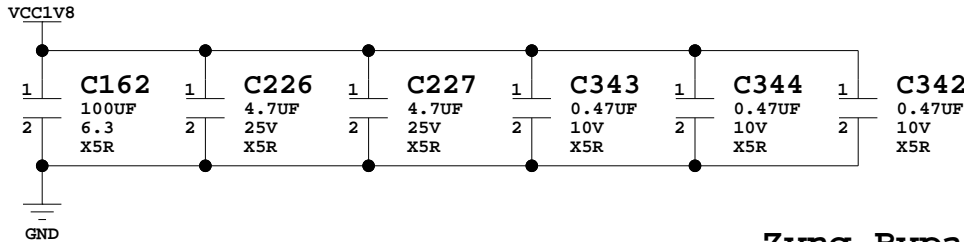
VCCBRAM 100uF (1), 4.7uF (1), 0.47uF (2)



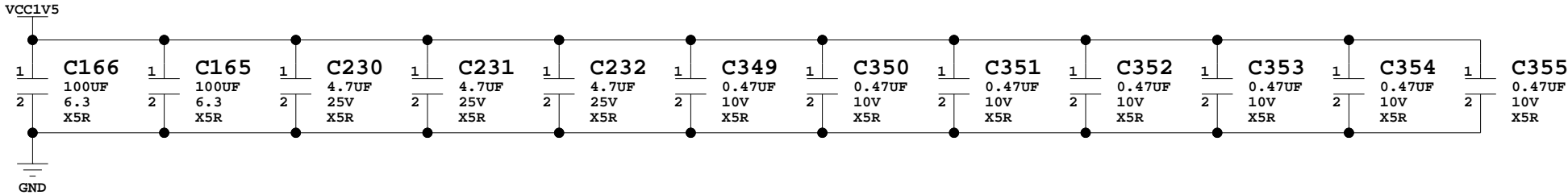
VCCP0_PS 100uF (1), 4.7uF (1), 0.47uF (2)




VCCP1_PS 100uF (1), 4.7uF (2), 0.47uF (3)



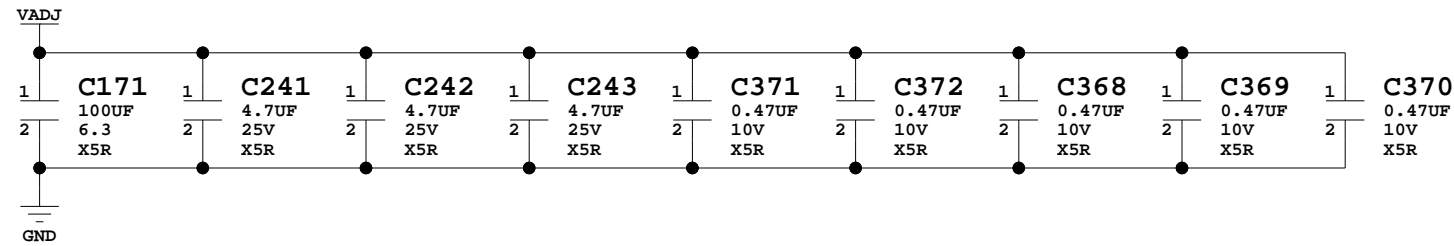
VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)



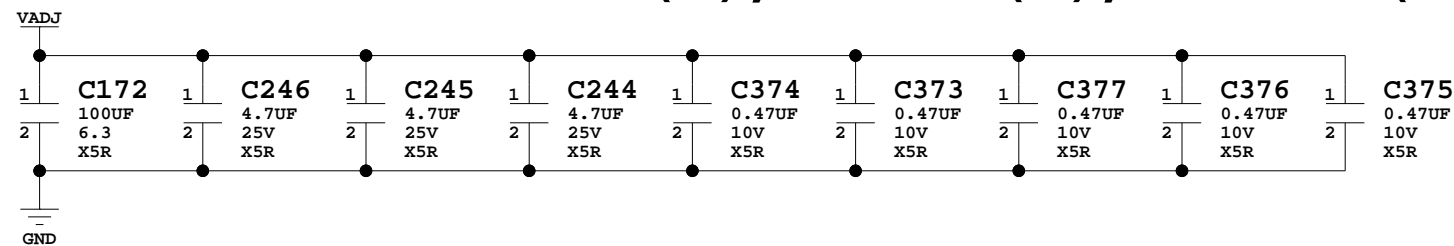
Zynq Bypass Capacitors

		
Title: Zynq Bypass Capacitors SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
Sheet 12 of 48	Drawn By BF	

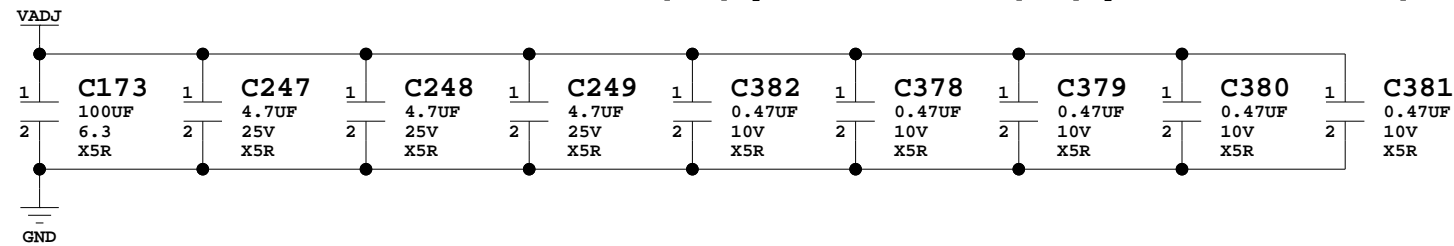
Bank 13 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



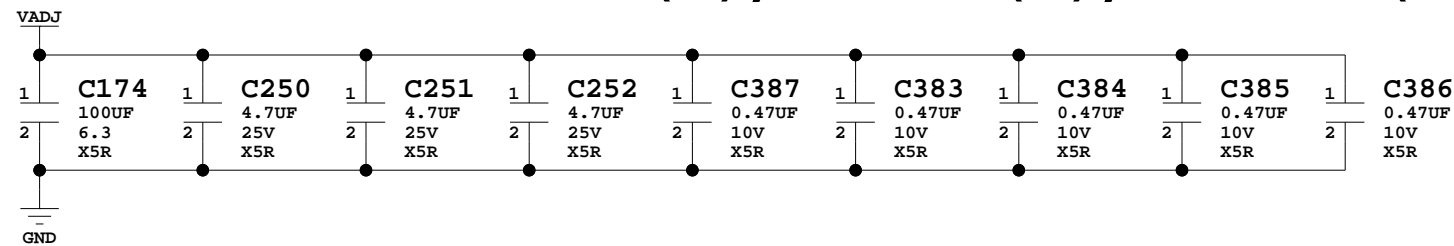
Bank 33 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



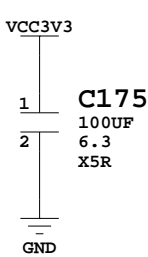
Bank 34 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)



Bank 35 VADJ 100uF (1), 4.7uF (3), 0.47uF (5)

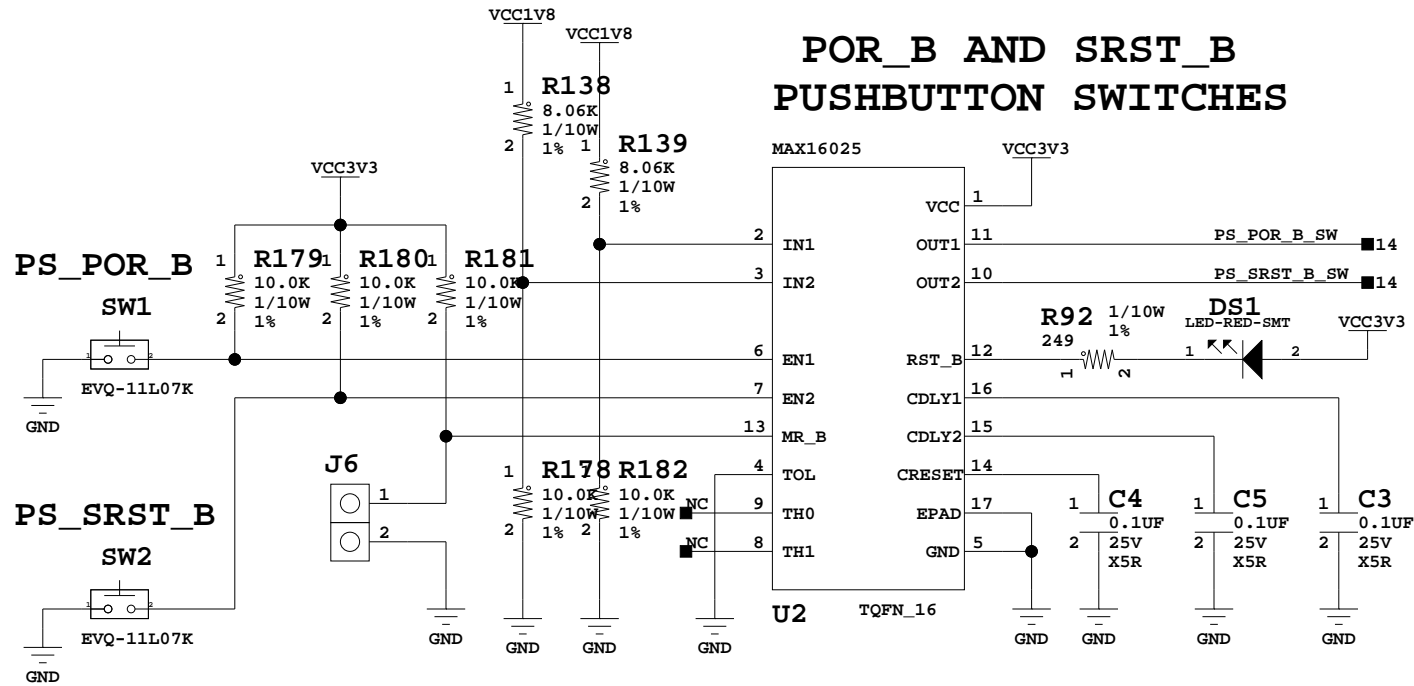


VCC2V5_PL 100uF (1)

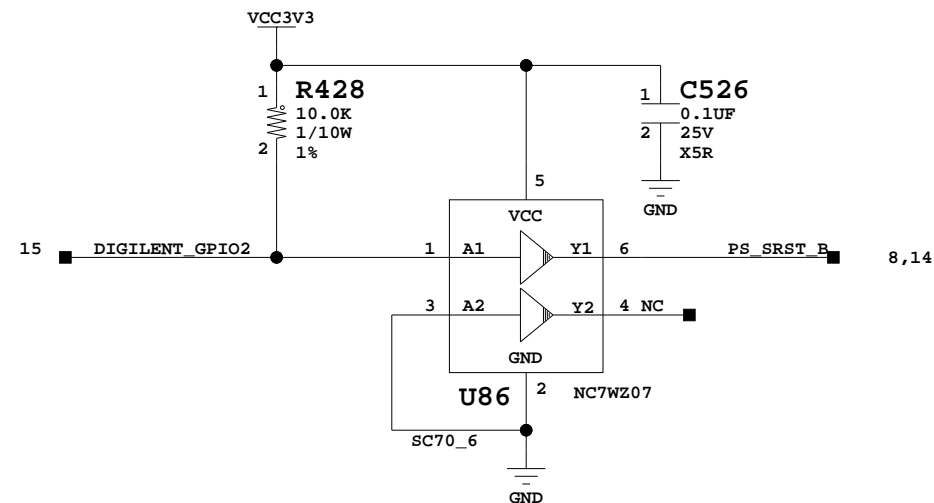
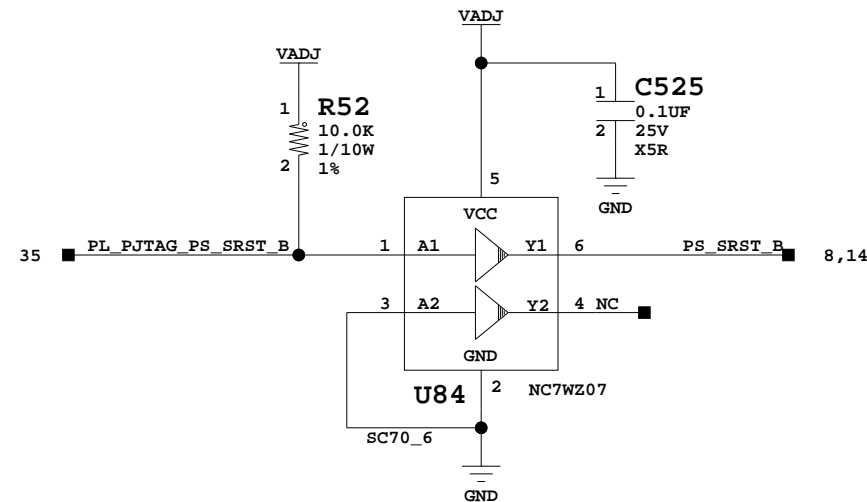
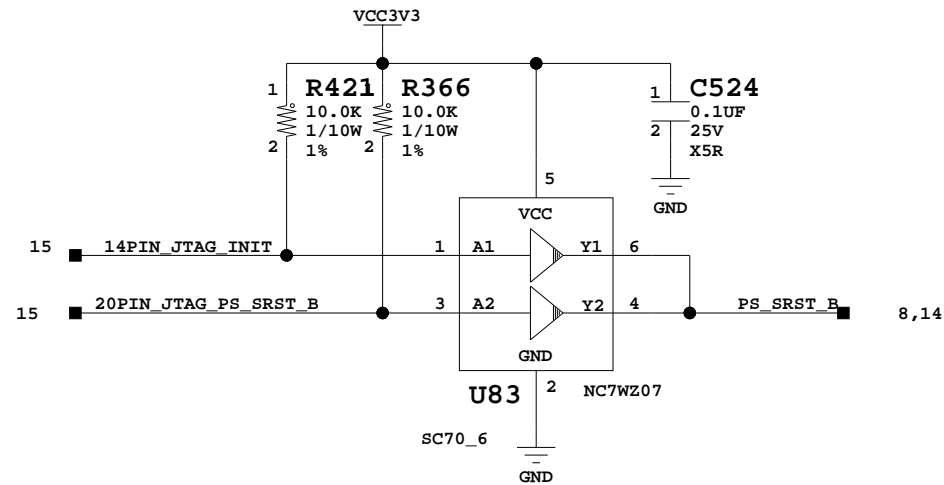
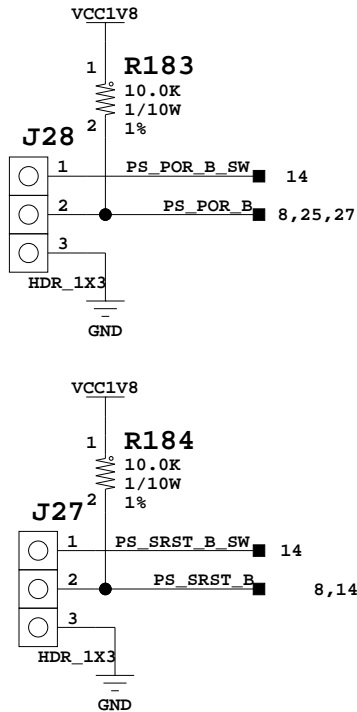
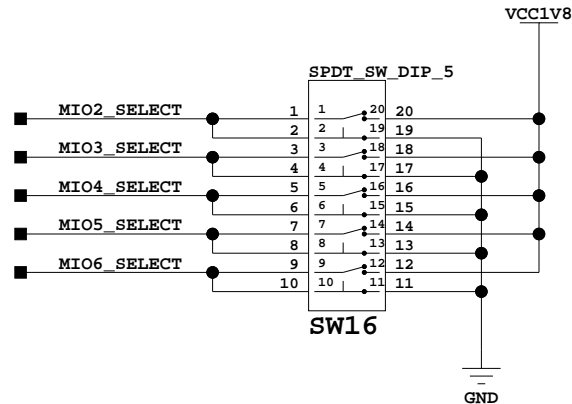
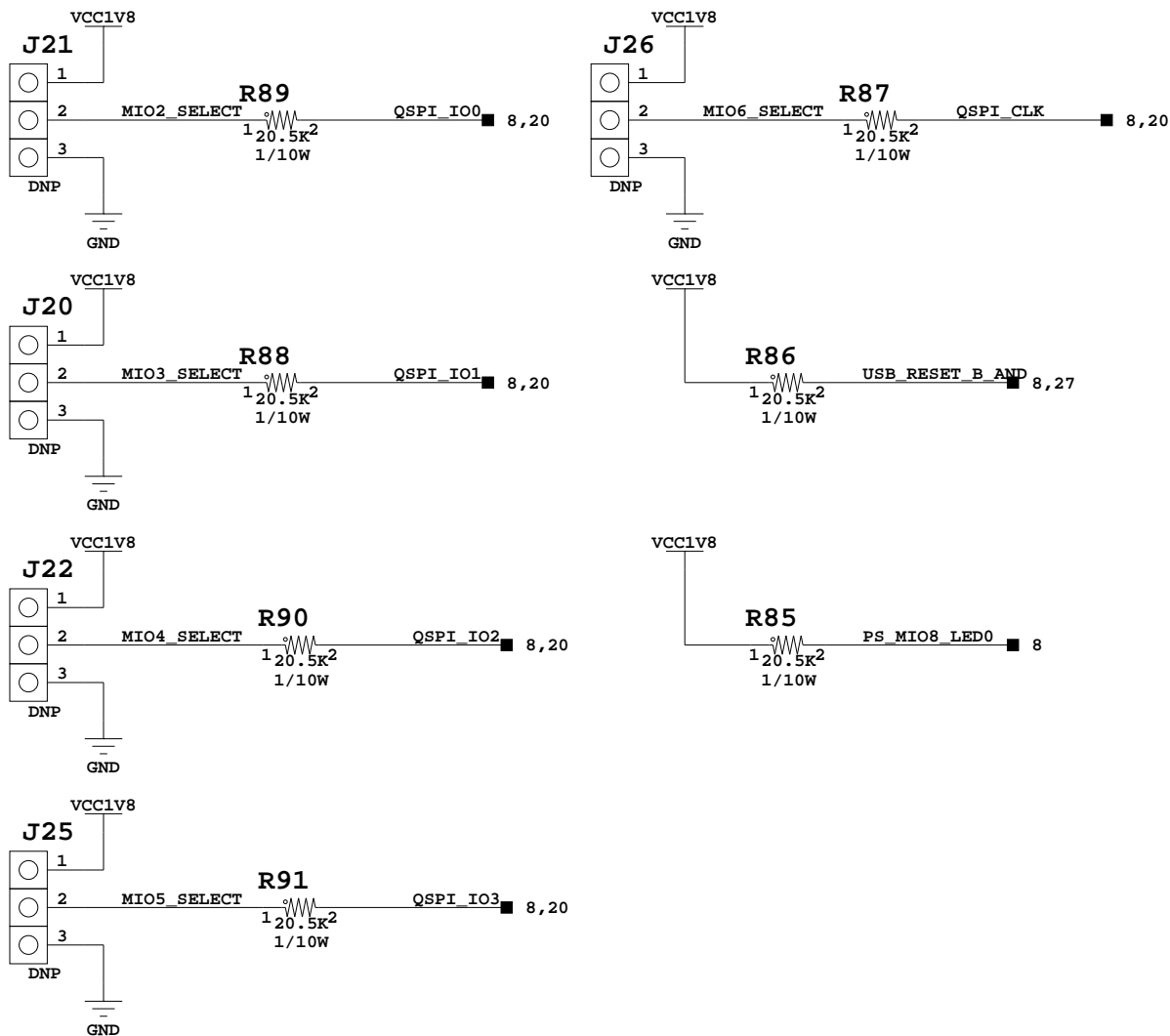


Zynq Bypass Capacitors

Title:		Zynq Bypass Capacitors SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
ASSY P/N:		0431696	
PCB P/N:		1280617	
SCH P/N:		0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
Sheet	13 of 48	Drawn By	BF

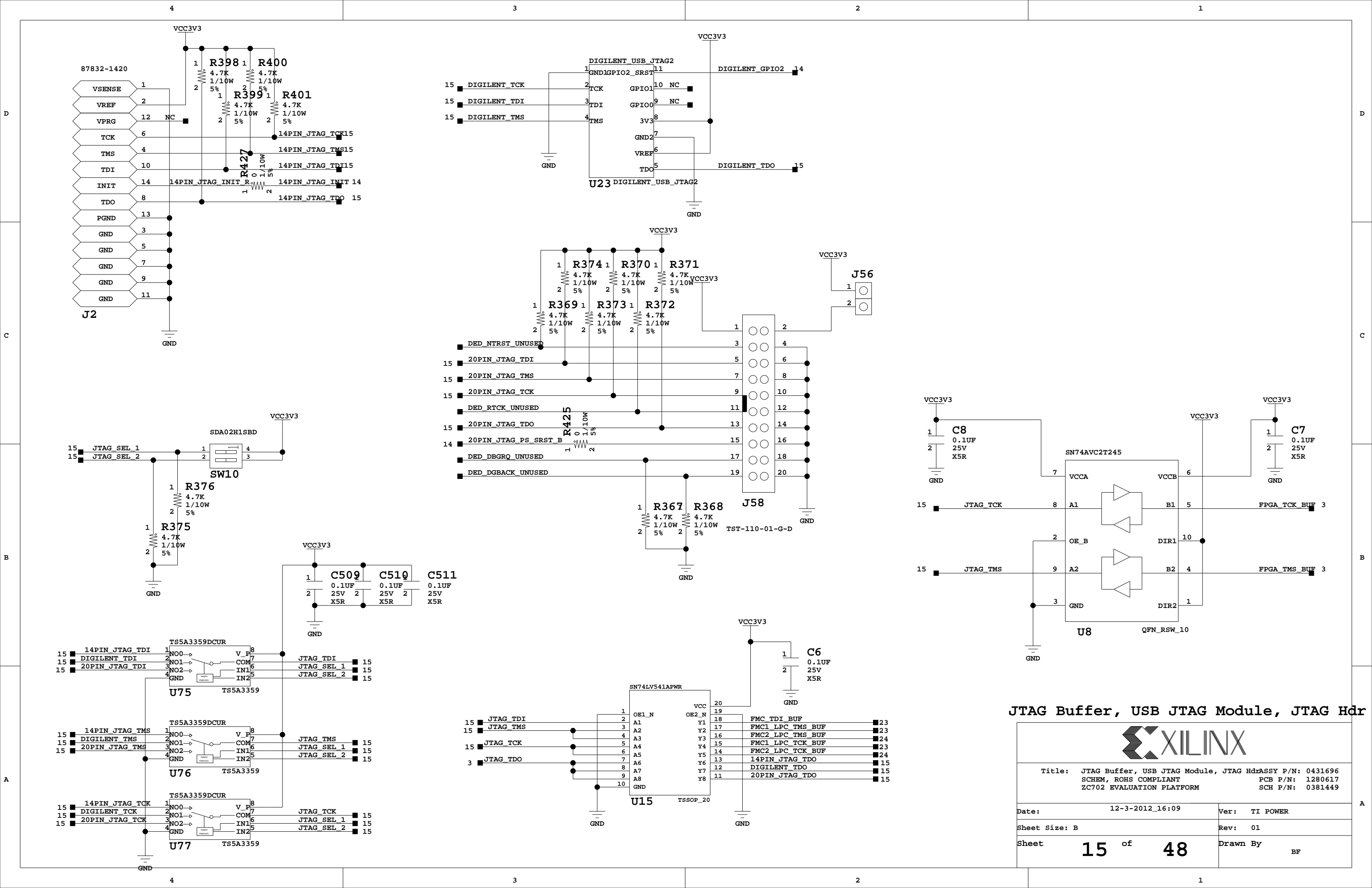


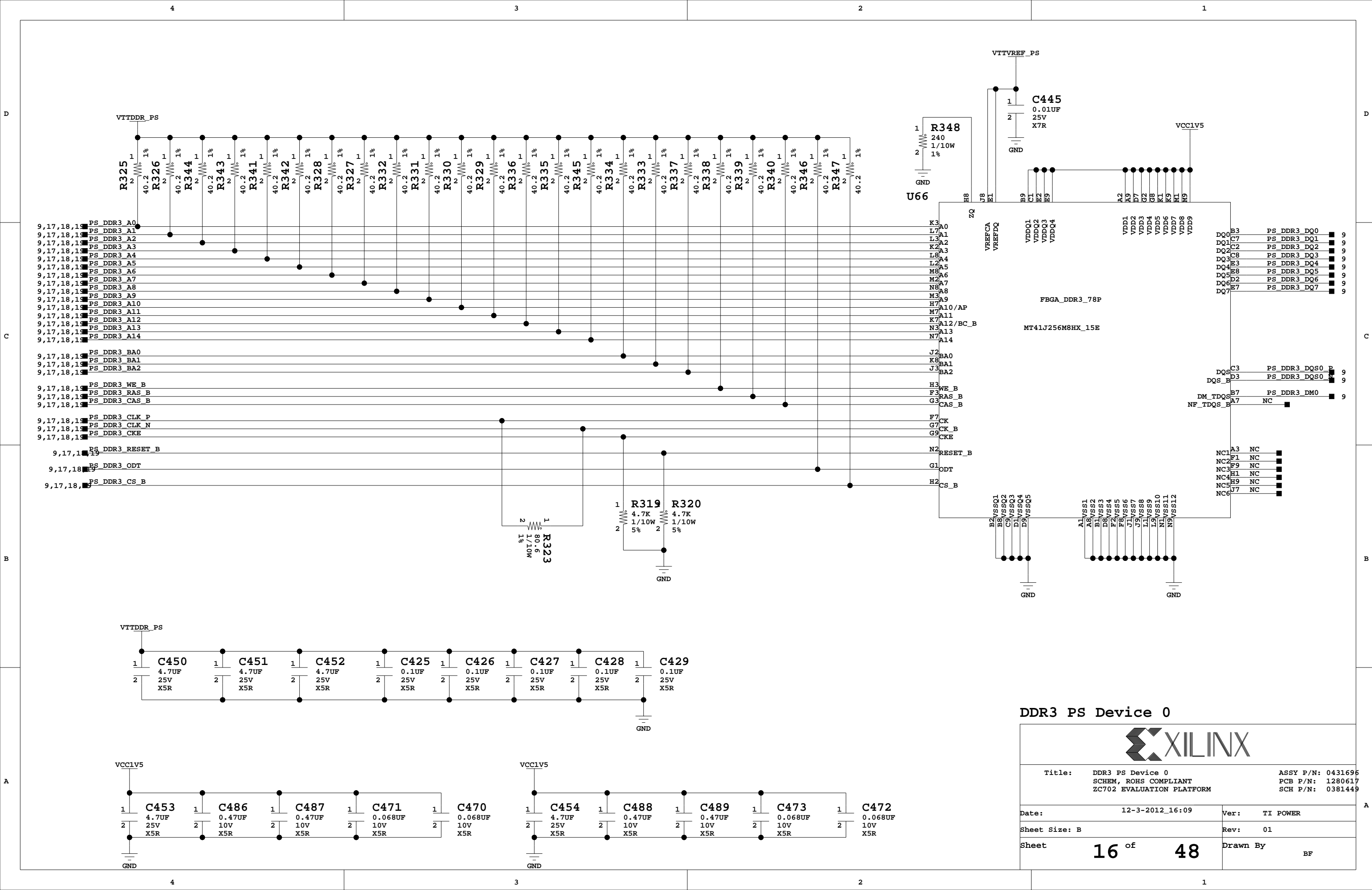
MIO[8:2] SELECTION HEADERS

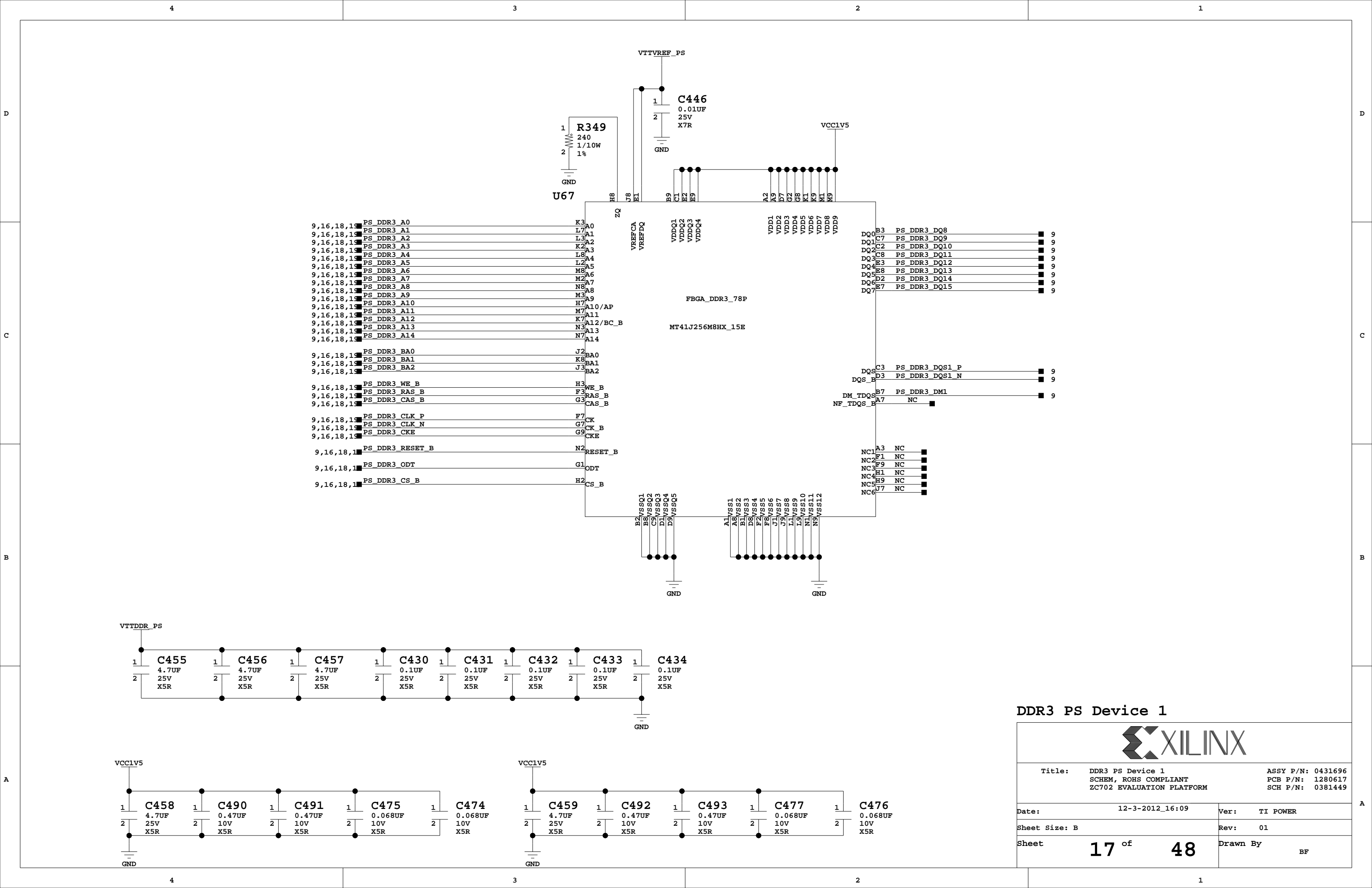


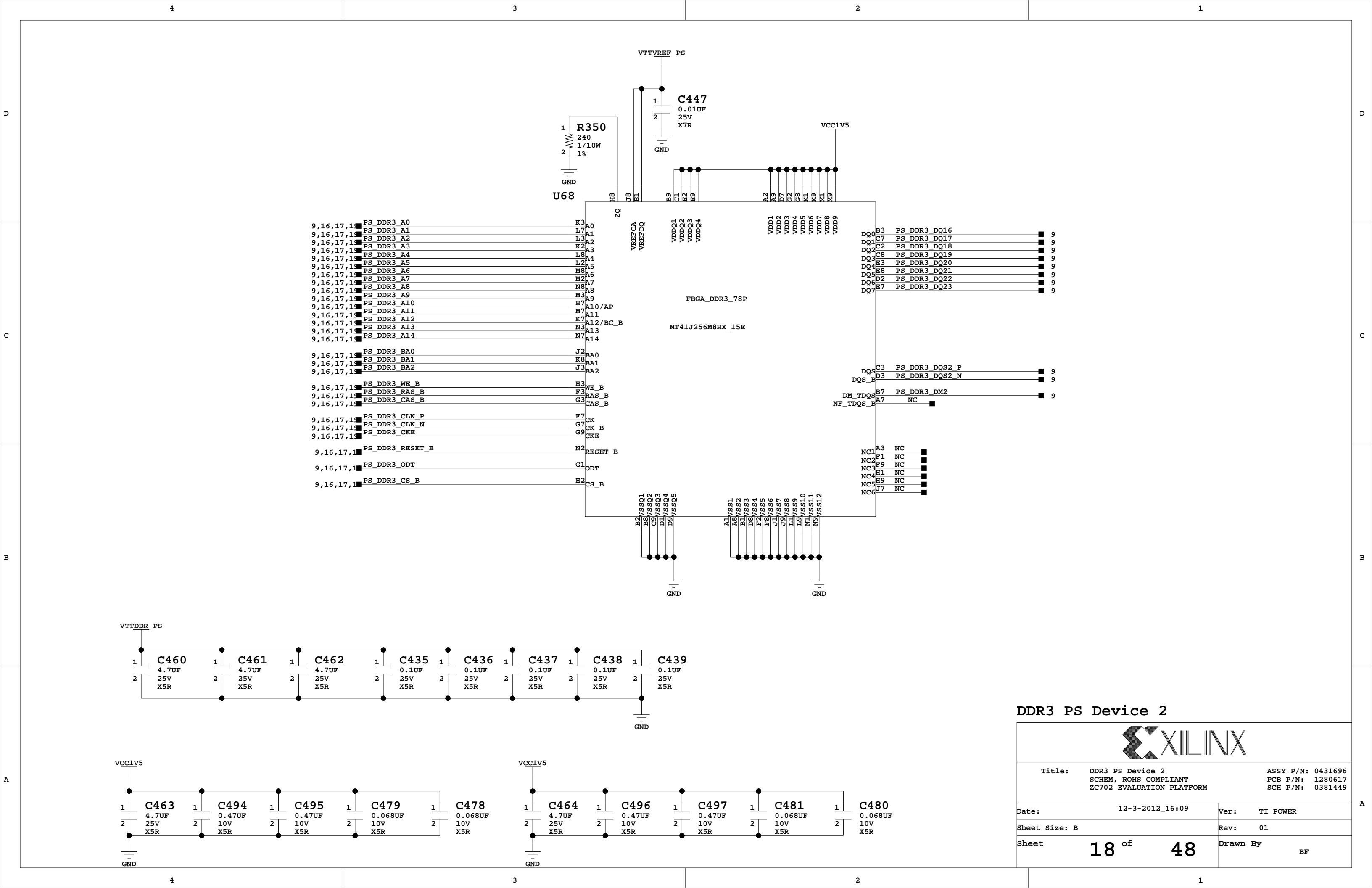
Power Supervisor, Zynq Config Pins, Reset

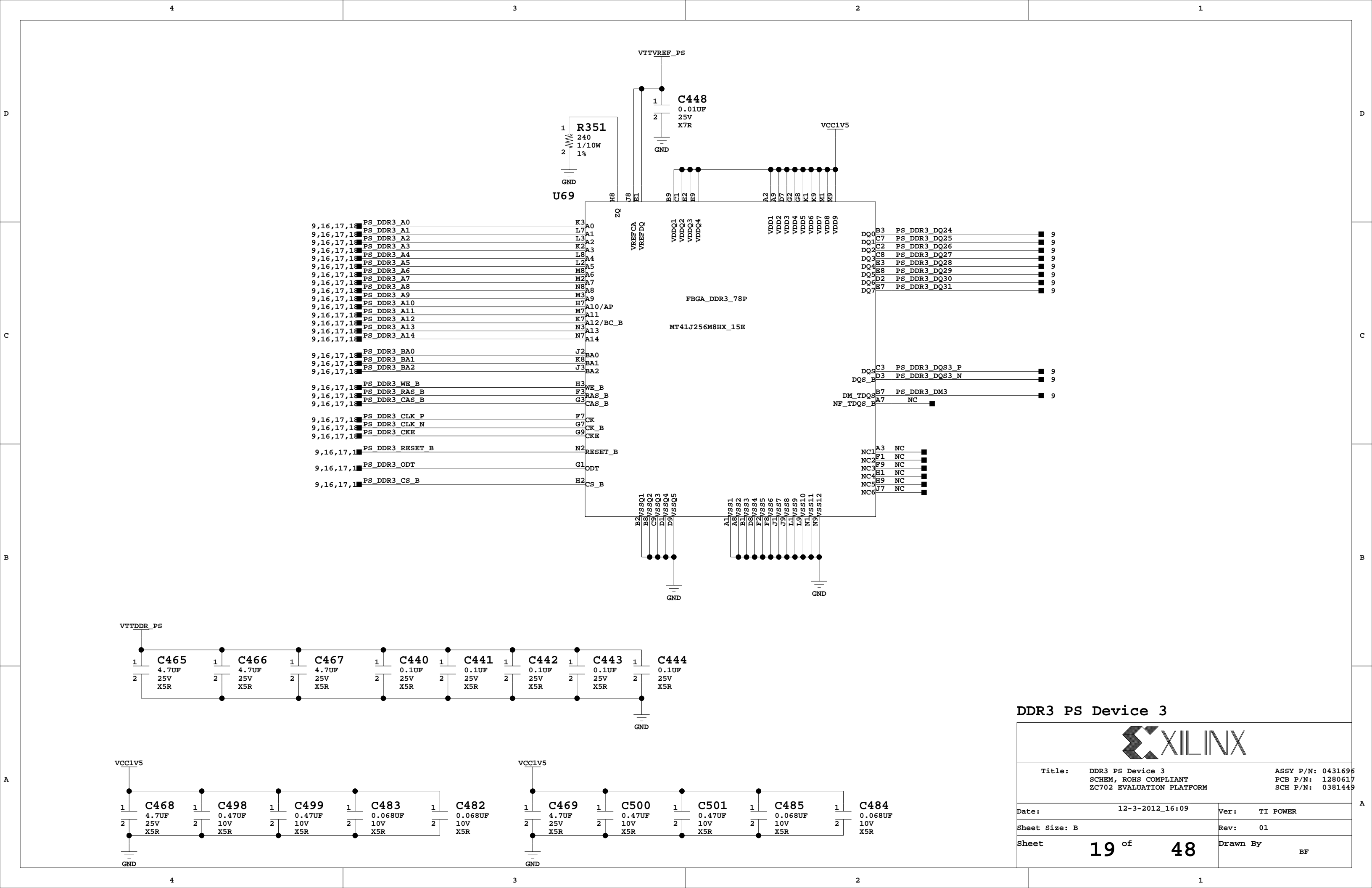
Title: Power Supervisor, Zynq Config Pins, ResetASSY P/N: 0431696 SCHEM, ROHS COMPLIANT PCB P/N: 1280617 ZC702 EVALUATION PLATFORM SCH P/N: 0381449			
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
Sheet	14 of 48	Drawn By	BF

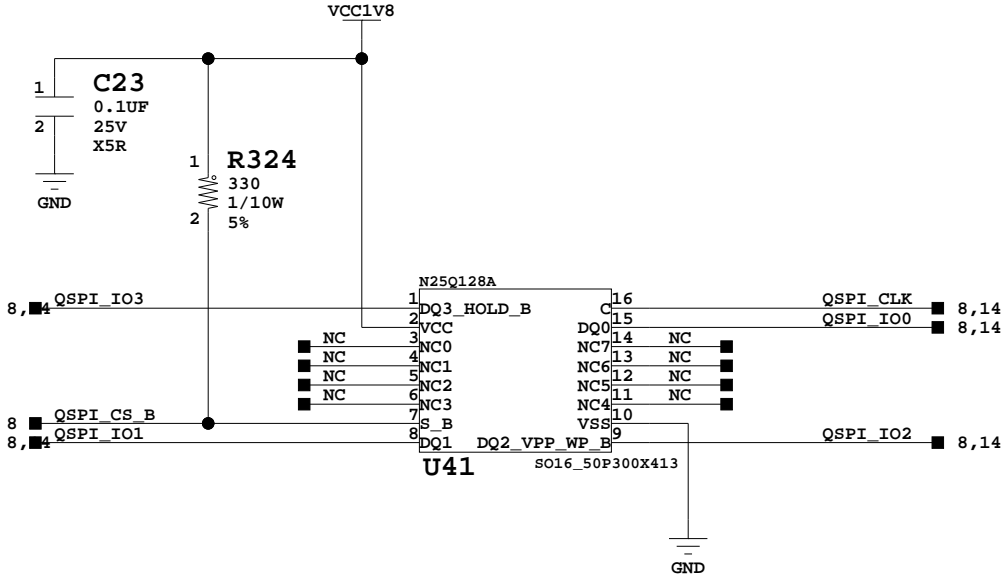












Quad SPI

Title:		Quad SPI SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
ASSY P/N:		0431696	
PCB P/N:		1280617	
SCH P/N:		0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
Sheet	20 of 48	Drawn By	BF

D

D

C

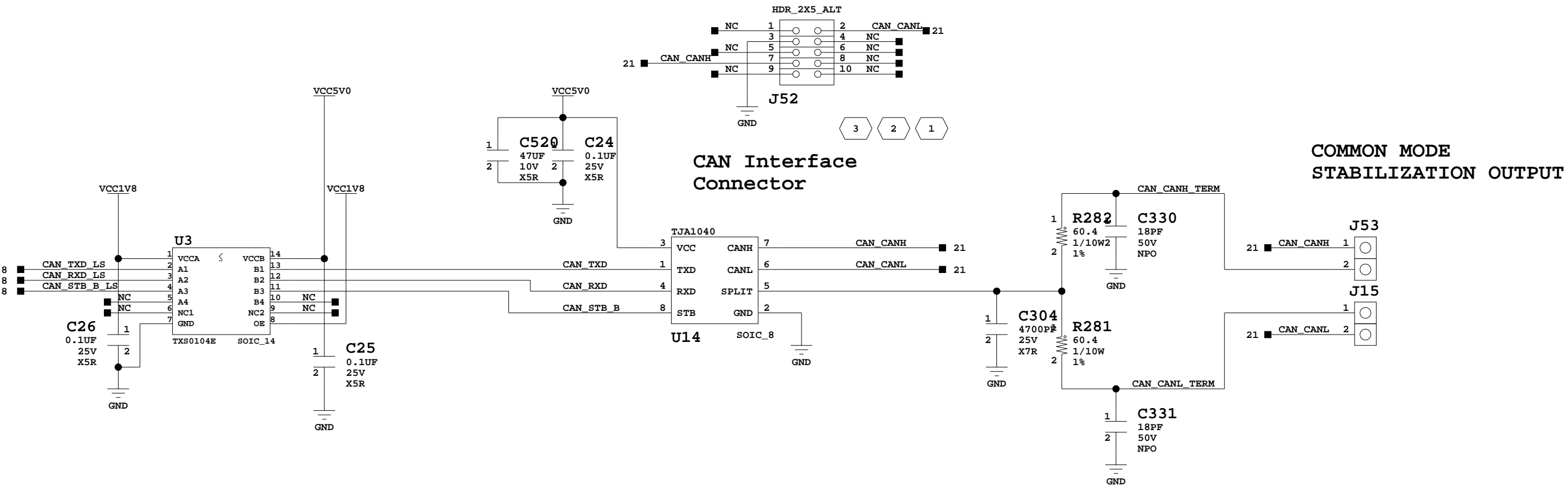
C

B

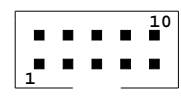
B

A

A



3 THE CONNECTOR PIN ORDER WITH RESPECT TO THE KEYWAY IS SHOWN HERE:



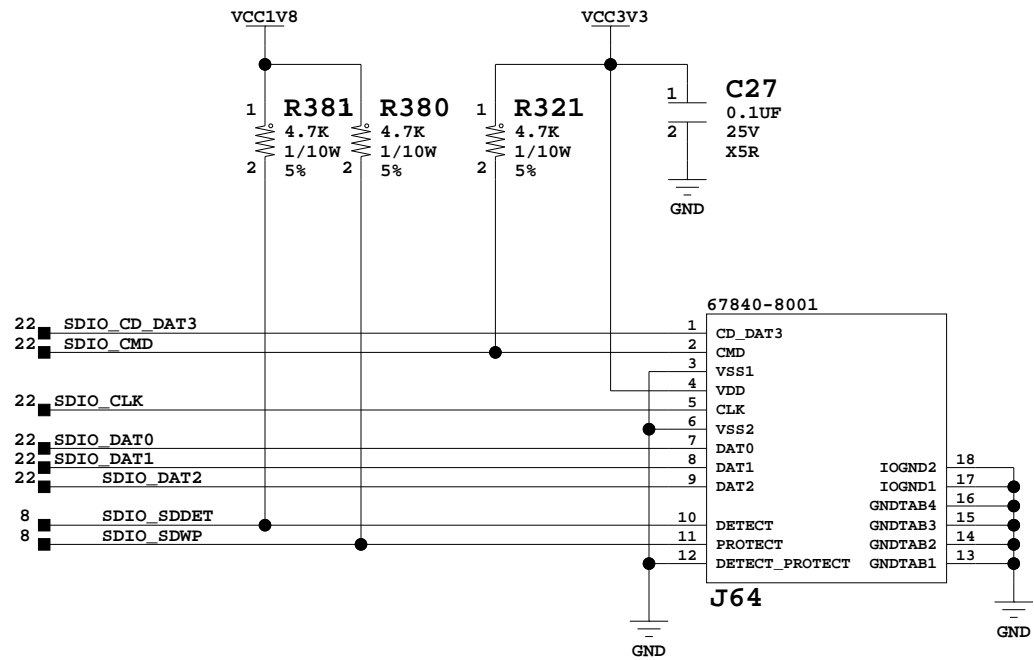
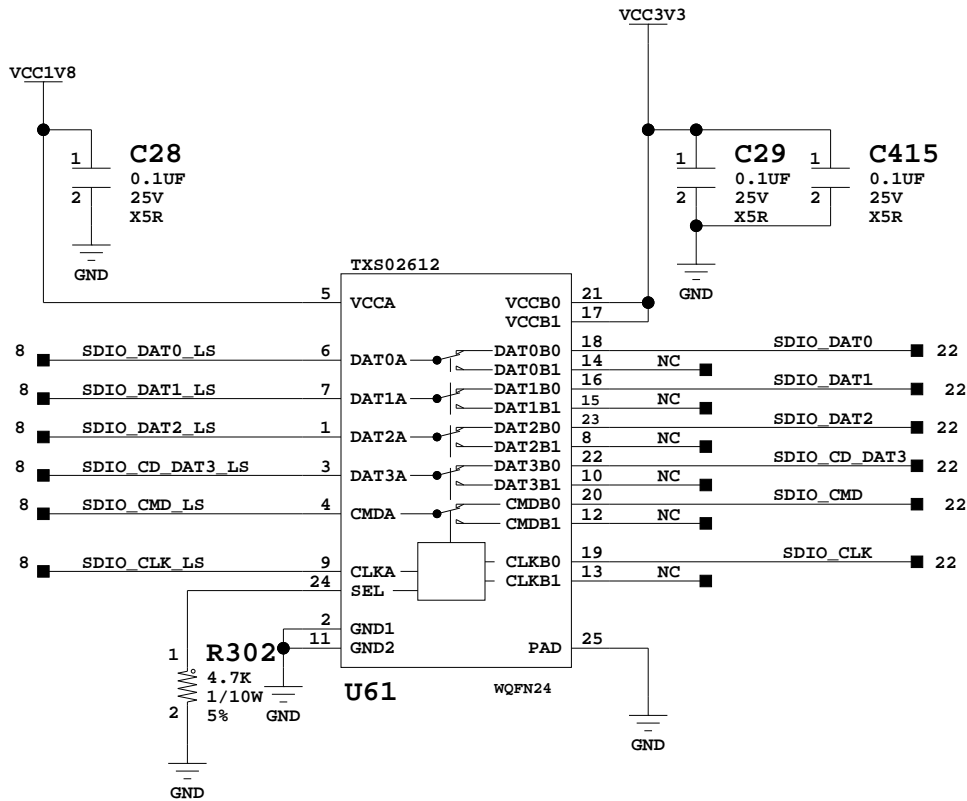
CONNECTOR (TOP VIEW)

2 CONNECTOR IS INTENDED TO MATE WITH PCCABLES.COM CABLE P/N 07120.

1 CO-LOCATE CAN INTERFACE CONNECTOR AND C/M STABALIZATION OUTPUT 2X1 HEADER

CAN Bus

Title: CAN Bus SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date: 12-3-2012_16:09	Ver: TI POWER		
Sheet Size: B		Rev: 01	
Sheet 21 of 48	Drawn By BF		



SD Card Connector



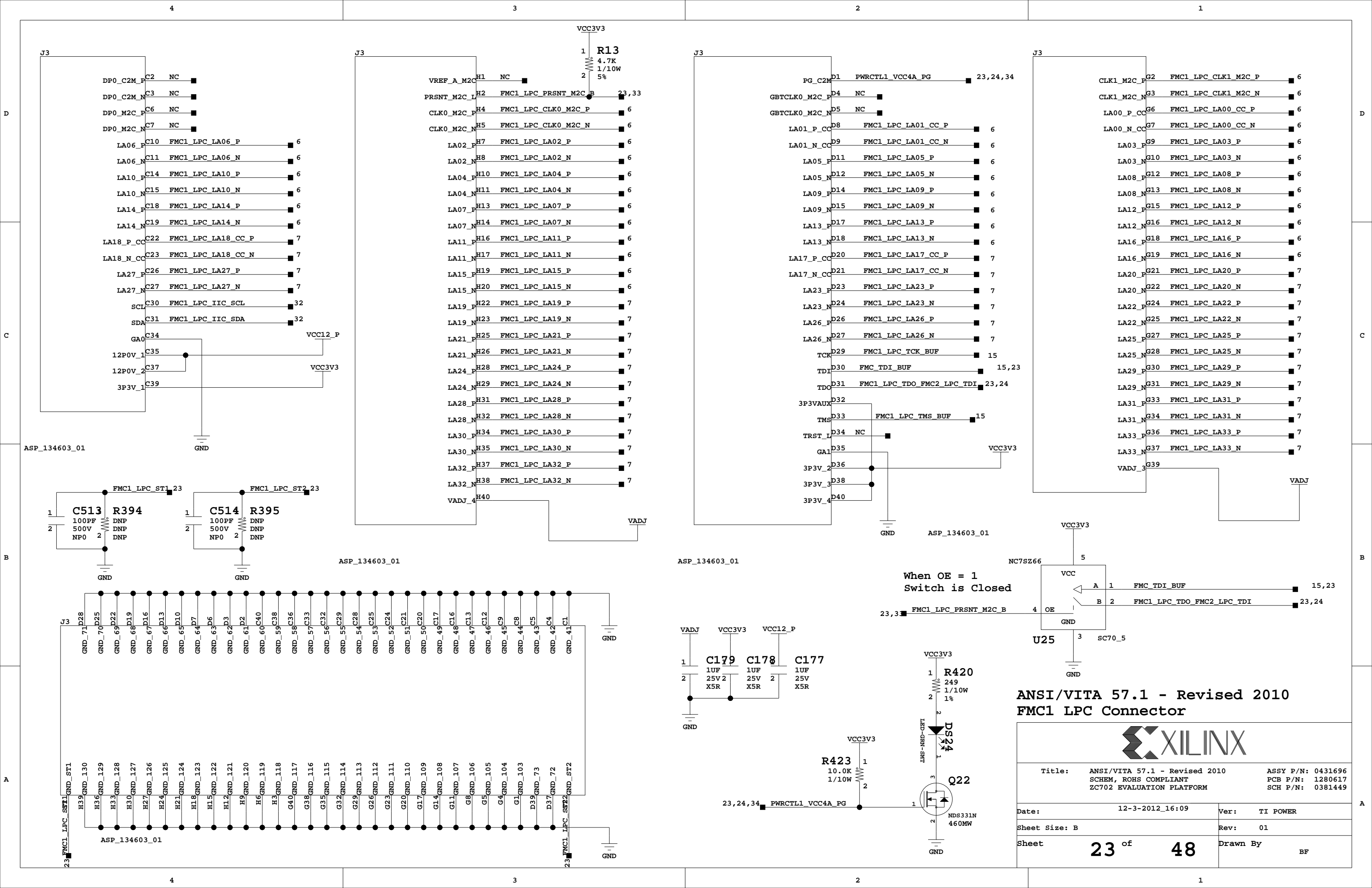
Title: SD Card Connector
SCHEM, ROHS COMPLIANT
ZC702 EVALUATION PLATFORM

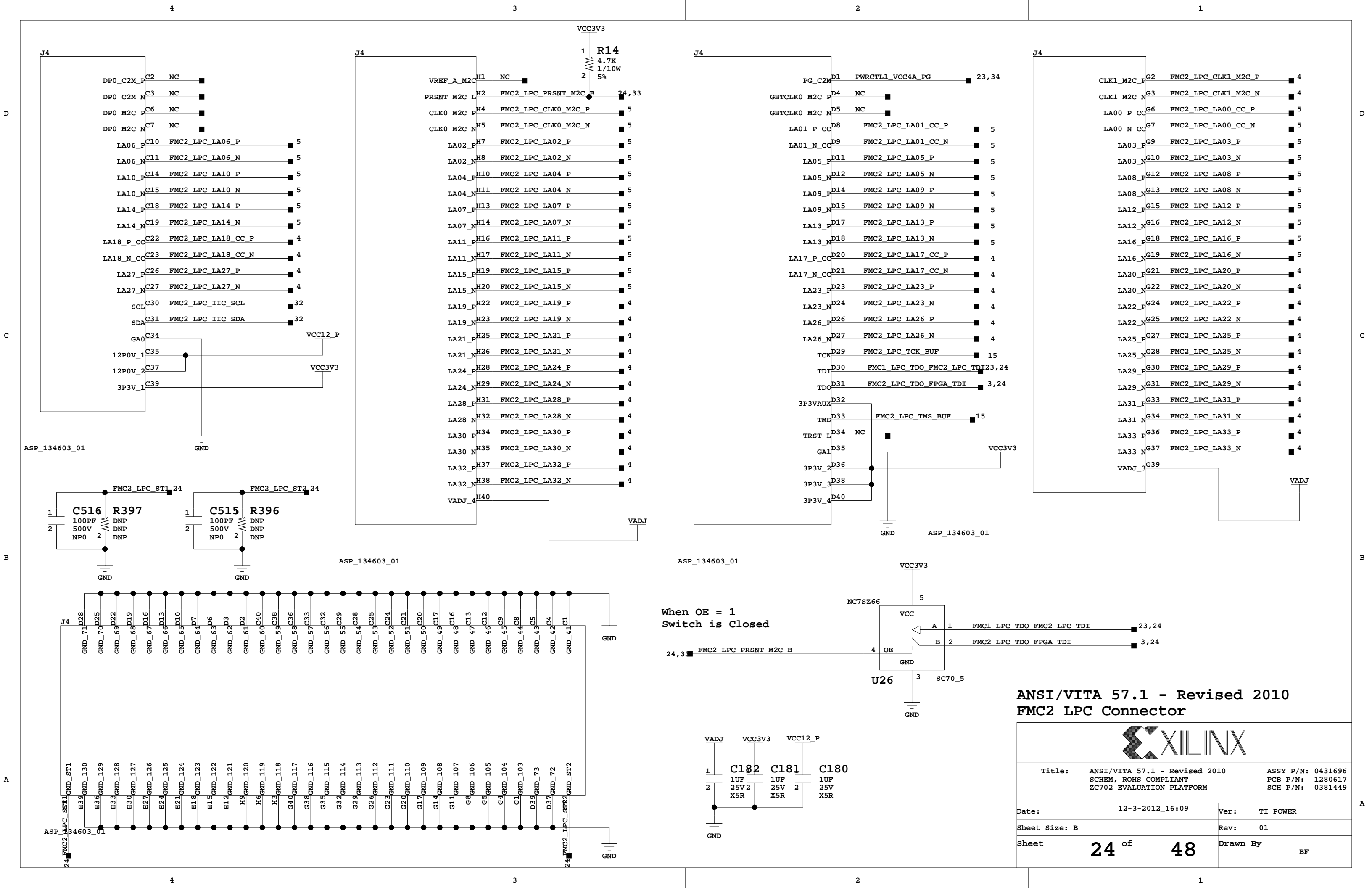
ASSY P/N: 0431696
PCB P/N: 1280617
SCH P/N: 0381449

Date: 12-3-2012_16:09 Ver: TI POWER

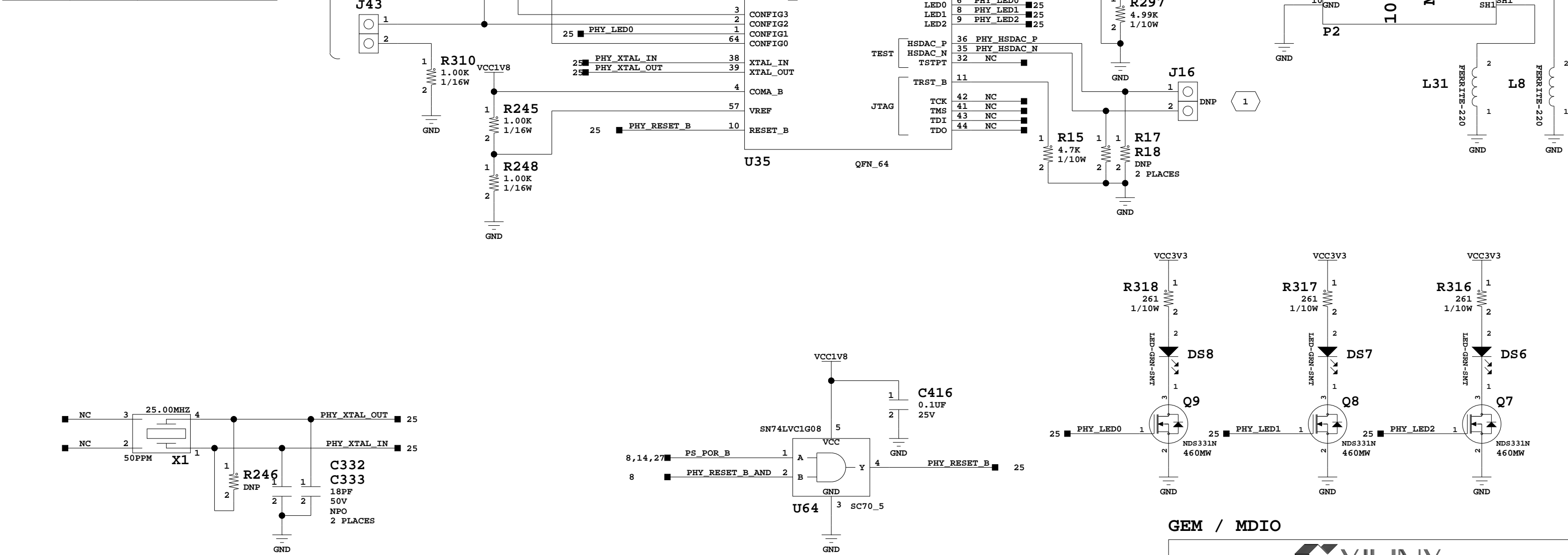
Sheet Size: B Rev: 01

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CONFIGURATION MAPPING			
PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1



2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

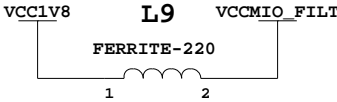
1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.

GEM / MDIO

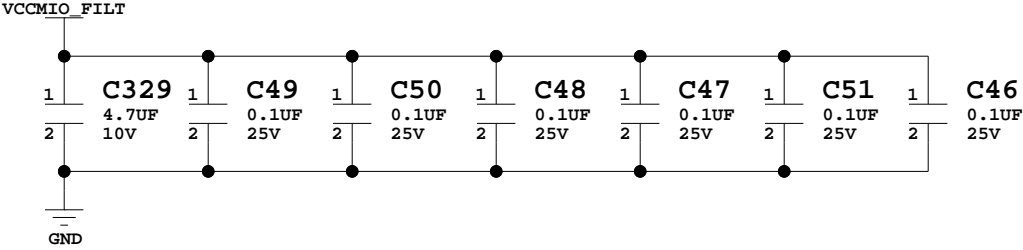


Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
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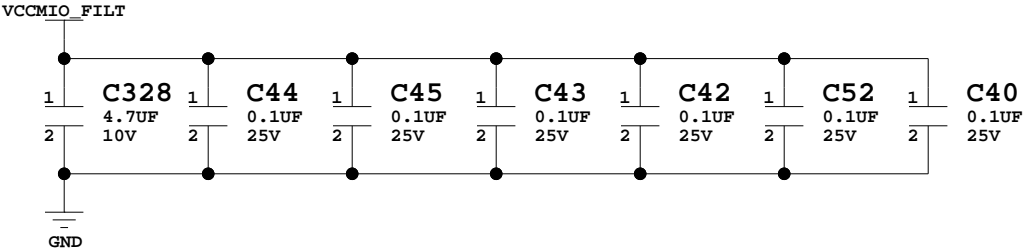
GEM / MDIO - POWER & DECOUPLING



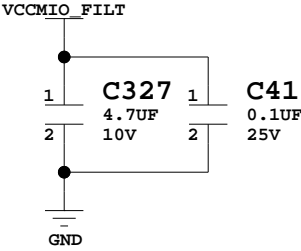
AVDDX, AVDDR, AVDDC



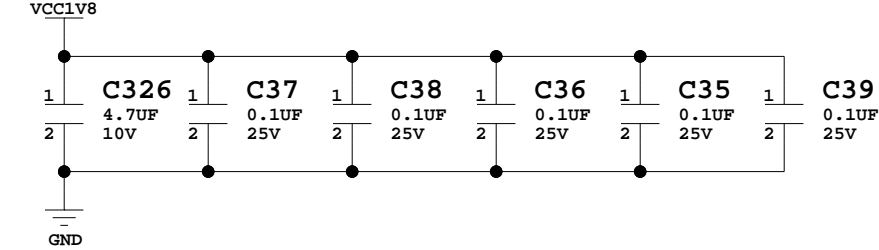
AVDD



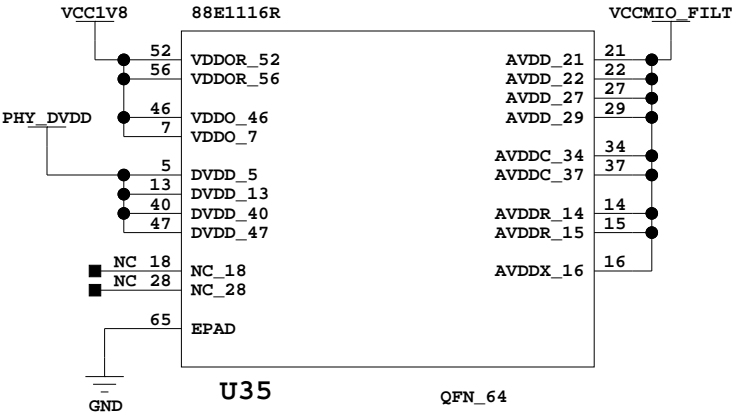
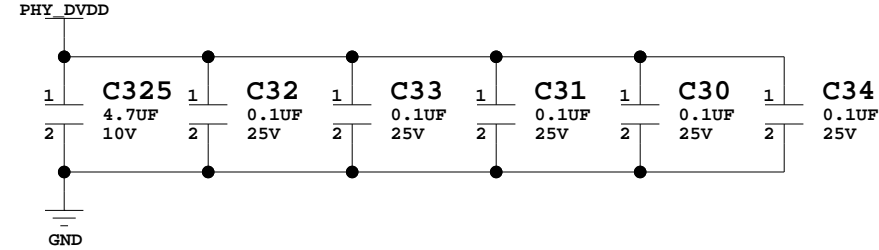
MAGNETICS / RJ45



VDDO, VDDOR



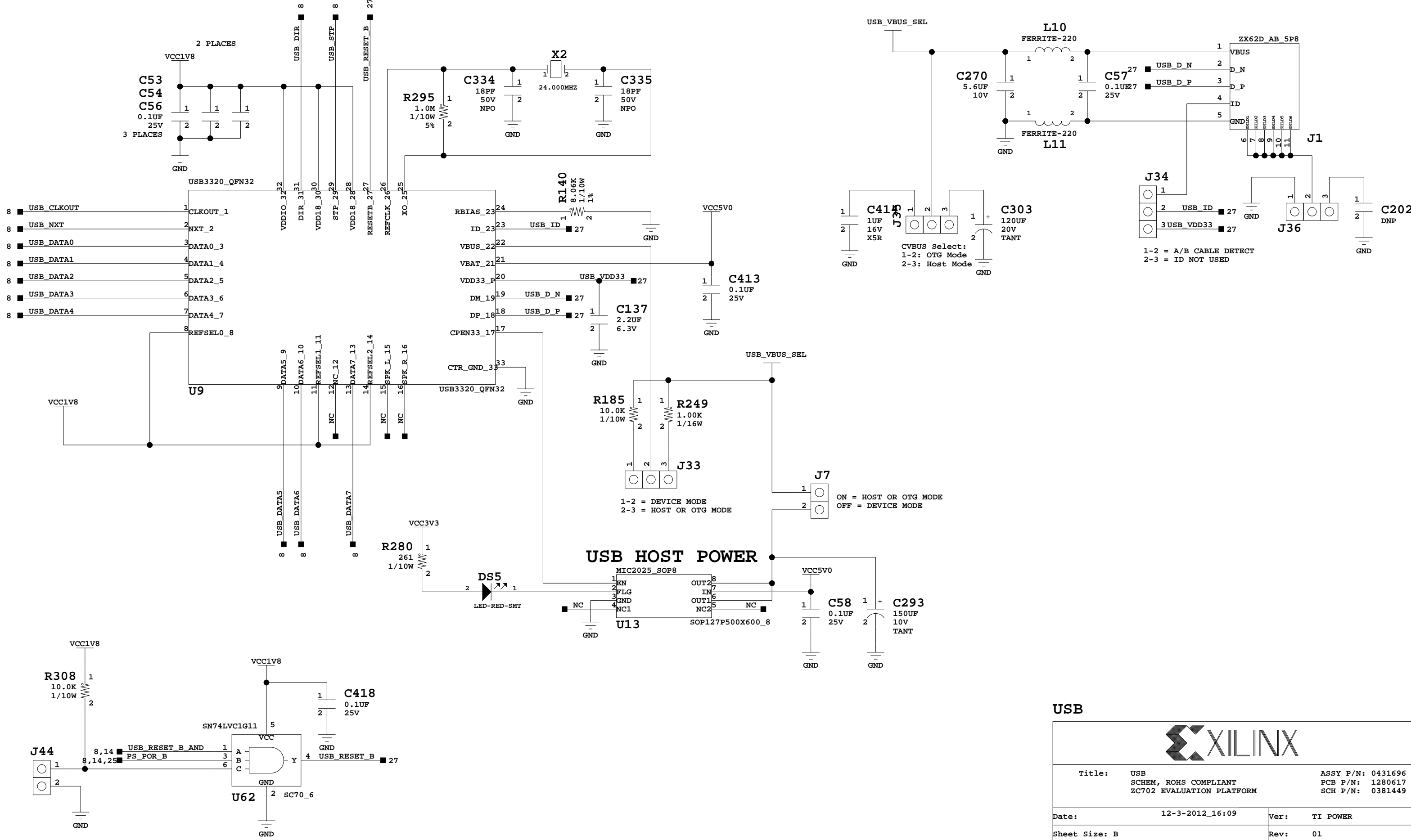
DVDD




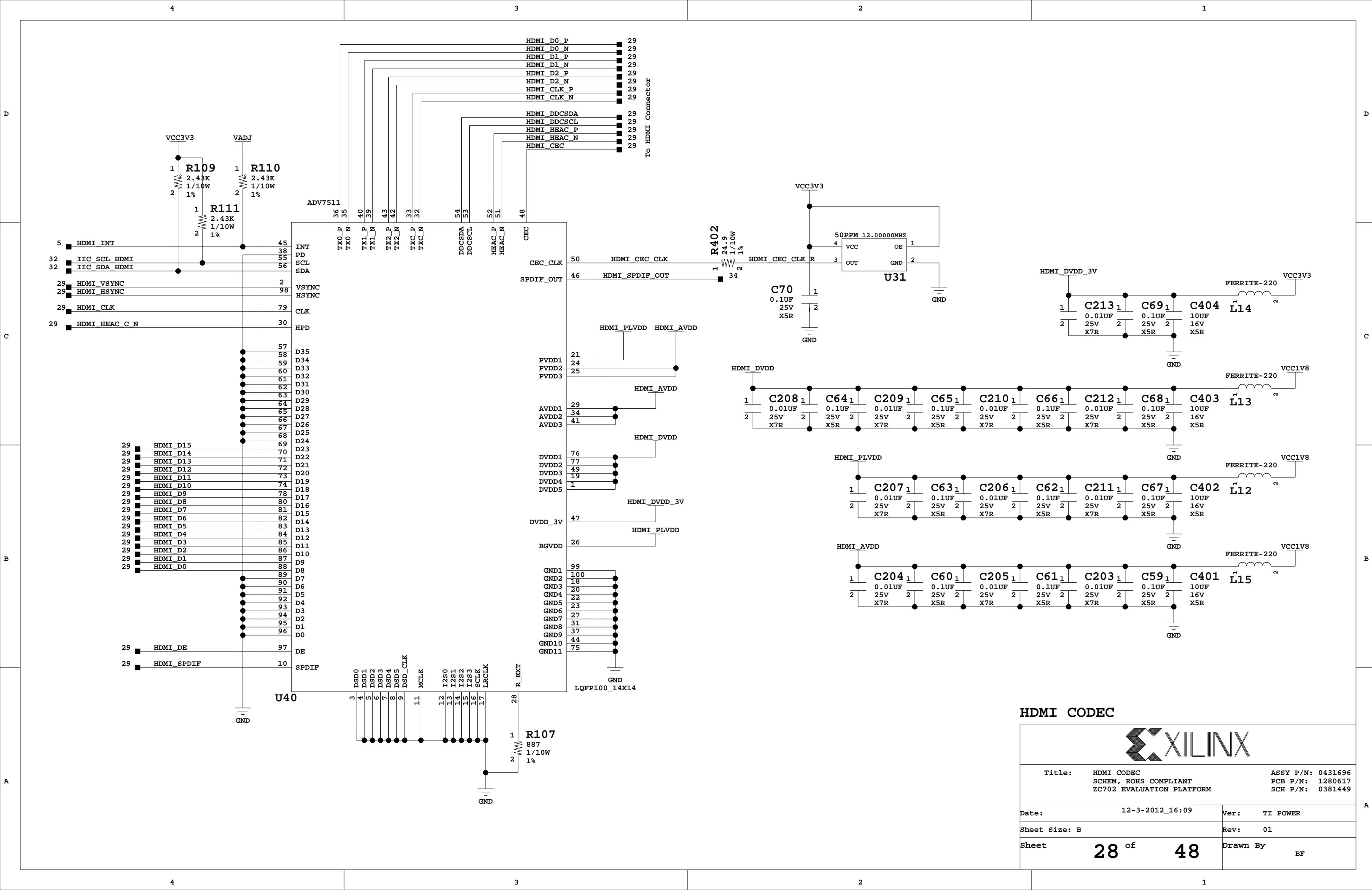
GEM / MDIO

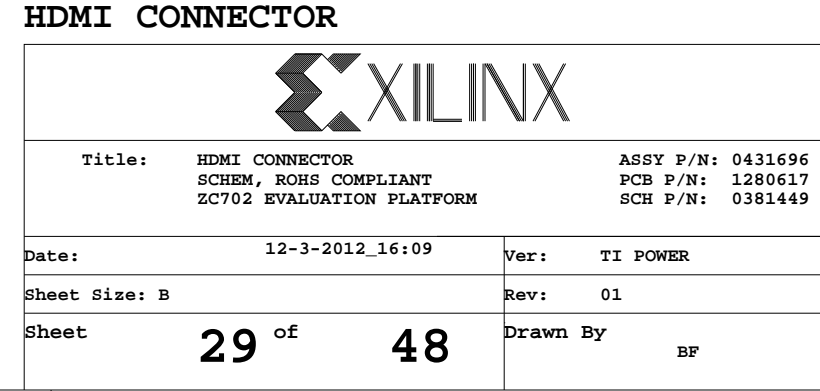
Title:		ASSY P/N: 0431696	
		PCB P/N: 1280617	
		SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
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USB 2.0 ULPI TRANSCEIVER AND CONNECTOR

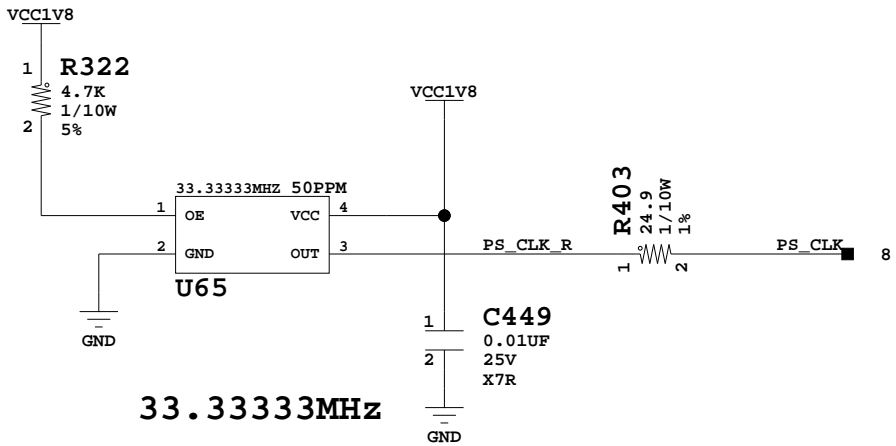
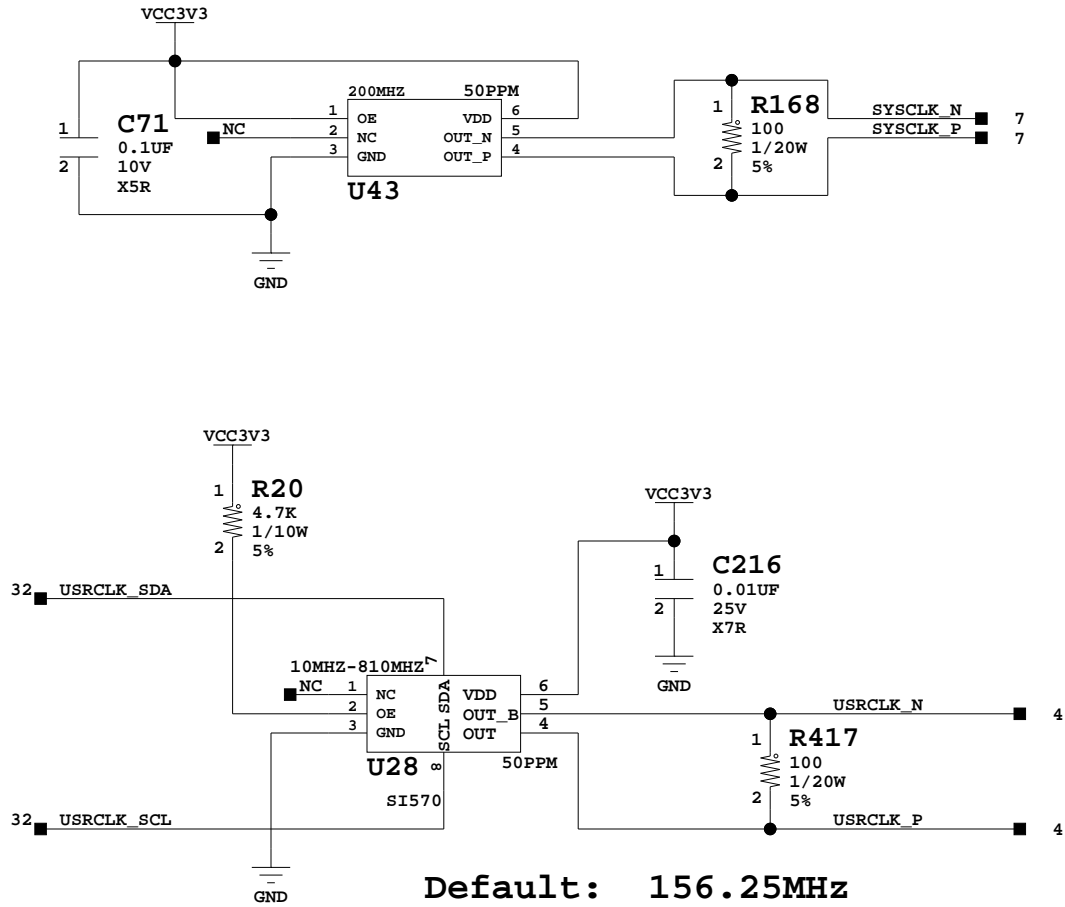


USB			
			
Title: USB SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date: 12-3-2012_16:09		Ver: TI POWER	
Sheet Size: B		Rev: 01	
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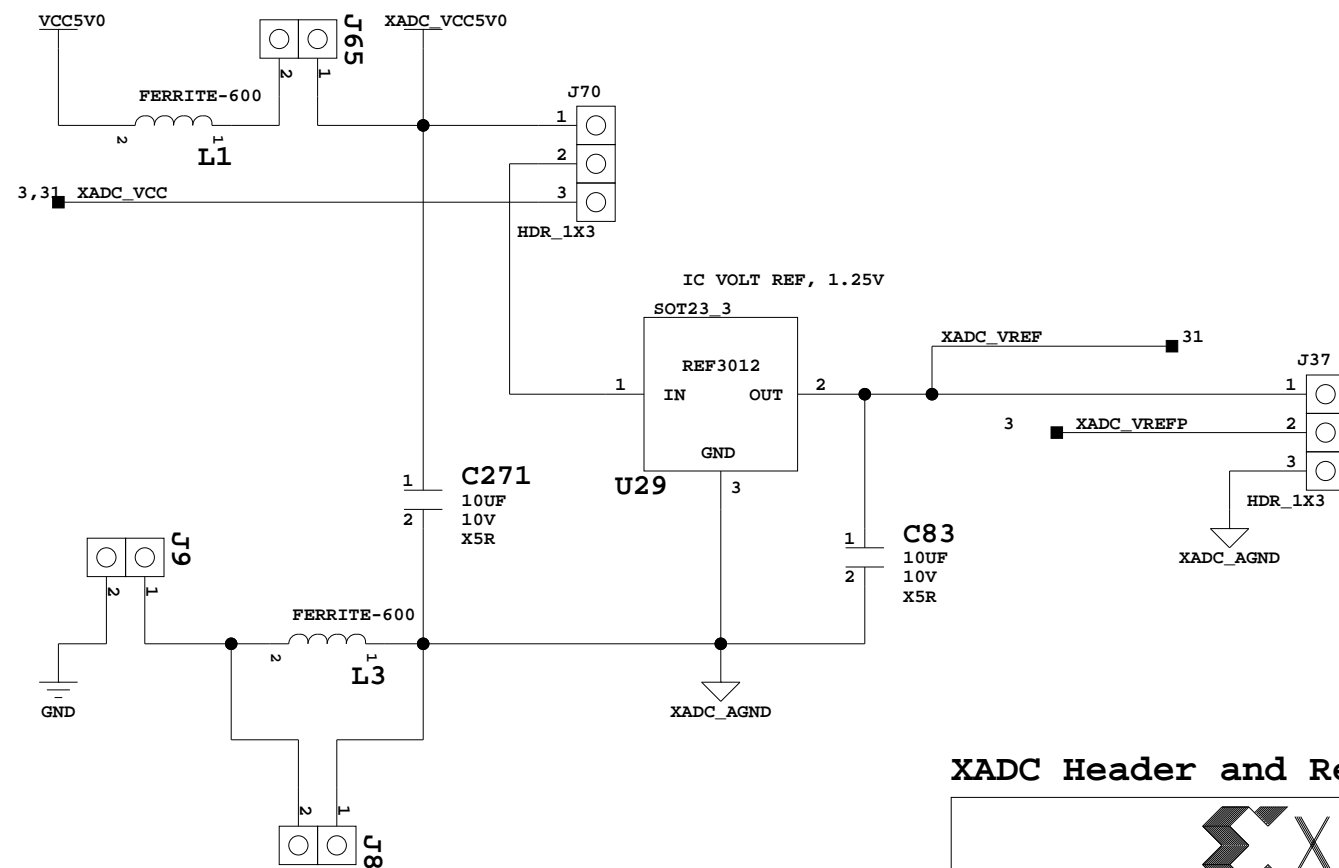
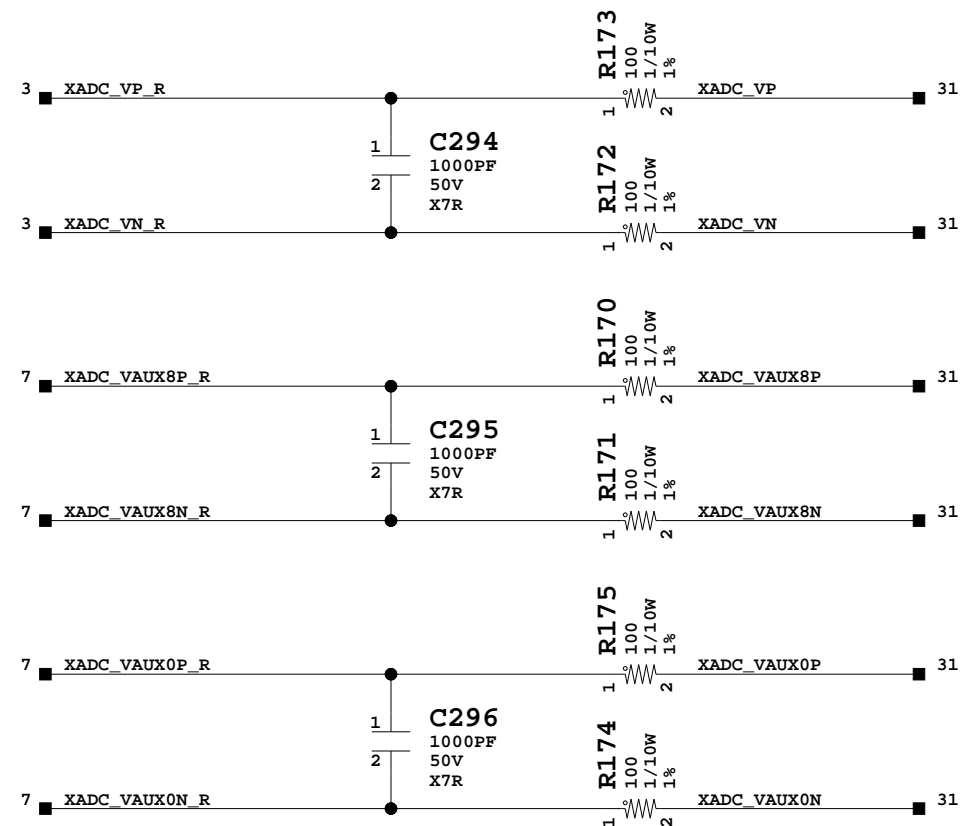
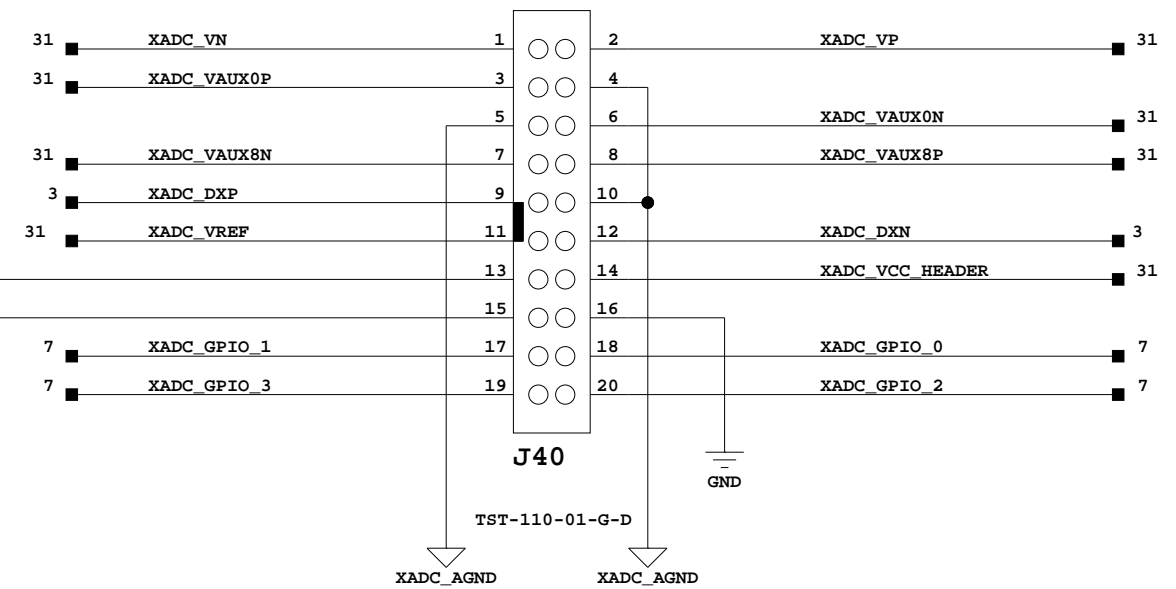
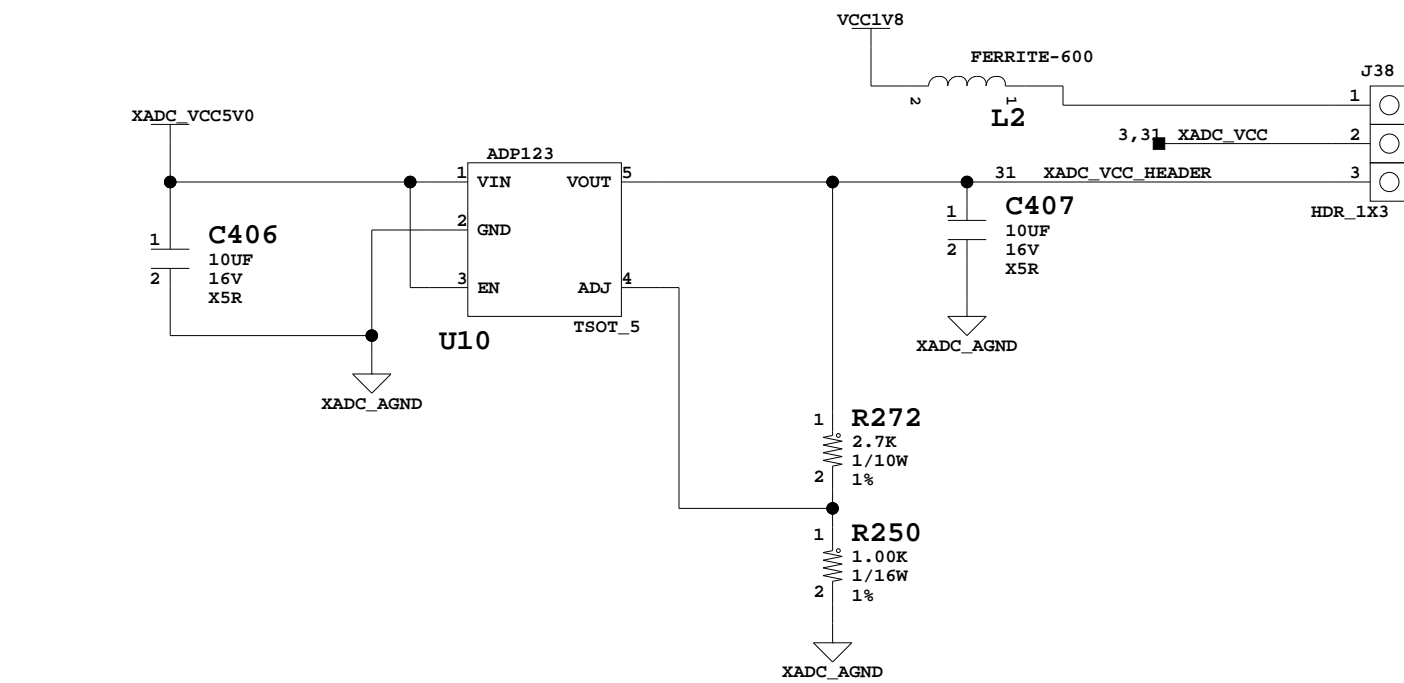


SIT9120AI-2D3-33E200.0000



Clocks

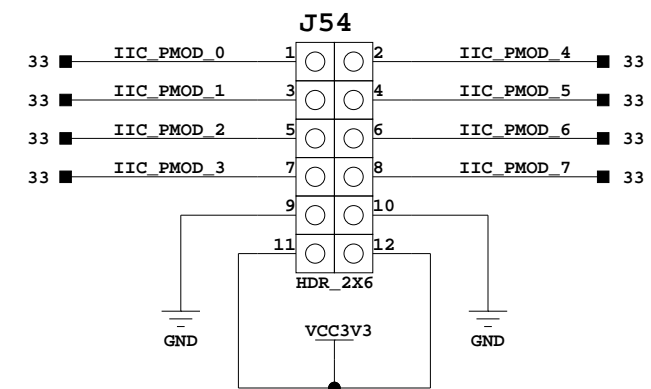
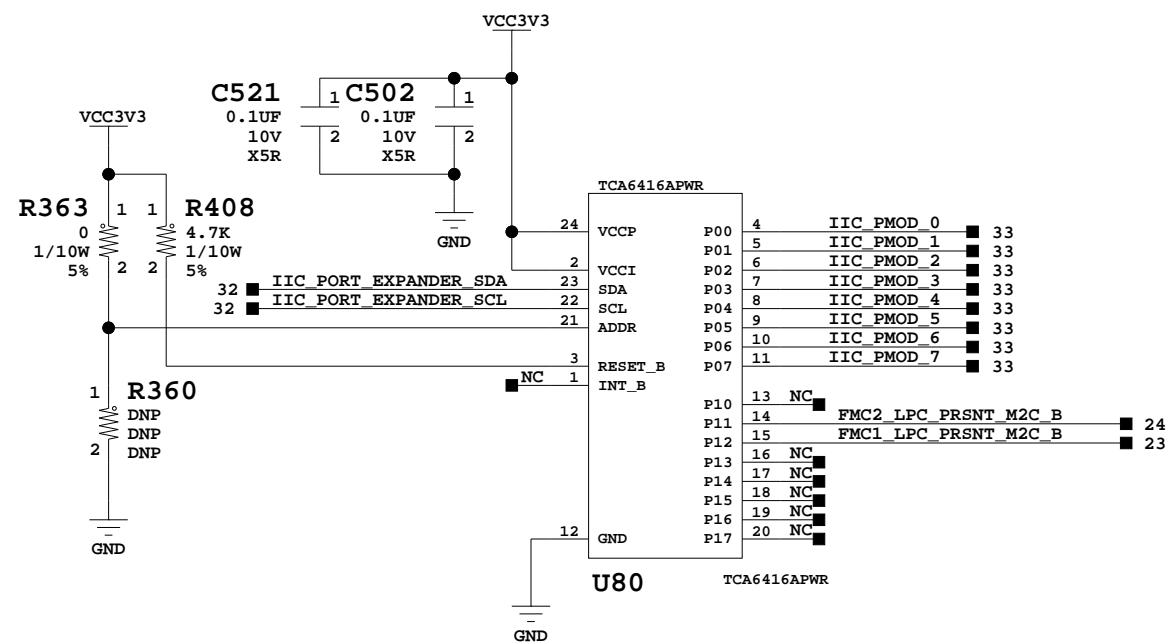
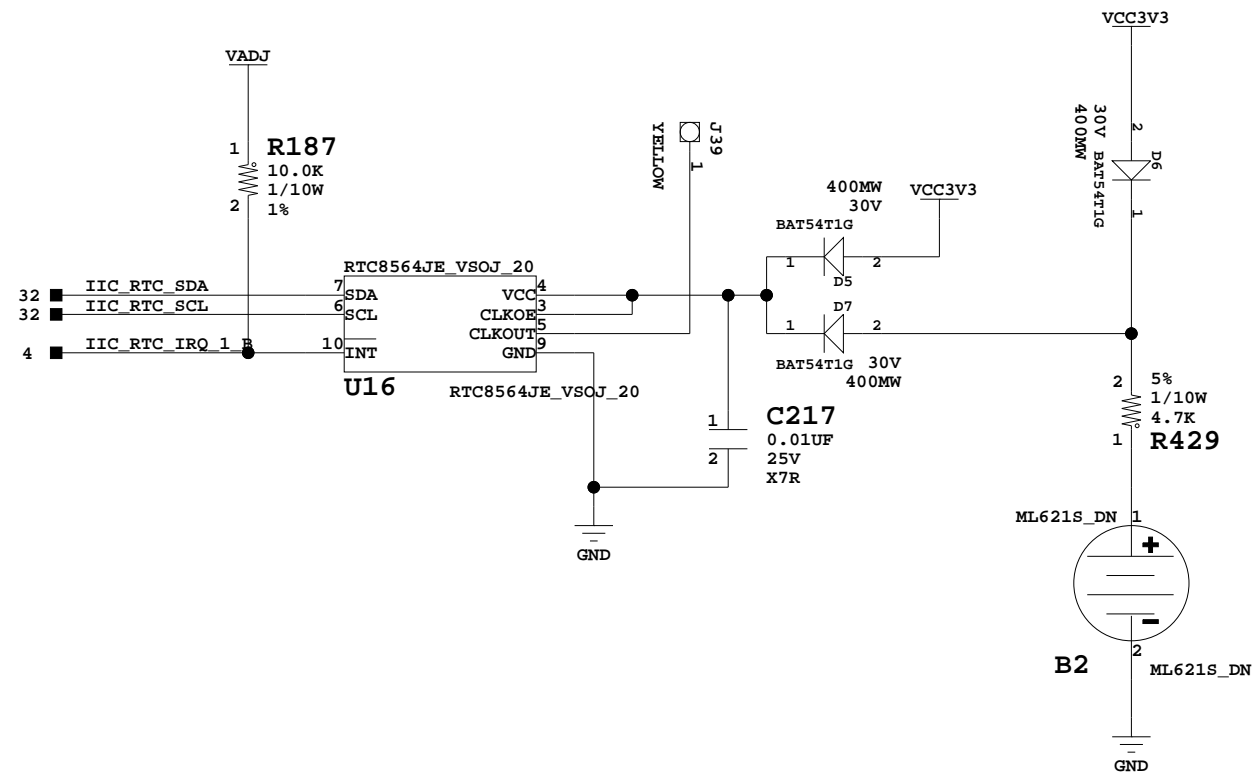
Title:		ASSY P/N: 0431696	
SCHEM, ROHS COMPLIANT		PCB P/N: 1280617	
ZC702 EVALUATION PLATFORM		SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
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XADC Header and Reference



Title: XADC Header and Reference SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date:	12-3-2012_16:09	Ver: TI POWER
Sheet Size: B		Rev: 01
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IIC Real Time Clock, Port Expander

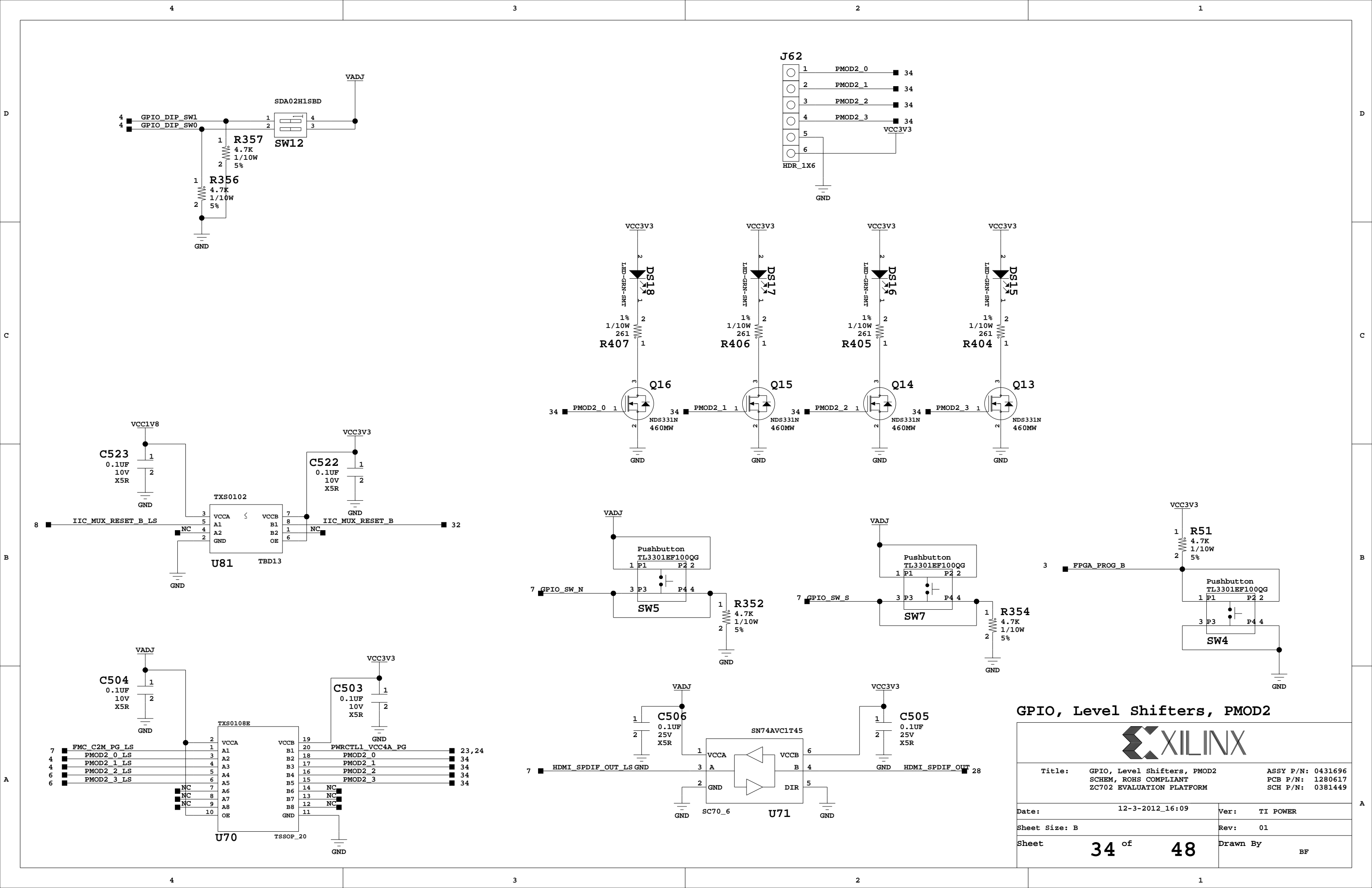


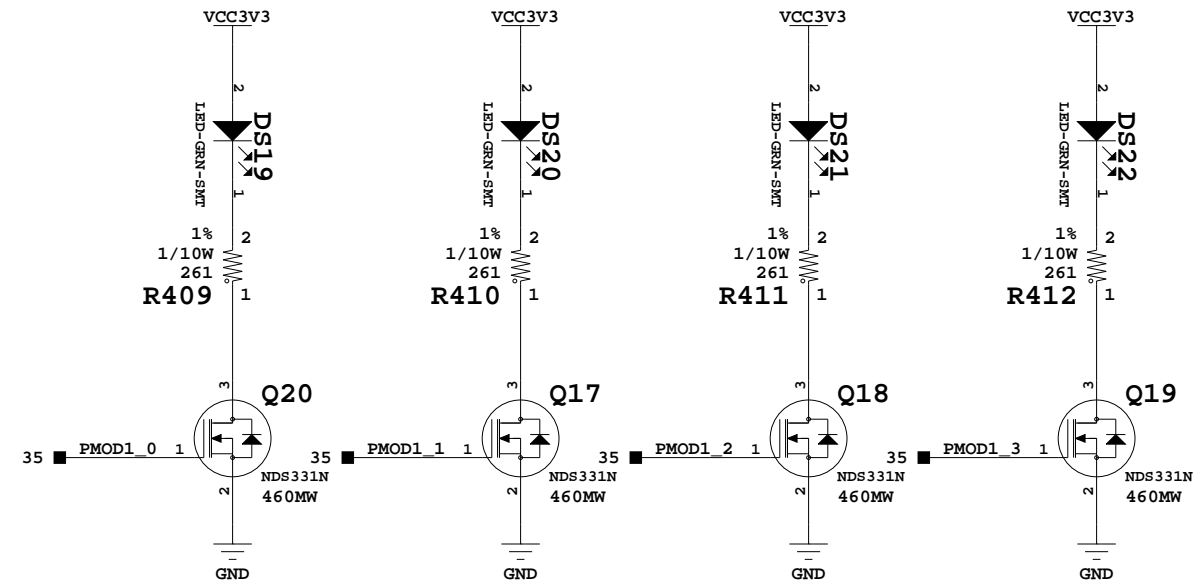
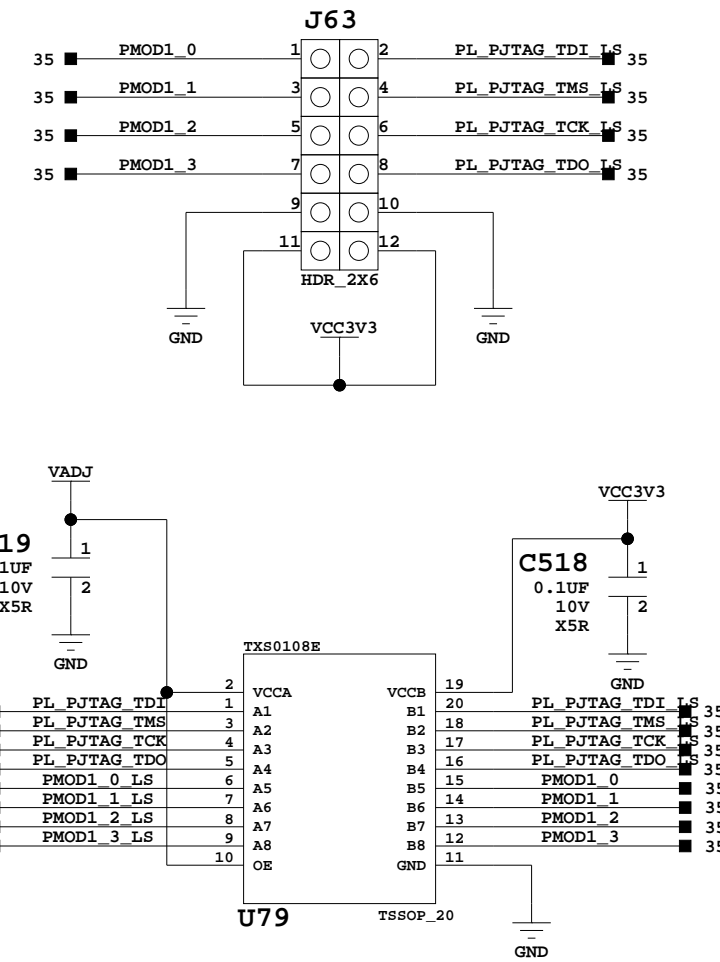
Title:	IIC Real Time Clock, Port Expander	ASSY P/N: 0431696
	SCHEM, ROHS COMPLIANT	PCB P/N: 1280617
	ZC702 EVALUATION PLATFORM	SCH P/N: 0381449

Date:	12-3-2012_16:09	Ver:	TI POWER
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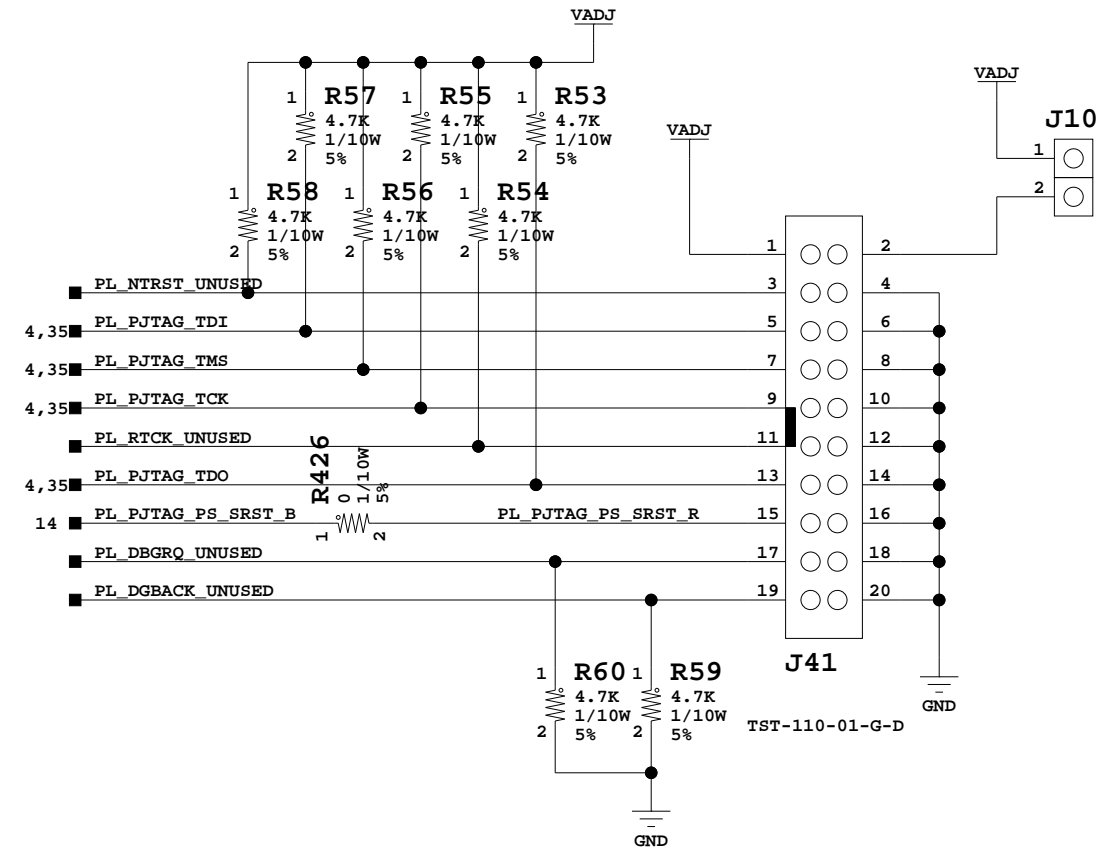
Sheet Size: B	Rev: 01
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Sheet	33	of	48	Drawn By	BF
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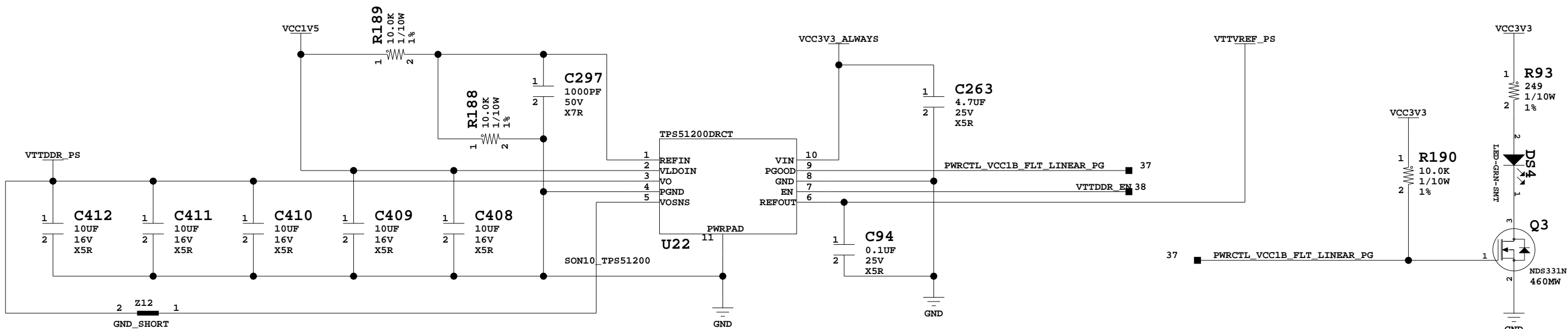
ARM PJTAG Header



ARM PJTAG Header, PMOD1



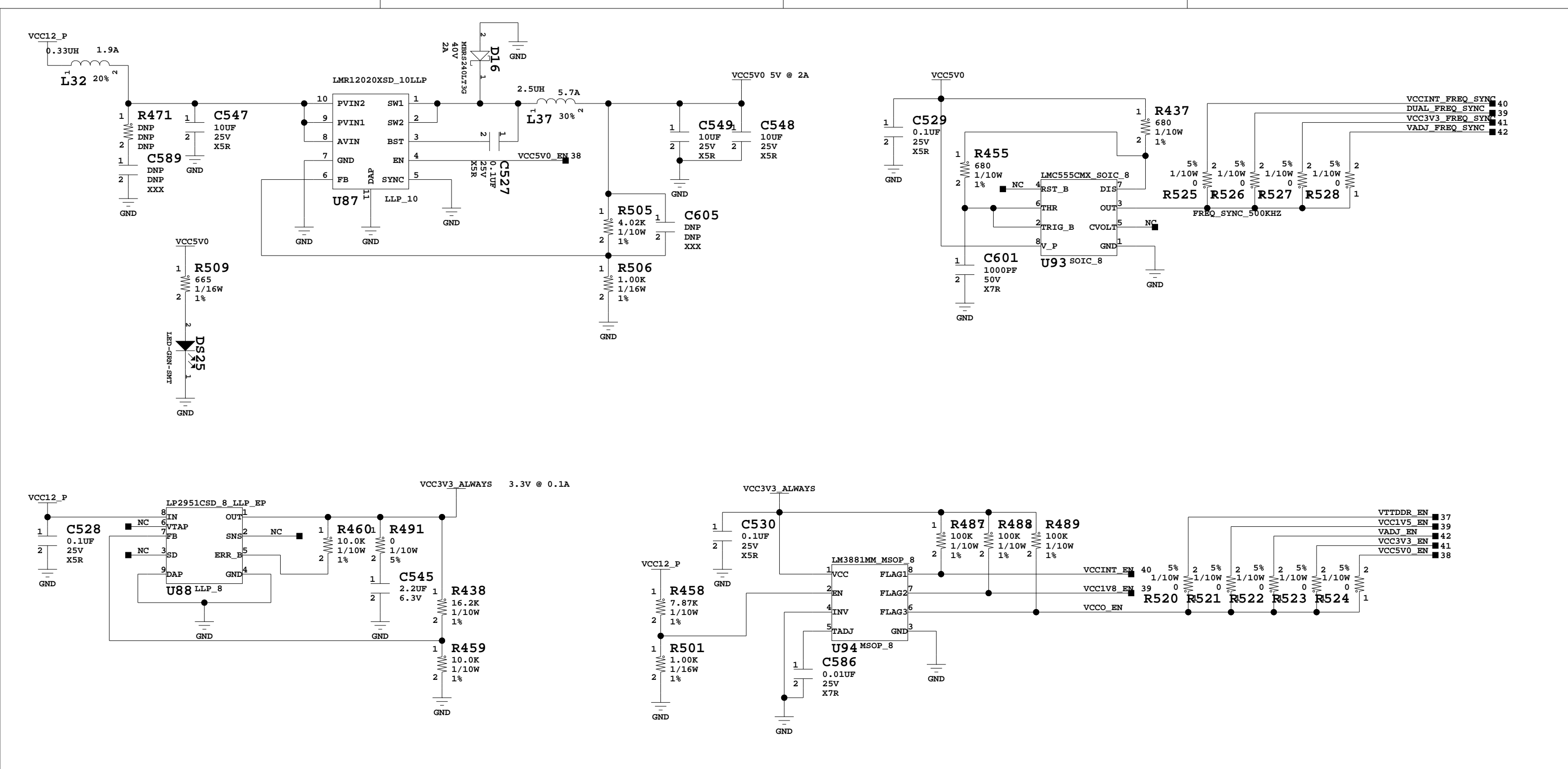
Title: ARM PJTAG Header, PMOD1 SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
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DDR TERMINATION REGULATOR

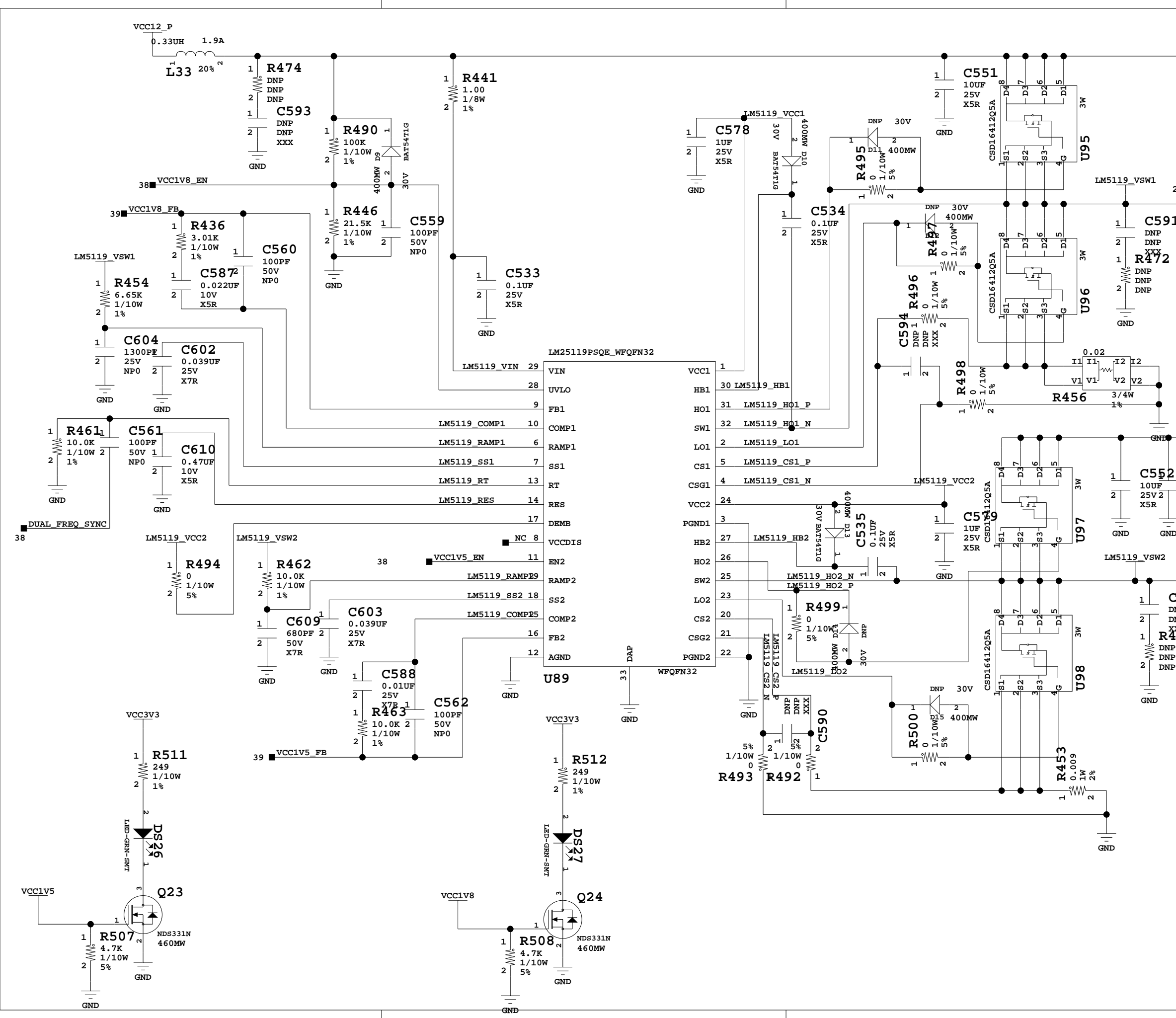


Title: DDR TERMINATION REGULATOR SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
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3.3V_always & 5.0V Regulator, Sync, Sequencer

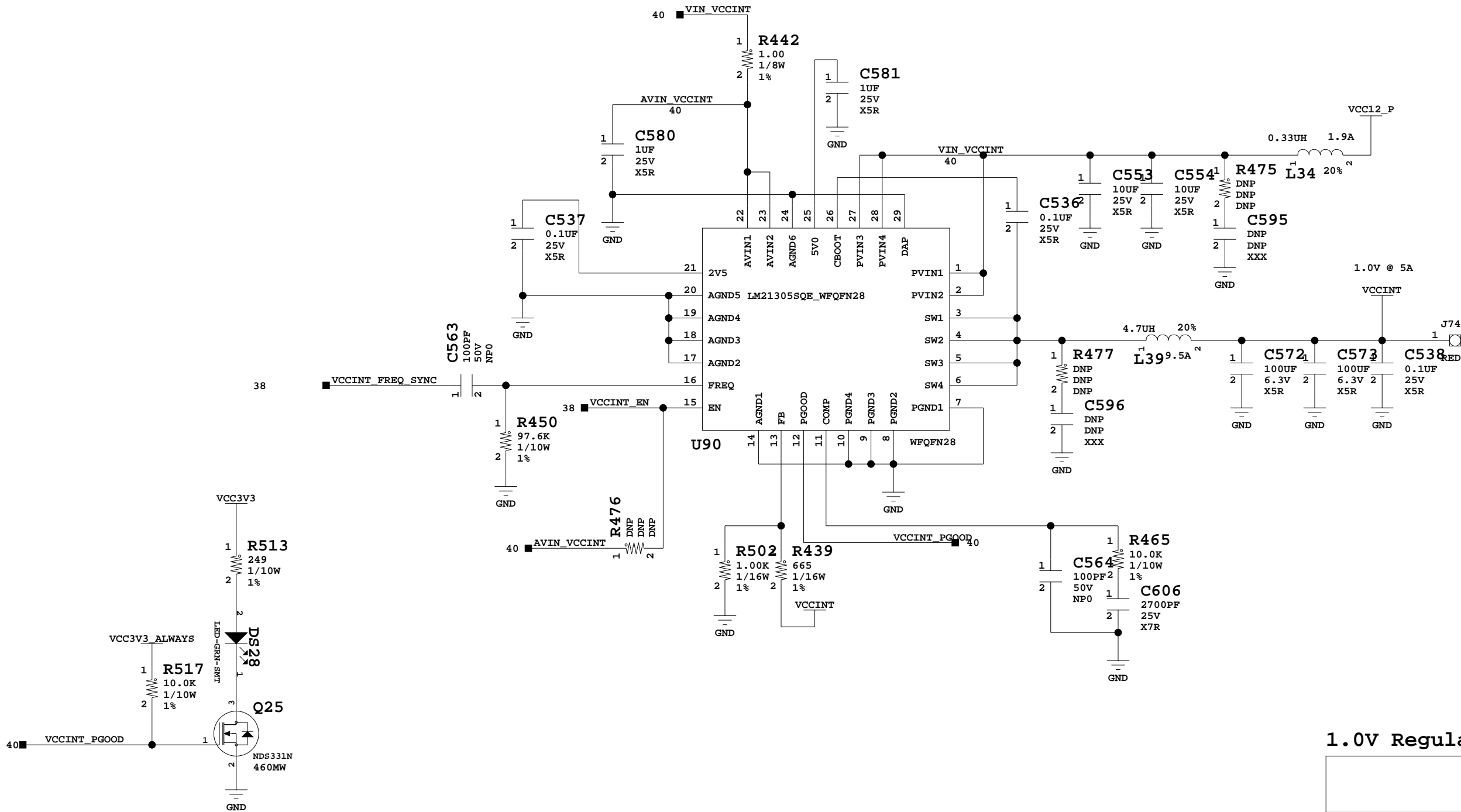
Title: 3.3V_always, 5.0V Reg, Sync, Sequencer SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM	
ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
Date: 12-3-2012_16:09	Ver: TI POWER
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Note: Pins 31/32, and 25/26 should be routed differentially up to the MOSFETs, refer to TI examples for layout guideline details

1.8V and 1.5V Regulator

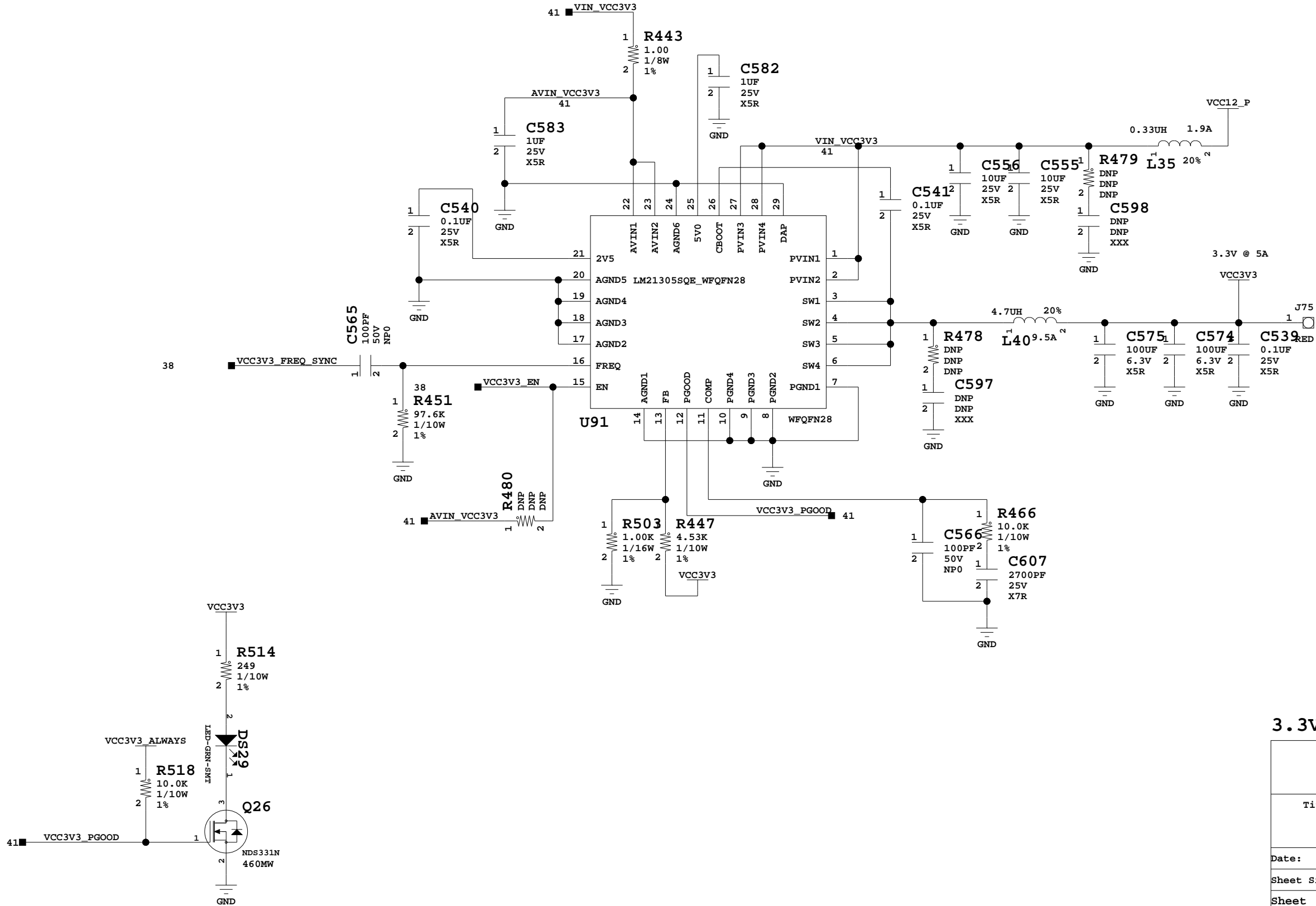
		Title: 1.8V and 1.5V Regulator SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449	
		Date: 12-3-2012_16:09	Ver: TI POWER		
Sheet Size: B		Rev: 01			
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1.0V Regulator

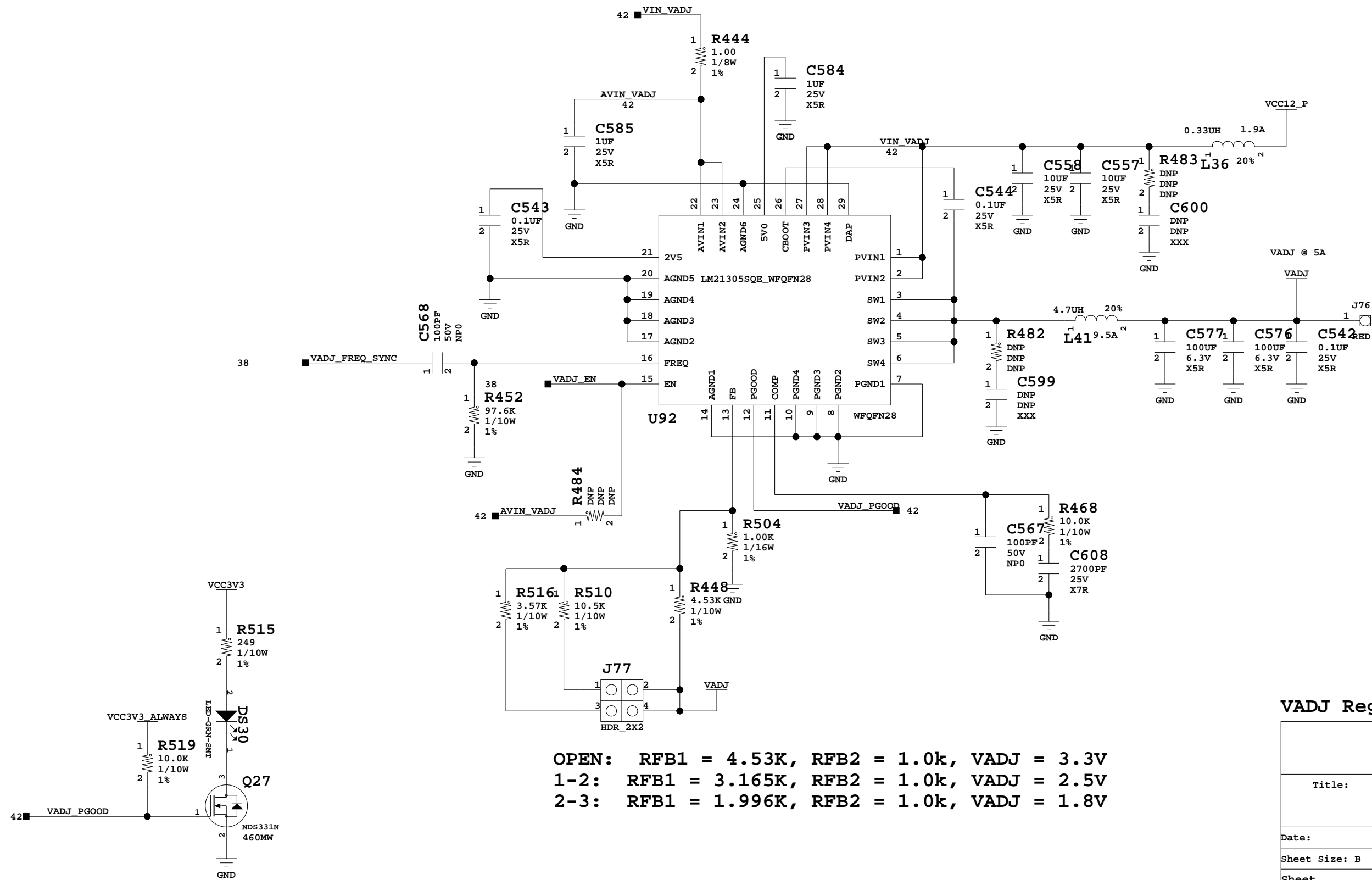


Title: 1.0V Regulator SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
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3.3V Regulator

Title: 3.3V Regulator SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
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VADJ Regulator



Title: VADJ Regulator SCHEM, ROHS COMPLIANT ZC702 EVALUATION PLATFORM		ASSY P/N: 0431696 PCB P/N: 1280617 SCH P/N: 0381449
Date: 12-3-2012_16:09	Ver: TI POWER	
Sheet Size: B	Rev: 01	
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Blank Page



Title:	Blank Page	ASSY P/N: 0431696
	SCHEM, ROHS COMPLIANT	PCB P/N: 1280617
	ZC702 EVALUATION PLATFORM	SCH P/N: 0381449

Date:	12-3-2012_16:09	Ver:	TI POWER
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Sheet Size: B	Rev: 01
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Blank Page



Title:	Blank Page	ASSY P/N: 0431696
	SCHEM, ROHS COMPLIANT	PCB P/N: 1280617
	ZC702 EVALUATION PLATFORM	SCH P/N: 0381449

Date:	12-3-2012_16:09	Ver:	TI POWER
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Sheet Size: B	Rev: 01
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Sheet	44	of	48	Drawn By	BF
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Blank Page



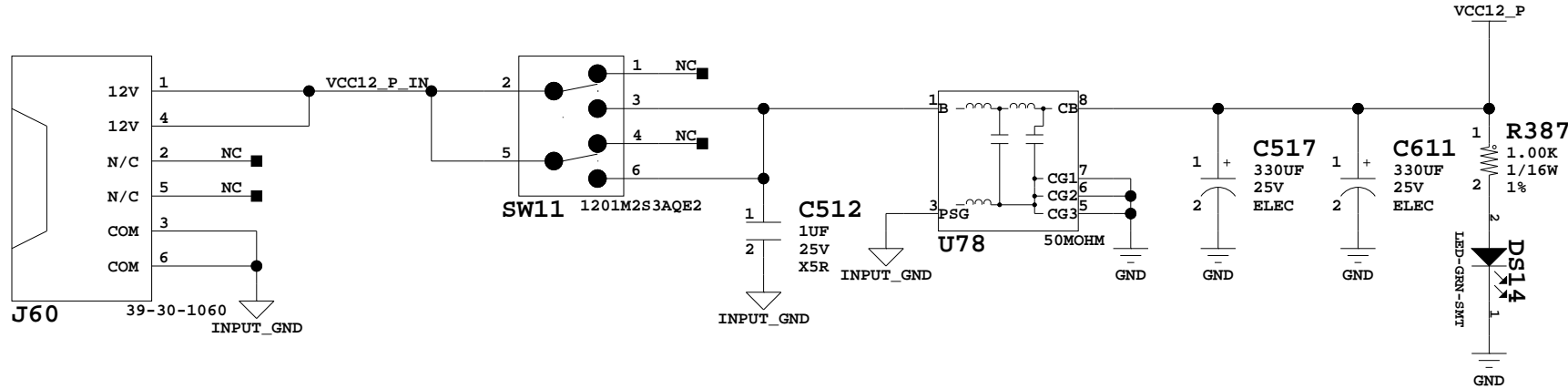
Title:	Blank Page	ASSY P/N: 0431696
	SCHEM, ROHS COMPLIANT	PCB P/N: 1280617
	ZC702 EVALUATION PLATFORM	SCH P/N: 0381449

Date:	12-3-2012_16:09	Ver:	TI POWER
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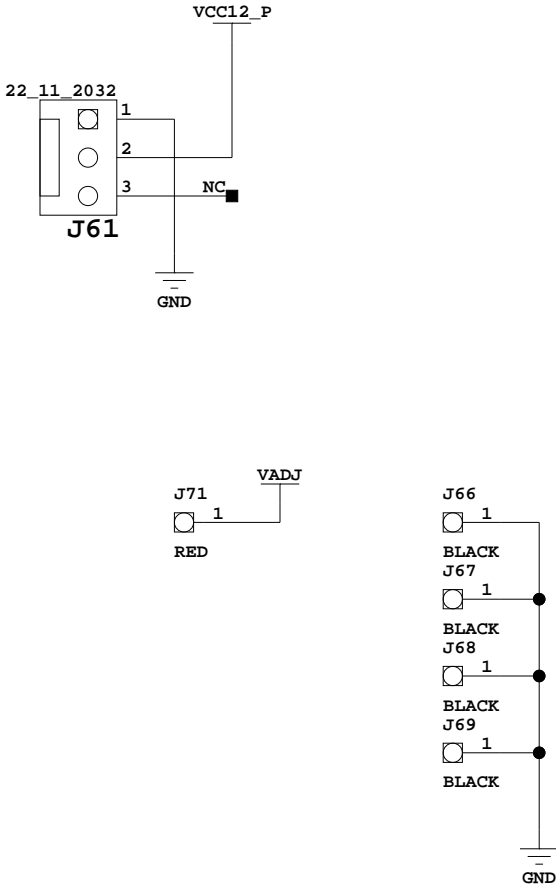
Sheet Size: B	Rev: 01
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4	3	2	1
D			
C			
B			
A			<div>Blank Page</div> <div><div>XILINX</div><div><div>Title:Blank Page</div><div>ASSY P/N: 0431696</div><div>ZC702 EVALUATION PLATFORM</div><div>PCB P/N: 1280617</div><div>SCHEM, ROHS COMPLIANT</div><div>SCH P/N: 0381449</div><div>12-3-2012_16:09</div></div><div><div>Date:</div><div>Ver: TI POWER</div></div><div><div>Sheet Size: B</div><div>Rev: 01</div></div><div><div>Sheet</div><div>46</div><div>of</div><div>48</div><div>Drawn By</div><div>BF</div></div></div>
4	3	2	1



Keyed Fan Header



Power Connector and switch, PMBus Header

Title:		Power Connector and switch, PMBus Header	
SCHEM, ROHS COMPLIANT		ASSY P/N: 0431696	
ZC702 EVALUATION PLATFORM		PCB P/N: 1280617	
		SCH P/N: 0381449	
Date:	12-3-2012_16:09	Ver:	TI POWER
Sheet Size:	B	Rev:	01
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