ZC706 GTX IBERT Design Creation

November 2014

XTP243

Revision History

Date	Version	Description
11/24/14	10.0	Regenerated for 2014.4.
10/08/14	9.0	Regenerated for 2014.3.
06/09/14	8.0	Regenerated for 2014.2.
04/16/14	7.0	Regenerated for 2014.1.
12/18/13	6.0	Regenerated for 2013.4.
10/23/13	5.0	Regenerated for 2013.3.
06/19/13	4.0	Regenerated for Vivado 2013.2.
04/16/13	3.1	Added AR54225.
04/03/13	3.0	Recompiled for 14.5.
01/18/13	2.1	Minor Updates
12/18/12	2.0	Regenerated for 14.4.
10/23/12	1.0	Initial version.

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ZC706 IBERT Overview

- Xilinx ZC706 Board
- Software Requirements
- Setup for the ZC706 IBERT Designs
- Testing with User Provided Hardware
  - Testing Banks 111, 112
- Create IBERT Design for Banks 111, 112
- References

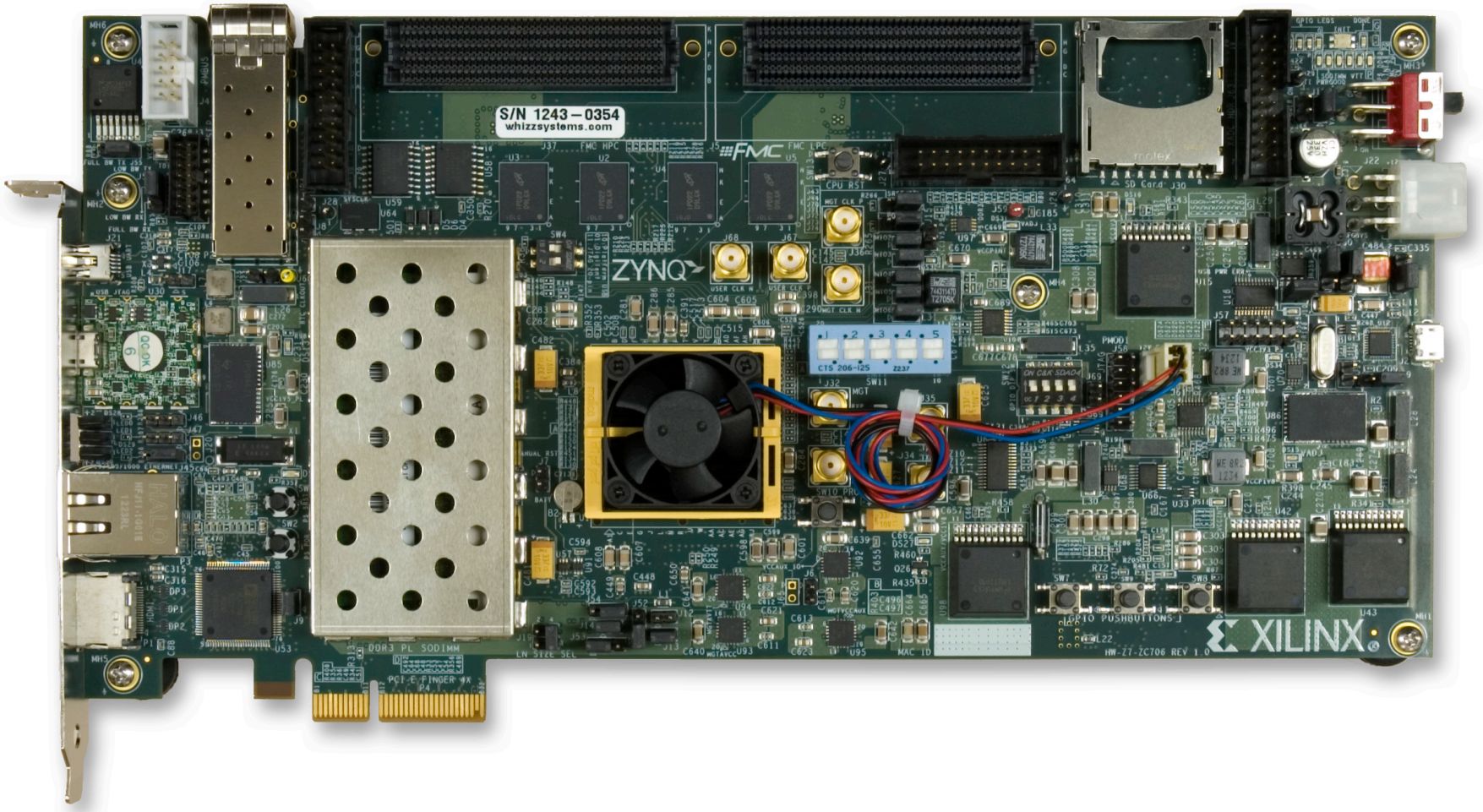
Note: This presentation applies to the ZC706

ZC706 IBERT Overview

- **Description**
  - The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Zynq-7000 GTX transceivers. A graphical user interface is provided in Vivado
- **Reference Design IP**
  - LogiCORE IBERT Example Designs

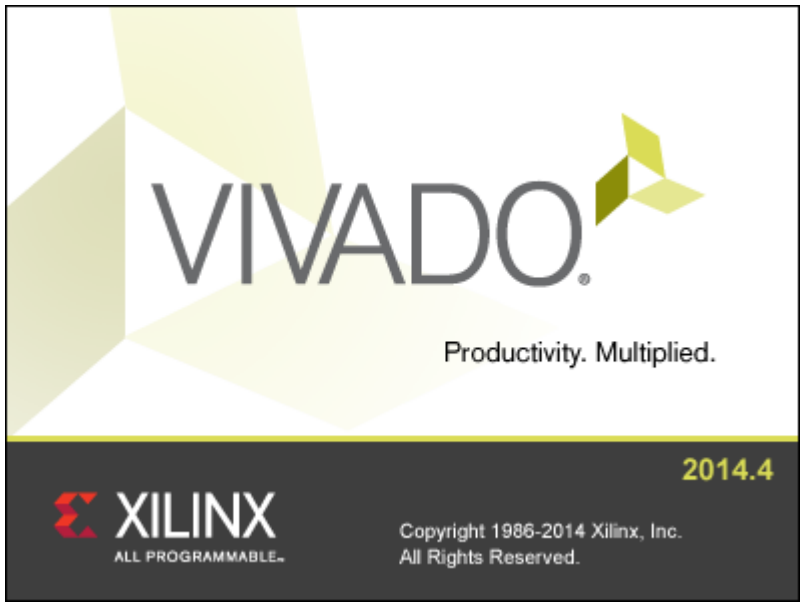
Note: Presentation applies to the ZC706

Xilinx ZC706 Board



Vivado Software Requirements

- Xilinx Vivado Design Suite 2014.4, Design Edition

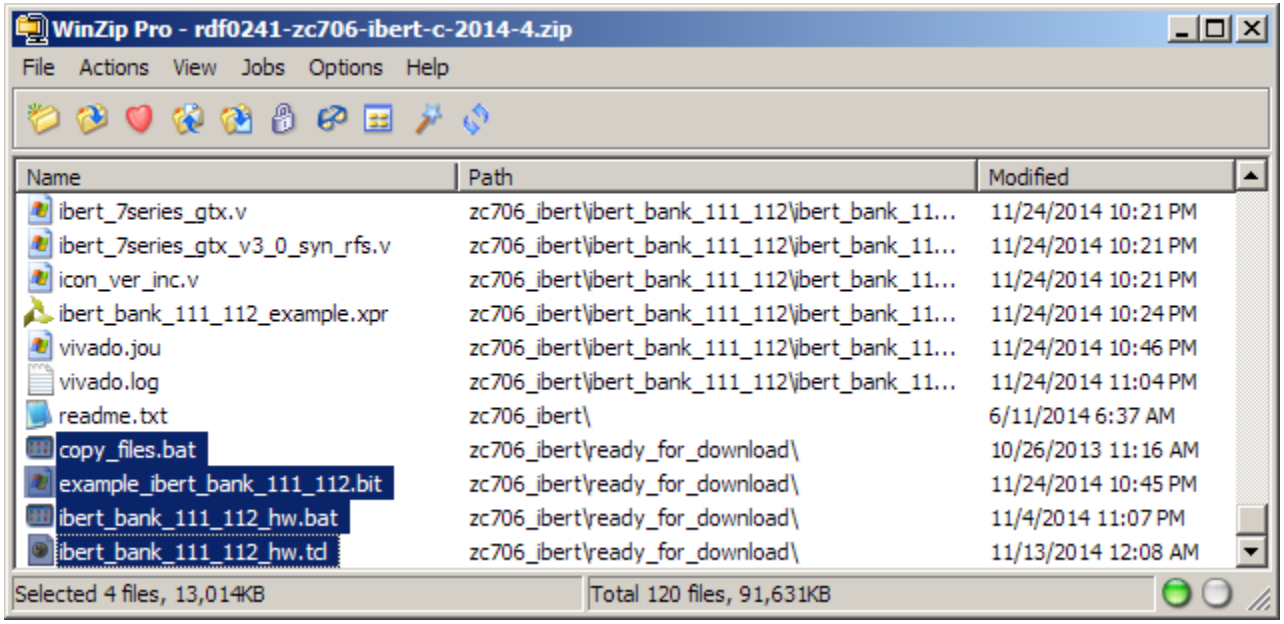


Note: Presentation applies to the ZC706

Setup for the ZC706 IBERT Designs

Setup for the ZC706 IBERT Designs

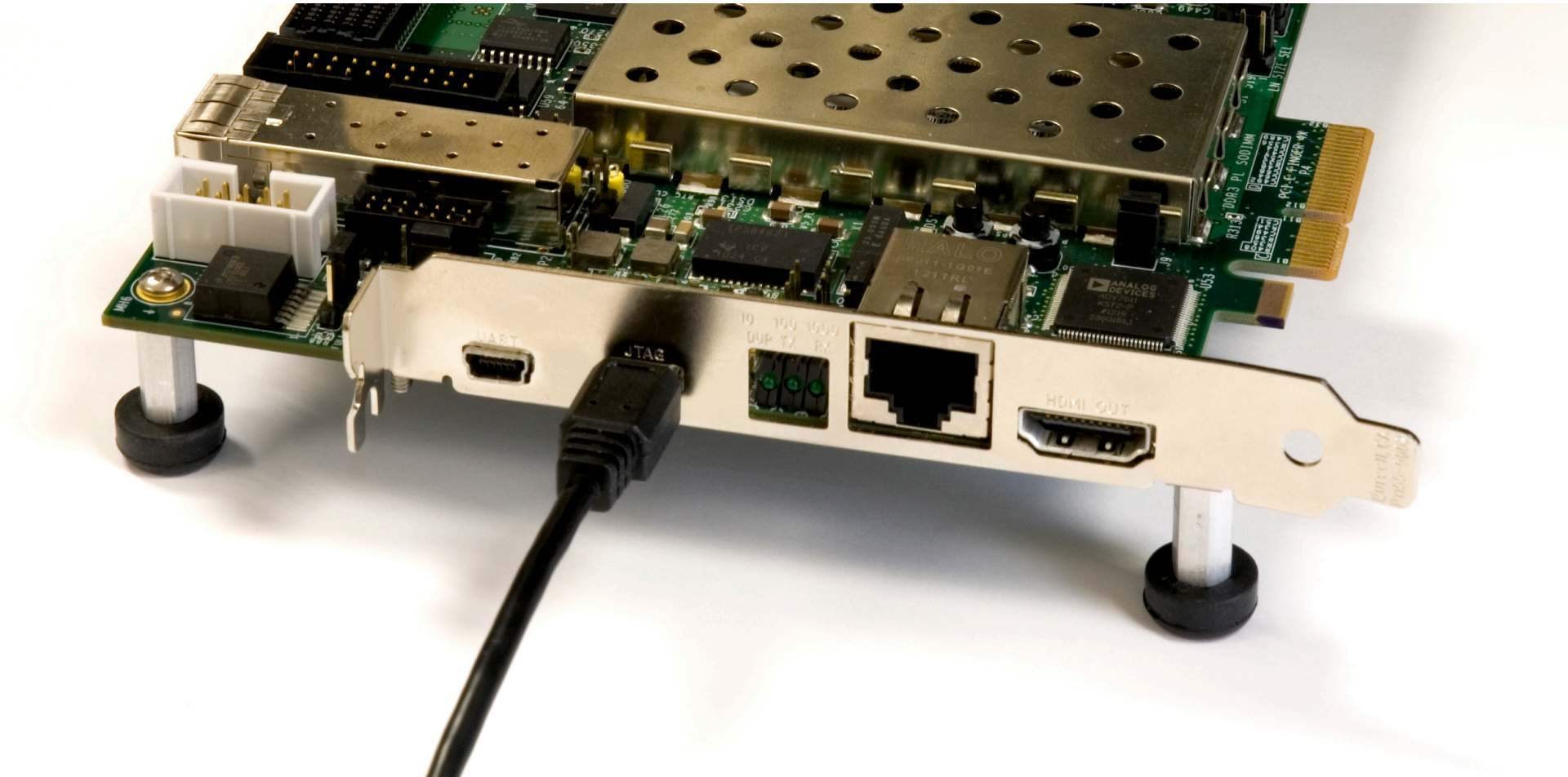
- **Open the ZC706 GTX IBERT Design Files (2014.4 C) ZIP file, and extract these files to your C:\ drive:**
  - zc706_ibert\ready_for_download*
  - Available through http://www.xilinx.com/zc706



Note: Presentation applies to the ZC706

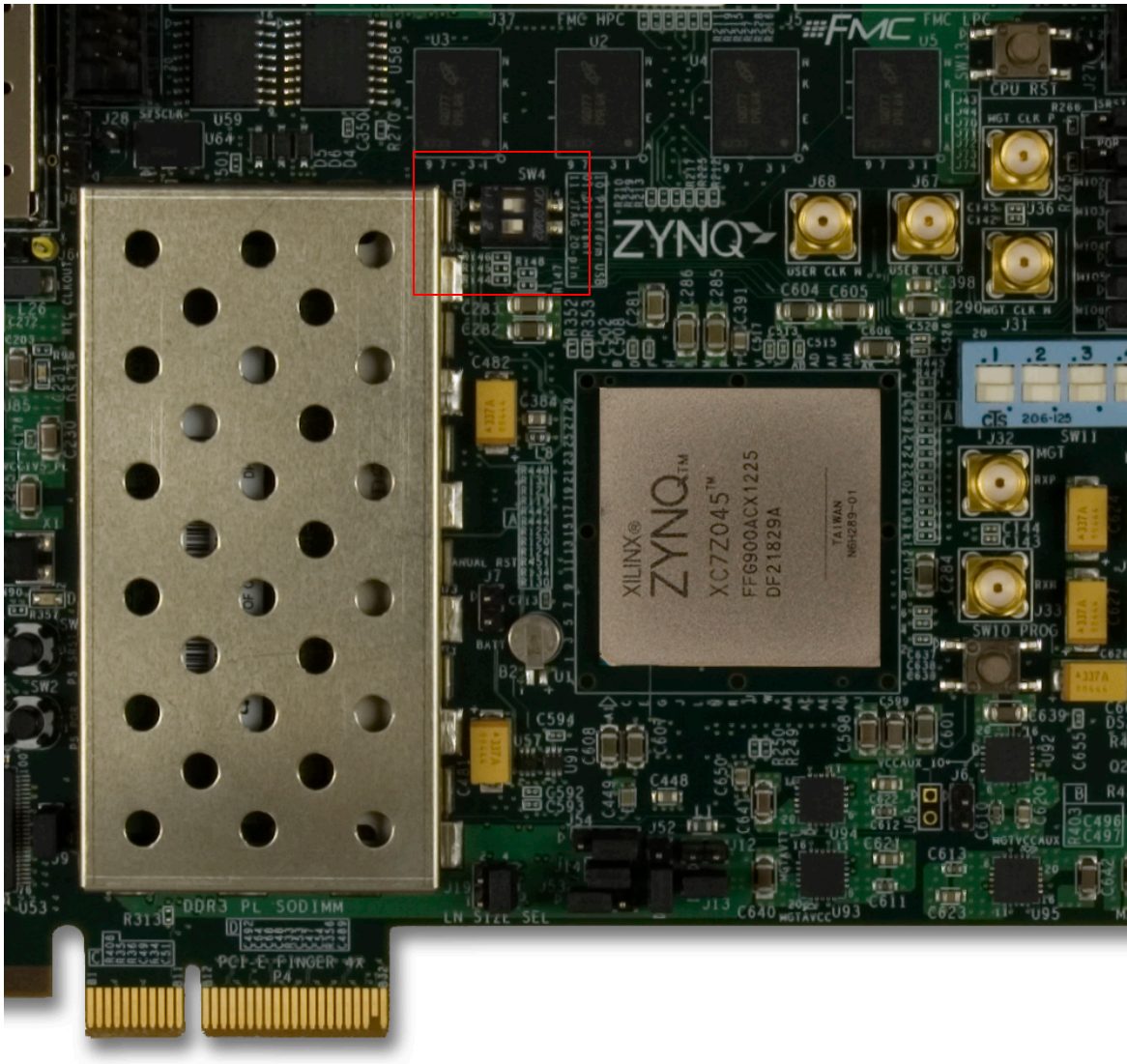
Setup for the ZC706 IBERT Designs

- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the ZC706 board**
  - Connect this cable to your PC
  - Power on the ZC706 board



Setup for the ZC706 IBERT Designs

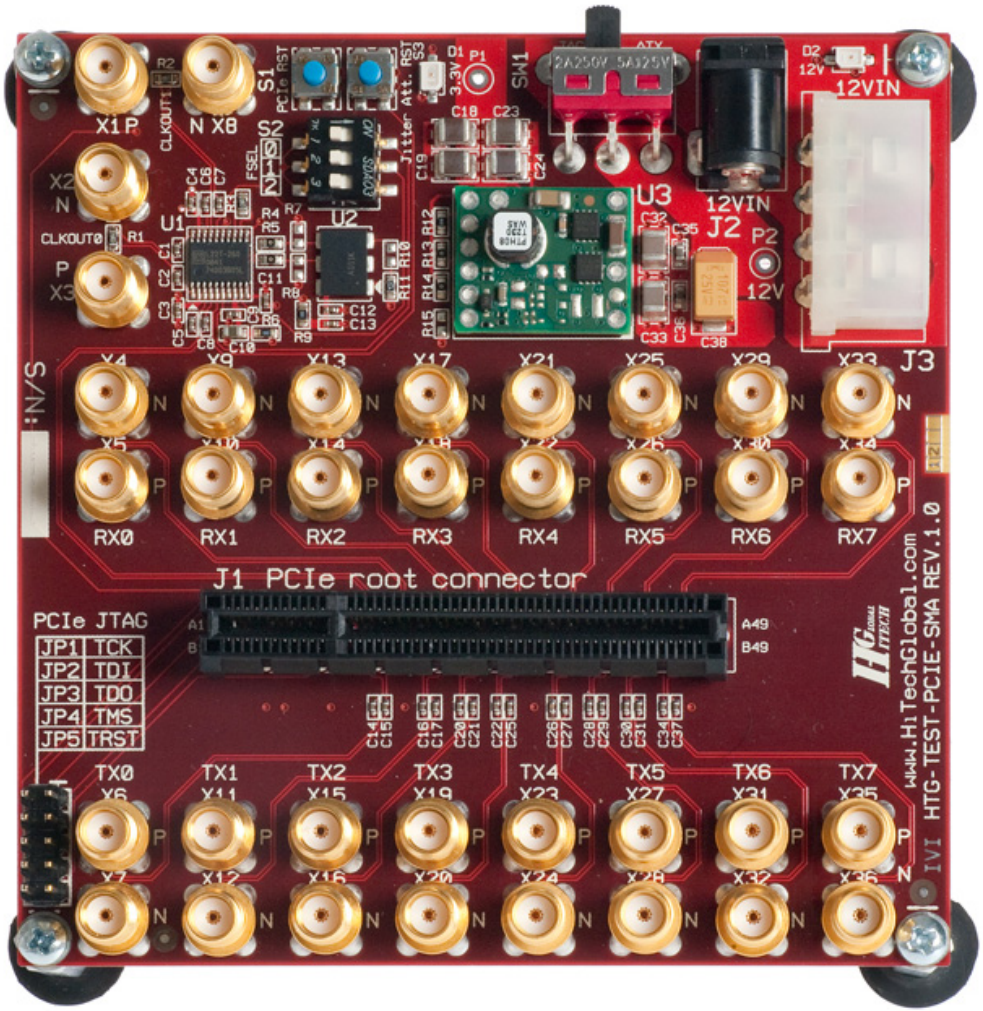
- **Set the JTAG Select Switch, SW4, to 01**
  - If using a Platform Cable USB (II) JTAG Cable, set SW4 to 10



Testing with User Provided Hardware

Testing with User Provided Hardware

- **For testing Banks 111 and 112:**
- **PCIe Testing Hardware:**
  - HiTechGlobal PCI Express Test & SerialIO Expansion Module
  - HTG-TEST-PCIE-SMA
  - 16 SMA cables required
  - Requires power supply, either:
    - 4-pin Peripheral power connector from ATX power supply
  - Or:
    - HiTechGlobal PWR-12V-6A
- **Attach all SMA cables and insert ZC706**
- **Power on both boards**



Note: Presentation applies to the ZC706

Testing with User Provided Hardware

- **SMA Cables**
  - www.rosenbergerna.com
  - Part number: 72D-32S1-32S1-00610A

- **SMA Quick connects**
  - RADIALL
  - Part number: R125791501
  - Available here or here

Note: Presentation applies to the ZC706

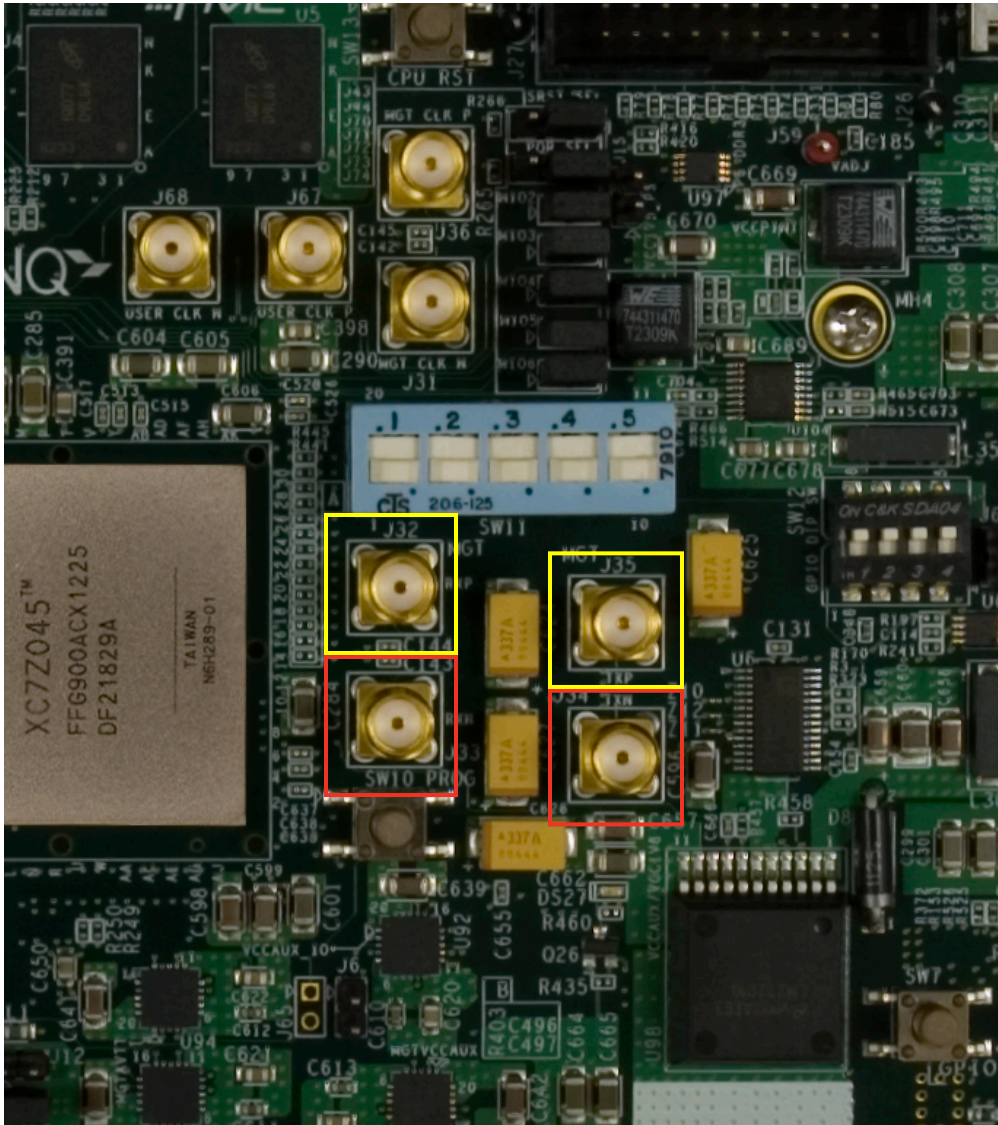
Testing with User Provided Hardware

- **For testing Bank 111 and 112, Optical Loopback Adapter**
  - www.molex.com
  - SFP Loopback Adapter, 5.0 db Attenuation
  - Part # 74765-0904
- **The ZC706 uses 1 adapter**
  - Insert into SFP on ZC706

Note: Presentation applies to the ZC706

ZC706 GTX IBERT Design – Banks 111, 112

- **Using the SMA cables:**
  - Connect J32 to J35
  - Connect J33 to J34

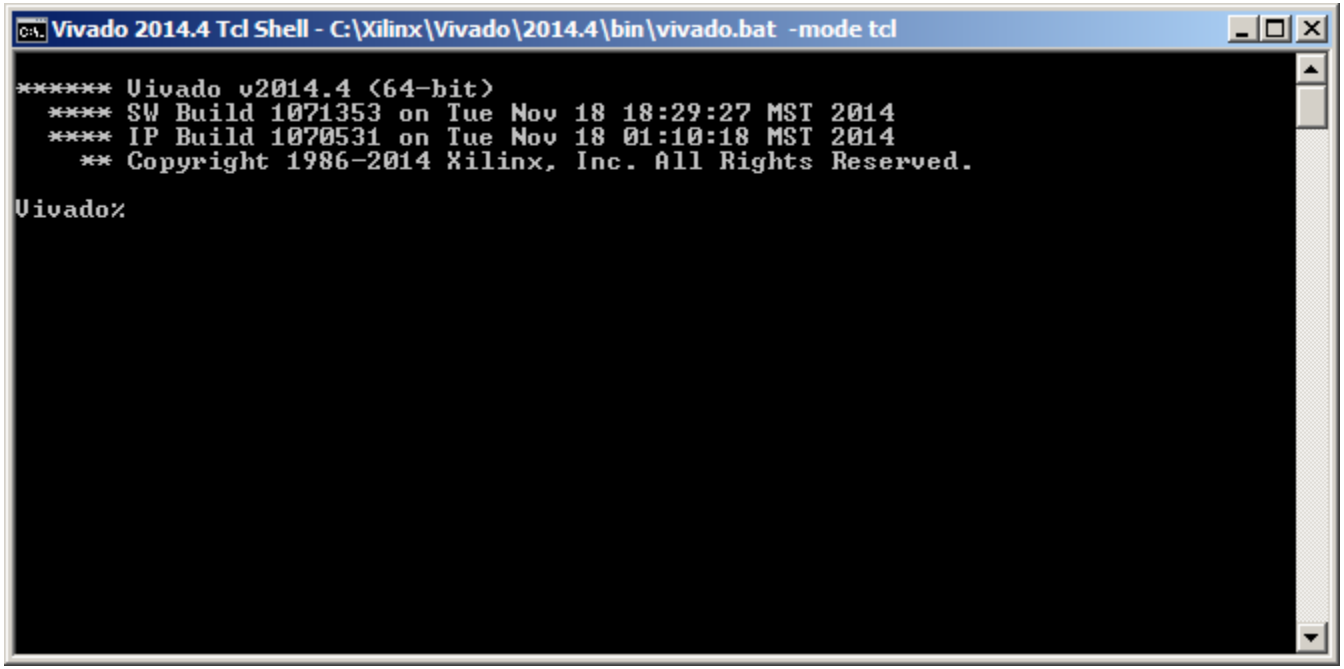


ZC706 GTX IBERT Design – Banks 111, 112

ZC706 GTX IBERT Design – Banks 111, 112

- Open a Vivado Tcl Shell:

  Start → All Programs → Xilinx Design Tools → Vivado 2014.4 → Vivado 2014.4 Tcl Shell

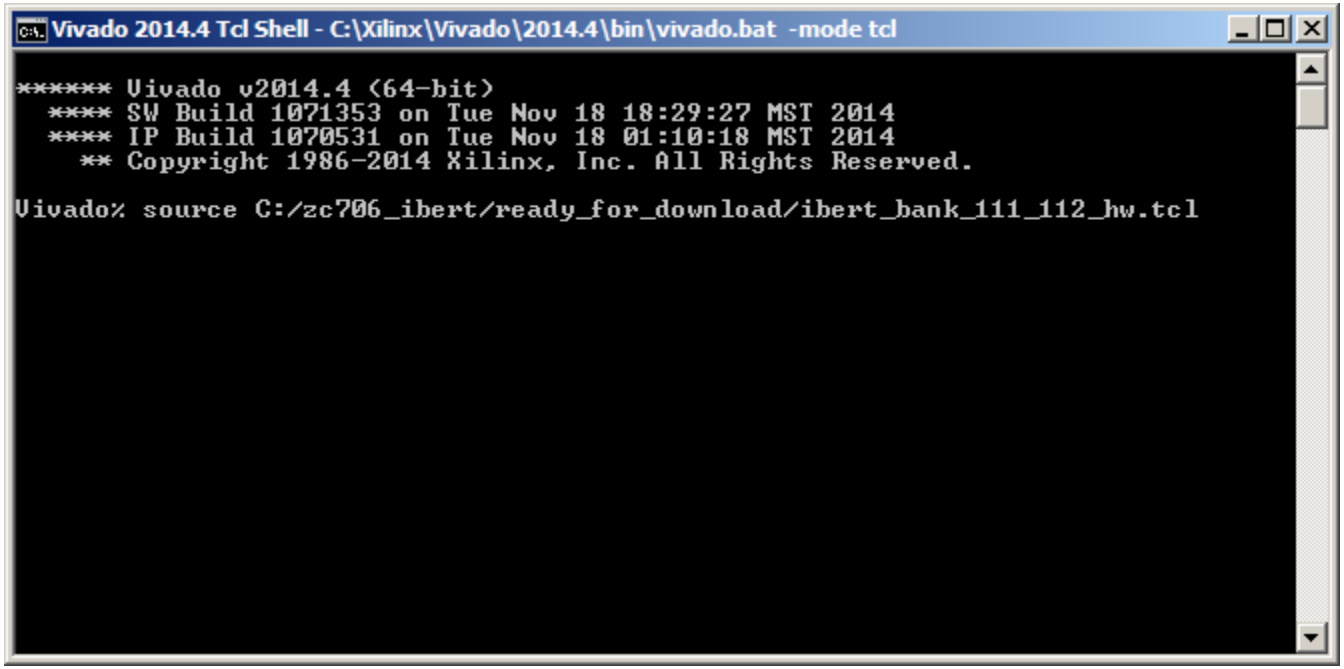


Note: Presentation applies to the ZC706

ZC706 GTX IBERT Design – Banks 111, 112

- Open a Vivado Tcl Shell and type:

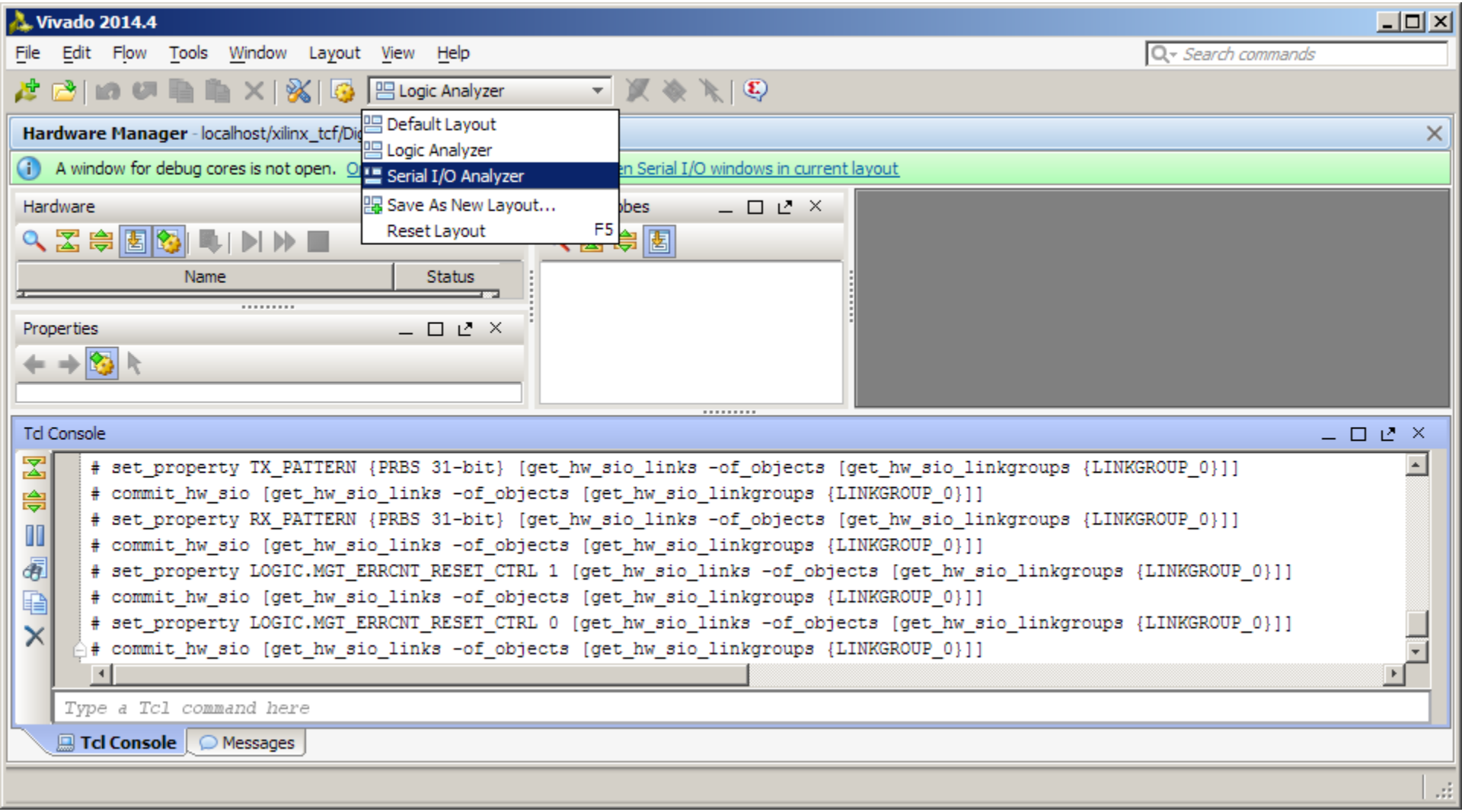
  source C:/zc706_ibert/ready_for_download/ibert_bank_111_112_hw.tcl



Note: Presentation applies to the ZC706

ZC706 GTX IBERT Design – Banks 111, 112

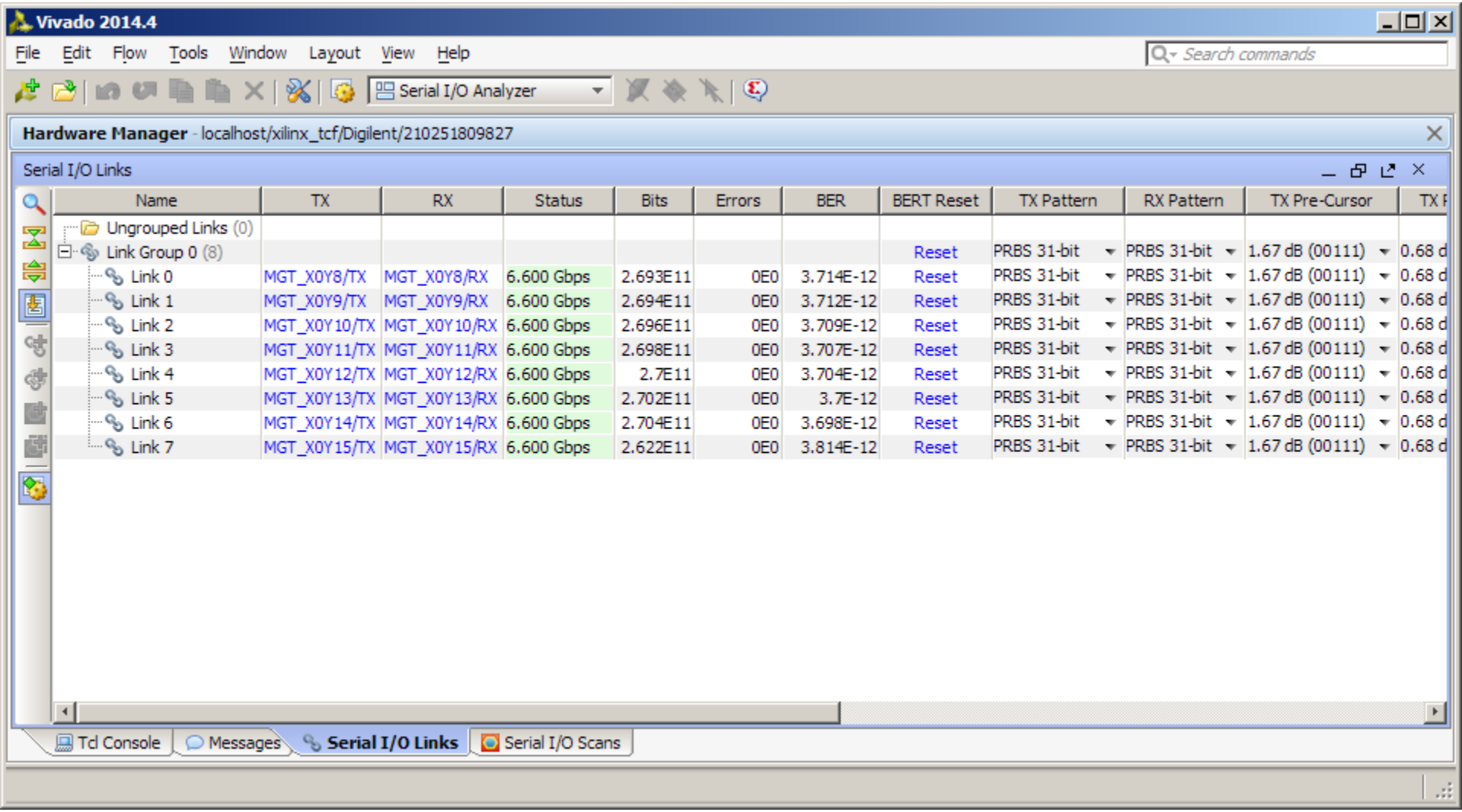
- If needed, set Vivado GUI layout to Serial I/O Analyzer



Note: Presentation applies to the ZC706

ZC706 GTX IBERT Design – Banks 111, 112

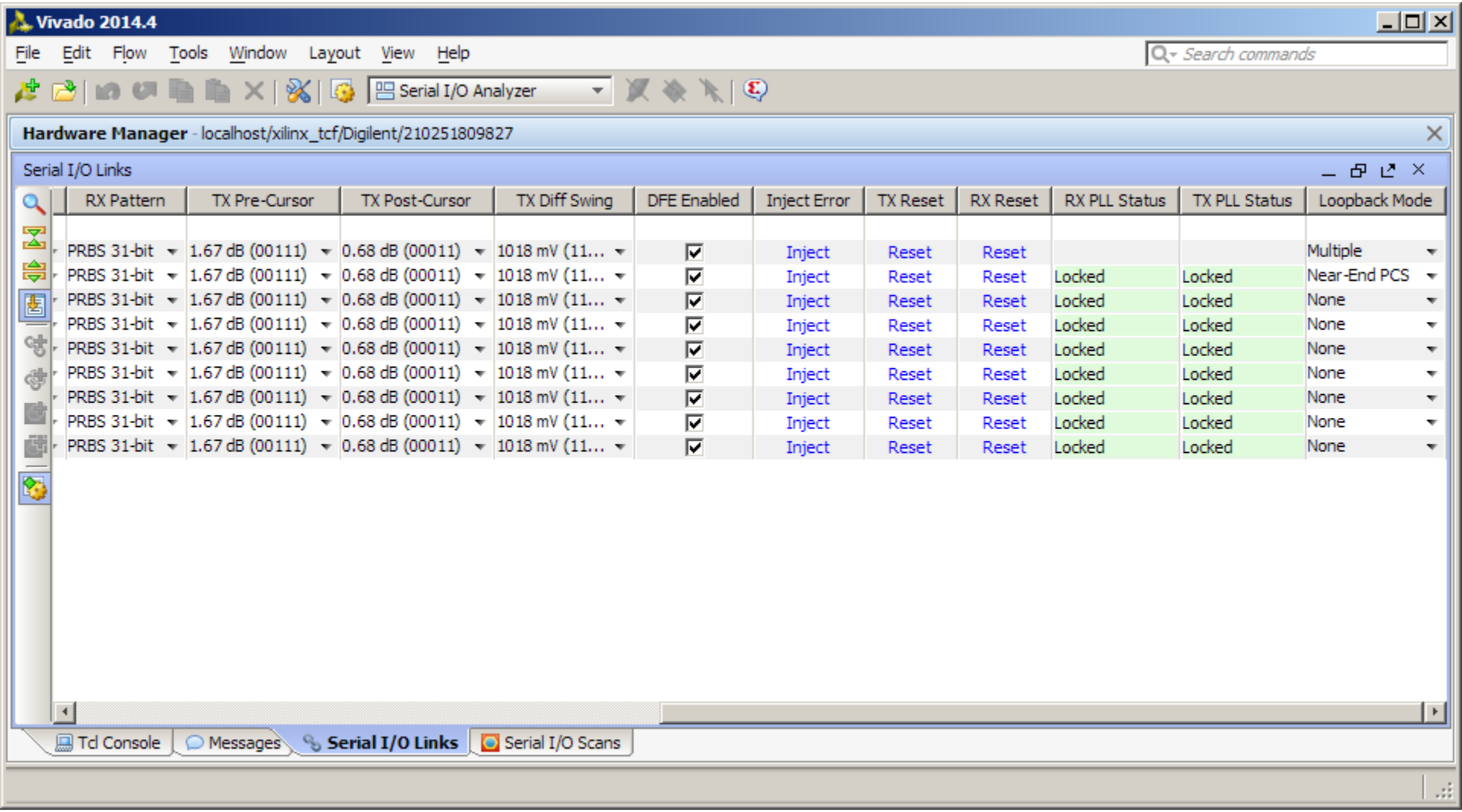
- The Status column shows the line rate is 6.6 Gbps for all GTXs



Note: Bank 111, 112: SMA, SFP+, LPC, PCIe

ZC706 GTX IBERT Design – Banks 111, 112

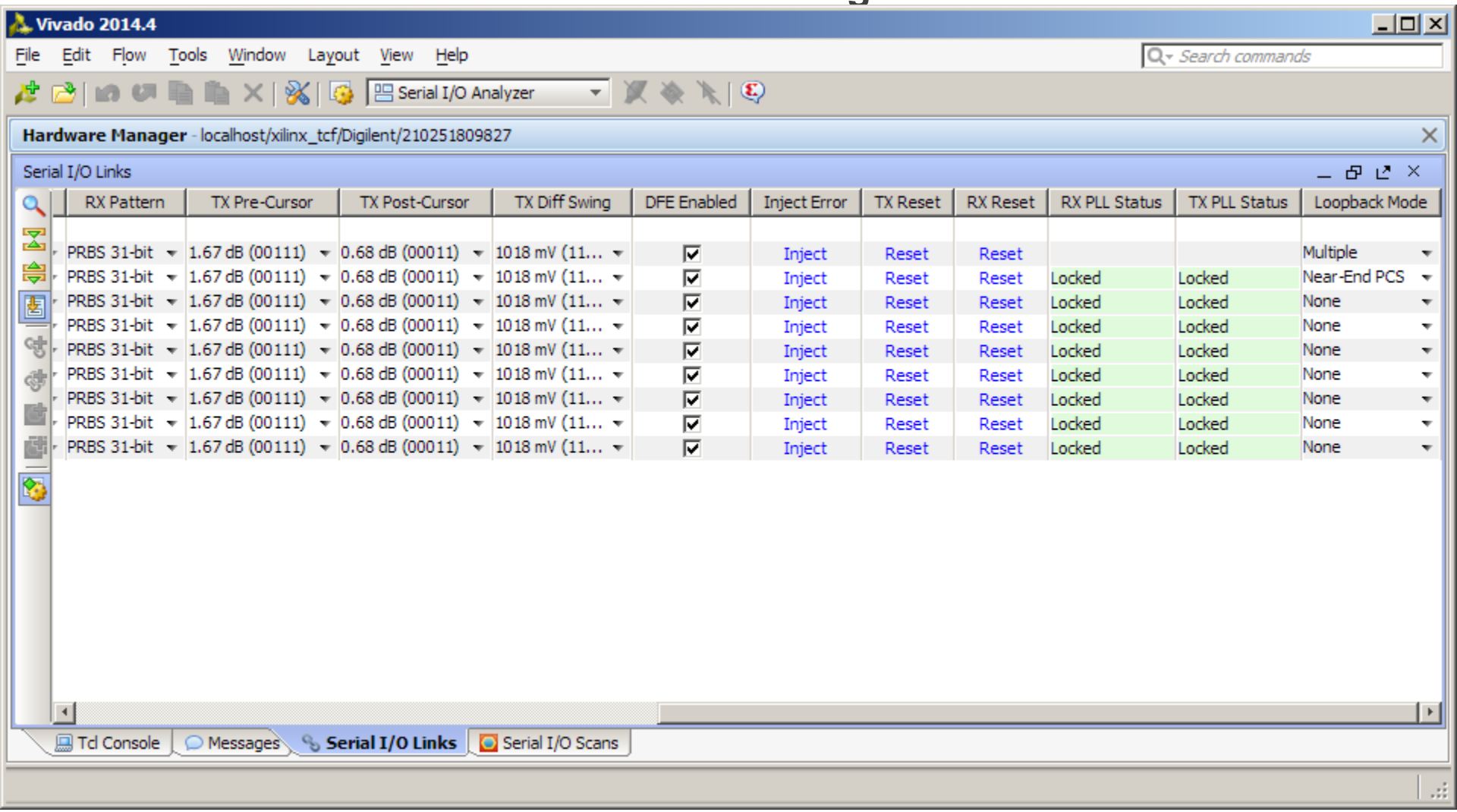
- Scroll to the right to view the Loopback Mode



Note: Presentation applies to the ZC706

ZC706 GTX IBERT Design – Banks 111, 112

- Loopback Mode is set to Near-End PMC for the first GTX
- Close Vivado GUI after finished viewing



Note: Presentation applies to the ZC706

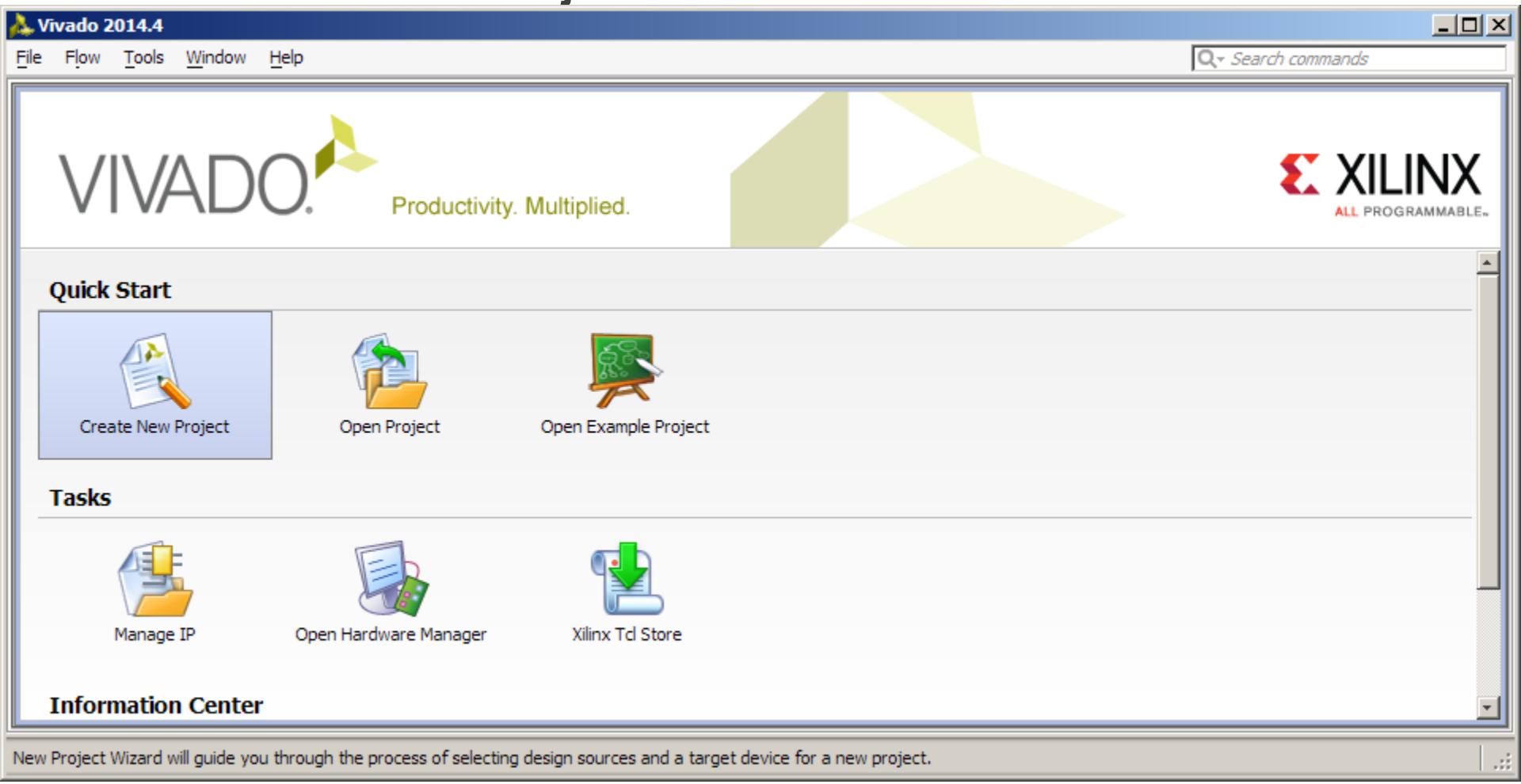
Create IBERT Design for Bank 111, 112

Create IBERT Design for Banks 111, 112

- Open Vivado

  Start → All Programs → Xilinx Design Tools → Vivado 2014.4 → Vivado

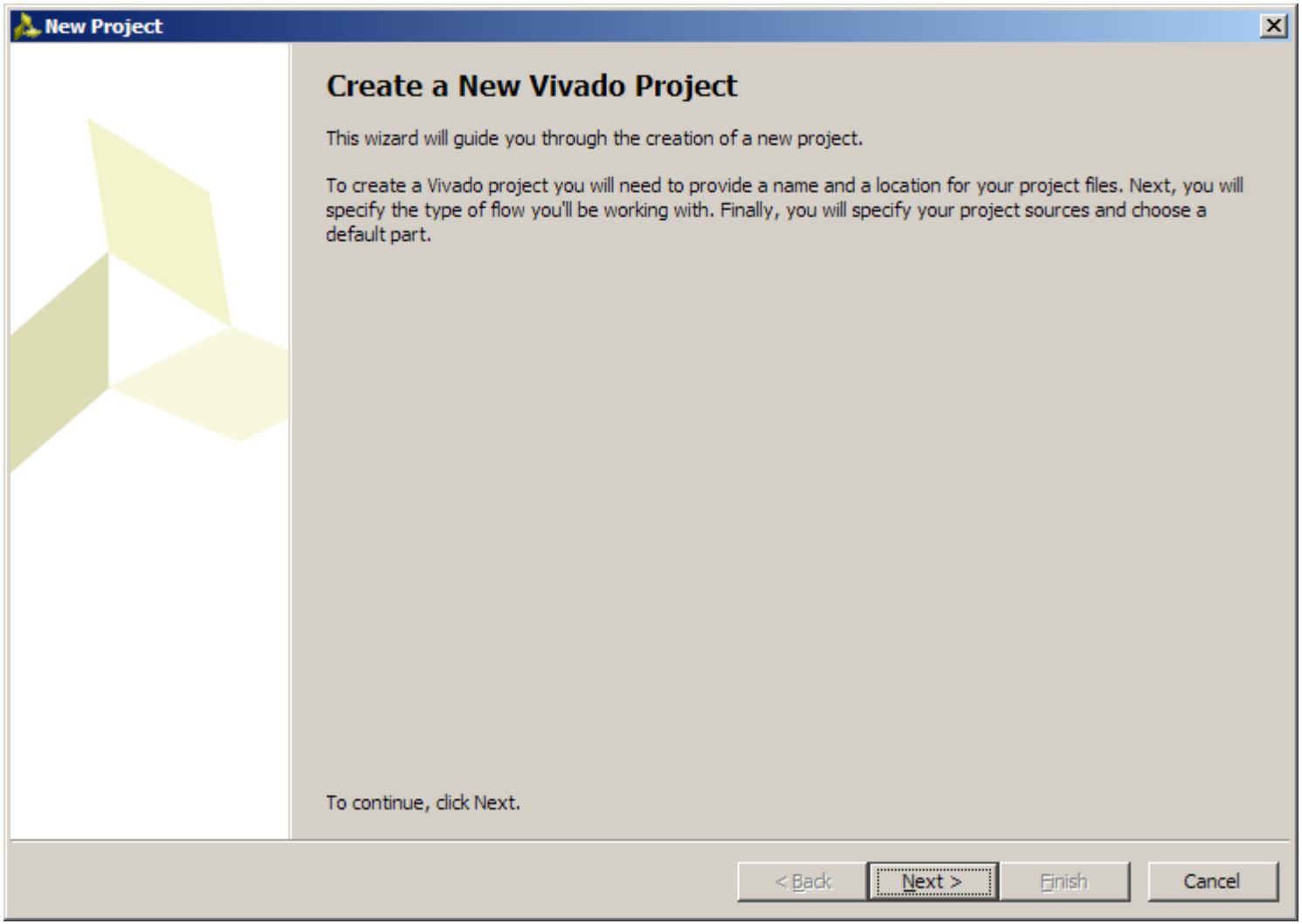
- Select Create New Project



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

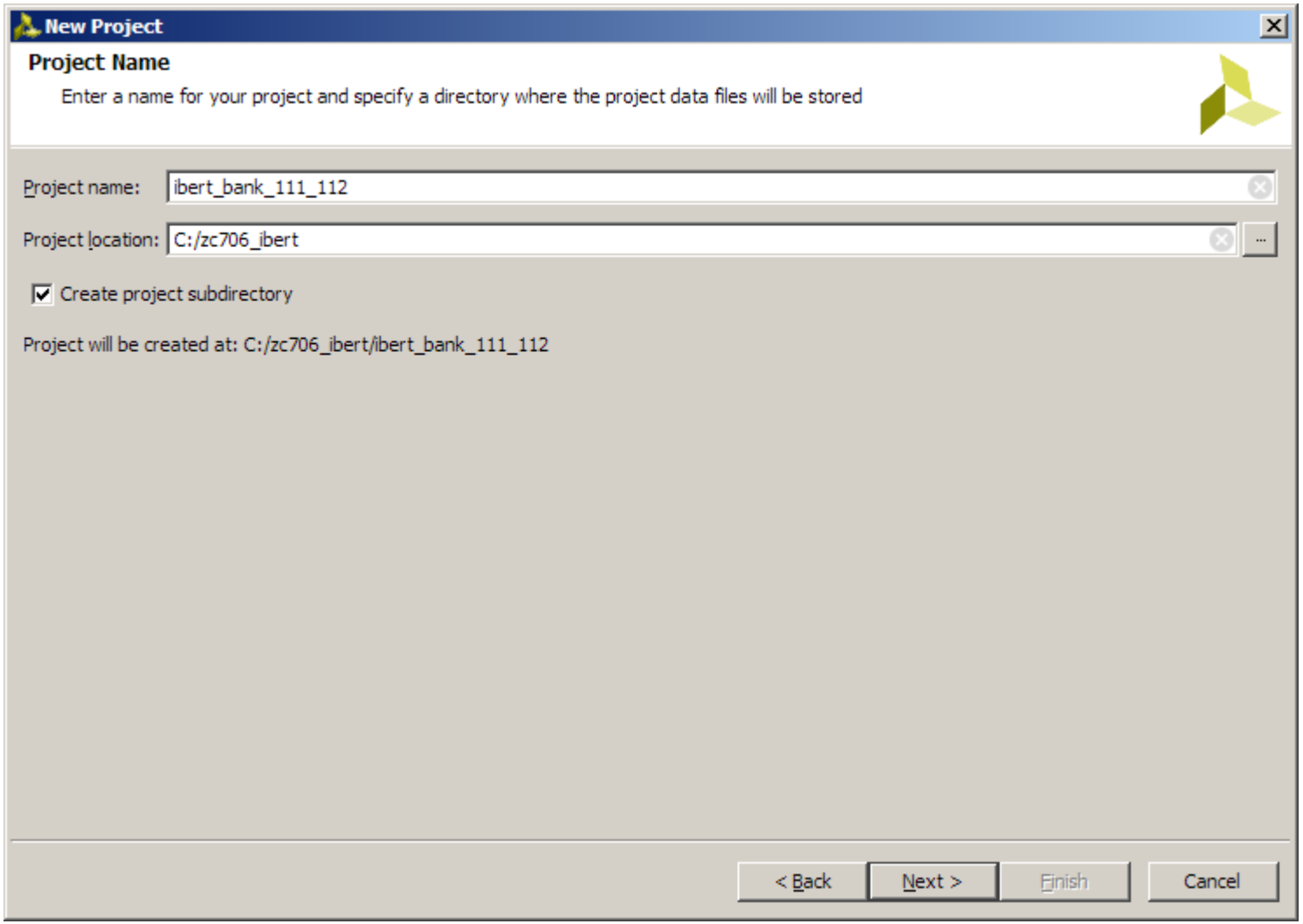
- Click Next



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

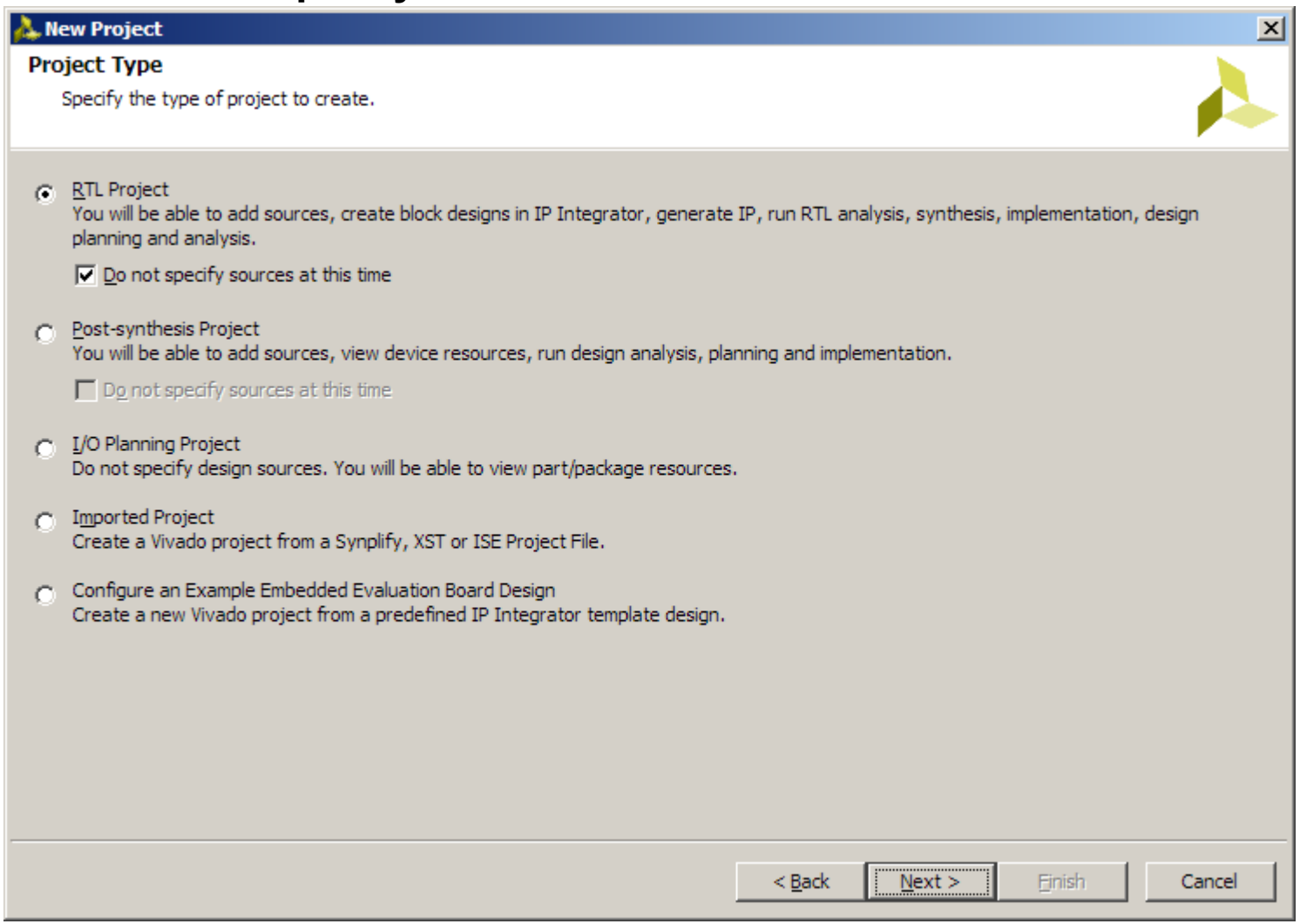
- Set the Project name and location to ibert_bank_111_112 and C:/zc706_ibert; check Create project subdirectory



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

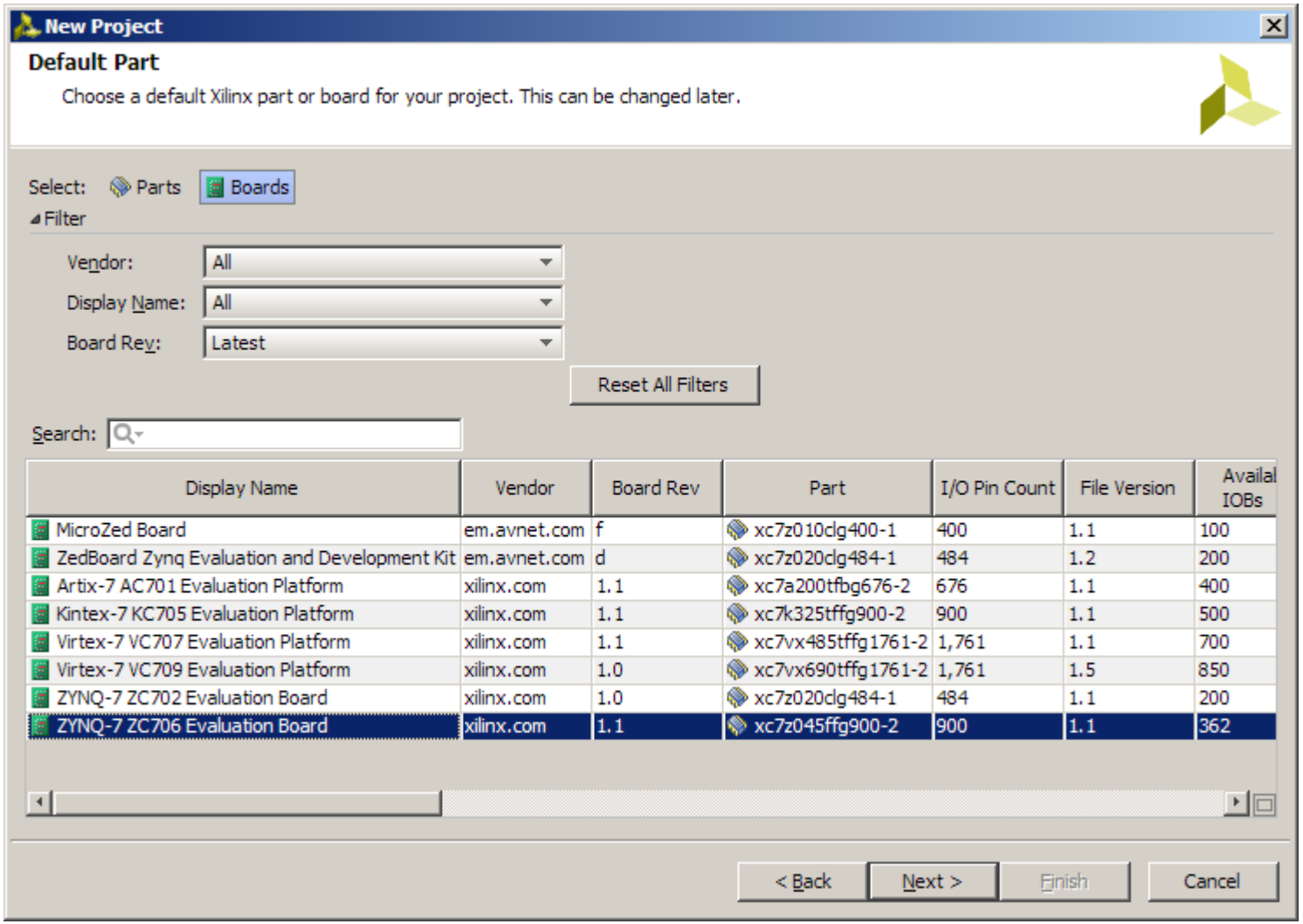
- **Select RTL Project**
  - Select **Do not specify sources at this time**



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

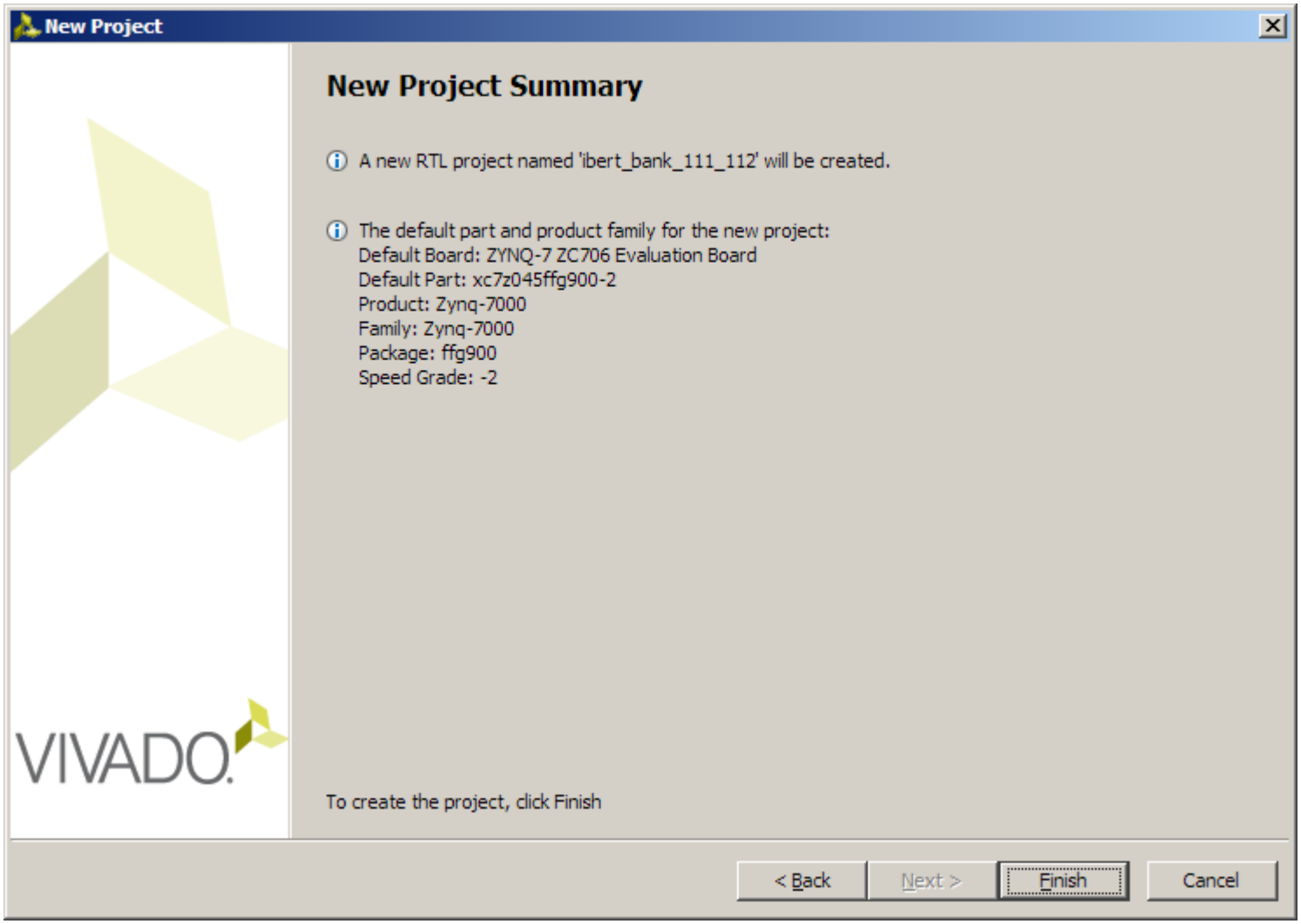
Select the ZC706 Board



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

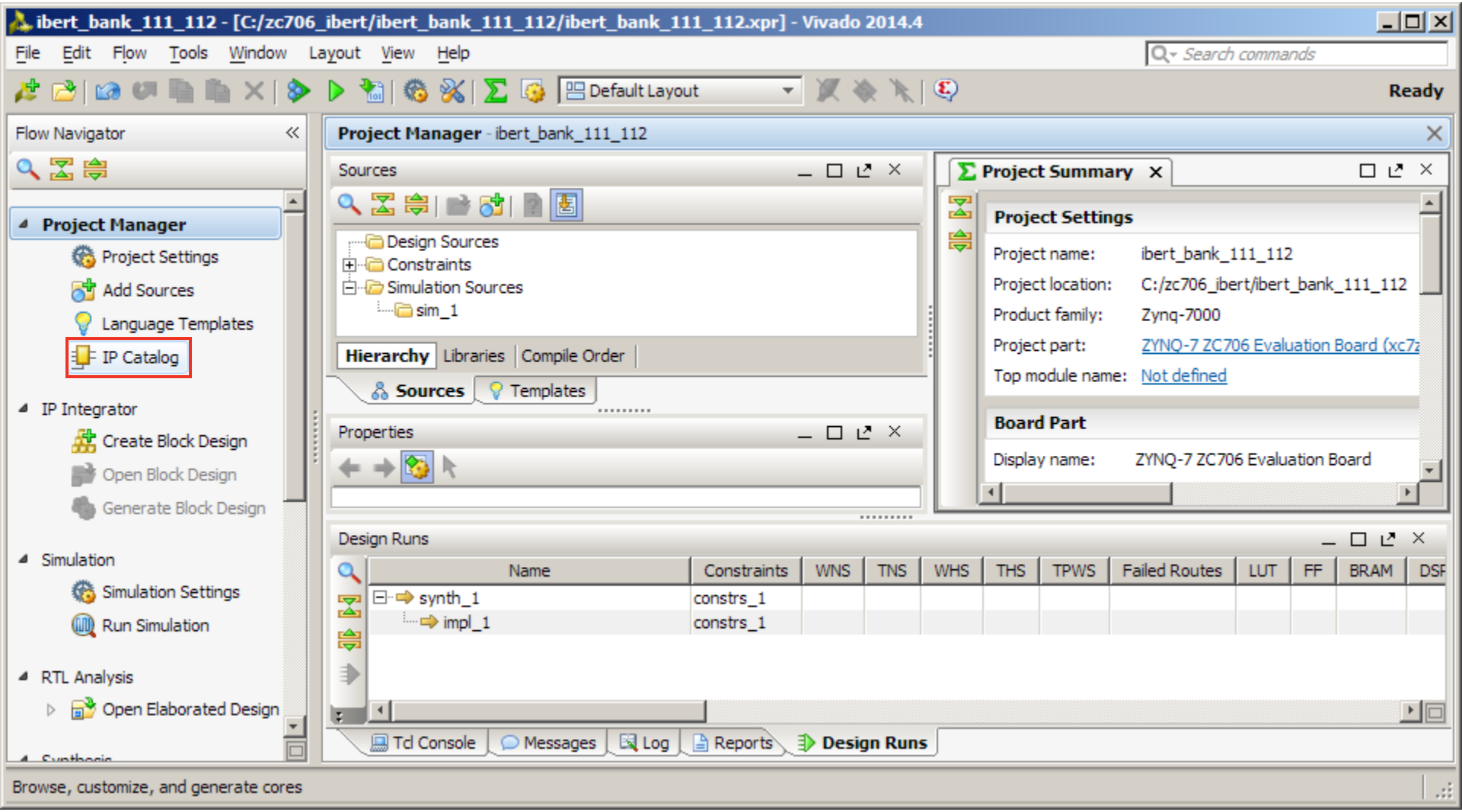
- Click Finish



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

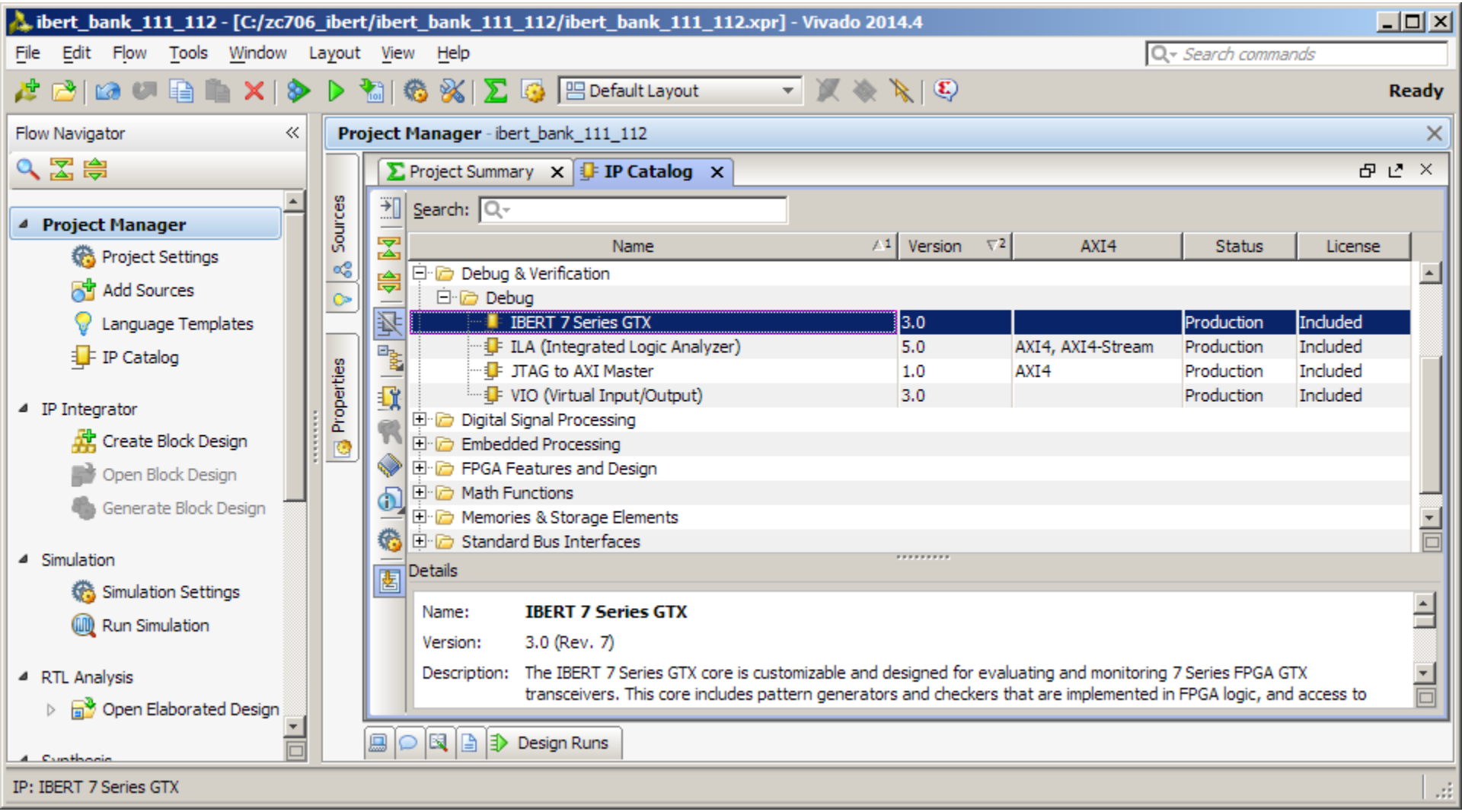
- Click on IP Catalog



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

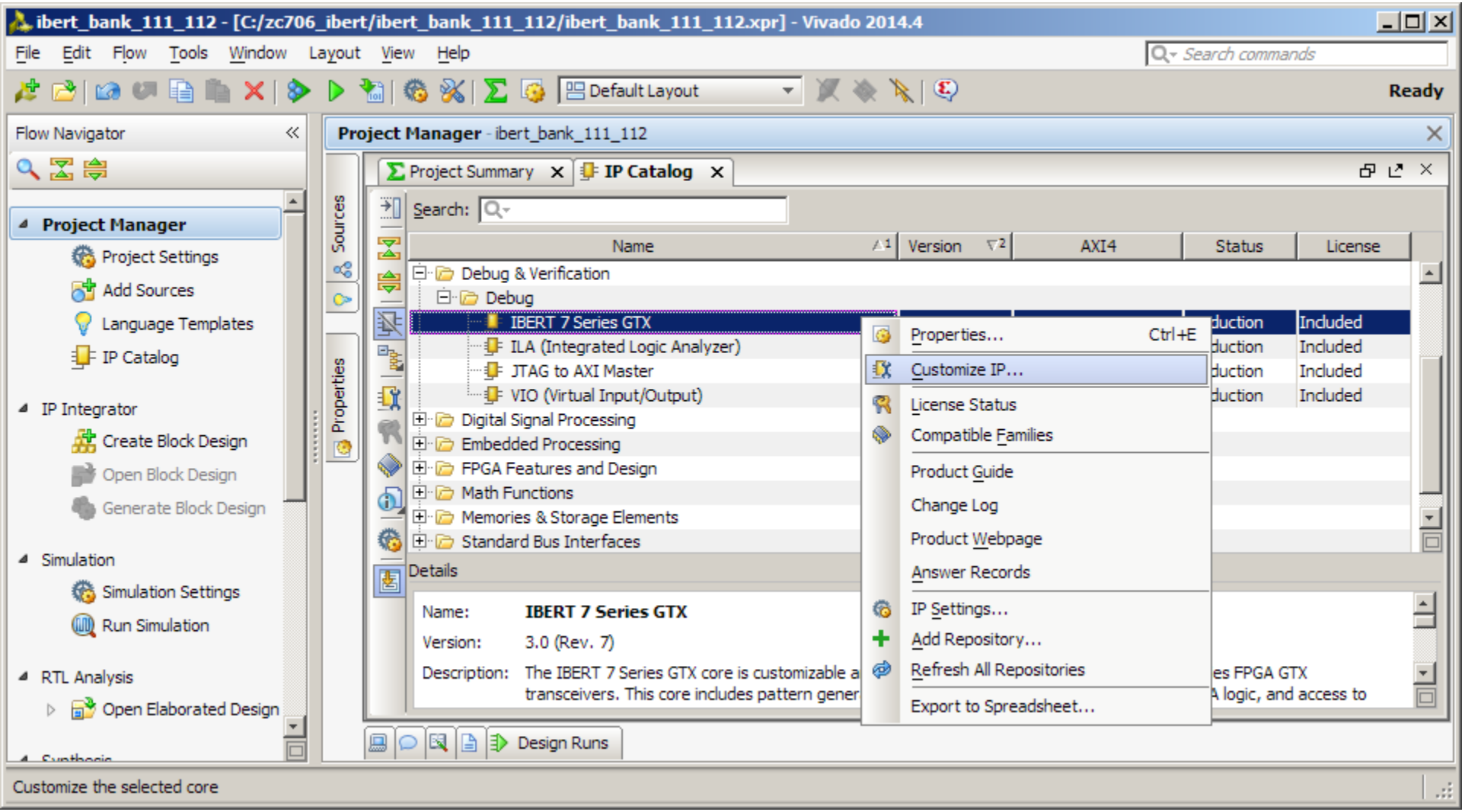
- Select IBERT 7 Series GTX, v3.0 under Debug & Verification



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

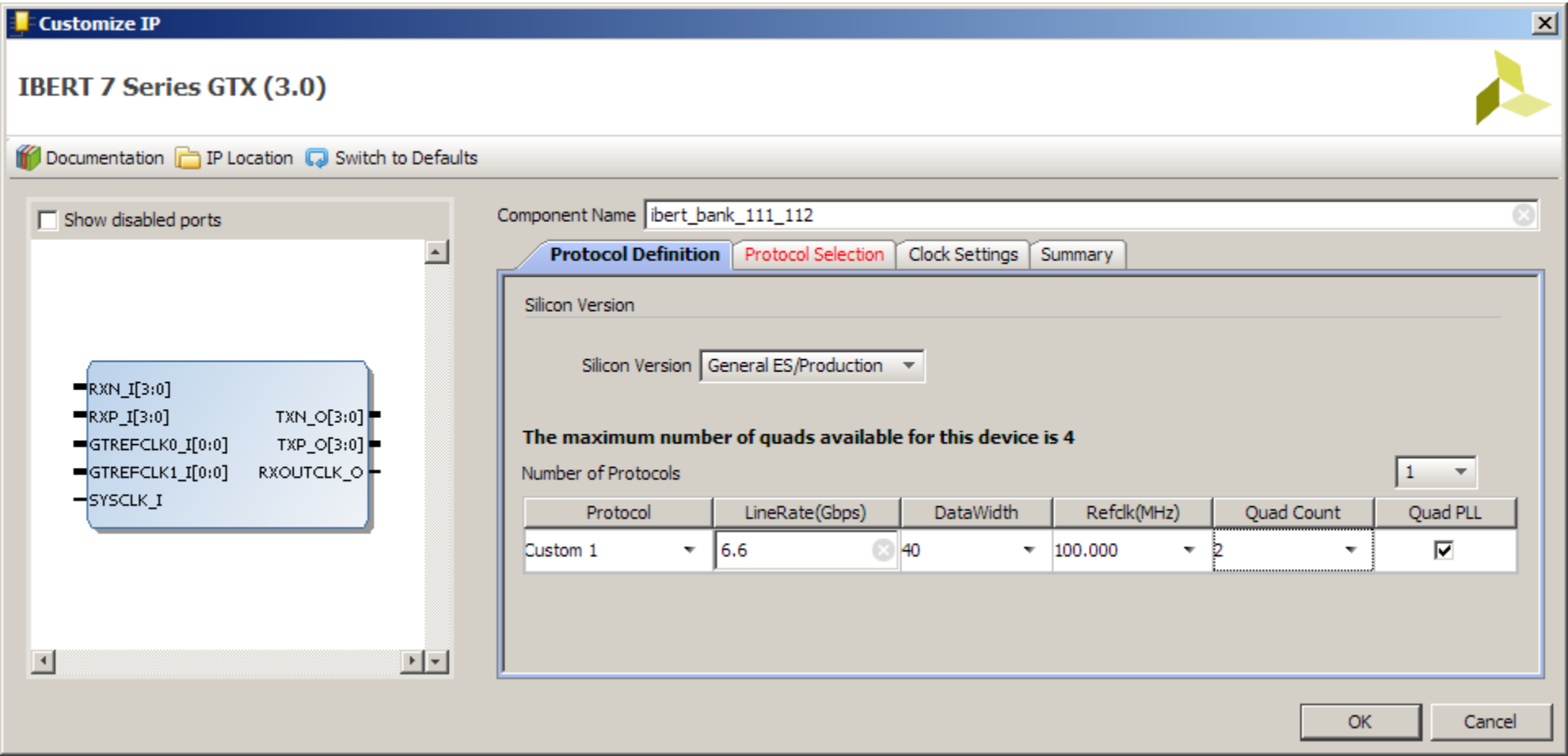
- Right click on IBERT 7 Series GTX and select Customize IP…



Note: Presentation applies to the ZC706

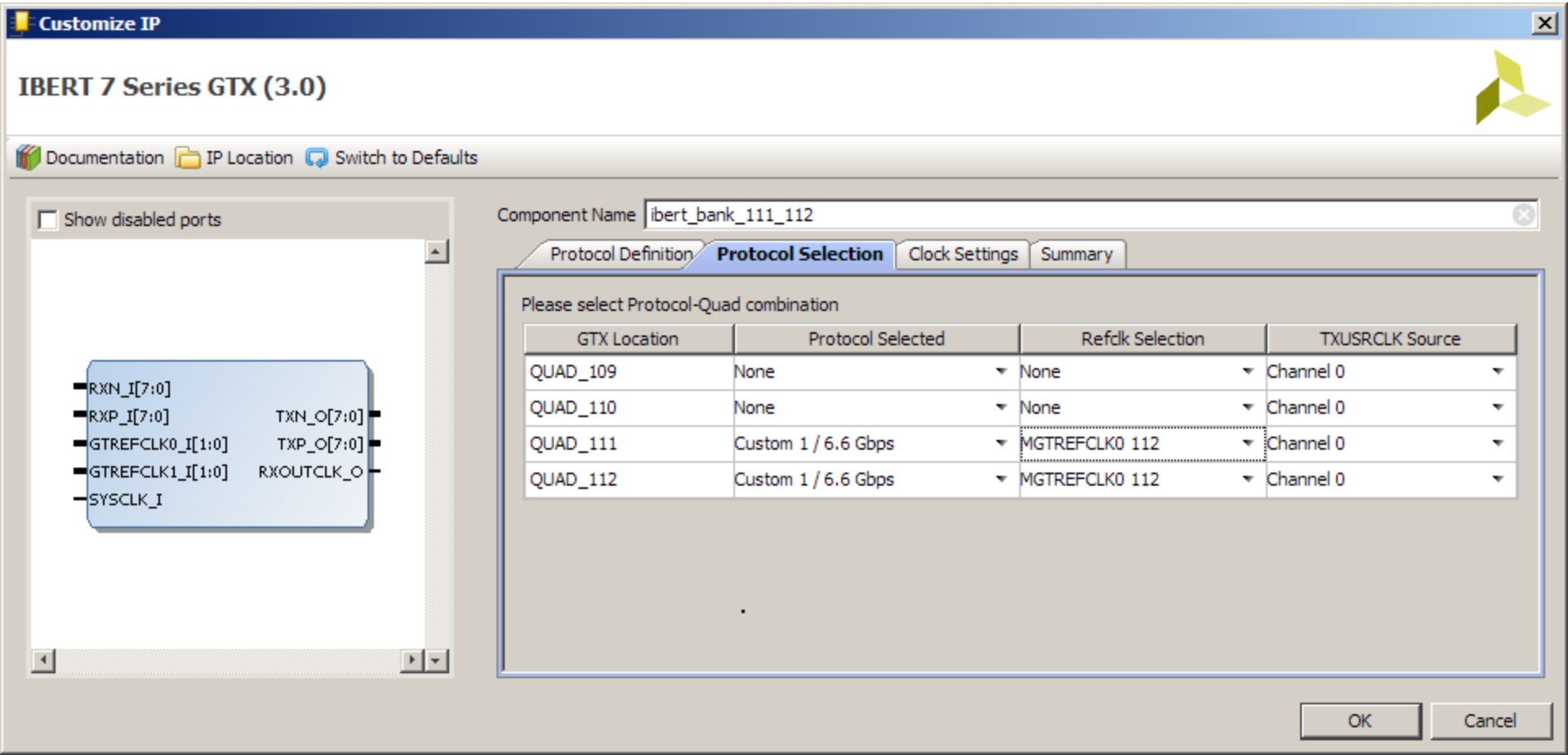
Create IBERT Design for Banks 111, 112

- Set the Component name: ibert_bank_111_112
- Under the Protocol Definition tab
  - Silicon Version: **General ES / Production**
  - Protocol: LineRate: **6.6**, DataWidth: **40** Refclk: **100.000** Quad Count: **2**



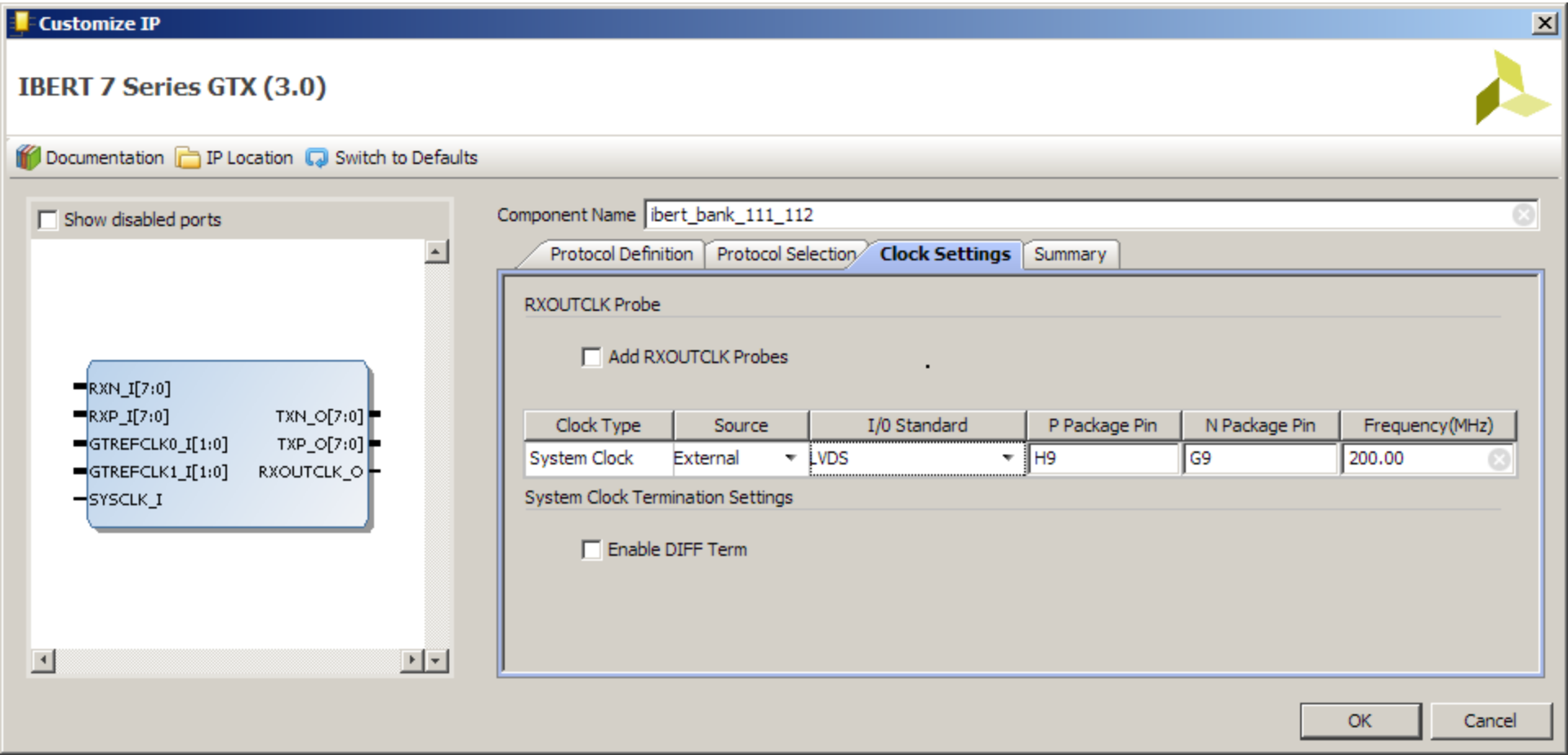
Create IBERT Design for Banks 111, 112

- Under the Protocol Selection tab
- Set QUAD_111 and QUAD_112 to
  - **Custom 1 / 6.6 Gbps**, and **MGTREFCLK0 112**



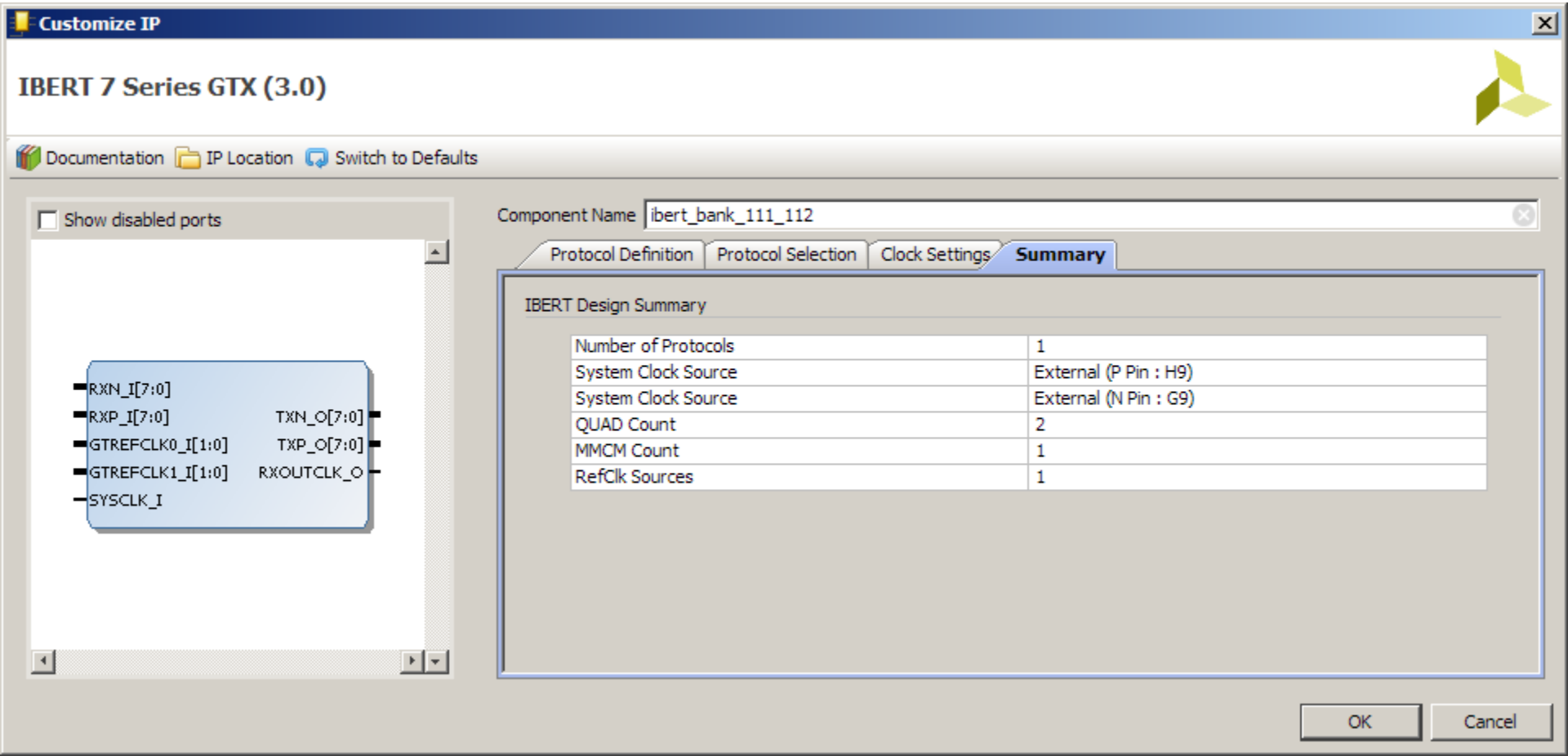
Create IBERT Design for Banks 111, 112

- **Under the Clock Settings tab, set the System Clock:**
  - **LVDS**, P Pin Location: **H9**, N Pin Location: **G9**



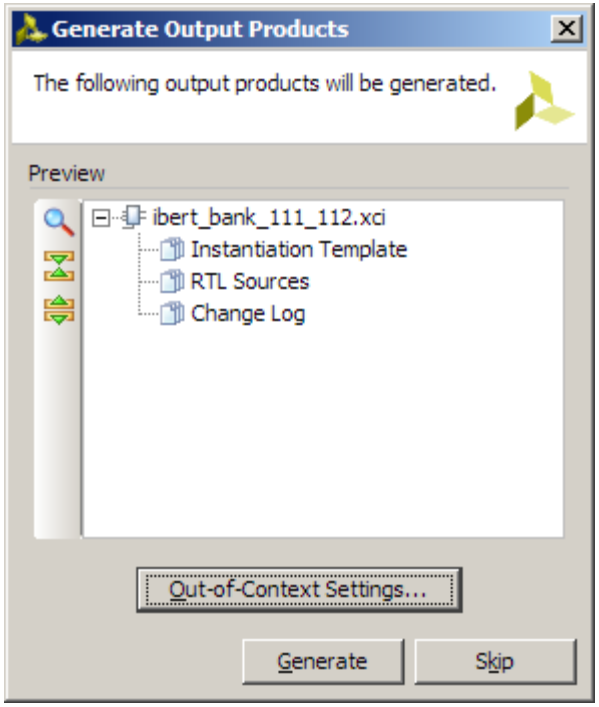
Create IBERT Design for Banks 111, 112

- Review the summary and click OK



Create IBERT Design for Banks 111, 112

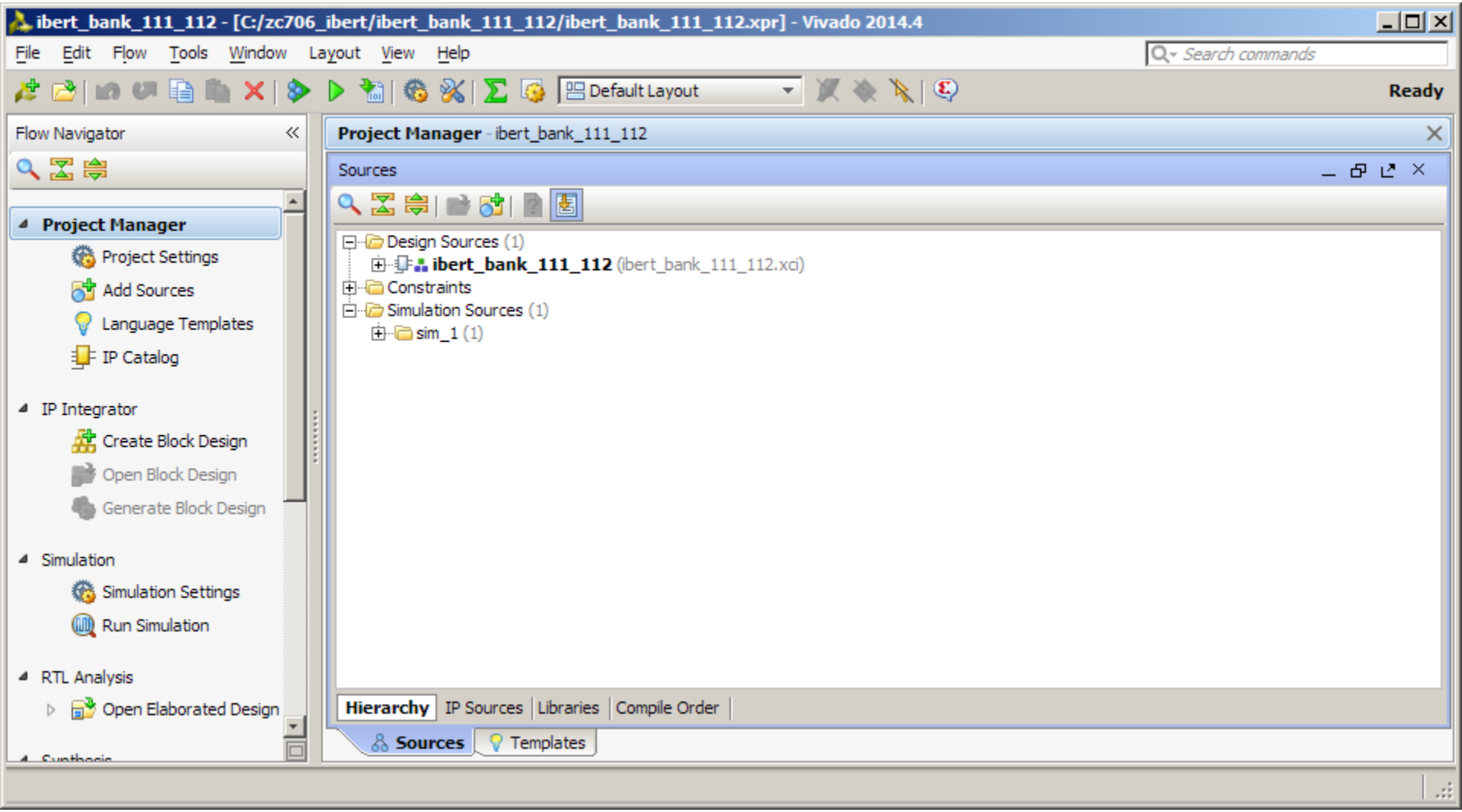
- Click Generate



Note: Presentation applies to the ZC706

Create IBERT Design for Banks 111, 112

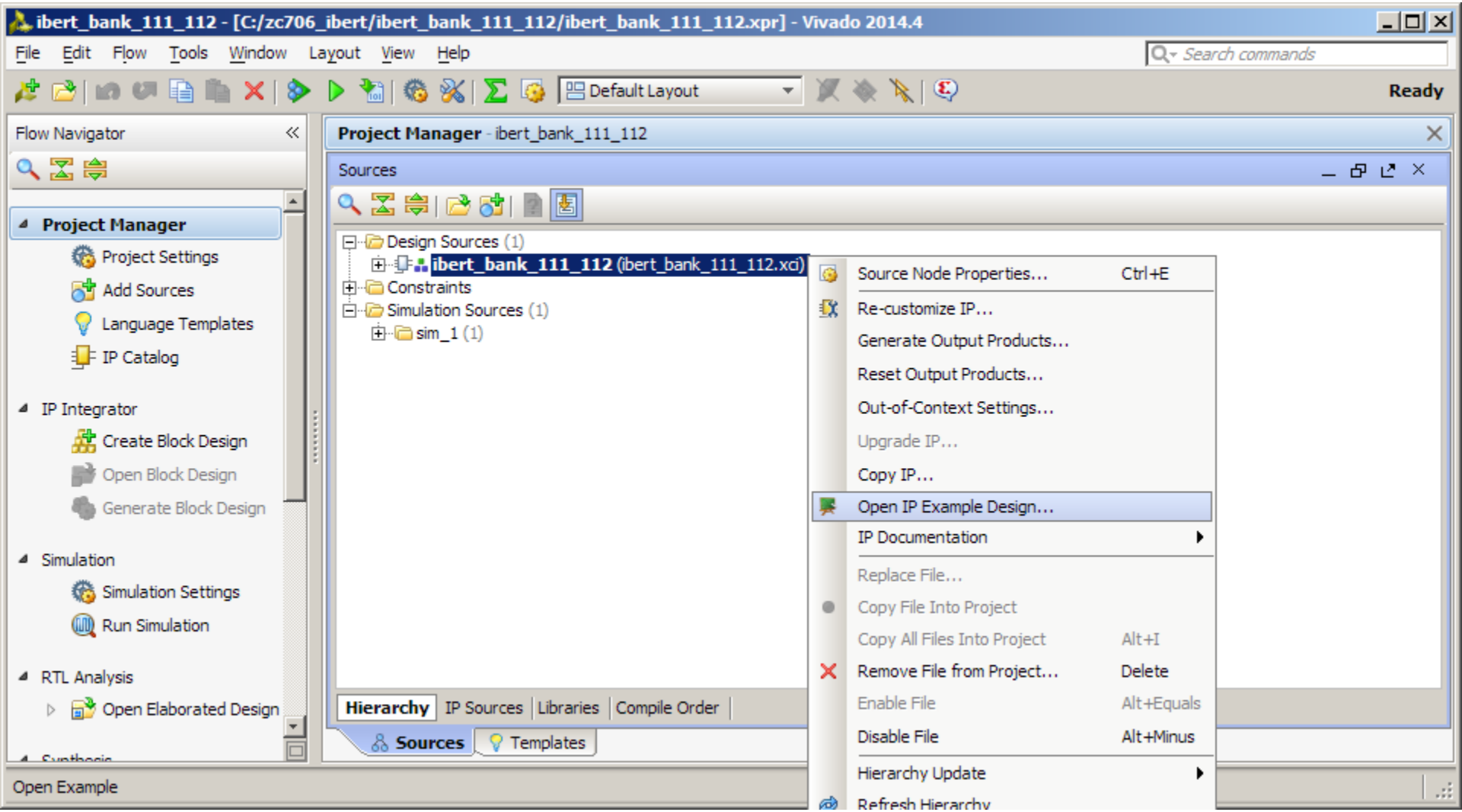
- Bank 111 & 112 IBERT design appears in Design Sources



Note: Presentation applies to the ZC706

Compile Example Design

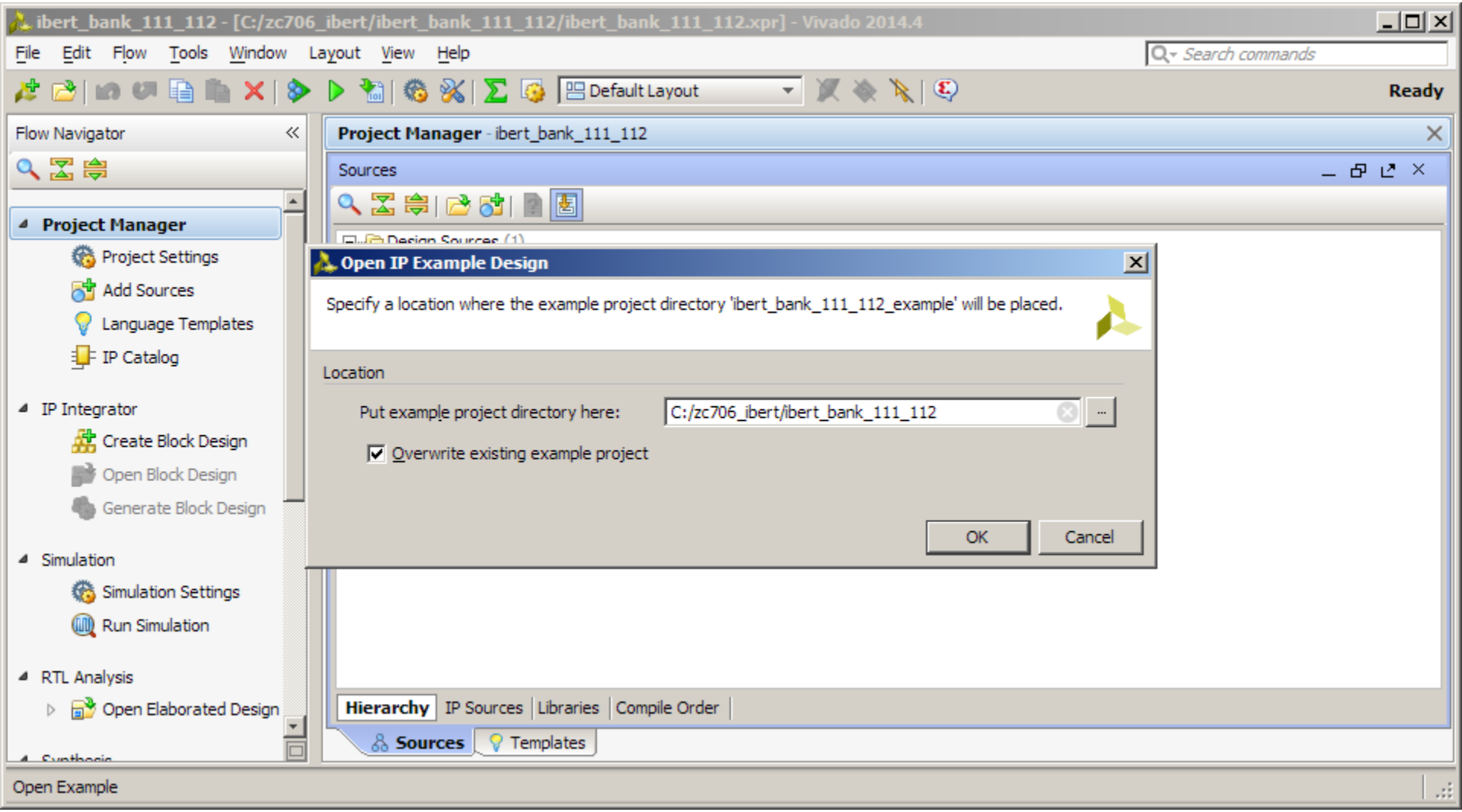
- Right click on ibert_bank_111_112 and select Open IP Example Design…



Note: Presentation applies to the ZC706

Compile Example Design

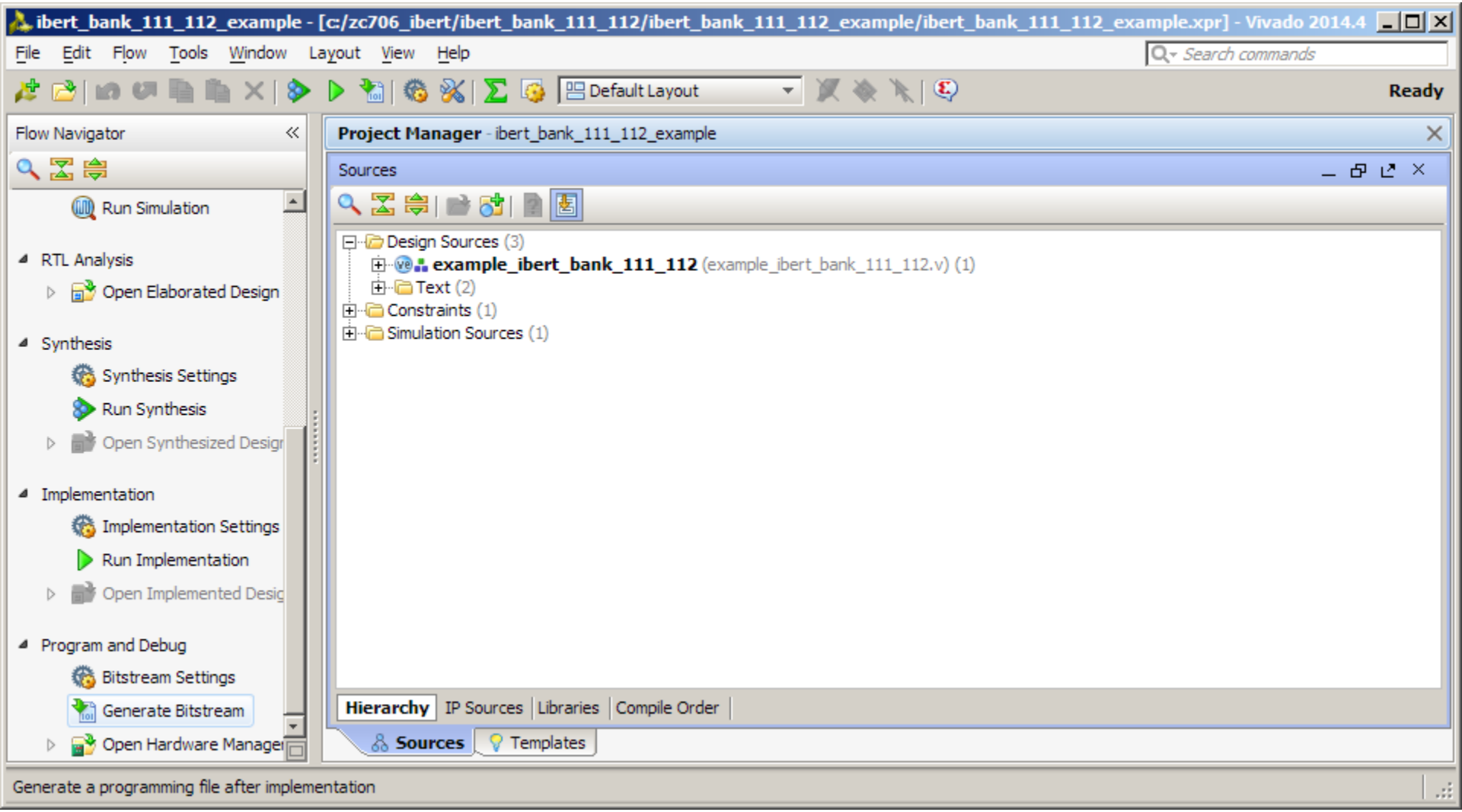
- Set the location to C:/zc706_ibert/ibert_bank_111_112 and click OK



Note: Presentation applies to the ZC706

Compile Example Design

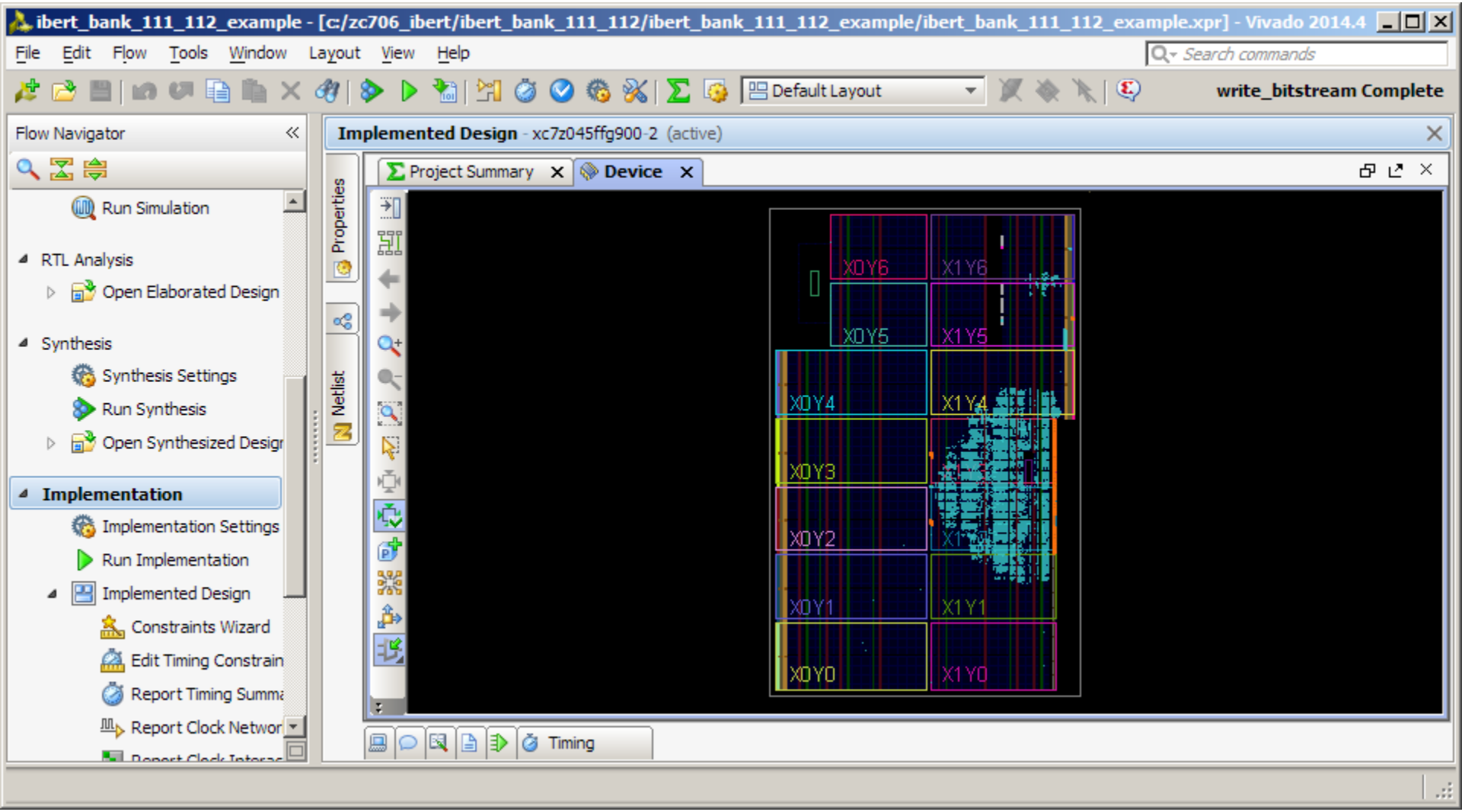
- A new project is created
- Click Generate Bitstream



Note: The original project window can be closed

Compile Example Design

- Open and view the Implemented Design



Note: Presentation applies to the ZC706

References

References

- **IBERT IP**
  - LogiCORE IP Integrated Bit Error Ratio Tester for 7 Series GTX – PG132
    - http://www.xilinx.com/support/documentation/ip_documentation/ibert_7series_gtx/v3_0/pg132-ibert-7series-gtx.pdf
- **Vivado Programming and Debugging**
  - Vivado Design Suite Programming and Debugging User Guide
    - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

- **Zynq-7000**
  - Zynq-7000 All Programmable SoC
    - http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm
- **ZC706 Documentation**
  - Zynq-7000 AP SoC ZC706 Evaluation Kit
    - http://www.xilinx.com/products/boards-and-kits/EK-Z7-ZC706-G.htm
  - ZC706 Getting Started Guide – UG961
    - http://www.xilinx.com/support/documentation/boards_and_kits/zc706/14_7/ug961-zc706-GSG.pdf
  - ZC706 User Guide – UG954
    - http://www.xilinx.com/support/documentation/boards_and_kits/zc706/ug954-zc706-eval-board-xc7z045-ap-soc.pdf