Product Change Notification PCN2002-04

CoolRunner™ XCR3064XL CPLD: Change in Wafer Fabrication Facility

April 1, 2002

Overview: This notification is to inform you of a change in the wafer fab facility for the XCR3064XL CoolRunner XPLA3 CPLD. The XCR3064XL will transition from a 0.35µm five-layer metal Flash CMOS process at the Philips MOSIV wafer fab in Nijmegen to a 0.35µm five-layer metal Flash CMOS process at UMC, Taiwan.

This change is being made to improve Xilinx's ability to support this product effectively, competitively, and to accommodate our customers' high volume demands.

Two other members of the XPLA3 family – XCR3128XL and XCR3256XL – are also fabricated at the Philips MOSIV plant, but are not scheduled for transition to the UMC facility at this time. A separate process change notification will be communicated at a later date if necessary. The remaining members of the family – XCR3032XL, XCR3384XL and XCR3512XL – have always been fabricated at the UMC fab using the same 0.35µm five-layer metal Flash CMOS process technology which will now be used to fabricate the XCR3064XL.

Upon availability of the production units from UMC in July 2002, customers may expect to receive the XCR3064XL device from either UMC or MOSIV until the MOSIV inventory is depleted.

The XCR3064XL devices fabricated at UMC exhibit some performance improvements. The following table lists the datasheet changes that occur as a result of the change in fabrication location:

Data sheet measurement	Current MOSIV spec	UMC spec
Write / erase cycles	1,000	10,000
V_{OH}	Min. of 2.4V when I_{OH} = -8 mA	No change when V_{CC} = 3.0 V to 3.6V Adding the following conditions: If V_{CC} = 2.7V to 3.0V, min = 2.0V If I_{OH} = -500µA, min = 90% V_{CC}
f_{SYSTEM}	6 ns Tpd = 145 MHz	6 ns Tpd = 175 MHz (no change to other speeds)
T_F	6 ns Tpd = 2.4 ns	6 ns Tpd = 1.2 ns (no change to other speeds)
T_{PCO}	6 ns Tpd = 6.5 ns	6 ns Tpd = 7.0 ns (no change to other speeds)
T_{PTCK}[1]	Not present	6 ns Tpd = 2.5 ns 7.5 ns Tpd = 2.7 ns 10 ns Tpd = 3.3 ns
T_{LOGI3} (Fold-back NAND delay)	6 ns Tpd = 6.0 ns 7.5 ns Tpd = 7.5 ns 10 ns Tpd = 9.5 ns	6 ns Tpd = 2.0 ns 7.5 ns Tpd = 2.5 ns 10 ns Tpd = 3.0 ns

[1]This parameter added to the XPLA3 Family timing model for T_{PCO} measurement. See the family data sheet (DS012) for timing model information.

Qualification Data: The following is the qualification data for the 0.35µm process at UMC:

Lot #	Part	Package	Test	Quantity	Hours/Cy	Fails	Status
X8522LT	XCR3032XL	VQ44	HTOL	80	24	0	continue
			@145°C		48	0	continue
					256	0	continue
					500	0	continue
					1000	0	complete
X0026LT	XCR3032XL	VQ44	HTOL	80	256	0	complete
			@145°C				
X8535HS	XCR3032XL	VQ44	HAST	76	100	0	complete
			@130°C/85%RH				
X8535TC	XCR3032XL	VQ44	Temp Cycle	76	200	0	continue
			@-65°C / +150°C		500	0	continue
			Condition C		1000	0	complete

Key Dates: Qualification samples of the XCR3064XL fabricated at UMC are available today. Use special ordering number SCD0771 to obtain these qualification samples. These qualification samples will be equivalent to the production devices of the XCR3064XL fabricated at UMC that will be shipping in July 2002. Product specifically manufactured on the MOSIV process at Philips can be ordered until June 28, 2002. Please contact your Xilinx Sales Representative to obtain qualification samples or production devices.

Traceability: These devices can be distinguished by a 3-letter code located on the second line of the package topmark in between the package/pin code and the datecode. The 3-letter code will be "BMN" for product manufactured at UMC, and "APN" for product manufactured at MOSIV. See example below.

Note: The original PCN issued on April 1, 2002, incorrectly referenced the 3-letter code for product manufactured at UMC as "BMN." The correct reference is "AMN." - July 23, 2002

Example of a package topmark:

	ACTUAL TOPMARK	DESCRIPTION
Line 1:	XCR3064XL™	Xilinx Device Type
Line 2:	VQ100AMN0240	VQ100 = Package Type A = Circuit Design Revision M = UMC Wafer Fab N = 0.35µm Fab Process 0240 = Date Code
Line 3:	F1130085A	Assembly Lot Number
Line 4:	6C	6 = Speed C = Grade

Response and Contact: Per JEDEC Standard JESD46B, customers should acknowledge receipt of the PCN within 30 days of delivery of the PCN. Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change. After acknowledgement, lack of additional response within the 90-day period constitutes acceptance of the change.

Please contact your Xilinx Sales Representative to obtain qualification samples or production devices. For additional information or questions, please send email to the Quality Assurance group at pcn@xilinx.com, or directly by fax at (408) 369-1718.