Clarification on Handling Unconnected V_{CCINT} Pins for Virtex Devices

PCN2004-12 (v1.0) August 9, 2004 Product/Process Change Notice - FYI

Overview

Previous versions of the Virtex™ data sheet were not specific about how to handle extra (unused) incremental V_{CCINT} pins that were designated as "unconnected". The latest data sheet documents the correct handling of the incremental V_{CCINT} pins (Virtex 2.5V FPGA Pinout Tables v2.8, July 19, 2002). Failure to properly handle incremental V_{CCINT} pins may result in incompatibility issues.

Description

For original Virtex devices (0.25µm 5-layer metal process), each V_{CCINT} die pad was connected directly to a V_{CCINT} ball on the package. For certain device/package combinations (as noted in Table 1), the die has fewer V_{CCINT} pads than there were V_{CCINT} balls on the package. The extra V_{CCINT} balls were not physically connected to the die and were designated as "unconnected". These extra V_{CCINT} package balls are referred to in this document as "incremental V_{CCINT} pins" and in the data sheet as "superset" or "bold" pins.

For newer Virtex devices (0.22/0.18µm 6-layer metal process, as described in PCN2000-08), all the V_{CCINT} pads on the die are connected to an internal package plane. This plane is also connected to all the designated V_{CCINT} balls on the package.

This change improves power distribution of the V_{CCINT} in the packages and prevents inadvertent cases where a V_{CCINT} ball was not connected as required, which can result in inadequate power support for sections of the device.

To maintain compatibility between devices, all incremental V_{CCINT} pins on the package (see Table 1) should either be

a) Connected to the V_{CCINT} plane of the board, or
b) Left unconnected (floating)

The incremental V_{CCINT} should not be used for functions other than those outlined above. Failure to do so might result in incompatibility issues between devices. The latest data sheet – Virtex 2.5V FPGA Pinout Tables (v2.8) clarifies how to handle the incremental V_{CCINT} pins.

The Virtex data sheets are available at:

http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=/Data+Sheets/FPGA+Device+Families/Virtex&iLanguageID=1

Products Affected

This scenario applies only to the device/package combination and incremental V_{CCINT} pins listed in the following table:

Device	Package	Incremental V_{CCINT} Pins
XCV300	BG432	B26, C7, F1, F30, AE29, AF1, AH8, AH24
XCV400	BG560	B12, C22, M3, N29, AB2, AB32, AJ13, AL22
XCV600	BG560	B12, C22, M3, N29, AB2, AB32, AJ13, AL22

Table 1 - Device/package combination and incremental VCCINT pins

Traceability

Virtex devices manufactured on the 0.25µm 5-layer metal process are designated with a process geometry code of “P”. Virtex devices manufactured on the 0.22/0.18µm 6-layer metal process are designated with a process geometry code of “S”. The Virtex devices with process geometry code of "S" contain the internal V_{CCINT} package plane.

Figure 1 shows package top-mark example and the location of the process geometry code.

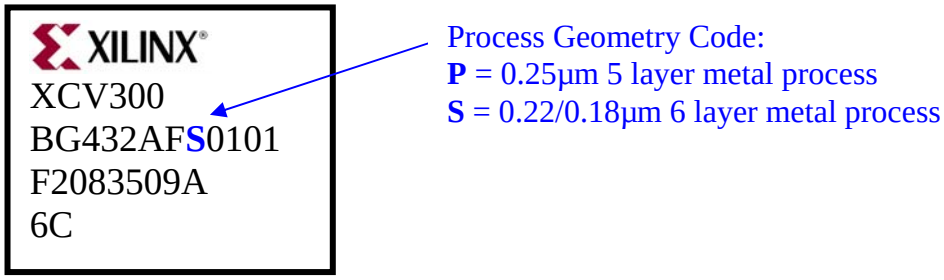

Figure 1 - Package top-mark example

Recommendation

No response is required to this PCN. For additional information or questions, please contact Xilinx Technical Support.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
8/9/04	1.0	Initial release.