



Circuit Revision Change to the XC9500XL Family of CPLD Devices

PCN2004-25 (v1.1) January 24, 2005

Product/Process Change Notice - FYI

Overview

The purpose of this notification is to communicate a circuit revision change to the XC9500XL™ family of CPLD devices.

Description

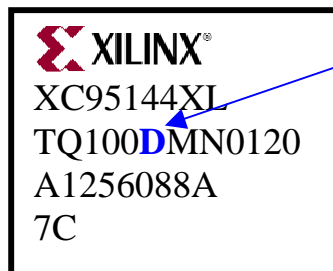
As part of the Xilinx continuous improvement process, a new circuit revision is being released for each member of the XC9500XL family of CPLD devices. This new circuit revision increases the tolerance of the configuration circuitry to non-monotonic power supply ramps and provides a more robust solution in customer applications. This revision is backward compatible to the revision C material that is currently shipping in production. The new circuit revision can be identified by design circuit revision code D (see *Traceability* below).

Products Affected

This change affects all package, temperature, and speed grade combinations of all XC9500XL family members – XC9536XL, XC9572XL, XC95144XL, and XC95288XL.

Traceability

The design circuit revision code on the package topmark can be found as shown below.



Design Circuit
Revision Code

Key Dates

See below for first production shipments by family member. Customers should expect to receive devices of both circuit revisions until inventory of the earlier circuit revision is depleted.

Family Member	First Production Shipments
XC9536XL	January 2005
XC9572XL	Late October 2004
XC95144XL	Late October 2004
XC95288XL	January 2005

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Recommendation

No response is required to this PCN. For additional information or questions, please contact [Xilinx Technical Support](#).

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/11/2004	1.0	Initial release.
01/24/2005	1.1	Remove reference to SCD0768 since these part numbers will not transition to circuit revision D.