Transition to Step 1 and New Package Substrate for Select Virtex-5 LXT and SXT FPGA Devices

Overview

The purpose of this notification is to communicate a transition to Step 1 and a 10-layer package substrate for select Virtex®-5 LXT and SXT FPGA devices.

Description

This notification includes the following changes to be implemented:

- **Introduction of Step 1:** Specific LXT and SXT devices will begin transitioning to a new mask revision, designated as Step 1, which will improve the CDM ESD performance. The current production silicon is designated as Step 0. The Step 1 devices are form, fit, function, and bitstream compatible with Step 0. (For information on the Xilinx Stepping Methodology, see Xilinx Answer 20947).
- **Package change:** LXT and SXT devices in packages greater than 1000 pins will begin transitioning to 10-layer package substrates, as part of the Xilinx material standardization for the Virtex-5 FPGA family. This change is backward-compatible with current production devices. This change will not affect the current package outline drawing.

Key Dates and Ordering Information

Key dates for this notice are detailed in Key Dates for Package Transition.

Table 1: **Key Dates for Package Transition**

Notification Date	Transition Period*	Implementation Date** (Cross-shipping starts)
December 31, 2007	January 1, 2008 - April 30, 2008	May 1, 2008

* If a qualification of the new material is necessary, customers can order samples of Step 1 10-layer devices by appending "S1" to the end of standard part numbers from January 1, 2008 through April 30, 2008.

** Starting from May 1, 2008, orders using standard part numbers will receive devices in either Step 0 or Step 1, 8-layer or 10-layer.

© Copyright 2007 - 2009 Xilinx, Inc. All Rights Reserved. XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

Products Affected

Table 2 summarizes the changes and example ordering codes for the affected LXT and SXT devices. This change applies to all speeds and grades for the devices listed in Summary of Affected Devices (with Example Ordering Codes).

Table 2: **Summary of Affected Devices (with Example Ordering Codes)**

Devices	Transitioning to Step 1?	Transitioning to 10-layer Package Substrate?	Prior to Transition Period Example Ordering Part No. (before Jan 2007)	During Transition Period Example Ordering Part No. (Jan 2007 to April 2008)	After Transition Period Example Ordering Part No. (after April 2008)
XC5VLX50T-FF(G)1136 XC5VLX85T-FF(G)1136 XC5VLX110T-FF(G)1136 XC5VLX110T-FF(G)1738 XC5VSX50T-FF(G)1136 XC5VSX95T-FF(G)1136	Yes	Yes	XC5VLX50T-1FF1136C (Step 0, 8-Layer)	XC5VLX50T-1FF1136C (Step 0, 8-Layer) XC5VLX50T-1FF1136CS1 (Step 1, 10-Layer)	XC5VLX50T-1FF1136C (Step 0 or Step 1, 8-Layer or 10-Layer) XC5VLX50T-1FF1136CS1 (Step 1, 10-Layer)
XC5VLX30T-FF(G)665 XC5VLX50T-FF(G)665 XC5VSX50T-FF(G)665	Yes	No	XC5VLX30T-1FF665C (Step 0, 8-Layer)	XC5VLX30T-1FF665C (Step 0, 8-Layer) XC5VLX30T-FF665CS1 (Step1, 8-Layer)	XC5VLX30T-1FF665C (Step 0 or Step 1, 8-Layer) XC5VLX30T-FF665CS1 (Step 1, 8-Layer)

Traceability

Step 1 10-layer devices can be ordered by appending "S1" to the end of the standard part number. Standard ordering part numbers may be fulfilled with either 8-layer or 10-layer substrates.

The top mark facilitates traceability.

Step 1 devices can be visually identified by the additional "1" at the end of the third line of the package top mark (see Example Top Mark).

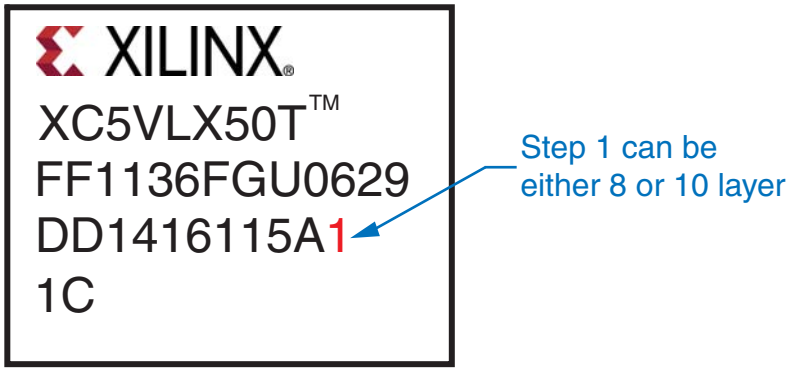

Figure 1: **Example Top Mark**

Response

Note: In accordance with JESD46-C, this change is deemed accepted by the customer if no acknowledgement is received within 30 days from this notice.

No response is required by this notice. For additional information or questions, please contact Xilinx Technical Support.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the MySupport website (http://www.xilinx.com/support). Register today and personalize your "MyAlerts" area to include Customer Notifications. This change provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Xilinx Answer Record 18683.

Additional Documentation

Below is a list of documents that are associated with this notice:

- Qualification Report (RPT091)
- FAQ: Implications of XCN07026 (XTP030)
- Xilinx Stepping Methodology (Answer Record 20947)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/24/07	1.0	Initial release.
03/11/08	1.0.1	Added Additional Documentation section.
06/15/09	1.0.2	Minor edit to remove XTP027 from the Additional Documentation section.
07/29/09	1.0.3	Update traceability top mark section to add additional clarification for Step 1 device.

Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN ("PRODUCTS") ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY OR PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.