Virtex-6: GTX User Guide, Data Sheet (SYSMON DCLK) and JTAG ID Changes

XCN10032 (v1.0) September 27, 2010 **Product Change Notice - For Your Information**

Overview

The purpose of this notification is to inform Xilinx customers of the following changes to the Virtex®-6 FPGA user guide, data sheet and JTAG revision codes:

- User Guide: GTX transceivers general guidance
- Data Sheet: System Monitor (SYSMON) DCLK data sheet change
- JTAG revision code: change for ongoing production enhancements

Description

The following general guidance is provided for the *Virtex-6 FPGA GTX Transceivers User Guide* (UG366) http://www.xilinx.com/support/documentation/user_guides/ug366.pdf.

GTX Transceiver Static Operating Behavior

The TXOUTCLK and RXRECCLK output ports might operate at reduced frequency in buffer bypass mode if conditions (1) and (2) persist for more than 15,000 cumulative hours at 65°C Tj, 2,500 cumulative hours at 85°C Tj, or 800 cumulative hours at 100°C Tj:

1. Power has been applied to VCCINT.
2. The device is in one of the following states:
    a. The FPGA is not configured
    b. The FPGA is configured, but the transceiver is un-instantiated
    c. The transceiver is instantiated, but no reference clock is toggling
    d. The transceiver is instantiated, but is held in reset or power-down

Reason for change

The reason of change is detailed in *Xilinx Answer Record 35055* http://www.xilinx.com/support/answers/35055.htm. For more information, refer to the sections titled 'TX Buffer Bypass' and 'RX Buffer Bypass' in the *Virtex-6 FPGA GTX Transceivers User Guide* for a description of the buffer bypass modes. The impact of reducing operating frequency is that it will result in increased bit error rates.

Products Affected

This change includes Virtex-6 LXT and SXT FPGA products, speed (-1, -2, -3, and -1L) and temperature grades (C and I) and Virtex-6 CXT FPGA products, speed (-1 and -2) and temperature grades (C and I). The products affected include all standard part numbers and specification control document (SCD) versions of the standard part numbers.

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The following changes have been made to the *Virtex-6 FPGA DC and Switching Characteristics Data Sheet* (DS152) http://www.xilinx.com/support/documentation/data_sheets/ds152.pdf.

System Monitor clock (SYSMON DCLK)

The System Monitor (SYSMON) clock (DCLK) maximum frequency specification is being revised from 250 MHz to 80 MHz in the *Virtex-6 FPGA DC and Switching Characteristics Data Sheet*.

This change will appear in "Analog-to-Digital Specification" of the data sheet. The parameter changing is **DRP Clock frequency (DCLK)**.

Reason for change

The System Monitor intermittently generates an incorrect analog-to-digital conversion when the SYSMON clock (DCLK) frequency is greater than 80MHz. All on-chip sensors and external channel monitoring is affected. For this reason the maximum frequency specification for DCLK is being revised down from 250MHz to 80MHz. All designs should be updated to use 80MHz maximum. The System Monitor specification is not impacted in any other way. For additional information, refer to *Xilinx Answer Record 36642* http://www.xilinx.com/support/answers/36642.htm.

Products Affected

This change includes Virtex-6 LXT and SXT FPGA products, speed (-1, -2, -3, and -1L) and temperature grades (C and I). The products affected include all standard part numbers and specification control document (SCD) versions of the standard part numbers.

The following changes have been made to the **JTAG ID revisions** for Virtex-6 devices:

JTAG ID revisions

The JTAG ID revision will change for Virtex-6 LXT, SXT and CXT FPGA devices as part of ongoing production enhancements.

The production JTAG ID revisions for each device are shown in Table 1 in the Additional Documentation section of this document.

Products Affected

This change includes all Virtex-6 LXT and SXT FPGA products, speed (-1, -2, -3, and -1L) and temperatures grade (C and I) and all Virtex-6 CXT FPGA products, speed (-1 and -2) and temperatures grade (C and I). The products affected include all standard part numbers and specification control document (SCD) versions of the standard part numbers. For instructions on how to read JTAG ID CODE, follow *Xilinx Answer Record 37579* http://www.xilinx.com/support/answers/37579.htm.

Products Affected

Refer to each item in the Description for products affected.

Key Dates and Ordering Information

These changes are effective upon this PCN release.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support http://www.xilinx.com/support/techsup/tappinfo.htm.

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Additional Documentation

Virtex-6 Production Errata:
http://www.xilinx.com/support/documentation/virtex-6.htm

DS152, *Virtex-6 FPGA DC and Switching Characteristics,* Data Sheet:
http://www.xilinx.com/support/documentation/data_sheets/ds152.pdf

UG366, *Virtex-6 FPGA GTX Transceivers,* User Guide:
http://www.xilinx.com/support/documentation/user_guides/ug366.pdf

Table 1: **JTAG ID Revision Codes for Production Devices**

Device	Production Devices
XC6VLX75T	JTAG ID revision=4 or JTAG ID revision=6
XC6VLX130T	JTAG ID revision=4 or JTAG ID revision=6
XC6VLX195T	JTAG ID revision=4 or JTAG ID revision=6
XC6VLX240T	JTAG ID revision=4 or JTAG ID revision=6
XC6VLX365T	JTAG ID revision=0 or JTAG ID revision=2
XC6VLX550T	JTAG ID revision=0 or JTAG ID revision=2
XC6VLX760	JTAG ID revision=2 or JTAG ID revision=4
XC6VSX315T	JTAG ID revision=4 or JTAG ID revision=6
XC6VSX475T	JTAG ID revision=4 or JTAG ID revision=6
XC6VCX75T	JTAG ID revision=4
XC6VCX130T	JTAG ID revision=2 or JTAG ID revision=4
XC6VCX195T	JTAG ID revision=4
XC6VCX240T	JTAG ID revision=2 or JTAG ID revision=4

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
9/27/10	1.0	Initial release.

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