Quality Alert – Virtex®-6 BRAM/FIFO Timing Issue

Overview

The ISE® 11.x, 12.x and 13.1 TRCE/Timing Analyzer tools do not correctly analyze certain control signals and address lines of the Virtex®-6 36Kb BRAM (RAMB36E1), 18Kb BRAM (RAMB18E1), and 18Kb FIFO (FIFO18E1) when used in SDP, TDP, or ECC modes, potentially resulting in unreported setup and hold time violations. The unreported violations may result in read and write errors in silicon and are not reported in the unconstrained path report section of the timing report.

Description

All aspect ratio configurations of the 36Kb BRAM (RAMB36E1), the 18Kb BRAM (RAMB18E1), the 36Kb FIFO (FIFO36E1) and the 18Kb FIFO (FIFO18E1) are affected by this issue.

All Virtex®-6 designs with these specific blocks must be reviewed to assess whether this issue affects the design. Designs created with timing analysis performed in ISE® 13.2 or later are not affected by this issue.

Previous architectures and 7-Series are not impacted by this issue.

As part of the resolution detailed, a new version of the Speedfile is included in ISE® 13.2 and the patches referenced in AR42444.

Products Affected

All Virtex®-6 devices with designs that use these specific blocks with timing analysis performed in ISE® 13.1 or previous software tools without available patches for this issue are affected.

Recommendations

Xilinx recommends that all affected designs have timing reanalyzed using the guidance provided in AR42444, or use ISE® 13.2 or later.

If it is determined that an existing design has timing failures that are unacceptable, the design must be re-implemented according to the recommendations in AR42444.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
July 07, 2011	1.0	Initial release.
July 08, 2011	1.1	Remove sentence ‘The 36Kb FIFO configuration is not affected’ and add the 36Kb FIFO (FIFO36E1) to the affected list.

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