

## Overview

The purpose of this notification is to communicate that Xilinx is transitioning to pin gate mold (PGM) in plastic ball grid array FG(G) and BG(G) packages. Xilinx's Assembly Suppliers are transitioning by the end of Jan, 2014. This notification applies to all XC Commercial (C) and Industrial (I) grade FPGA products.

## Description

Xilinx's Assembly Suppliers are transitioning from corner gate mold to pin gate mold for FG(G) and BG(G) packages. Suppliers are converting mature PBGA devices to PGM for improved productivity. PGM process is designed with the JEDEC compliant larger mold cap still meeting Xilinx's outer package dimensions.

In addition:

1. Minor Change in the Marking Template: PGM ejector pin will move to the center of the package while CGM ejector pin remains at the pin 1 indicator location. The new marking template with PGM & CGM will be applied to all of BG(G)256, FG(G)320, FG(G)400, FG(G)456, FG(G)484 and FG(G)676 devices packages as shown in [Figure 1](#).
2. Shipping Tray: change in the shipping tray for the 23mmx23mm PBGA packages. The new 23mmx23mm PBGA Daewon tray matrices are designed to be compatible with the current shipping trays, and will have the same X/Y tray dimensions. However, the new 23mmx23mm Daewon trays are non-stackable with current tray due to a slip lock feature. The new trays have larger cavity pocket at bottom of cell cavity that's designed for CGM and PGM (larger mold body). Xilinx recommends that customers not stack or mix the new Daewon trays with the current shipping trays. Please reference [Table 2](#) and [Figure 2](#) for clarification.

These changes have no effect on form, fit, function or reliability.

## Products Affected

This change affects all standard and specification control document (SCD) XC Commercial (C) and Industrial (I) grade devices listed in [Table 1](#).

Table 1: Affected FPGA devices family using PGM

Device	Package	Device	Package	Device	Package	Device	Package
XC95288XL	BG(G)256	XC2S600E *	FG(G)456	XC6SLX150	FG(G)484	XC3S4000	FG(G)676
XC3S1000	FG(G)320	XC2V1000 *	FG(G)456	XC6SLX150T	FG(G)484	XC3S5000	FG(G)676
XC3S1200E	FG(G)320	XC2V250 *	FG(G)456	XC6SLX25	FG(G)484	XC3SD1800A	FG(G)676
XC3S1500	FG(G)320	XC2V500 *	FG(G)456	XC6SLX25T	FG(G)484	XC3SD3400A	FG(G)676
XC3S1600E	FG(G)320	XC2VP2	FG(G)456	XC6SLX45	FG(G)484	XC6SLX100	FG(G)676
XC3S200A	FG(G)320	XC2VP4	FG(G)456	XC6SLX45T	FG(G)484	XC6SLX100T	FG(G)676
XC3S400	FG(G)320	XC2VP7	FG(G)456	XC6SLX75	FG(G)484	XC6SLX150	FG(G)676
XC3S400A	FG(G)320	XC3S1000	FG(G)456	XC6SLX75T	FG(G)484	XC6SLX150T	FG(G)676
XC3S500E	FG(G)320	XC3S1500	FG(G)456	XC2S400E *	FG(G)676	XC6SLX45	FG(G)676
XC3S1200E	FG(G)400	XC3S2000	FG(G)456	XC2S600E *	FG(G)676	XC6SLX75	FG(G)676
XC3S1600E	FG(G)400	XC3S400	FG(G)456	XC2V1500 *	FG(G)676	XC6SLX75T	FG(G)676
XC3S400A	FG(G)400	XCMECH	FG(G)456	XC2V2000 *	FG(G)676	XCE0102 *	FG(G)676
XC3S400AN	FG(G)400	XCV200E *	FG(G)456	XC2V3000 *	FG(G)676	XCE0103 *	FG(G)676
XC3S700A	FG(G)400	XCV300E *	FG(G)456	XC2VP20	FG(G)676	XCE0203	FG(G)676
XC2S100E *	FG(G)456	XC3S1400A	FG(G)484	XC2VP30	FG(G)676	XCMECH	FG(G)676
XC2S150	FG(G)456	XC3S1400AN	FG(G)484	XC2VP40	FG(G)676	XCV400E *	FG(G)676
XC2S150E *	FG(G)456	XC3S1600E	FG(G)484	XC3S1000	FG(G)676	XCV405E *	FG(G)676
XC2S200	FG(G)456	XC3S700A	FG(G)484	XC3S1400A	FG(G)676	XCV600E *	FG(G)676
XC2S200E *	FG(G)456	XC3S700AN	FG(G)484	XC3S1400AN	FG(G)676		
XC2S300E *	FG(G)456	XC6SLX100	FG(G)484	XC3S1500	FG(G)676		
XC2S400E *	FG(G)456	XC6SLX100T	FG(G)484	XC3S2000	FG(G)676		

\* Devices are under [XCN12026](#) PDN.

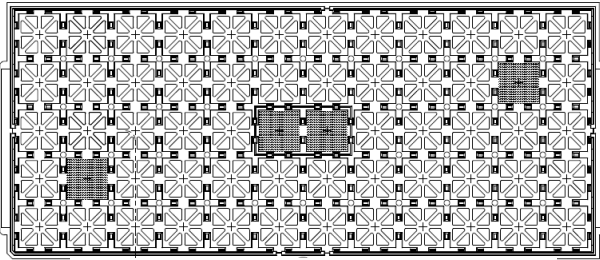
Below examples are for new making templates of both PGM & CGM.



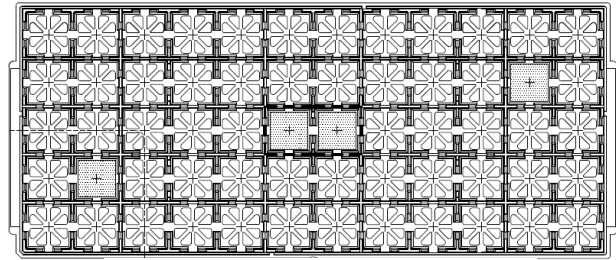
Figure 1: marking templates

Table 2: Tray Information

Tray Description	Current Tray		New Tray	
	Daewon Tray Part Number	Xilinx Drawing	Daewon Tray Part Number	Xilinx Drawing
JEDEC L/P PBGA TRAY (60 pockets) for 23x23mm pkg	1F1-2323-919 Rev. A	SIT0089	T0812012 Rev. B	SIT0148



Current Tray: 1F1-2323-919 Rev.A  
Vendor: Daewon



New Tray: T0812012 Rev.B  
Vendor: Daewon

Figure 2: Tray Details

## Key Dates and Ordering Information

Xilinx will begin to cross ship both PGM and CGM packages with the new marking template by Feb 1<sup>st</sup>, 2014.

## Qualification Data

Supplier's have previously qualified PGM packages and have been in production since 2009. Xilinx will perform additional qualification using Xilinx device/packages listed in [Table 3](#). Xilinx qualification data will be available per the schedule in [Table 4](#).

Table 3: Qualification Plan

Device	Package	Reliability Test	SS
XC6SLX100T	FGG676	PC3+TCB1000x	25 x 3lots
XC2VP40	FGG676	PC3+TCB1000x	25 x 3lots
XC3S5000	FGG676	PC3+TCB1000x	25 x 3lots

Table 4: Qualification Schedule

Package Type	Mold cavity type	Estimated Conditional Qualification Schedule	Estimated Production Release Schedule
Wire Bond FG(G) Package	Pin Gate mold	Jun 30 <sup>th</sup> ,2013	Feb 1 <sup>st</sup> , 2014

## Response

No response is required. For additional information or questions, please contact [Xilinx Technical Support](#).

**Important Notice:** Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (<http://www.xilinx.com/support>). Register today and personalize your “Documentation and Design Advisory Alerts” area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Answer Record 18683: <http://www.xilinx.com/support/answers/18683.htm>.

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## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/17/12	1.0	Initial release.
01/25/13	1.0.1	Minor update to add “PGM” to shipping tray under the description section.

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