



Spartan-6 FPGA BUFIO2 and BUFIO2_2CLK Primitives DIVIDE Attribute Allowed Values Change

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Product Change Notice

Overview

The purpose of this notification is to advise customers of a change to the supported values for the BUFIO2 and BUFIO2_2CLK primitives DIVIDE attribute for all Spartan®-6 FPGAs. This change affects all Spartan-6 FPGAs including Commercial/Industrial XC, Automotive XA, Defense-grade XQ, and all associated specification control document (SCD) devices.

Description

The BUFIO2 and BUFIO2_2CLK primitives DIVIDE attribute value of 2 is no longer supported. The previously allowed and changed set of supported values for the BUFIO2 and BUFIO2_2CLK primitives DIVIDE attribute are shown in Table 1.

Table 1: BUFIO2 and BUFIO2_2CLK Primitives DIVIDE Attribute Allowed Values Change

Primitive	DIVIDE Attribute	
	Previously Allowed Values	New Allowed Values
BUFIO2	1 ⁽¹⁾ , 2, 3, 4, 5, 6, 7, 8	1 ⁽¹⁾ , 3, 4, 5, 6, 7, 8
BUFIO2_2CLK	2 ⁽¹⁾ , 3, 4, 5, 6, 7, 8	3 ⁽¹⁾ , 4, 5, 6, 7, 8

Notes:

1. Default value.

Beginning with ISE® 14.6, an instance of the BUFIO2 or BUFIO2_2CLK primitive with DIVIDE=2 results in a DRC error.

The [UG382, Spartan-6 FPGA Clocking Resources User Guide](#), v1.8, will be updated with this change.

For additional information and work-arounds, refer to [Answer Record 56113](#), *Design Advisory for Spartan-6 BUFIO2, DIVIDE=2 Issue*.

LogiCORE IP Affected

The LogiCORE™ IP DisplayPort® v3.2 (or earlier) interconnect protocol implementation for Spartan-6 FPGAs uses the BUFIO2 with DIVIDE=2 to generate RXUSRCLK2 from the GTP receive clock.

Products Affected

This change affects all Spartan-6 FPGAs including Commercial/Industrial XC, Automotive XA, Defense-grade XQ, and all associated specification control document (SCD) devices.

Recommendations

Xilinx recommends reviewing designs for affected products and IP for instances of BUFIO2 or BUFIO2_2CLK with DIVIDE=2. All affected designs should follow guidance provided in [Answer Record 56113](#) (or [Answer Record 51964](#) for affected DisplayPort designs).

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Response

No response is required. For additional information or questions, please contact [Xilinx Technical Support](#).

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Additional Documentation

UG382, *Spartan-6 FPGA Clocking Resources User Guide*
http://www.xilinx.com/support/documentation/user_guides/ug382.pdf

Answer Record 56113, *Design Advisory for Spartan-6 BUFIO2, DIVIDE=2 Issue*
<http://www.xilinx.com/support/answers/56113.htm>

Answer Record 51964, *LogiCORE IP DisplayPort v3.2 - Clocking Structure for GTP 2-Byte Mode Interface*
<http://www.xilinx.com/support/answers/51964.htm>

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/13	1.0	Initial release.

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