Customer Update XCU099602

XC4000 Dual Layer Metal (DLM) to Triple Layer Metal (TLM) Design Considerations

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On January 1, 1997, Xilinx will start shipping the XC4000 devices manufactured in a 0.5 Triple Layer Metal (TLM) process. While every effort has been made to ensure 100% form fit and function compatibility between the previous Dual Layer Metal (DLM) material and the new TLM material, there are two known differences that the user should understand. After evaluation, these two known differences are believed to affect less than 1% of all designs.

Mode Pins Pull-Up Resistors

During configuration, the three mode pins (M0, M1, and M2) will have active internal pull-up resistors (the DLM devices do not activate Mode-pin pull-up resistors during configuration.) This change only affects XC4000 designs that use pull-down resistors on Mode pins, in order to establish a Low logic level during configuration. Such pull-down resistors must now be of a value of max 4.7 k ohm per Mode-pin. (Xilinx data book schematics have traditionally listed 5 k ohm, and some users have successfully used 10 k ohm in the past.)

Increased Supply Current When Writing Into RAM

When using CLBs as RAM, there will be an increase in supply current of 0.01 mA per CLB and MHz of Write Strobe (WS) activity. A CLB-RAM counts as one CLB, whether it is used as 16 x 1, 16 x 2, or 32 x 1 RAM.
This current becomes significant only when many CLBs are used as RAM, and are being written at a high rate:

- 100 CLBs @ 10 MHz WS: 10 mA of additional current
- 200 CLBs @ 30 MHz WS: 60 mA of additional current

This additional supply current is insignificant in most applications, and is often compensated by a generally slightly lower power consumption of the new TLM devices.
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