Spartan-II 2.5V FPGA Automotive IQ Product Family: Introduction and Ordering

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Product Specification

Introduction

The Spartan™-II 2.5V Field-Programmable Gate Array (FPGA) Automotive IQ product family gives users high performance, abundant logic resources, and a rich feature set. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1.

Spartan-II devices deliver more gates, I/Os, and features per Dollar/Euro than other FPGAs by combining advanced 0.18 µm process technology with a streamlined Virtex™-based architecture. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Guaranteed to meet full electrical specifications over T_J = –40°C to +125°C
- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex architecture
  - Unlimited reprogrammability
- System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Zero hold time simplifies system timing
- Fully supported by powerful Xilinx development system
  - Foundation™ ISE Series: Fully integrated software
  - Alliance Series™: For use with third-party tools
  - Fully automatic mapping, placement, and routing
- Refer to Spartan-II 2.5V FPGA Detailed Functional Description (DS001-2) for device functional description
- Other than the DC parameters listed, all other DC specifications are the same as referenced in the Spartan-II 2.5V FPGA DC and Switching Characteristics (DS001-3) data sheet
- Refer to Spartan-II 2.5V FPGA Pinout Tables (DS001-4) for all pin descriptions

Table 1: **Spartan-II FPGA Family Members**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	132	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	176	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	176	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

Notes:

1. All user I/O counts do not include the four global clock/user input pins. See details in Table 3, page 3.

DC Specifications

Absolute Maximum Ratings(1)

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND(2)		–0.5	3.0	V
V_{CCO}	Supply voltage relative to GND(2)		–0.5	4.0	V
V_{REF}	Input reference voltage		–0.5	3.6	V
V_{IN}	Input voltage relative to GND(3)	5V tolerant I/O(4)	–0.5	5.5	V
		No 5V tolerance(5)	–0.5	V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output	5V tolerant I/O(4)	–0.5	5.5	V
		No 5V tolerance(5)	–0.5	V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65	+150	°C
T_J	Junction temperature		-	+135	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. V_{IN} should not exceed V_{CCO} by more than 3.6V over extended periods of time (e.g., longer than a day).
4. Spartan-II I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the packaging Information on the Xilinx website.

Recommended Operating Conditions

Symbol	Description	Min	Max	Units
T_J	Junction temperature	–40	125	°C
V_{CCINT}	Supply voltage relative to GND(1,2)	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND(2,3)	1.4	3.6	V
T_{IN}	Input signal transition time(4)	-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). For every 50 mV reduction in V_{CCINT} below 2.375V (nominal V_{CCINT} – 5%), all delay parameters increase by 3%.
2. Supply voltages may be applied in any order desired.
3. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
4. Input and output measurement threshold is ~50% of V_{CCO}.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S15	-	60	mA
		XC2S30	-	115	mA
		XC2S50	-	125	mA
		XC2S100	-	140	mA
		XC2S150	-	165	mA
		XC2S200	-	200	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.

Spartan-II Product Availability

Table 2 shows the package and speed grades available for Spartan-II family devices. Table 3 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

Table 2: **Spartan-II Package and Speed Grade Availability**

	Pins	100	208	256	456	144
	Type	Plastic VQFP	Plastic PQFP	Fine Pitch BGA	Fine Pitch BGA	Plastic TQFP
Device	Code	VQ100	PQ208	FG256	FG456	TQ144
XC2S15	-5	Q	-	-	-	Q
XC2S30	-5	-	Q	-	-	Q
XC2S50	-5	-	Q	Q	-	Q
XC2S100	-5	-	Q	Q	-	Q
XC2S150	-5	-	Q	Q	-	-
XC2S200	-5	-	Q	-	Q	-

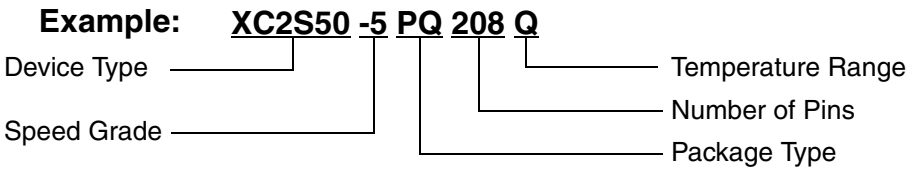
Notes:
1. Q= Automotive IQ, T_J = –40°C to +125°C.

Table 3: **Spartan-II User I/O Chart(1)**

Device	Maximum User I/O	Available User I/O According to Package Type				
		VQ100	TQ144	PQ208	FG256	FG456
XC2S15	86	60	86	-	-	-
XC2S30	132	-	92	132	-	-
XC2S50	176	-	92	140	176	-
XC2S100	176	-	92	140	176	-
XC2S150	176	-	-	140	176	-
XC2S200	284	-	-	140	-	284

Notes:
1. All user I/O counts do not include the four global clock/user input pins.

Ordering Information



Device Ordering Options

Device
XC2S15
XC2S30
XC2S50
XC2S100
XC2S150
XC2S200

Speed Grade	
-5	Standard Performance

Number of Pins / Package Type	
VQ100	100-pin Very Thin Plastic QFP
TQ144	144-pin Plastic Thin QFP
PQ208	208-pin Plastic QFP
FG256	256-ball Fine Pitch BGA
FG456	456-ball Fine Pitch BGA

Temperature Range (T_J)	
Q = Automotive IQ	–40°C to +125°C

Revision History

Version No.	Date	Description
1.0	06/17/2002	Initial Xilinx release.
1.1	11/26/2002	Updated Max User I/O in Table 1 and Table 3 for XC2S100 and XC2S150: changed to 176.
1.2	02/14/2003	Added references to Spartan-II data sheet, added DC Characteristics Over Operating Conditions table.
1.3	05/21/2004	Added VQ100 to Table 2 and Table 3. Added VQ100 to Ordering Information.
1.4	10/18/2004	Added "Not to be used in new designs" watermark; moved to "Mature Products"
2.0	08/09/2013	This product is obsolete/discontinued per XCN11010.

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