

Features

- Guaranteed to meet full electrical specifications over $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
- System frequency up to 100 MHz (10 ns)
- Available in small footprint packages
- Optimized for high-performance 3.3V systems
 - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals — ideal for multi-voltage system interfacing and level shifting
 - Technology: 0.35 μm CMOS process
- Advanced system features
 - In-system programmable enabling higher system reliability through reduced handling and reducing production programming times
 - Superior pin-locking and routability with FastCONNECT™ II switch matrix allowing for multiple design iterations without board re-spins
 - Input hysteresis on all user and boundary-scan pin inputs to reduce noise on input signals
 - Bus-hold circuitry on all user pin inputs which reduces cost associated with pull-up resistors and reduces bus loading
 - Full IEEE Standard 1149.1 boundary-scan (JTAG) for in-system device testing
 - Fast concurrent programming
- Slew rate control on individual outputs for reducing EMI generation
- Refer to XC9500XL Family data sheet (DS054) for architecture description
- Refer to XC9536XL data sheet (DS058) and XC9572XL

data sheet (DS057) for pin tables

Description

The XC9500XL 3.3V CPLD Automotive IQ product family is targeted for leading-edge, high-performance, low-voltage extended industrial (-40°C to $+125^\circ\text{C}$) applications.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in the XC9500XL device can be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC} , the following equation may be used:

$$I_{CC} \text{ (mA)} = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045 \text{ mA/MHz}) f$$

where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Table 1: XC9500XL Device Family

Device	Macrocells	Usable Gates	Registers	f_{SYSTEM} (MHz)
XC9536XL	36	800	36	100
XC9572XL	72	1,600	72	100

Table 2: XC9500XL Packages and User I/O Pins (not including four dedicated JTAG pins)

Device	VQ44	VQ64	TQ100
XC9536XL	34	36	-
XC9572XL	34	52	72

Absolute Maximum Ratings⁽¹⁾

Symbol	Description	Min.	Max.	Units
V_{CC}	Supply voltage relative to GND	-0.5	4.0	V
V_{IN}	Input voltage relative to GND ⁽²⁾	-0.5	5.5	V
V_{TS}	Voltage applied to 3-state output ⁽²⁾	-0.5	5.5	V
T_{STG}	Storage temperature (ambient)	-65	+150	°C
T_J	Junction temperature	-	+150	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- For soldering guidelines, see the Package Information on the Xilinx website.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
T_A	Ambient temperature	-40	+125	°C
V_{CCINT}	Supply voltage for internal logic and input buffers	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation	3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation	2.3	2.7	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	5.5	V
V_O	Output voltage	0	V_{CCIO}	V

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance) @ $T_A = 70^\circ\text{C}$	10,000	-	Cycles

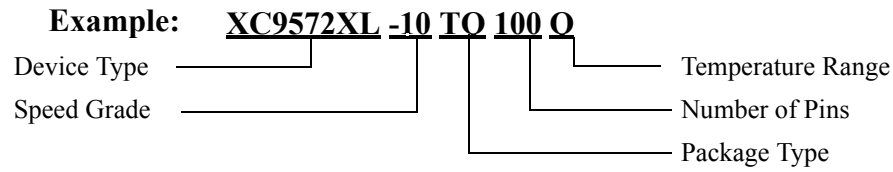
Component Availability

Pins		44	64	100
Type		Plastic VQFP	Plastic VQFP	Plastic TQFP
Code		VQ44	VQ64	TQ100
XC9536XL	-10	Q	Q	-
XC9572XL	-10	Q	Q	Q

Notes:

- Q = Automotive IQ ($T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$).

Ordering Information



Device Ordering Options

Device	Speed		Package		Temperature	
XC9536XL	-10	10 ns pin-to-pin delay	VQ44	44-pin Quad Flat Pack (VQFP)	Q = Automotive IQ	T _A = -40°C to +125°C
XC9572XL			VQ64	64-pin Quad Flat Pack (VQFP)		
			TQ100	100-pin Thin Quad Flat Pack (TQFP)		

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/17/02	1.0	Initial Xilinx release.
07/17/02	1.1	Updated N _{PE} Quality and Reliability specification.
02/03/03	1.2	Added reference to XC9500XL, XC9536XL, and XC9572XL data sheets.
05/17/04	1.3	Updated the VQ44 column of Table 2 and the Component Availability table on page 2.