Important Product Information: Do Not Discard

XC18V00 PROM Errata and Deviations from XC18V00 Data Sheet

DS026-E01 (v1.1) March 10, 2004 **Errata Notice**

These errata apply ONLY to XC18V00 PROMs. These errata DO NOT apply to any other PROMs. If using a different PROM, check for errata specific to that device.

Thank you for your interest in the enclosed XC18V00 devices. Although Xilinx has made every effort to ensure that these devices are of the highest possible quality, these devices are subject to the limitations described in the following errata. Please note that while these errata will not affect most customer applications, we recommend that you review these errata and the deviations from the published data sheets to ensure that the enclosed unit(s) meet(s) your application requirements.

Obtaining the Most Recent Version of This Document

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Devices Affected by These Errata

These errata apply only to the following part numbers with the topmark “ART” (Table 1).

Device Types	XC18V512PC20C, XC18V512SO20C, XC18V512VQ44C, XC18V01PC20C, XC18V01SO20C, XC18V01VQ44C, XC18V02PC44C, XC18V02VQ44C, XC18V04PC44C, XC18V04VQ44C
Packages	VQ44, PC44, PC20, SO20
Date Codes	All

Table 1: **Devices Affected**

How to Identify an Affected Device

These errata affect the above part numbers with topmarking “ART” (see examples in Table 2) and specific IDCODEs described in Table 3.

Sample topmark for the **44-pin VQFP and PLCC** Packages	Sample topmark for the **20-pin SOIC** Package	Sample topmark for the **20-pin PLCC** Package
		

Table 2: **Examples of Topmarks**

Device	IDCODE
XC18V512	05033093h
XC18V01	05034093h
XC18V02	05035093h
XC18V04	05036093h

Table 3: **IDCODEs Affected**

Operational Guidelines

1. Follow the data sheet to ensure that an external 4.7 KΩ (or lower) resistor is connected to the PROM’s OE/RESET# pin and the FPGA’s INIT# pin.
2. When using FPGA DONE to drive PROM CE#, make sure that the signal is within the specification and has a fast rise and fall time. When the FPGA DONE signal is used to light an LED and also drive the PROM CE#, use an external buffer to drive the LED.
3. Use a Master mode FPGA CCLK pin as the configuration CLK source instead of an external free-running clock.

Important Product Information: Intermittent Configuration Failure

Overview

Under certain conditions, the affected PROM devices will intermittently fail to configure a Xilinx FPGA(s). The data in the PROM is NOT affected, because the cause is only related to the improper synchronization of the configuration signals CCLK, OE/RESET#, and CE#. In most applications, customers will not be affected by these errata. The following matrix (Table 4) summarizes the customer's exposure to the phenomenon—conditions that lead to an intermittent configuration failure and symptoms observed during a failure.

Conditions → / Symptoms ↓		External Free-Running Clock Driving CCLK	FPGA Sourced Clock Driving CCLK			
			No pull-up on OE/RESET# (INIT#)		*Pull-up on OE/RESET# (INIT#)*	
			LED on CE# (DONE)	*No LED on CE# (DONE)*	*LED on CE# (DONE)*	*No LED on CE# (DONE)*
Rotated Bits Pattern	*Serial Bitstream*	√	√	√	√	
	Parallel Bitstream					
Extra 32 Bits Pattern	*SpartanXL or earlier XC4K or earlier*	√				
	Spartan-II or later Virtex or later					
Missing 32 Bits Pattern		√				

√ indicates exposure to configuration failure

Table 4: **Failure Exposure Matrix**

Implications

Most customers will not be affected by these errata, because the majority of all configuration applications use the FPGA's clock source to drive the CCLK signal (Master-Serial or Master-Parallel Configuration Modes) and follow the "Operational Guidelines" (listed above).

In a very few cases, when customers are using an external free-running clock to drive the CCLK signal (Slave-Serial or Slave-Parallel Configuration Modes), there is no application work-around that will avoid exposure to the phenomenon. Therefore, customers who are using an external free-running clock need to convert their ordering code to SCD0799. This will ensure that they will not receive affected devices identified in Table1, Table 2, and Table 3.

Conditions Leading to Intermittent Configuration Failure

This phenomenon is inherent in every device identified in Table 1, Table 2, and Table 3. Any of the following conditions (or any combination thereof) will lead to intermittent configuration failure:

- A slow ramp of the OE/RESET# (INIT#) signal. As specified in the data sheet, an external resistor of 4.7KΩ (or lower) is required to quickly pull up the FPGA INIT and PROM OE/RESET# signal line. If the FPGA INIT and PROM OE/RESET# signal line rises too slowly, then system noise might corrupt the PROM's internal address counters, thus keeping the FPGA from configuring properly.
- A staircase voltage of the CE# (DONE) signal. As specified in the FPGA data sheet, do not exceed 12 mA sink current on the FPGA DONE pin. Beware of LED driving circuits. Using DONE

to drive the LED and the PROM CE# pin directly (unbuffered) exceeds this specification. This also affects the FPGA driveDONE option.

- When the FPGA V_{CC} powers up after the PROM V_{CC}, the CE#-DONE and OE/RESET#-INIT signals may transition slowly (while the FPGA is powering up and before these signals are pulled low by the FPGA).
- A configuration design that utilizes a free-running clock.

Slow Ramp of the OE/RESET# (INIT#) Signal

A pull-up resistor is required to properly propagate this signal through the PROM (Figure 1). Figure 2 shows a clean OE/RESET# (INIT#) signal. However, a slow ramp could potentially allow system noise to propagate through the PROM's input buffer (Figure 3), thus creating short reset pulses that might cause the internal circuits to get out of sync. The observed failure rate ranges from 1% to 5% of configuration cycles.

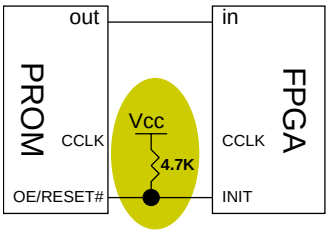


Figure 1: 4.7KΩ Pull-Up Required

Figure 2: OE/RESET# (INIT#) with Pull-Up Resistor

Figure 3: OE/RESET# (INIT#) without Pull-Up Resistor

Recommendation:

Follow the data sheet to ensure that an external 4.7KΩ (or lower) resistor is connected to the PROM's OE/RESET# pin and the FPGA's INIT pin. Ensure that the FPGA T_{ICCK} specification is met (500ns). This translates to a T_{RISE} and T_{FALL} time of 500 ns for the PROM's OE/RESET# signal.

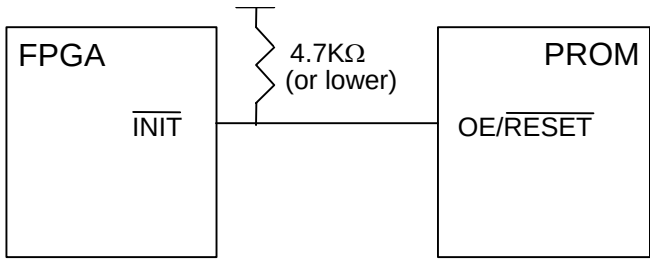


Figure 4: Recommended Resistor Value

Staircase Voltage of the CE# (DONE) Signal

The FPGA has a sink current specification of 12 mA that is exceeded when an unbuffered LED is tied to the CE# (DONE) signal (Figure 5). In this scenario, the CE# (DONE) signal is held at an intermediate voltage level that mimics multiple input pulses (Figure 7). These pulses propagate through the PROM and cause the internal circuits to get out of sync. The observed failure rate is up to 50% of configuration cycles. Figure 6 shows a clean CE# (DONE) signal when it is not tied to an LED.

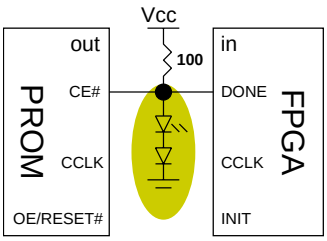


Figure 5: Unbuffered LED

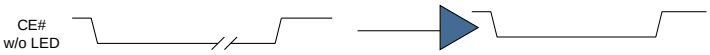


Figure 6: CE# (DONE) without LED

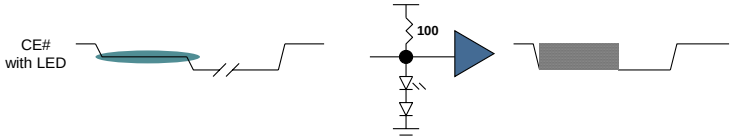


Figure 7: CE# (DONE) with an Unbuffered LED

Recommendation:

When using FPGA DONE to drive PROM CE# (to reduce standby power), make sure that the signal is within the specification and has a fast rise and fall time. Use an external buffer to drive any LED (Figure 8). If DONE is not used to drive CE#, it can be connected to an LED (Figure 9).

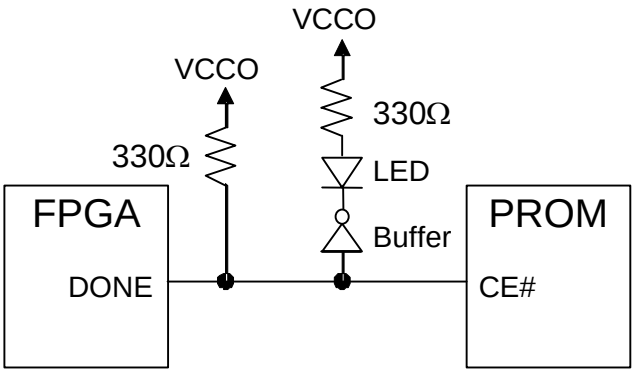


Figure 8: (LED with Buffer Circuit)

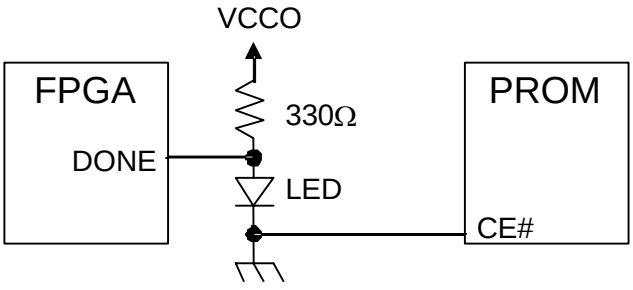


Figure 9: (Unbuffered LED)

When the FPGA V_{CC} powers up after the PROM V_{CC}

Recommendations:

1. If the FPGA cannot be powered up before the PROM, ensure that the INIT signal transitions Low before the DONE signal during FPGA power-up. One way to accomplish this is to use a lower-resistance pull-up on DONE and a higher-resistance pull-up on INIT. For example, tie the DONE signal to a 330Ω pull-up resistor and INIT to a 3.3KΩ pull-up resistor.
2. Another alternative is to disconnect the FPGA DONE signal from the PROM CE#, and connect CE# to Ground. To prevent contention on the configuration data line(s) when the PROM CE# is connected to Ground, either the FPGA design must drive the FPGA INIT# constantly Low (therefore driving the PROM OE/RESET# Low), or the FPGA design must not use the FPGA configuration data pins (DIN or D[0-7]) that are connected to the PROM.

Configuration System that Utilizes a Free-Running Clock

In most applications, the FPGA sources the CCLK signal, which synchronizes with the CE# (DONE) and OE/RESET# (INIT#) signals. However, in an asynchronous system (Figure 10), meaning when an external free-running clock drives the configuration clock signal (CCLK), there is a possibility that a missed or extra pulse (or pulses) can be interpreted by the PROM's internal counters as CCLK transitions while the OE/RESET# (INIT#) signal is in its intermediate phase (Figure 11). The observed failure rate ranges from 0.1% to 1% of configuration cycles.

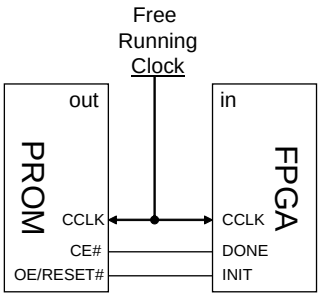


Figure 10: Asynchronous System

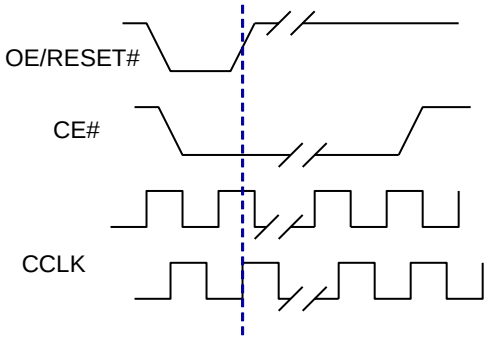


Figure 11: CCLK and OE/RESET# Collision

Recommendation:

There is no application work-around that will avoid exposure to the phenomenon when a free running clock is used. Therefore, customers who are using an external free-running clock need to convert their ordering code to SCD0799; this will ensure that they will not receive affected devices identified in Table1, Table 2, and Table 3.

Explanation of Symptoms and Root Cause

Rotated Bit Pattern

A Rotated Bit Pattern occurs when the Bit Counter and the Div8 circuit (Figure 12) becomes desynchronized. Data bits within a byte will be consistently rotated, byte by byte (Figure 13). Table 4 (above) summarizes the conditions where a Rotate Bit Pattern can occur.

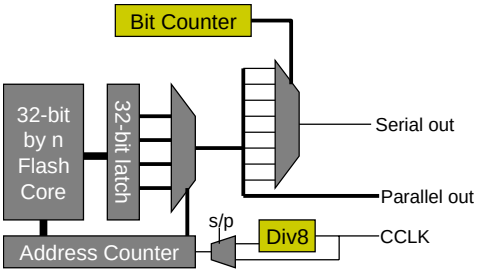
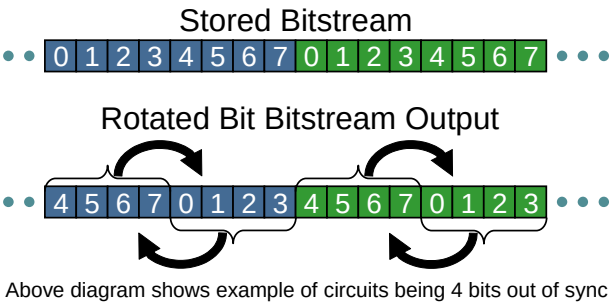


Figure 12: **Counter Circuits**



Above diagram shows example of circuits being 4 bits out of sync

Figure 13: **Example of Rotated Bit Pattern**

Extra 32 Bits Pattern

The Address Counter misses the first increment and repeats the first 32 bits. Table 4 (above) summarizes the conditions where an Extra 32 Bits pattern can occur.

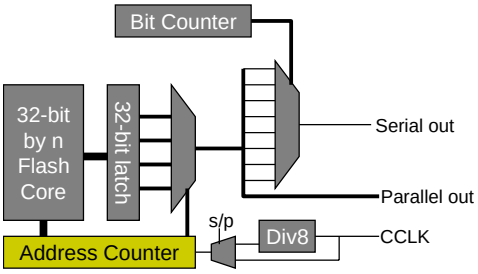


Figure 14: Counter Circuits

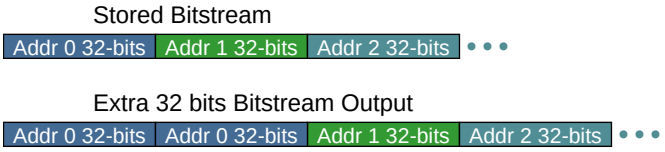


Figure 15: Example of an Extra 32 Bits Pattern

Missing 32 Bits Pattern

The Address Counter increments more than once and misses the second 32 bits. Table 4 (above) summarizes the conditions where a Missing 32 Bits pattern can occur.

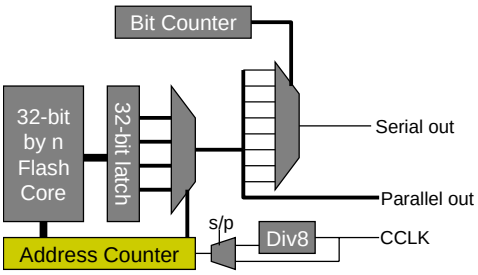


Figure 16: **Counter Circuits**

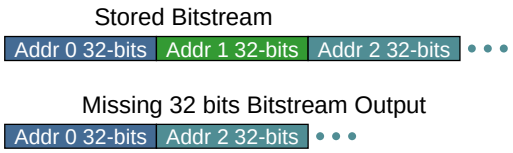


Figure 17: **Example of a Missing 32 Bits Pattern**

Design Fixes

As discussed above, most customers will not be affected by these errata. Unaffected customers, those who use the FPGA's clock source to drive the CCLK signal (Master-Serial & Master-Parallel Configuration Modes) and follow the "Operational Guidelines," should continue using the current devices. However, for those few customers who are affected by these errata, several fixes for the root cause are being implemented. Table 5 summarizes these fixes. Production devices from the new mask revision will be available by the middle of calendar year 2004, at which time Xilinx will issue a PCN to detail the changes and how affected customers can order the new mask revision devices.

		FIXES			
		Add hysteresis to OE/RESET# and CE# input buffers	Re-synchronize bit and byte (div8) counters at each byte increment	Synchronize internal reset to configuration clock	Suppress re-initiation of internal reset/pre-load while a reset/pre-load is in progress
Symptoms	Rotated Bits Pattern	√	√		√
	Extra 32 Bits Pattern			√	
	Missing 32 Bits Pattern			√	
Conditions	Slow Ramp OE/RESET# (INIT#)	√	√		√
	Staircase Voltage of CE# (DONE)	√	√		√
	External Free Running Clock			√	

Table 5: **Summary of Design Fixes**

Additional Questions or Clarifications

If additional questions arise or clarifications are needed regarding these errata, please contact your local Xilinx field application engineer (FAE) or sales representative. For the phone number in your area, see www.xilinx.com/support/services/contact_info.htm.

Any feedback with regard to these errata can be e-mailed to qa_com@xilinx.com.