Important Product Information

XCF08P, XCF16P, and XCF32P PROM Engineering Sample Errata and Deviations from the Platform Flash PROM Data Sheet

Dear Xilinx Customer,

Thank you for your interest in the enclosed Platform Flash PROM XCF00P Engineering Sample (ES) devices. Although Xilinx has made every effort to ensure that these devices are of the highest possible quality, these devices are subject to the limitations described in the following errata. Please review these errata to ensure that the enclosed unit(s) meet your application requirements.

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Devices Affected by These Errata

These errata apply only to engineering samples of the XCF00P PROM, as shown in Table 1.

Table 1. XCF00P Platform Flash PROM Engineering Samples Affected by These Errata.

Device Types:	XCF08PFS48CES, XCF16PFS48CES, XCF32PFS48CES, XCF08PVO48CES, XCF16PVO48CES, XCF32PVO48CES
Packages:	FS48, VO48
Temperature Grades:	All CES
Date Codes:	All

How to Identify an Affected Device

These errata affect all Platform Flash PROMs marked as XCF08P, XCF16P, or XCF32P device types with an Engineering Sample designation (indicated by an “ES” marking) and with JTAG IDCODE revision code 0000 (binary).

Operational Guidelines

Software/Programming

1. iMPACT 6.1.03i (or later) is required.
2. Xilinx Parallel Cable IV (PC4) operation at 5 MHz is required.

Device Application

1. Follow the data sheet recommendation to ensure that an external 4.7 KΩ (or lower) resistor is connected to the PROM's OE/RESET# pin and the FPGA's INIT# pin.
2. When using FPGA DONE to drive PROM CE#, make sure that the signal is within the specification and has a fast rise and fall time. When the FPGA DONE signal is used to light an LED and also drive the PROM CE#, use an external buffer to drive the LED.
3. Use a Master mode FPGA CCLK pin as the configuration CLK source instead of an external free-running clock.
4. Connect the PROM BUSY pin to the FPGA BUSY pin *only* when the FPGA is set to use a parallel (SelectMAP) configuration mode. For serial configuration mode, the PROM BUSY pin must be left unconnected or must be driven Low.
5. At power-up, apply V_{CCINT} with a power supply ramp that rises from 0V to the minimum operating voltage in less than 300 µs.

TCK Must Be Greater Than 3 MHz

Overview

A design-related timing issue requires that TCK frequency must run faster than 3 MHz during JTAG programming and JTAG readback. This does not affect boundary-scan test or FPGA configuration (CLK timing).

Implication

The affected devices do not program or read back properly with TCK frequency less than 3 MHz.

Workaround

Use PC4 and iMPACT 6.1.03i (or later) with a 5 MHz setting to program and read back the Platform Flash PROM (XCF08P, XCF16P, and XCF32P).

FPGA Might Not Start Up Correctly if PROM CLK_OUT Is Used

Overview

After the FPGA asserts the DONE signal, the affected devices might not provide sufficient extra clocks for the FPGA to start up correctly. The affected devices provide from 0 to 2 extra clocks after DONE is asserted. Some FPGAs might require up to 6 extra clocks to start up properly.

Implication

The affected PROM devices cannot be used to generate the configuration clock reliably.

Workaround

Use the Master FPGA CCLK as the configuration clock source.

PROM Decompressor Is Not Enabled

Overview

The affected PROM devices do not have the decompressor enabled.

Implication

The decompression feature of these devices should not be used.

PROM Might Not Issue Correct Data for Free-Running CLK Source

Overview

The affected PROM devices intermittently might not synchronize correctly to an external, free-running clock upon a Low-to-High (output enable) transition on the OE/RESET# input.

Implication

The affected PROM devices might not issue the correct data stream.

Workaround

Use the Master FPGA CCLK as the configuration clock source. The FPGA Master clock is enabled only after the FPGA INIT# (PROM OE/RESET#) signal has safely transitioned to a High level.

BUSY Pin Must Be Low for Erase and Program Operations

Overview

A logic design issue allows the BUSY input signal to block the in-system programming circuits.

Implication

When the BUSY input is High, erase or program operations on the PROM might fail.

Workaround

Ensure the BUSY input signal is Low during in-system programming. For serial configuration mode, leave the BUSY input unconnected. The internal pull-down resistor keeps an unconnected BUSY input Low. For parallel configuration mode, connect the PROM BUSY pin to the FPGA BUSY pin and ensure the FPGA design does not drive the FPGA BUSY pin High after configuration. Prior to configuration, the parallel mode FPGA drives the BUSY pin Low.

VCCINT Power Supply Must Ramp in Less Than 300 µs

Overview

The PROM contains an internal clock that drives the PROM's power-on reset circuit soon after the V_{CCINT} voltage level crosses the power-on reset threshold (T_{VCCPOR}). The PROM's internal clock runs faster at lower V_{CCINT} voltage levels. When the V_{CCINT} voltage level is near the recommended operating range of 1.65V-2.00V, the PROM's internal clock runs sufficiently slowly for the power-on reset circuit to be successful. However, when the V_{CCINT} power-on ramp is slow, the V_{CCINT} voltage level might remain well below the recommended operating range while the power-on reset circuit is activated. At low V_{CCINT} voltage levels, the internal clock frequency might exceed the capabilities of the power-on reset circuit, resulting in a failure of the power-on reset circuit.

Implication

A failure within the power-on reset circuit might cause improper initialization of the PROM's JTAG IDCODE register, programming registers, and configuration download registers. As a result of the power-on-reset failure, the device might fail to exhibit a proper JTAG IDCODE, might fail in-system programming operations, and might fail to download its contents to an FPGA.

Workaround

Apply V_{CCINT} with a power supply ramp that rises from 0V to the minimum recommended operating voltage in less than 300 µs. This fast power ramp drives the V_{CCINT} operating voltage to a sufficient level prior to the execution of the power-on reset sequence, allowing the power-on reset circuit to successfully complete its initialization sequence.

Additional Questions or Clarifications

If additional questions arise or clarifications are needed regarding these errata, please contact your local Xilinx field application engineer (FAE) or sales representative. For the phone number in your area, see: http://www.xilinx.com/support/services/contact_info.htm.