XCF08P, XCF16P, & XCF32P Errata and Deviations from the Data Sheet Power on Reset

DS123-E03 (v1.1) July 6, 2005 **Errata Notice**

Introduction

Thank you for your interest in the Xilinx XCF08P, XCF16P, & XCF32P PROM products. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in this Errata notification.

Device Identification

This erratum applies only to the XCF08P, XCF16P, & XCF32P PROMs. This erratum does not apply to any other Xilinx PROMs.

Table 1: **Devices Affected by This Erratum**

Device Types	Devices
Parts:	XCF08PVO48C, XCF08PFS48C XCF16PVO48C, XCF16PFS48C XCF32PVO48C, XCF32PFS48C
Packages:	VO48, FS48
Date Codes:	522 and older (work week 22 of year 2005 and older)

Traceability

The affected devices have date codes 522 and older (i.e., work week 22 in the year 2005, or older).

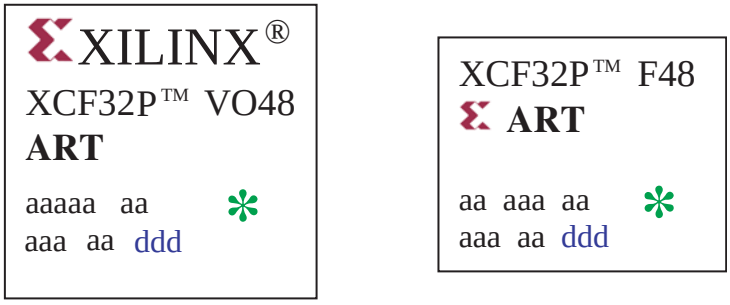

Figure 1: **Left, TSOP-48 (VO48) Package; right, FBGA-48 (FS48) Package**
Legend: a = alphanumeric characters; ddd = 3-character numeric date code.

Hardware Errata Details

This section provides a detailed description of the hardware issue at the release time of this document

PROM Must Be Powered Up Faster Than 1ms

Application affected by this issue:

Some of the devices listed above may fail in some applications during “Power on Reset Activation.” Devices that have a VCCint ramp during “Power on Reset Activation” that is slower than 1ms may see failures.

For more information on the “Power on Reset Activation” specification, refer to the data sheet “Platform Flash System Programmable Configuration PROM Datasheet” (DS123).

Description of the issue:

XCF08P, XCF16P, and XCF32P devices that have a VCCint ramp during “Power on Reset Activation” that take longer than 1ms to reach 1.6V may potentially see failures. The following diagram describes the region of operation for parts that are affected by the errata.

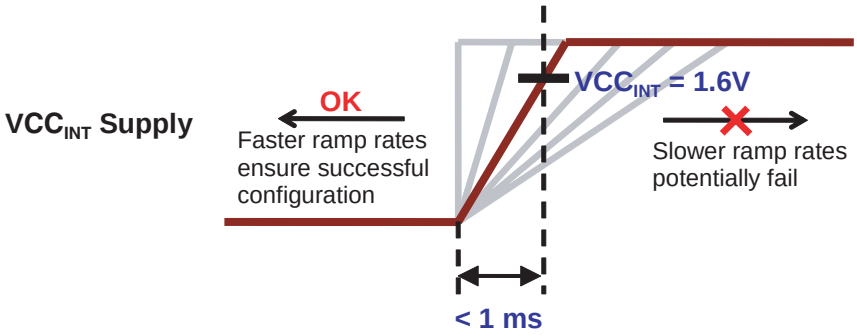

Figure 2: **Requirements for VCC_{INT}**

These products have been in high volume production since December 2004 without failures until recently from two customers. These devices failed to power up correctly during prototyping or manufacturing test. All or some of the following symptoms might occur during power up:

- The PROM JTAG IDCODE is all 1's
  This will prevent the programming of the FPGA bitstream into the PROM, because the programming solution (such as, a 3rd party programmer, a Xilinx cable/desktop programmer, etc.) will fail to recognize the PROM.
- PROM OE/RESET (FPGA INIT_B) is held Low from power-up and is never released High
  This will prevent the FPGA from configuring.
- No data output from PROM
  This will prevent the FPGA from configuring.

Corrective Action

Xilinx implemented a test program to correct the errata and ensure the devices meet the Power on Reset Activation specification

Customer Option

For devices that have a date code on or before “522” and have not been retested to the new Xilinx test program, there are two possible options for this errata

1. Ensure that VCCint ramps up to 1.6V faster than 1ms for the affected devices listed above
2. Xilinx implemented a test program to ensure the devices meet the Power on Reset Activation specification. Order parts that have been screened. Screened parts will have an asterisk mark (“*”) on the top side (see Figure 1, above). For ordering instructions, please contact your Xilinx Sales Representative.

Additional Questions or Clarifications

If questions arise regarding this erratum, please contact your Xilinx Technical Support:
http://www.xilinx.com/support/clearexpress/websupport.htm or
your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

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http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

Revision History

Date	Version	Description
06/24/05	1.0	Initial release
07/06/05	1.1	Revised for typographical error correction, production date release, and addition of Figure 2.