!! Important Product Information: Do Not Discard !!

Engineering Sample Errata Sheet

XC2VP2 ES Devices

Dear Xilinx Customer,

Thank you for your interest in the enclosed Virtex-II Pro Engineering Sample (ES) devices.

The Device Errata and Operational Guidelines apply to the Virtex-II Pro XC2VP2 ES devices with JTAG IDCODE revision code = **0000** (binary). For additional clarification or help with implementation related issues, please contact your Xilinx FAE for assistance.

Device Errata

1. Vccint for production devices is specified at 1.5V +/- 5%. For currently sampling ES devices, Vccint is required at 1.65V +/- 3%. The absolute maximum for Vccint is 1.7V.

Operational Guidelines

1. ISE/Foundation 5.1i is required.
2. ESD: Please handle with care and exercise standard CMOS ESD handling procedures at all times.
3. Mounting guideline: please refer to the label on the device packaging to ensure that the enclosed samples are mounted in accordance with the listed Moisture Sensitivity Level under EIA JEDEC Standard J-STD-020-A.

Notification List

Please note the following information that applies to all Virtex-II Pro ES and Production Devices.

1. Vbatt Voltage Specification – The Vbatt Voltage range is 1.0V to 2.65V.
2. DCM Fixed-Negative-Phase-Shift – Refer to http://support.xilinx.com answer record 13349.