!! Important Product Information: Do Not Discard !!

Product Notice

XC2V8000 C Devices

Dear Xilinx Customer,

Thank you for your interest in the enclosed Virtex-II devices. We would like you to be aware of the following information that has been updated in the Virtex-II Data Sheet and in the Virtex-II Platform FPGA User Guide. This information applies to all XC2V8000 devices with JTAG IDCODE revision code = **0000** (binary). If you have any questions, please contact your Xilinx FAE for assistance.

1. **Bitstream Encryption** – If your application requires Triple DES Bitstream Encryption, please request SCD 0774 when ordering devices. Devices ordered without this SCD do not support this feature and might not function properly, if an incorrectly keyed bitstream is loaded into the device. For further details or ordering assistance, please contact your Xilinx FAE or local sales office.

2. **Package Coplanarity -** The enclosed devices might not meet the XC2V8000 FF1152 & XC2V8000 FF1517 (XC2V8000-FF) package specification for coplanarity. Coplanarity is indicated by the *aaa* parameter in the ***Flip-Chip BGA (FF1152) Package*** Specification and ***Flip-Chip BGA (FF1517) Package*** Specification. The Virtex-II Flip-Chip package coplanarity specification is 8 mils (0.200 mm max). While the average coplanarity of the XC2V8000-FF parts is between 7 and 8 mils, the maximum can be as high as 10 mils (0.254 mm). Xilinx does not ship any parts with coplanarity exceeding 10 mils. Standard mounting practices should be applied to these packages. From analysis and empirical data, Xilinx has determined that the XC2V8000-FF packages flatten out to less than 6 mils at board mounting temperatures. Even though the XC2V8000-FF package might exceed the coplanarity spec, you should not experience any board-level assembly and reliability issues with these devices.