



These errata apply **ONLY** to Spartan-3 XC3S4000 and XC3S4000L FPGAs, including both production devices and engineering samples. These errata **DO NOT** apply to any other Spartan-3 FPGA. If using a different Spartan-3 FPGA, check for errata specific to that device.

Thank you for your interest in Spartan-3 XC3S4000 or XC3S4000L FPGA devices. Although Xilinx has made every effort to ensure that these devices are of the highest possible quality, these devices are subject to the limitations described in the following errata. Please review these errata to ensure that XC3S4000 or XC3S4000L FPGA devices meet your application requirements. Xilinx wants you to know about any known issues that may potentially affect your Spartan-3 application. This notice also includes [advisories](#) on the latest Spartan-3 design practices.

## Obtaining the Most-Recent Errata Version

By its very nature, an errata notification is a living document and is subject to updates based on recent findings. If this document is printed or saved locally in electronic form, please check for the most recent release, available to registered users via the Xilinx web site.

[http://www.xilinx.com/xlnx/xweb/xil\\_publications\\_display.jsp?category=-1210888](http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=-1210888)

## Devices Affected by This Errata

These errata only apply to the XC3S4000 or XC3S4000L FPGA as shown in [Table 1](#). Both engineering sample (ES) and production silicon (no ES marking) are affected. The [errata details](#) may further limit the class of devices affected by a specific issue.

*Table 1: Spartan-3 XC3S4000 FPGAs Affected by This Errata*

Device Types:	XC3S4000 XC3S4000L
Packages:	All
Speed Grades:	All
Date Codes:	All

## How to Identify an Affected Device

These errata affect all Spartan-3 FPGAs marked with an “XC3S4000” device type, including the XC3S4000L. The latest mask set, which is errata free, is fabricated at the UMC 300 mm wafer facility using 90 nm process technology and has an “EGQ” mask/fabrication/process code. The previous revision ‘A’ mask set is also fabricated at the UMC 300 mm wafer facility, also using 90 nm process technology and uses a “AGQ” mask/fabrication/process code. Devices fabricated at the UMC 200 mm wafer facility using 90 nm process technology have an “AFQ” mask/fabrication/process code, as indicated in [Table 2](#). Few XC3S4000 FPGAs were ever built at the 200 mm wafer facility.

*Table 2: Spartan-3 Production Facilities, Mask, and Fabrication/Process Codes*

Production Facility	Mask Revisions	Fabrication/Process Code	Example Top Mark
UMC 200 mm, 90 nm (8D)	A	FQ	<a href="#">Figure 1</a>
UMC 300 mm, 90 nm (12A)	A	GQ	<a href="#">Figure 2</a>
	E		

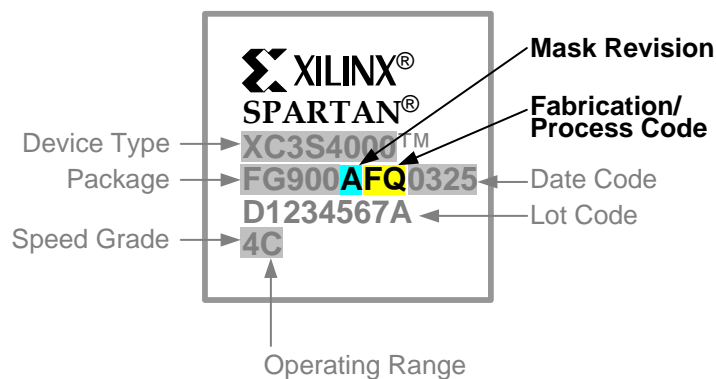


Figure 1: Spartan-3 FPGA from UMC 200 mm facility with “FQ” Fabrication/Process Code Marking

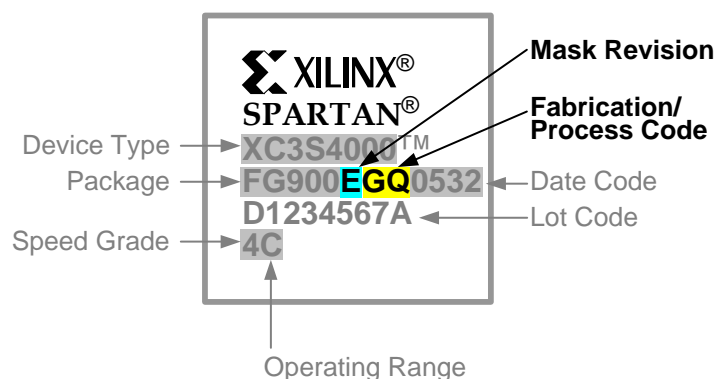


Figure 2: Spartan-3 FPGA from UMC 300 mm facility with “GQ” Fabrication/Process Code Marking

## Hardware Errata Summary

Table 3 summarizes the known hardware issues with the XC3S4000 or XC3S4000L FPGA. See “[Hardware Errata Details](#)” for a detailed description of each known issue. Table 3 also shows which mask revision is affected by a particular errata item.

Table 3: Hardware Errata Summary

Errata Issue	Mask/Fabrication/Process Code		
	“AFQ”	“AGQ”	“EGQ”
<a href="#">DCM Using CLK2X Feedback May Lose Lock</a>	Applies	N/A	N/A
<a href="#">Some Power Up Sequences where the VCCINT Supply Powers Up Last May Fail to Configure</a>	Applies	N/A	N/A
<a href="#">JTAG INTEST Instruction during UPDATE_DR Operation Potentially Forces Dedicated Configuration Input Pins to Invalid Value</a>	Applies	N/A	N/A
<a href="#">If HSWAP_EN Input Is High, Pull-Up Resistors Are Momentarily Enabled on User-I/O at the End of Configuration</a>	Applies	N/A	N/A
<a href="#">Readback Feature Not Available on Devices with “GQ” Fabrication/Process Code Marking Built Before Date Code “0532”</a>	N/A	Applies	N/A for devices with “0532” date code or later
<b>Mask Revision</b>	Initial	Revised	Latest
<b>Products</b>	XC3S4000	XC3S4000 XC3S4000L	XC3S4000 XC3S4000L

N/A=Not Applicable

## Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

### DCM Using CLK2X Feedback May Lose Lock

#### *Applications Affected by This Issue*

This issue only affects applications that use the DCM CLK2X output signal as the CLKFB feedback input to the DCM.

This issue only affects the XC3S4000 FPGAs shown in [Table 4](#), marked with the “AFQ” mask/fabrication/process code as shown in [Figure 1](#). Few such XC3S4000 FPGAs were ever built.

**Table 4: Spartan-3 XC3S4000 FPGAs Affected by the CLK2X Feedback Issue**

Device Types:	XC3S4000
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

#### *Description of Issue*

The DCM compensates for delay on the routing network by monitoring an output clock, either CLK0 or CLK2X, through a BUFGMUX. If a design uses the CLK2X output as the feedback clock for a DCM, the LOCKED output may go Low and the DCM may stop operating correctly after tens of milliseconds.

#### *Correction/Workaround/Resolution*

Use feedback from the CLK0 (through a BUFGMUX) instead of CLK2X and change the CLK\_FEEDBACK attribute from 2X to 1X. There is no difference in DCM performance. The CLK2X output is still valid and available for the application but it cannot be used for feedback to the CLKFB pin.

This issue is corrected on XC3S4000L FPGAs and on XC3S4000 FPGAs with a “GQ” fabrication/process code marking, as shown in [Figure 2](#).

### Some Power Up Sequences where the VCCINT Supply Powers Up Last May Fail to Configure

#### *Applications Affected by This Issue*

This issue potentially affects some applications where the VCCINT power supply is the last supply to reach its Power-On Reset (POR) voltage threshold. This issue only affects devices with the “FQ” fabrication/process code, as indicated in [Table 5](#). Few such XC3S4000 FPGAs were ever built.

Applications where VCCINT reaches its POR threshold first or second are not affected.

**Table 5: Spartan-3 XC3S4000 FPGAs Affected by the VCCINT Supply Sequence Issue**

Device Types:	XC3S4000
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

### Description of Issue

Three voltage-supply inputs—VCCINT, VCCAUX and the VCCO supply to Bank 4—control the behavior of the Spartan-3 and Spartan-3L Power On Reset (POR) circuit. When applying power, a Power-On Reset (POR) circuit within the FPGA monitors each of these three rails. Once the voltages on each of the three rails exceed their respective POR thresholds, the POR circuit allows the FPGA to continue with its configuration process.

In the potentially failing condition, the VCCINT supply must be the last supply to reach its valid POR voltage and the ramp rate must be slower than 500  $\mu$ S. When the FPGA fails to configure, the INIT\_B remains Low and the FPGA ignores the PROG\_B program pin. Even with the worst identified power sequence, actual failures only occur on a small percentage of devices, typically measured in parts per million. The issue is more pronounced at cold temperatures.

### Correction/Workaround/Resolution

**OPTION 1:** Use Spartan-3 FPGAs fabricated from the 300 mm production facility.

**OPTION 2:** Use a power-on sequence where VCCINT is not the last supply to reach its POR threshold level.

VCCINT must reach its maximum POR threshold ( $V_{CCINTT} = 1.0V$ ) before or coincident with VCCAUX reaching its minimum threshold ( $V_{CCAUXT} = 0.8V$ ). This supply sequence and threshold relationship is illustrated in [Figure 3](#).

Alternatively, VCCINT must reach its maximum POR threshold ( $V_{CCINTT} = 1.0V$ ) before or coincident with VCCO\_4 supplying I/O bank 4 reaching its minimum threshold ( $V_{CCO4T} = 0.4V$ ). This supply sequence and threshold relationship is also illustrated in [Figure 3](#).

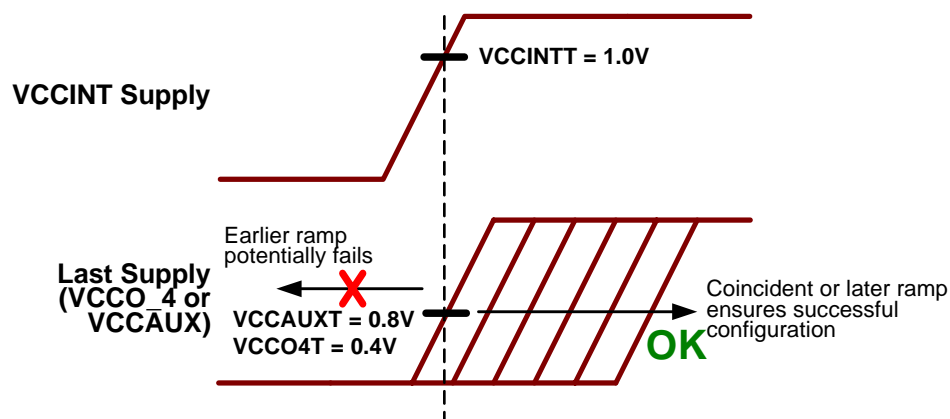


Figure 3: Requirements when VCCINT is not the Last Supply

The lowest power-consuming sequence is to apply VCCAUX before or coincident with VCCINT, then VCCINT followed by VCCO\_4. If VCCINT is applied before VCCAUX, the VCCINT supply consumes a surplus current until the VCCAUX supply reaches its maximum POR threshold, VCCAUXT. This additional current is a few hundred to several hundred milliamps (mA). This additional current is not required for successful configuration and the surplus current disappears when VCCAUX is applied.

Power-sequencing restrictions apply neither for the VCCO supplies to I/O Banks 0 through 3 nor for the VCCO supplies to I/O Banks 5 through 7, as these voltage rails are not inputs to the POR circuit.

**OPTION 3:** In a system that requires that the VCCINT supply is last in the power-up sequence, ensure that it ramps to its maximum POR threshold voltage ( $V_{CCINTT} = 1.0V$ ) in less than < 500  $\mu$ S, as shown in [Figure 4](#).

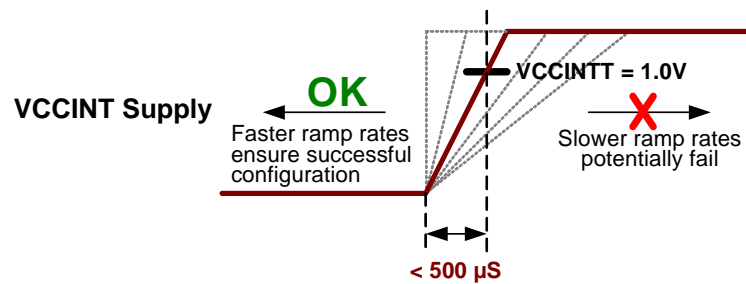


Figure 4: Use Faster VCCINT Ramp Rate if VCCINT is Last Supply

### JTAG INTEST Instruction during UPDATE\_DR Operation Potentially Forces Dedicated Configuration Input Pins to Invalid Value

#### Applications Affected by This Issue

This issue only affects applications that use the JTAG INTEST feature. If used at all, this feature is typically part of a JTAG-based device test procedure.

This issue does not affect applications that use the JTAG interface to download configuration data.

This issue only affects the XC3S4000 FPGAs shown in [Table 6](#), marked with the “AFQ” mask/fabrication/process code as shown in [Figure 1](#). Few such XC3S4000 FPGAs were ever built.

Table 6: Spartan-3 XC3S4000 FPGAs Affected by the JTAG INTEST Instruction Issue

Device Types:	XC3S4000
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

#### Description of Issue

The dedicated configuration input pins may be inadvertently forced High or Low during a JTAG INTEST operation.

After the device is configured, the M2, M1, M0, and HSWAP\_EN pins may be driven High or Low without consequence. The INTEST operation does not affect these pins unless the FPGA is un-configured.

However, if the INTEST operation drives HSWAP\_EN Low during an UPDATE\_DR operation, then the FPGA restarts its configuration process. Because PROG\_B follows HSWAP\_EN in the JTAG chain, the Low in HSWAP\_EN shifts into PROG\_B, inadvertently triggering a device reconfiguration.

#### Correction/Workaround/Resolution

Do not shift a '0' into the HSWAP\_EN position during device test using JTAG INTEST. If the JTAG operation consistently drives HSWAP\_EN High, then the PROG\_B pin is never driven Low during the operation. However, the other dedicated configuration inputs may still see invalid values.

This issue is corrected on XC3S4000L FPGAs and XC3S4000 FPGAs with a “GQ” fabrication/process code marking, as shown in [Figure 2](#).

## If HSWAP\_EN Input Is High, Pull-Up Resistors Are Momentarily Enabled on User-I/O at the End of Configuration

### Applications Affected by This Issue

This issue only affects applications that drive HSWAP\_EN High or leave it unconnected during configuration to disable weak pull-up resistors on the I/O. The issue has no effect on the use of pull-ups after configuration and the HSWAP\_EN pin is a "don't care" after configuration.

This issue only affects the XC3S4000 FPGAs shown in [Table 7](#), marked with the "AFQ" mask/fabrication/process code as shown in [Figure 1](#). Few such XC3S4000 FPGAs were ever built.

Table 7: Spartan-3 XC3S4000 FPGAs Affected by the HSWAP\_EN Issue

Device Types:	XC3S4000
Mask Revision Codes:	A only
Fabrication/Process Codes:	FQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

### Description of Issue

A High (the default) on HSWAP\_EN disables weak pull-up resistors on all pins that are not actively involved in the configuration process, placing these pins in a high-impedance state. At the very end of the configuration process, the pull-up resistors within each user-I/O pin are momentarily enabled, just before the I/Os become operational.

### Correction/Workaround/Resolution

Configure with pull-ups active by driving HSWAP\_EN Low. This is the recommended solution, as users should not rely on floating outputs to hold the value during configuration. The output behavior can be guaranteed if pull-ups are enabled.

Alternatively, use external pull-downs to insure logical 0 if an I/O must be Low during configuration.

This issue is corrected on XC3S4000L FPGAs and XC3S4000 FPGAs with a "GQ" fabrication/process code marking, as shown in [Figure 2](#).

## Readback Feature Not Available on Devices with "GQ" Fabrication/Process Code Marking Built Before Date Code "0532"

### Applications Affected by This Issue

This issue only applies to those designs using the Readback feature on the XC3S4000 or XC3S4000L FPGAs shown in [Table 8](#) with an "AGQ" Fabrication/Process Code marking, as shown in [Figure 2](#).

Table 8: Spartan-3 XC3S4000 FPGAs Affected by the Readback Issue

Device Types:	XC3S4000 XC3S4000L
Mask Revision Codes:	A (any date code) and E with date codes prior to "0532"
Fabrication/Process Codes:	GQ only
Packages:	All
Speed Grades:	All
Date Codes:	All

This issue affects all manifestations of device readback, including Slave Parallel and Master Parallel readback and JTAG readback. Otherwise, the XC3S4000 or XC3S4000L FPGA functions normally.

**Description of Issue**

The readback feature is not available for the devices indicated in [Table 8](#).

**Correction/Workaround/Resolution**

XC3S4000 FPGAs with an “FQ” Fabrication/Process Code marking fully support the Readback feature. Similarly, XC3S4000 and XC3S4000L FPGAs with an “EGQ” Mask/Fabrication/Process Code marking and with a Date Code of “0532” or later fully support Readback. XC3S4000 and XC3S4000L FPGAs ordered using the standard part number (without SCD codes) scheduled for delivery after 15-AUG-2005 automatically include the latest mask revision and Readback functionality.

**Advisories**

This section advises designers of any potential software changes that may affect their XC3S4000 or XC3S4000L FPGA applications. [Table 9](#) summarizes the advisories and indicates which software update will correct the issue.

Table 9: Advisories and Software Update

Advisory	ISE Version
<a href="#">Bitstream Update Required using ISE 6.3i, Service Pack 1 (SP1) or Later</a>	ISE 6.3i, Service Pack 1
<a href="#">New FACTORY_JF Settings Required for Spartan-3 DCMs</a>	ISE 8.2i

**Bitstream Update Required using ISE 6.3i, Service Pack 1 (SP1) or Later**

Spartan-3 block RAM internal timing is controlled by settings in the FPGA configuration bitstream. Through yield analysis, new optimal bitstream settings were identified for specific Spartan-3 device types. These new settings improve the block RAM internal timing margin, which consequently improves overall product yield and availability. **These new settings do not affect any timing in the FPGA application**, only internal timing relationships within the block RAM. The specific improved internal block RAM timing path is the relationship between the write-enable timing and the input latch-enable timing.

These new bitstream settings are now the default settings starting with Xilinx ISE 6.3i, Service Package 1, available for download from the Xilinx web site after September 13, 2004. XC3S4000 FPGAs are tested using these new bitstream settings beginning with date codes “0433”, corresponding to Work Week 33 of 2004. [Figure 5](#) shows an example top marking for a Spartan-3 FPGA. The relevant fields to identify an affected device are highlighted and include the **Device Type** and the **Date Code**.

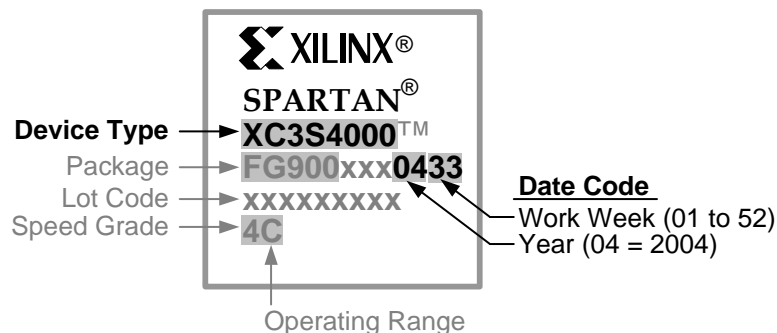


Figure 5: Example Spartan-3 Package Markings

Please regenerate any Spartan-3 FPGA configuration bitstreams created using software versions prior to Xilinx ISE 6.3i development software, Service Pack 1. By updating the bitstream, the application can use any existing or future production Spartan-3 FPGA device.

### New FACTORY\_JF Settings Required for Spartan-3 DCMs

#### Applications Affected by This Issue

This issue potentially affects applications that use Digital Clock Managers (DCMs). This issue only affects an application if and only if ...

- The application uses one or more DCMs
- One of the DCMs uses phase shifting, either fixed or variable mode.
- The phase shift is negative or very slightly positive (< 600 ps).

Unless a design meets these exact criteria, this issue can be safely ignored.

#### Description of Issue

The DCM automatically compensates for process, voltage, and temperature (PVT) changes and consequently it periodically updates its delay tap settings. The rate at which the update occurs is controlled by an internal attribute called FACTORY\_JF. Xilinx has identified an optimal FACTORY\_JF setting value (FACTORY\_JF=8080). Other settings may potentially fail to track properly over process, voltage, and temperature.

Without using the optimal settings, the DCM could potentially, with low probability, fail to assert the LOCKED output, could lose lock, or could produce erroneous clock outputs.

#### Correction/Workaround/Resolution

The new optimal settings are applied starting with Xilinx ISE 8.2i. If using an earlier version, modify the new FACTORY\_JF=8080 settings on each DCM instantiated in the design. [Table 10](#) shows the best available options to update the DCM settings, depending on current design status.

**Table 10: Options for Updated FACTORY\_JF DCM Setting**

Method	Design Status	Steps After Editing
<a href="#">FPGA Editor</a>	Design complete, no further edits planned	Rerun Bitstream Generator
<a href="#">Constraints File</a>	Design in progress	Rerun Design Implementation
<a href="#">VHDL</a> or <a href="#">Verilog</a> Source Code	Design in progress	Rerun complete flow

#### FPGA Editor

If the design is complete, with no further edits planned, then FPGA Editor offers the easiest method to update the FACTORY\_JF setting.

- Invoke the FPGA Editor. On Windows PCs, select **Start** → **Xilinx ISE 6** → **Accessories** → **FPGA Editor**.
- Select **File** → **Open**. Select the \*.ncd file for the completed design. Set the **Edit Mode** to "Read Write" mode as shown in [Figure 6](#).



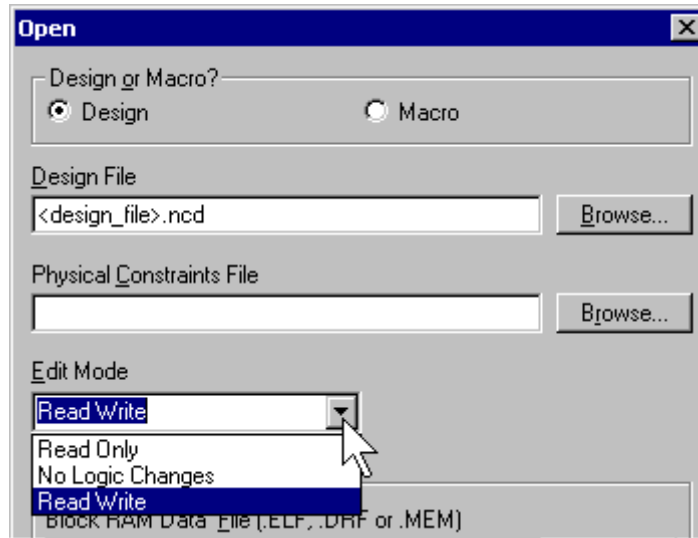


Figure 6: Enable User Editing in FPGA Editor

- For each DCM used in the design ...
  - Select the DCM block using the cursor.
  - Click 'editblock' from the right-most command button bar.
  - Click the Edit Mode button from the icon bar, as shown in [Figure 7](#).



Figure 7: Click "Edit Mode" Button to Change DCM Settings

- Check the two 0X80 options for the FACTORY\_JF DCM attribute, as shown in [Figure 8](#).

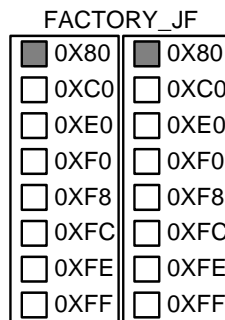


Figure 8: Edit Block View of DCM FACTORY\_JF Settings

- After all DCMs are modified, save the design.
- Re-run the Bitstream Generator.

### Constraints File

An easy option for designs in progress is to apply a user constraint. Edit an existing user constraints file (UCF) or create a new file and add the following constraint for every DCM used in the design.

```
INST <dcm_inst> FACTORY_JF = "8080";
```

### VHDL

When using VHDL, update the FACTORY\_JF values in both the DCM component declaration and in all component instantiations of the DCM. The following code snippet provides an example for XST VHDL. The VHDL source for other logic synthesis packages may vary slightly.

```
component DCM    -- DCM component declaration
  generic(
    . . .
    FACTORY_JF : bit_vector :=  x"8080";
    . . .
  );
. . .

DCM_INST : DCM    -- DCM instantiation
  generic map(
    . . .
    FACTORY_JF => x"8080",
    . . .
  )
```

### Verilog

When using Verilog, update the FACTORY\_JF values as shown in the following XST Verilog code snippet.

```
DCM DCM_INST (
    . . .
);

. . .
// synthesis attribute FACTORY_JF of DCM_INST is "8080"
. . .
// synopsys translate_off
. . .
defparam DCM_INST.FACTORY_JF = 16'h8080;
. . .
// synopsys translate_on
```

### Clock Wizard

The Clock Wizard architecture wizard automatically generates a VHDL or Verilog description of a DCM design based on user input. If using Clock Wizard, update the HDL source as shown in the VHDL or Verilog examples above. Be forewarned that Clock Wizard overwrites the source file each time Clock Wizard is executed.

### Other References

- **Answer Record #21559: What is the correct value for the FACTORY\_JF attribute?**  
[http://www.xilinx.com/xlnx/xil\\_ans\\_display.jsp?getPagePath=21559](http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=21559)

## Design Software Requirements

The devices covered by these errata require the following Xilinx development software installations to create bitstream programming files.

- Xilinx ISE 8.2i or later  
(updates are available at the following web link)

[www.xilinx.com/xlnx/xil\\_sw\\_updates\\_home.jsp](http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp)

## Additional Questions or Clarifications

If additional questions arise regarding these errata, please contact your local Xilinx field application engineer (FAE) or sales representative. Alternatively, please contact Xilinx Technical Support.

[www.xilinx.com/company/contact.htm](http://www.xilinx.com/company/contact.htm)

Alternatively, please visit the Xilinx MySupport web site.

[www.xilinx.com/support/mysupport.htm](http://www.xilinx.com/support/mysupport.htm)

## Revision History

Date	Version No.	Description
16-DEC-2003	1.5	Initial release.
22-DEC-2003	1.6	Provided additional workarounds for <b>VCCO Fast Ramp</b> issue. Added workaround details and clarified that the LVDS_EXT standard is not supported in the <b>LVDS</b> issue.
9-FEB-2004	1.7	Included both engineering samples (ES) and production devices in errata notification. Updated <b>VCCO Fast Ramp</b> issue. Updated <b>LVDS</b> issue, including information on output voltage levels and bitstream generator settings. Added <b>DCM Negative Phase Shift</b> issue. Added <b>Maximum Guaranteed DCM Clock Output Frequency</b> issue.
5-MAR-2004	1.8	The <b>VCCO Fast Ramp</b> issue, the <b>LVDS</b> issue, the <b>Maximum Guaranteed DCM Clock Output Frequency</b> issue and the <b>I/O Leakage</b> issue are now described in the <b>Spartan-3 Data Sheet</b> . These issues are no longer covered as errata topics.
20-DEC-2004	2.2	Added <b>VCCINT Supply Sequence</b> issue. Added information about the <b>top markings</b> indicating the mask revision, fabrication facility, and process technology for a given Spartan-3 FPGA. Clarified <b>which erratum applies to which mask revision</b> . Added advisory on <b>FG676 VREF</b> issue. Added advisory on <b>New DCM FACTORY JF Settings</b> .
7-JAN-2005	2.3	Changed the mask revision code for devices manufactured at the UMC 300 mm, 90 nm facility (12A) from 'B' to 'A' in <b>Table 2</b> . Also updated <b>Table 8</b> for the 'A' mask revision code. Updated <b>Table 3</b> and the Workaround section of the <b>VCCINT Supply Sequence</b> issue as this issue was removed for devices manufactured at the UMC 300 mm, 90 nm facility (12A).
8-AUG-2005	2.4	Updated <b>Table 2</b> and <b>Table 3</b> to add mask revision 'E', which is errata-free for FPGAs with date codes of "0532" or later. Updated <b>Readback</b> because this issue is corrected for mask revision 'E' devices with date codes of "0532" or later. Updated workarounds section of <b>VCCINT Supply Sequence</b> issue to clearly define available options. Updated the advisory on <b>New DCM FACTORY JF Settings</b> to clarify the conditions when the new settings are required.
14-DEC-2006	2.5	Updated <b>New DCM FACTORY JF Settings</b> to note that ISE 8.2i automatically includes the new settings.