Virtex-4 XC4VLX80CES Errata

EN017 (v1.1) February 15, 2006 **Errata Notification**

Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VLX80 FPGA. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VLX80 devices as shown in Table 1.

Table 1: **XC4VLX80 FPGA Devices Affected by These Errata**

Devices	XC4VLX80CES	JTAG ID (Revision Code): 3
Packages	All	
Speed Grades	All	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST EMPTY OFFSET or ALMOST FULL OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact Xilinx technical support for SP4 help. Updates are available on the following web page:

  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

  The Stepping should be set to "1" in the constraint file (UCF file):

  CONFIG STEPPING = "1";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

© 2005–2006 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, and other designated brands included herein are trademarks of Xilinx, Inc.
All other trademarks are the property of their respective owners.

http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

Traceability

The XC4VLX80 is marked as shown in Figure 1.

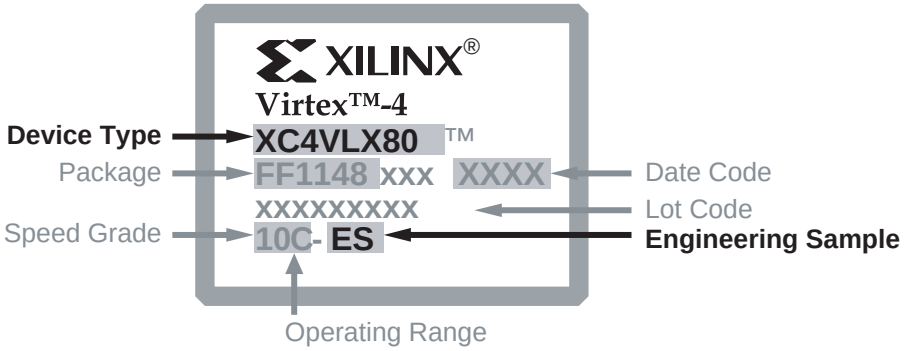

Figure 1: **Example XC4VLX80CES Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx web site at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an email alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/user guides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/user guides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/user guides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/user guides/ug075.pdf)

Revision History

Date	Version	Description
04/21/05	1.0	Initial release.
02/15/06	1.1	Added the FIFO16 section. Updated Design Software Requirements section. Replaced the LVTTL I/O standard with LVCMOS I/O standard in the Notes and Recommendations section. Removed System Monitor errata because it is no longer in the Virtex-4 data sheet.