Virtex-5 TXT and FXT FPGA Production Errata

EN062 (v1.0) March 31, 2009 **Errata Notification**

Introduction

Thank you for designing with the Xilinx Virtex®-5 family of devices. Although Xilinx has made every effort to ensure the highest possible quality, the devices listed in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to the Virtex-5 devices, as shown in Table 1.

Table 1: **Virtex-5 Devices Affected by These Errata**

Devices	XC5VTX150T	JTAG ID (Revision Code): All
	XC5VTX240T	JTAG ID (Revision Code): All
	XC5VFX30T	JTAG ID (Revision Code): All
	XC5VFX70T	JTAG ID (Revision Code): All
	XC5VFX100T	JTAG ID (Revision Code): All
	XC5VFX130T	JTAG ID (Revision Code): All
	XC5VFX200T	JTAG ID (Revision Code): All
Packages	All	
Speed Grades	All	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

GTX Transceivers

Clock Correction

The Clock Correction feature of the Virtex-5 FPGA GTX transceiver can cause data corruption on the receiver when a clock correction sequence is skipped or added. See UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for more detailed information about the Clock Correction feature.

This issue can occur when all of the following conditions are true:

- Asynchronous operation: When the local reference clock of the Virtex-5 FPGA GTX transceiver is driven from a different oscillator than the far-end transceiver. This introduces a parts per million (PPM) offset in frequency between the operation of the transceivers, requiring clock correction to skip or add clock correction sequences on a periodic basis. This also implies that the RXUSRCLK and RXUSRCLK2 ports of the Virtex-5 FPGA GTX transceiver are derived from the local oscillator and not the RXRECCLK port.
- Clock Correction is enabled.
  - CLK_CORRECT_USE_0/1 attribute is set to **TRUE**.
- The length of the clock correction sequence is 1 or 3 Bytes.
  - CLK_COR_ADJ_LEN_0/1 attribute is set to **1** or **3**.

When the conditions described above are met, one of the multiple work-around options described below shall be used to mitigate this issue. XAUI, PCIe®, SRIO, and Infiniband are the most common protocols affected but only when used in asynchronous operation.

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Work-around

If the application permits, implement one of the following work-around options:

- Use synchronous clocking
- Convert to 2 byte or 4 byte clock correction sequence
- If the application does not permit one of these options, see Answer Record 32164.

All versions of UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* subsequent to the current version, v2.1, will properly reflect the Clock Correction behavior described herein.

Operational Guidelines

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.63 (or later), Xilinx ISE™ Design Suite 10.1, Service Pack 3 (or later).

Traceability

See UG195, *Virtex-5 FPGA Packaging and Pinout Specification* for package marking.

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For additional questions regarding these errata, please contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
03/31/09	1.0	Initial Xilinx release.

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