

## Introduction

Thank you for participating in the Spartan®-6 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

## Devices

These errata apply to the Spartan-6 devices shown in [Table 1](#).

*Table 1: Devices Affected by These Errata*

Devices	JTAG ID (Revision Code)
XC6SLX45-2CSG324CES	1
XC6SLX45-2FGG484CES	1

## Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

### Block RAM

#### ***Dual Port Block RAM Address Overlap in READ\_FIRST and Simple Dual Port Mode***

When using the block RAM in True Dual Port (TDP) READ\_FIRST mode or Simple Dual Port (SDP) mode, with different clocks on ports A and B, the user must ensure certain addresses do not occur simultaneously on both ports when both ports are enabled and one port is being written to. Failure to observe this restriction can result in read and/or memory array corruption.

The description is found in the Conflict Avoidance section in v1.2 of [UG383](#), *Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.1, published 10/28/09. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE® 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

#### **Work-around**

See [Answer Record 34533](#).

## 9K Simple Dual Port Block RAM Width Restriction

The Spartan-6 FPGA RAMB8BWBR in Simple Dual Port (SDP) mode (RAM\_MODE=SDP) only supports the 36-bit data width on both ports. Failure to set both ports to 36 bits (DATA\_WIDTH\_A=36, DATA\_WIDTH\_B=36) can result in data corruption.

The description is found in the Possible Configurations section in v1.2 of [UG383](#), *Spartan-6 FPGA Block RAM Resources User Guide*.

This description was originally added to the *Spartan-6 FPGA Block RAM Resources User Guide*, v1.2, published 02/23/10. This errata is being provided to highlight this change and ensure that all users are aware of this design restriction. ISE 12.1 software provides appropriate warnings for possible violations of these restrictions.

This issue will not be fixed in silicon.

### Work-around

See [Answer Record 34541](#).

## Memory Controller Block (MCB)

### MCB Performance

[DS162](#), *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics* (v1.5 or later) includes new data rate specifications for DDR2 and DDR3 interfaces implemented with the MCB. The new data rates are supported in the Standard MCB performance mode when operating within the standard  $V_{CCINT}$  recommended operating conditions. In addition, a new Extended MCB performance mode has been introduced with  $V_{CCINT}$  operating conditions that allow the MCB to operate at the originally specified performance.

Table 2: MCB Performance Specification Comparison

Performance Specification	$V_{CCINT}$ Operating Range	DDR2 / DDR3 Performance
		-2
Original (No Longer Supported)	1.14V – 1.26V	667 Mb/s
New (Standard Performance)	1.14V – 1.26V	625 Mb/s
New (Extended Performance)	1.2V – 1.26V	667 Mb/s

This errata is being provided to highlight this change and ensure that all MCB users are aware of the new performance modes and specifications. The ISE 12.2 software (with MIG 3.5) will provide support for selection and timing validation of the new Standard and Extended MCB performance modes. Prior to the ISE 12.2 software release, these modes can be used by adhering to the correct  $V_{CCINT}$  range and ensuring that MIG tool selections are made in compliance with the new performance specifications.

[Answer Record 35818](#) contains additional information.

### MCB Calibration

For the devices listed in [Table 1](#), for designs using Calibrated Input Termination, use the pin locations in [Table 3](#) for the RZQ reference resistor.

Table 3: Required RZQ Pins

Package	MCB Bank 1	MCB Bank 3
CSG324	Pin M14	Pin L6
FGG484	Pin M19	Pin K7

## ***MCB and Suspend***

In the devices listed in [Table 1](#), the MCB does not support the self-refresh mode of the external memory during FPGA Suspend.

## ***MCB Address Bus Hold Time***

In the devices listed in [Table 1](#), some bits of the MCB address bus (mcbx\_dram\_addr) can violate the input hold time ( $t_{IH}$ ) specification of the memory device.

### **Work-around**

See [Answer Record 34089](#).

## **DCM Minimum Frequency**

The Digital Clock Manager (DCM\_SP or DCM\_CLKGEN) minimum frequency does not meet the data sheet specifications in the devices listed in [Table 1](#). The following specifications deviate from the data sheet:

- CLKIN\_FREQ\_DLL Min: 25 MHz
- CLKOUT\_FREQ\_CLK0 Min: 25 MHz
- CLKOUT\_FREQ\_CLK90 Min: 25 MHz
- CLKOUT\_FREQ\_2X Min: 50 MHz
- CLKOUT\_FREQ\_DV Min: 1.6 MHz
- CLKIN\_FREQ\_FX Min: 0.8 MHz
- CLKOUT\_FREQ\_FX Min: 25 MHz
- CLKOUT\_FREQ\_FXDV: 0.8 MHz

## **Device DNA**

Device DNA is not supported in the devices listed in [Table 1](#). Do not use this feature.

## **Readback CRC**

Readback CRC for SEU detection (POST\_CRC) is not supported in the devices listed in [Table 1](#).

## **Operational Guidelines**

### ***Design Software Requirements***

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx development software installation.

- Speed specification v1.01 (or later), Xilinx ISE® Design Suite 11.3 (or later).
- Upgrading to ISE 12.1 or later is recommended.

### ***Operating Conditions Required when Using I/O Delay Variable Mode***

In the devices listed in [Table 1](#), when using I/O Delay Variable Mode, the operating conditions must be:

- $V_{CCINT} = 1.20V$  to  $1.26V$
- Junction temperature ( $T_J$ ) =  $25^{\circ}C$  to  $85^{\circ}C$

The I/O delay variable mode (also known as I/O delay calibration and reset) is used when the IODELAY2 CAL or RST are used or when IODELAY2 IDELAY\_TYPE attribute is set to VARIABLE\_FROM\_ZERO, VARIABLE\_FROM\_HALF\_MAX, or DIFF\_PHASE\_DETECTOR.

## Traceability

The XC6SLX45 is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

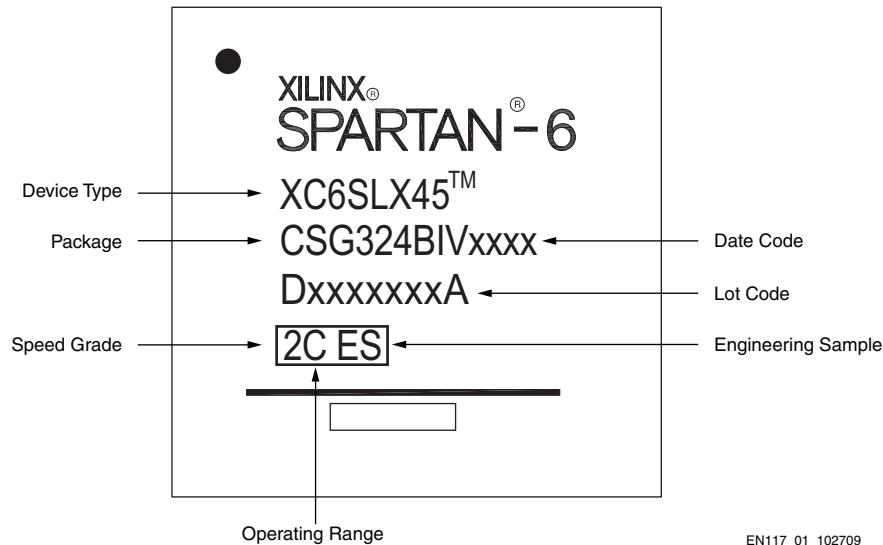


Figure 1: XC6SLX45-2CSG324CES Marking

## Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact.htm>.

## Revision History

Date	Version	Description
09/28/09	1.0	Initial Xilinx release.
10/14/09	1.1	Improved <a href="#">DCM Minimum Frequency</a> with reduced specifications. Removed the Quiescent Current operational guideline because it is not a deviation from existing specifications; see <a href="#">Answer Record 33641</a> for more information on quiescent current.
11/02/09	1.2	Added <a href="#">MCB and Suspend</a> and <a href="#">Readback CRC</a> .
02/17/10	1.3	Added <a href="#">MCB Address Bus Hold Time</a> .
05/07/10	1.4	Added <a href="#">Dual Port Block RAM Address Overlap in READ_FIRST and Simple Dual Port Mode</a> and <a href="#">9K Simple Dual Port Block RAM Width Restriction</a> sections.
06/25/10	1.5	Added <a href="#">MCB Performance</a> . Updated <a href="#">Design Software Requirements</a> .

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