

Introduction

Thank you for participating in the Virtex®-7 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (revision code)	Packages	Speed Grades	Junction Temperature Range
Virtex-7	XC7V2000T CES9937	1	All	-1, -2	0°C to 85°C

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

External Memory Interfaces

Phaser Block Divide by Two Mode for DDR3 and DDR2

The Phaser block "divide by two" mode used to implement DDR3 and DDR2 external memory interfaces at frequencies from 303–399 MHz is not operational. The Phaser block must be used in 1:1 mode, which restricts the minimum supported DDR3 and DDR2 memory clock frequency to 400 MHz (800 Mb/s DDR).

Work-around

Select a Memory Clock frequency of 400 MHz (DDR3 or DDR2) or higher (DDR3 only) in the Memory Interface Generator (MIG) tool to ensure that the Phaser block is set to 1:1 mode.

DDR3 and DDR2 Memory Interfaces

When interfacing to DDR3 or DDR2 memories with Memory Interface Generator (MIG) IP, calibration failures can occur. Read data failures can also occur after a successful calibration.

Work-around

Contact Xilinx Technical Support for additional guidance.

DDR3 Maximum Interface Rate

The maximum physical interface (PHY) rate for DDR3 memory interfaces for the -2 speed grade in high-performance (HP) I/O banks with VCCAUX_IO = 2.0V is 1,600 Mb/s.

XADC

Integral Nonlinearity

The XADC has a four LSB (~1 mV) integral nonlinearity (INL) error versus the data sheet specifications ([DS183](#), *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics*, v1.5) of three LSBs.

XADC On-chip Reference Variation

The XADC on-chip reference source can exceed the [DS183](#), *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* data sheet specification of $1.25V \pm 1\%$ by an additional 0.5%. See [Answer Record 44971](#) for more information on the impact to XADC measurements when the on-chip reference source is used.

GTX Transceivers

Out-of-Band Signaling

The GTX transceiver circuitry for out-of-band (OOB) signaling is always enabled.

GTX Line Rate

The GTX transceiver operation is limited to a maximum of 6.6 Gb/s.

QPLL Frequency Range

The supported QPLL frequency range is 5.93–6.6 GHz.

TXOUTCLK and RXOUTCLK Ports

The GTX transceiver TXOUTCLK and RXOUTCLK ports can exhibit loss of edges or excessive jitter when used simultaneously within a GTX channel and with other channels in a transceiver Quad.

The following rules must be followed for proper operation of TXOUTCLK and RXOUTCLK:

- Use either TXOUTCLK or RXOUTCLK within any GTX channel, not both.
- Use either TXOUTCLK of GTX0 or RXOUTCLK of GTX1, not both.
- Use the reference clock directly from IBUFDS_GTXE2 to drive the fabric logic and GTX user clocks when necessary ([TX/RX]USRCLK, [TX/RX]USRCLK2).

Set RXOUTCLKSEL = 3'b000 when RXOUTCLK is not used. Set TXOUTCLKSEL = 3'b000 when TXOUTCLK is not used.

See [Answer Record 43244](#) for more information.

QPLL Use Mode

The QPLL can lose lock if reset at one temperature extreme and operated at the other.

Work-around

See [Answer Record 43244](#) for the user design work-around.

Receiver Link Margin

The receiver can have a reduction in jitter tolerance when used in full-rate mode (RXOUT_DIV = 1).

Work-around

See [Answer Record 43244](#) for attribute updates and equalization selection.

CPLL Jitter

The GTX CPLL when operated at 3.1 GHz, or above, can exhibit higher jitter when $V_{MGTAVTT}$ is higher than nominal.

Transmit Electrical Idle

The transmitter common mode voltage is higher than expected when TX electrical idle is enabled. The electrical idle detection in the receiver is not impacted when links are AC coupled.

Receiver Detection for PCIe

The Receiver Detection feature used for PCIe® applications is not supported.

Work-around

Set the following attributes to force the transmitter to always detect a receiver:

- TX_RXDETECT_REF = 3'b000
- RX_CM_SEL = 2'b11
- (PMA_RSV2[4], RX_CM_TRIM[2:0]) = 4'b1010

PCIe ASPM Support

ASPM L0s is not supported for Gen 2 (5 Gb/s) line rate.

Work-around

Set the following attributes on the Integrated Block for PCI Express to disable ASPM L0s:

- LINK_CAP_ASPM_OPTIONALITY = TRUE
- LINK_CAP_ASPM_SUPPORT = 0

See [Answer Record 43243](#) for additional details.

GTX Transceiver Power-Up/Power-Down

If the recommended sequence is followed, while $V_{MGTAVCC}$ is powered within its recommended operating range and $V_{MGTAVTT}$ is below 0.7V, an additional 50 mA per transceiver is drawn from $V_{MGTAVCC}$.

IEEE Std 1149.1 and IEEE Std 1149.6 for GTX Transceivers

In the devices listed in [Table 1](#), IEEE Std 1149.1 (JTAG) boundary-scan test commands are not supported for the GTX transceiver. IEEE Std 1149.6 (ACJTAG) boundary-scan test commands EXTEST_PULSE and EXTEST_TRAIN are not supported.

IEEE Std 1149.1 JTAG

IEEE Std 1149.1 (JTAG) IDCODE[31:0] is 136BF093 (hex).

SelectIO Resources

Internal Weak Pull-Ups/Pull-Downs for High-Range I/O Bank0

The internal weak pull-ups/pull-downs for the high-range (HR) I/O configuration bank 0 will not achieve valid logic-1 and logic-0 states for 1.8V and lower V_{CCO_0} . External resistors should be used for V_{CCO_0} of 1.8V and lower.

Power

Static Current

The devices listed in [Table 1](#) can exhibit up to 50% higher static current on all supplies, except $V_{MGTAVTT}$, compared to the static current reported in XPE 13.3 (or later). The $V_{MGTAVTT}$ supply can consume up to a total of 20 mA per powered transceiver Quad. Also, up to an additional 95 mA can be consumed by the $V_{MGTAVCC}$ supply for each powered and uninstantiated transceiver Quad.

Packaging

Package Assembly

Bake units for 4 hours at 125°C before assembly. Within 30 minutes of taking the units from the bake oven, assemble them on the final system board. Failure to follow this baking procedure can result in device damage during assembly.

Configuration

Single Event Upset (SEU) Detection and Correction

SEU detection or correction (POST_CRC=ENABLE) is not supported.

Design Tool Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.07 (or later) of Xilinx® Vivado Design Suite 2012.4 (or later) available at <http://www.xilinx.com/support/download/>. The -2 speed grade devices require a patch; refer to [Answer Record 53651](#).
- For GTX transceiver attribute updates, refer to [Answer Record 43244](#).
- See [Answer Record 47816](#) for the most current known issues and work-arounds for Xilinx Design Tools.

Traceability

The XC7V2000T devices listed in [Table 1](#) are marked as shown in [Figure 1](#).

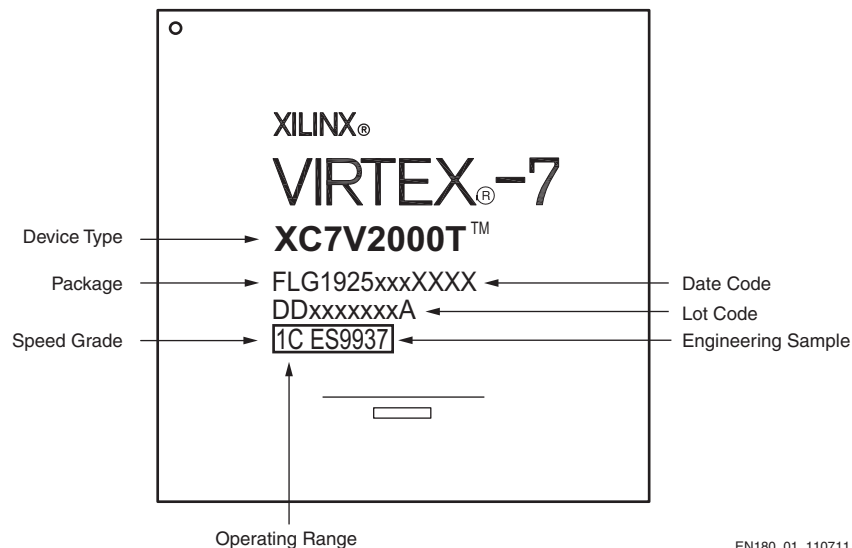


Figure 1: Example Device Top Mark

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support:

<http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative:

<http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/01/11	1.0	Initial Xilinx release.
01/24/12	1.1	Added Dual Rank for DDR3 and DDR2. Updated Phaser Block Divide by Two Mode for DDR3 and DDR2 and XADC On-chip Reference Variation . Added Out-of-Band Signaling .
02/28/12	1.2	Removed Dual Rank for DDR3 and DDR2; silicon support for dual rank reinstated.
03/29/12	1.3	Updated Package Coplanarity and Package Assembly .
02/12/13	1.4	Added DDR3 and DDR2 Memory Interfaces , DDR3 Maximum Interface Rate , and GTX Transceiver Power-Up/Power-Down . Updated Integral Nonlinearity , IEEE Std 1149.1 and IEEE Std 1149.6 for GTX Transceivers , and Design Tool Requirements . Removed Power-On/Off Requirement because it was added to DS183, <i>Virtex-7 FPGAs Data Sheet, DC and Switching Characteristics</i> , v1.1, 10/5/11. Removed Package Coplanarity; it was updated in the FL/FLG1925 package drawing in UG475, <i>7 Series FPGAs Packaging and Pinout Product Specification</i> , v1.8, 10/15/12. Removed Operational Guidelines regarding DDR3 and External V_{REF} because the requirement was added to DS183, <i>Virtex-7 FPGAs Data Sheet, DC and Switching Characteristics</i> , v1.5, 08/03/12.

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