

Introduction

Thank you for participating in the Virtex®-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades
Virtex-7	XC7VX485T CES	2	All	-1, -2

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

XADC

XADC On-Chip Reference Variation

The XADC on-chip reference source can exceed the [DS183](#), *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* specification of $1.25V \pm 1.0\%$ by an additional 0.5% ($1.25V \pm 1.5\%$). See [Answer Record 44971](#) for more information on the impact to XADC measurements when the on-chip reference source is used.

GTX Transceivers

QPLL Upper Band Usage

When using the QPLL upper band VCO mode (QPLL_CFG[6]=0), the $V_{MGTAVCC}$ power supply must be $1.05V \pm 30mV$.

The operating frequency range ($F_{GCPPLL\text{RANGE}2}$) of the QPLL upper band VCO mode (QPLL_CFG[6]=0) is 9.94 GHz to 10.3125 GHz. Due to this limitation, GTX data rates between 9.80 Gb/s to 9.93 Gb/s are not supported.

Out-of-Band Signaling

The GTX transceiver circuitry for out-of-band (OOB) signaling is always enabled.

CPLL Power Down

The GTX transceiver CPLL can become inoperative if conditions (1) and (2) persist for more than 8,000 hours:

1. Power has been applied to $V_{MGTAVCC}$ and $V_{MGTAVTT}$.
2. The device is in one of the following states:
 - a. The FPGA is not configured.
 - b. The FPGA is configured, but the transceiver is uninstantiated.
 - c. The transceiver is instantiated, but the CPLL is held in power-down state.

When the QPLL is being used, enabling each CPLL will consume up to 30 mA on the $V_{MGTAVTT}$ supply and 20 mA on $V_{MGTAVCC}$. See [Answer Record 45360](#) for more details.

GTX Transceiver Power-Up/Power-Down

If the recommended power sequences are not followed, then the GTX transceiver can become inoperative if $V_{MGTAVTT}$ is within its recommended operating range and $V_{MGTAVCC}$ is at a voltage less than 0.4V for more than 10,000 cumulative hours. An additional 100 mA per transceiver is drawn when $V_{MGTAVTT}$ is within its recommended operating range and $V_{MGTAVCC}$ is at a voltage less than 0.4V.

If the recommended sequence is followed, while $V_{MGTAVCC}$ is powered within its recommended operating range and $V_{MGTAVTT}$ is below 0.7V, an additional 50 mA per transceiver is drawn from $V_{MGTAVCC}$.

IEEE Std 1149.1 and IEEE Std 1149.6 for GTX Transceivers

IEEE Std 1149.1 (JTAG) boundary-scan test commands are not supported for the GTX transceiver. IEEE Std 1149.6 (ACJTAG) boundary-scan test commands EXTEST_PULSE and EXTEST_TRAIN are not supported.

GTX Transceiver Data Rate

The maximum GTX transceiver data rate (F_{GTXMAX}) is 6.6 Gb/s in the -1 speed grade.

Power

Static Power

All power supplies can exhibit up to 25% higher static current compared to the static current reported in XPE.

Also, up to an additional 30 mA per used transceiver, and up to an additional 50 mA per powered transceiver quad can be consumed by the $V_{MGTAVCC}$ supply. And, up to an additional 50 mA per powered transceiver quad can be consumed by the $V_{MGTAVTT}$ supply.

Design Tool Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.03 (or later) of Xilinx® ISE® Design Suite 13.4 (or later) available at <http://www.xilinx.com/support/download/>. The -2 speed grade devices designed with ISE Design Suite 14.2 require a patch; see [Answer Record 50886](#).
- For GTX transceiver attribute updates, refer to [Answer Record 45360](#).
- See Virtex-7 FPGA [Answer Record 46345](#) for known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Hardware Validation for Memory Interfaces

The memory interfaces listed in [Table 2](#) have been validated in hardware across the operating conditions for these devices at the time of publication. See [Answer Record 46521](#) for the latest hardware validation information.

Table 2: Hardware Validated Memory Interfaces

Type	Condition	Bank
DDR3	DIMM and Component Single Rank	HP
QDRII+	Component Single Rank	HP
RLDRAMII	Component Single Rank	HP
DDR2	DIMM and Component Single Rank	HP

Traceability

Figure 1 shows an example device top mark for the devices listed in [Table 1](#).

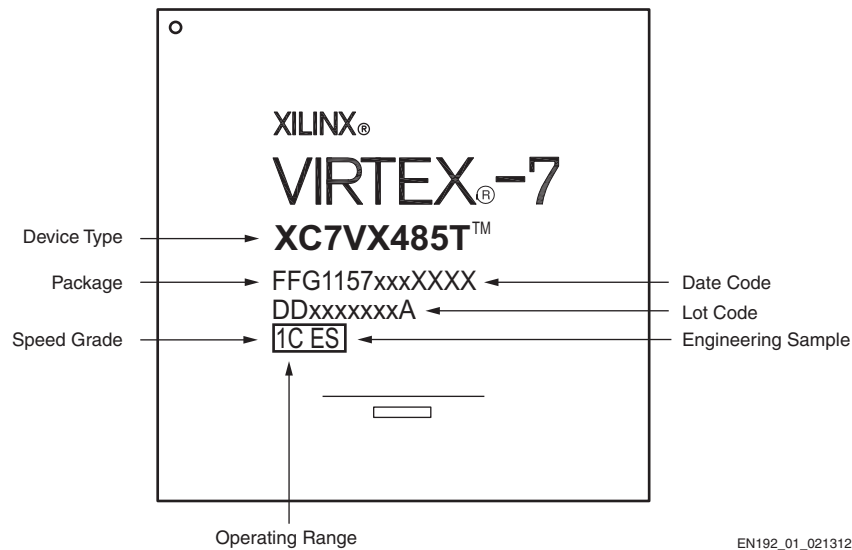


Figure 1: Example Device Top Mark

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Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/16/12	1.0	Initial Xilinx release.
02/28/12	1.1	Updated XADC . Added QPLL Upper Band Usage and Hardware Validation for Memory Interfaces .
10/25/12	1.2	Added XC7VX485T to the document. Added GTX Transceiver Data Rate . Updated XADC section to remove specifications that were updated in DS183, <i>Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics</i> v1.4, May 23, 2012. Updated GTX Transceiver Power-Up/Power-Down , Design Tool Requirements , and Hardware Validation for Memory Interfaces . Removed Physical Interface Rate for Memory Interfaces because the DDR3 requirement for data rates above 800 Mb/s was added to DS183, <i>Virtex-7 T and XT FPGAs Data Sheet: DC and .Switching Characteristics</i> v1.4, May 23, 2012.
02/26/13	1.3	Updated IEEE Std 1149.1 and IEEE Std 1149.6 for GTX Transceivers.

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