

Introduction

Thank you for participating in the Virtex®-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades
Virtex-7	XC7VX690T CES9937	0	All	-1, -2

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

GTH Transceivers

GTH Transceiver Power-On/Power-Off

While $V_{MGTAVCC}$ is powered within its recommended operating range and $V_{MGTAVTT}$ is below 0.7V, an additional 70 mA per transceiver is drawn from $V_{MGTAVCC}$.

Depending on the number of transceivers used, this extra current can be greater than the consumption reported in XPE.

Refer to [Answer Record 47443](#) for more information.

GTH Transceiver Eye Scan

To use the GTH receiver eye scan, RX_DATA_WIDTH must be set to 16, 32, or 64. Refer to [Answer Record 47128](#) for more information.

GTH Transceiver Link Margin Reduction

For GTH transceiver line rates up to 8.5 Gb/s, there can be up to a 0.05 UI increase in transmitter output jitter and up to a 0.05 UI decrease in receiver input jitter tolerance when multiple channels are used.

For GTH transceiver line rates higher than 8.5 Gb/s, there can be up to a 0.1 UI increase in transmitter output jitter and up to a 0.1 UI decrease in receiver input jitter tolerance when multiple channels are used.

See [Answer Record 47128](#) for additional information.

RXOUTCLK Port

For GTH transceiver line rates higher than 8.5 Gb/s, the GTH transceiver RXOUTCLK port, when configured to use the RXOUTCLKPCS or RXOUTCLKPMA path, can exhibit a phase jump of up to 2 UI of the line rate.

For the following applications:

- Buffer use mode: Specify an INPUT_JITTER timing constraint of 2 UI on the RXOUTCLK clock period.
- Buffer bypass mode: RXOUTCLK port cannot be used.

See [Answer Record 47128](#) for additional information.

PCIe

Virtual Channel Capability

The Virtual Channel Capability is always enabled in Configuration Space when the Secondary PCI Express® Capability is enabled.

Virtual Channel TC/VC Map

The Virtual Channel Resource Control register TC/VC Map is incorrectly reset to 8'h01 instead of the PCIe Base Specification 3.0 value of 8'hFF.

Loopback Exit

Reset of the LTSSM state machine is required to exit Loopback.Active state in loopback slave mode at Gen3 link speed.

Power Budgeting Capability

The Power Budgeting Capability is not supported.

Resizable BAR

The optional PCIe Resizable BAR (RBAR) capability is not supported through configuration. The RBAR feature can be initiated after the FPGA has been configured.

End-to-End CRC

When End-to-End CRC (ECRC) is used with multiple functions (PF0 and PF1 enabled), then ECRC must be enabled for either both functions or neither. It cannot be enabled independently on a per function basis. If only PF0 is used, then ECRC can be enabled or disabled as required.

TLP Processing Hints

The TLP Processing Hints (TPH) Completer is not supported.

D1 Power State

The D1 lower power device state is not supported.

Root Port

Root Port mode is not supported.

AER Header Log Overflow

For the Virtual Function Configuration Space, the optional AER Correctable Error Status register Header Log Overflow Status bit is not supported.

Function Level Reset

Function Level Reset (FLR) of SR-IOV Physical Functions is not supported. The ARI Capable Hierarchy bit in the Physical Function SR-IOV Control register is reset by a Function Level Reset of the Physical Function.

Power

Static Power

All power supplies can exhibit up to 50% higher static current compared to the static current reported in XPE.

Also, up to an additional 50 mA per powered transceiver Quad can be consumed by the $V_{MGTAVCC}$ supply.

Design Tool Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.03 (or later) of Xilinx® ISE® Design Suite 14.1 (or later) or Vivado™ Design Suite 2012.1 (or later) available at <http://www.xilinx.com/support/download/>
- For GTH transceiver attribute updates, refer to [Answer Record 47128](#).
- See Virtex-7 FPGA [Answer Record 47476](#) for the most current known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Hardware Validation for Memory Interfaces

The memory interfaces listed in [Table 2](#) have been validated in hardware across the operating conditions for these devices at the time of publication. See [Answer Record 46521](#) for the latest hardware validation information.

Table 2: Hardware Validated Memory Interfaces

Type	Condition	Bank
DDR3	DIMM and Component Single Rank	HP
QDRII+	Component Single Rank	HP
RLDRAMII	Component Single Rank	HP
DDR2	DIMM and Component Single Rank	HP

Traceability

Figure 1 shows an example device top mark for the devices listed in Table 1.

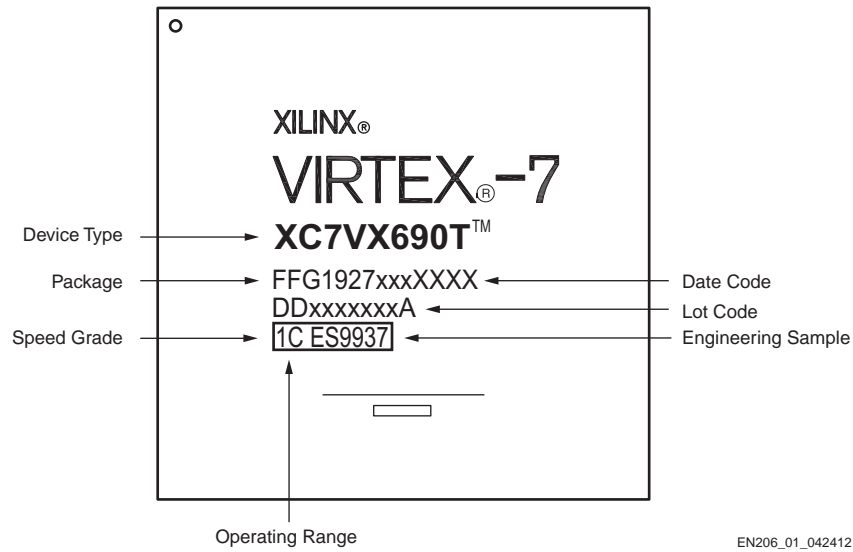


Figure 1: Example Device Top Mark

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/02/12	1.0	Initial Xilinx release.
05/24/12	1.1	Added -2 speed grade, Virtual Channel Capability , RXOUTCLK Port , PCIe , and Power Budgeting Capability . Updated Virtual Channel Capability and Design Tool Requirements . Changed ARI Capable Hierarchy to Function Level Reset and updated text. Removed Configuration Readback issue because it does not affect customer designs.
09/07/12	1.2	Removed the XADC errata because the specifications were added to DS183, Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics (v1.4) May 23, 2012. Removed the recommended sequence from GTH Transceiver Power-On/Power-Off because the specifications were added to DS183, Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics (v1.5) August 3, 2012. Updated GTH Transceiver Link Margin Reduction to change units from percentage to UI. Removed MGTA VCC Voltage Requirement errata because the requirement was added to DS183, Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics (v1.5) August 3, 2012. Updated Root Port . Removed the Physical Interface Rate for Memory Interfaces errata because the operating condition was added to DS183, Virtex-7 T and XT FPGAs Data Sheet: DC and Switching Characteristics (v1.4) May 23, 2012.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

Engineering Sample Disclaimer

ENGINEERING SAMPLE (ES) DEVICES ARE MADE AVAILABLE SOLELY FOR PURPOSES OF RESEARCH, DEVELOPMENT AND PROTOTYPING. ALL ES DEVICES ARE SOLD "AS-IS" WITH NO WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED. XILINX DOES NOT WARRANT THAT ES DEVICES ARE FULLY VERIFIED, TESTED, OR WILL OPERATE IN ACCORDANCE WITH DATA SHEET SPECIFICATIONS. XILINX DISCLAIMS ANY OBLIGATIONS FOR TECHNICAL SUPPORT AND BUG FIXES. XILINX SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION DIRECT, INDIRECT, INCIDENTAL, SPECIAL, RELIANCE, OR CONSEQUENTIAL DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF ES DEVICES IN ANY MANNER WHATSOEVER, EVEN IF XILINX HAS BEEN ADVISED OF THE POSSIBILITY THEREOF. XILINX MAKES NO REPRESENTATION THAT ES DEVICES PROVIDE ANY PARTICULAR FUNCTIONALITY, OR THAT ES DEVICES WILL MEET THE REQUIREMENTS OF A PARTICULAR USER APPLICATION. XILINX DOES NOT WARRANT THAT ES DEVICES ARE ERROR-FREE, NOR DOES XILINX MAKE ANY OTHER REPRESENTATIONS OR WARRANTIES, WHETHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, INCLUDING, WITHOUT LIMITATION, IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. THE FOREGOING STATES THE ENTIRE LIABILITY OF XILINX WITH RESPECT TO ES DEVICES.