Introduction

Thank you for participating in the Artix™-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: Devices Affected by These Errata

<table>
<thead>
<tr>
<th>Product Family</th>
<th>Device</th>
<th>JTAG ID (Revision Code)</th>
<th>Packages</th>
<th>Speed Grades</th>
<th>Junction Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Artix-7</td>
<td>XC7A100T CES</td>
<td>0</td>
<td>All</td>
<td>-1, -2</td>
<td>0°C to 85°C</td>
</tr>
<tr>
<td></td>
<td>XC7A200T CES</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>XC7A100T CES9910</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>XC7A200T CES9910</td>
<td></td>
<td></td>
<td></td>
<td>−40°C to 100°C</td>
</tr>
</tbody>
</table>

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

IEEE Std 1149.1 Boundary-Scan

**IEEE Std 1149.1 for Dedicated and SelectIO Resources (Applies only to XC7A100T Device)**

IEEE Std 1149.1 (JTAG) boundary-scan test commands SAMPLE, PRELOAD, EXTEST, and HIGHZ are not functional. All other JTAG commands, including device configuration and the ChipScope™ debugging tool, function as expected.

Design Tool Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx Design Tools:

- For GTP transceiver attribute updates, refer to Answer Record 47852.
- See Artix-7 FPGA Answer Record 52049 for the most current known issues and work-arounds for Xilinx Design Tools.
Traceability

Figure 1 shows an example device top mark for the devices listed in Table 1.

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact/index.htm.
## Revision History

The following table shows the revision history for this document:

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Description of Revisions</th>
</tr>
</thead>
<tbody>
<tr>
<td>10/25/12</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
<tr>
<td>05/03/13</td>
<td>1.1</td>
<td>Removed XADC-ADC Accuracy because the specifications are now included in the data sheet, DS181, <em>Artix-7 FPGAs Data Sheet: DC and Switching Characteristics</em>, v1.5, February 1, 2013. Updated Design Tool Requirements.</td>
</tr>
</tbody>
</table>

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