Zynq UltraScale+ RFSoC Production Errata

EN291 (v1.5) March 29, 2021 **Errata Notification**

Introduction

Thank you for designing with the Zynq® UltraScale+™ RFSoC family. Although Xilinx has made every effort to ensure the highest possible quality, the devices listed in Table 1 are subject to the limitations described in the following errata.

Devices

These errata apply to one or more of the devices shown in Table 1. Refer to the **Device** column of Table 2 for specific device applicability for each errata item.

Table 1: **Devices Affected by These Errata**

Product Family	Device	Speed Grade	Junction Temperature Range	IDCODE[31:0](1)	Package
Zynq UltraScale+ RFSoC	XCZU21DR	All	All	147E1093	All
	XCZU25DR			147E5093	
	XCZU27DR			147E4093	
	XCZU28DR			147E0093	
	XCZU29DR			147E2093	
	XCZU39DR			147E6093	
	XCZU43DR			147FD093	
	XCZU46DR			147F8093	
	XCZU47DR			147FF093	
	XCZU48DR			147FB093	
	XCZU49DR			147FE093	
XQ Zynq UltraScale+ RFSoC	XQZU21DR	All	All	147E1093	All
	XQZU28DR			147E0093	
	XQZU29DR			147E2093	
	XQZU48DR			147FB093	
	XQZU49DR			147FE093	

Notes:

1. The most-significant hexadecimal digit (IDCODE[31:28]) is a revision field. These errata affect devices with the shown revision, or later.

Links to Detailed Errata Descriptions

This section provides links to detailed descriptions of each issue known at the release time of this document. Additional information, including any work-arounds, is available in the associated answer record linked from each errata description. A list of software tools that implement errata work-arounds is found in Xilinx Answer 68750.

In the summary tables, the Topic and Errata Issue items listed in the "Errata Issue" column are clickable links to the more detailed information in the body of the document. Topics are listed in *alphabetical order*, while errata issues, *within each topic,* are listed in *reverse chronological order* (i.e., new issues listed first). New, updated, or newly closed errata issues appear in ***blue, bold, italic*** type; existing errata or previously closed errata issues appear in regular blue type.

Table 2: **Summary Table of Processing System Issues**

Errata Issue	Device	Xilinx Answer(1)	Status
Processing System (PS) Errata			
Application Processing Unit			
PMU Counter Values Might Be Inaccurate When Monitoring Certain Events	All	68878	Will Not Fix
An Eviction Might Overtake A Cache Clean Operation	All	68874	Will Not Fix
A Store-Exclusive Instruction Might Pass When It Should Fail	All	68875	Will Not Fix
Loads Of Mismatched Size Might Not Be Single-Copy Atomic	All	68876	Will Not Fix
Reads Of PMEVCNTR<n> Are Not Masked By HDCR.HPMN	All	68877	Will Not Fix
AArch64 Unconditional Branch Might Jump To Incorrect Address	All	68880	Will Not Fix
Direct Branch Instructions Executed Before A Trace Flush Might Be Output In An Atom Packet After Flush Acknowledgment	All	68882	Will Not Fix
APB Data Is Not Masked When PSLVERR Is Set	All	68946	Will Not Fix
Incorrect Prefetch In V7S Mode	All	66115	Will Not Fix
Updating A Translation Entry To Change Page Size Might Cause Data Corruption	All	66116	Will Not Fix
Instruction Sequences Containing AES Instructions Might Produce Incorrect Results	All	65853	Will Not Fix
Load Might Read Incorrect Data	All	65854	Will Not Fix
Memory Locations Might Be Accessed Speculatively Due To Instruction Fetches When HCR.VM Is Set	All	65855	Will Not Fix
Non-Allocating Reads Might Prevent A Store Exclusive From Passing	All	65857	Will Not Fix
Write Of JMCR In EL0 Does Not Generate An UNDEFINED Exception	All	65858	Will Not Fix

Table 2: **Summary Table of Processing System Issues *(Cont'd)***

Errata Issue	Device	Xilinx Answer(1)	Status
Boot and Configuration			
Boot From NAND Might Fail If There Is Data Corruption In The First Parameter Page	All	68615	Will Not Fix
Controller for PCI Express			
Sending Modified Compliance Pattern Requires Additional PCIe Register Programming	All	68534	Will Not Fix
PCIe DMA Status Update Might Happen After Interrupt Is Generated	All	68535	Will Not Fix
Under Heavy Read Traffic Conditions, The AXI-PCIe Bridge Arbitration Algorithm Might Incorrectly Select A Winning Requestor	All	68536	Will Not Fix
AXI-PCIe Bridge Does Not Drop MemWr TLP With ECRC Errors	All	68537	Will Not Fix
PCIe Generates Two Fatal Errors For Poisoned CfgWr TLPs	All	68539	Will Not Fix
PCIe Logs Incorrect Header In AER Register	All	68540	Will Not Fix
Controller For PCI Express Might Not Exit From Loopback Mode	All	68541	Will Not Fix
PCIe DMA Completion Error Status Bit From Aborted DMA Transfers Might Persist Through DMA Channel Reset	All	68542	Will Not Fix
DDR Memory Controller			
DDR Memory Controller Minimum Data Rate Is 1,000Mb/s	I and M Temperature Grade Devices	71707	Will Not Fix
LPDDR3/LPDDR4 Temperature Derating Does Not Work When Initial DRAM Temperature Is Greater Than 85°C	All	70769	Will Not Fix
DDR Memory Controller Does Not Meet tSTAB Requirement For DDR3/DDR4 RDIMMs	All	68543	Will Not Fix
Accessing Unimplemented Registers In DDR Controller Causes Slave Error	All	65865	Will Not Fix
Gigabit Ethernet Controller			
Incorrect Transmission Of Pause Frames In Response To Reception Of Pause Frames With Unicast Or Known Multicast Address	All	68546	Will Not Fix
I2C			
Dynamically Changing Controller Mode To Master From A Previous Slave Mode Might Cause Unnecessary Transfer On The I2C Bus	All	65869	Will Not Fix
PS-GTR			
Multi-lane Link Alignment Of PCIe Might Require Greater Than One SKP Ordered Set	All	65875	Will Not Fix
PS-GTR Ignores PCIe SKP Ordered Set With Odd Boundary Alignment	All	68547	Will Not Fix

Table 2: **Summary Table of Processing System Issues *(Cont'd)***

Errata Issue	Device	Xilinx Answer(1)	Status
Real-Time Processing Unit (RPU)			
Self-Modify Code In Non-Cacheable Memory Might Not Work With A Slow Memory System	All	68548	Will Not Fix
Processor Might Deadlock Or Lose Data When Configured With Cache-ECC	All	65878	Will Not Fix
Watchpoint Access In A Store Multiple Is Not Masked	All	65879	Will Not Fix
SATA Controller			
Switching From Slumber Or Partial Sleep To The Active State Does Not Always Work Properly	All	68971	Will Not Fix
Incorrect Indication Of Overflow As CRC Error	All	65880	Will Not Fix
Incorrect SRST Completion Indication To SATA Host Software	All	65881	Will Not Fix
SATA Device Sleep State Is Not Supported In The Controller	All	65882	Will Not Fix
SD/SDIO/eMMC Controller			
In An Asynchronous Multiprocessing Environment, The SD/SDIO Tap Delays Might Get Asynchronously Updated, Resulting In Incorrect Configuration Of Tap Delay Settings	All	68549	Will Not Fix
Default Value Of SDIO Auto-Tuning Refresh Register Is Incorrect	All	68550	Will Not Fix
SD Auto-Tuning Requires Received Data Buffer To Be Emptied By Software	All	68551	Will Not Fix
Switching From 64-Bit DMA Mode To 32-Bit DMA Mode Might Cause Incomplete Data Transfer	All	65883	Will Not Fix
Security			
PS DNA Is Not Write Protected And Is Different Than PL DNA	All	71342	Will Not Fix
SPI Controller			
SPI Controller Might Not Update RX_NEMPTY Flag, Showing Incorrect Status Of The Receive FIFO	All	65885	Will Not Fix
System Test and Debug			
PS DDR Inputs Do Not Switch To Boundary-Scan Compatible Mode	All	69180	Will Not Fix
ETM Might Assert AFREADY Before All Data Has Been Output	All	68879	Will Not Fix
ETM Might Lose Counter Events While Entering wfx Mode	All	68883	Will Not Fix
ETM Might Trace An Incorrect Exception Address	All	68884	Will Not Fix
APB Access To ETM Space While Core Is In Retention Will Never Complete	All	68885	Will Not Fix
ETM Does Not Report IDLE State When Disabled And Using OS Lock	All	68886	Will Not Fix
ATB Asynchronous Bridge Breaks Discovery In Integration Mode	All	65887	Will Not Fix
TPIU Fails To Output Sync After The Pattern Generator Is Disabled In Normal Mode	All	65889	Will Not Fix
Reset State Of ATB Flush Acknowledge Is Incorrect	All	65890	Will Not Fix

Table 2: **Summary Table of Processing System Issues *(Cont'd)***

Errata Issue	Device	Xilinx Answer(1)	Status
Timestamp Replicator Might Stall Synchronization	All	65892	Will Not Fix
USB 2.0 / 3.0 Host and Device, and USB 2.0 OTG Controller			
System Might Hang During Suspend/Resume Stages	All	67667	Will Not Fix
The tPortConfiguration Timer Resets During Recovery, Violating USB 3.0 Specification	All	68553	Will Not Fix
USB 2.0 Host Controller Does Not Assert Port Reset In Resume State	All	68554	Will Not Fix
Incorrect Assertion Of Hot Reset Might Occur In USB 3.0 Host Mode	All	68555	Will Not Fix
Request For U3 Transition Might Get Dropped When The USB 3.0 Host Controller Transitions From U1 To U2 State	All	68556	Will Not Fix
USB Full-Speed Device Does Not Enter Hibernation State During Disconnect	All	68557	Will Not Fix

Notes:

1. A list of software tools that implement errata work-arounds is found in Xilinx Answer 68750.

Processing System (PS) Errata Detailed Descriptions

Application Processing Unit

PMU Counter Values Might Be Inaccurate When Monitoring Certain Events

Xilinx Answer 68878

The performance monitor counters might be inaccurate when detecting some types of events.

This is a third-party errata (Arm, Inc. 855827); this issue will not be fixed.

An Eviction Might Overtake A Cache Clean Operation

Xilinx Answer 68874

The memory store transaction order for simultaneous cache line eviction trigger and cache clean operation might be stored to memory in the wrong order.

This is a third-party errata (Arm, Inc. 855873); this issue will not be fixed.

A Store-Exclusive Instruction Might Pass When It Should Fail

Xilinx Answer 68875

A Load-Exclusive instruction to cacheable memory might set the monitor to the exclusive state when the processor does not have exclusive access to the line. A subsequent Store-Exclusive instruction might pass when it should fail.

This is a third-party errata (Arm, Inc. 855872); this issue will not be fixed.

Loads Of Mismatched Size Might Not Be Single-Copy Atomic

Xilinx Answer 68876

In some unusual code sequences, the CPU might not meet the requirements of a single-copy atomic load.

This is a third-party errata (Arm, Inc. 855830); this issue will not be fixed.

Reads Of PMEVCNTR<n> Are Not Masked By HDCR.HPMN

Xilinx Answer 68877

EL2 software might not always restrict access to the performance counters by non-secure EL0 and EL1 software to a subset of the counters.

This is a third-party errata (Arm, Inc. 855829); this issue will not be fixed.

AArch64 Unconditional Branch Might Jump To Incorrect Address

Xilinx Answer 68880

When executing in AArch64 state with address translation disabled and under certain conditions, an unconditional immediate branch instruction to a single specific address might jump to an incorrect address.

This is a third-party errata (Arm, Inc. 852521); this issue will not be fixed.

Direct Branch Instructions Executed Before A Trace Flush Might Be Output In An Atom Packet After Flush Acknowledgment

Xilinx Answer 68882

When trace is enabled, the processor attempts to combine multiple direct branch instructions into a single atom packet. If an atom packet is in the process of being generated, the processor does not force completion of the packet prior to acknowledging the flush request.

This is a third-party errata (Arm, Inc. 852071); this issue will not be fixed.

APB Data Is Not Masked When PSLVERR Is Set

Xilinx Answer 68946

When the APB access to the performance monitor, breakpoint, or watchpoint registers is disabled, the register value is erroneously included with the APB response.

This is a third-party errata (Arm, Inc. 855874); this issue will not be fixed.

Incorrect Prefetch In V7S Mode

Xilinx Answer 66115

Under certain conditions, the Cortex-A53 MPCore memory management unit (MMU) might incorrectly prefetch a single descriptor past the 1KB boundary of the L2 table, resulting in a prefetch abort.

This is a third-party errata (Arm, Inc. 826419); this issue will not be fixed.

Updating A Translation Entry To Change Page Size Might Cause Data Corruption

Xilinx Answer 66116

When the MMU prefetches a translation table entry and the page size of the prefetched translation table entry has changed, then the MMU updates the cache with incorrect translation table attributes that do not correspond to the old or the new entry.

This is a third-party errata (Arm, Inc. 841119); this issue will not be fixed.

Instruction Sequences Containing AES Instructions Might Produce Incorrect Results

Xilinx Answer 65853

Certain sequences of instructions that include AES instructions might cause incorrect results to be generated when executed in AArch64 state on the Cortex-A53 processor.

This is a third-party errata (Arm, Inc. 845819); this issue will not be fixed.

Load Might Read Incorrect Data

Xilinx Answer 65854

When executing in AArch32 state at EL0, a load instruction to the same offset within a different 4GB region as a recent previous load in AArch64 state might read incorrect data.

This is a third-party errata (Arm, Inc. 845719); this issue will not be fixed.

Memory Locations Might Be Accessed Speculatively Due To Instruction Fetches When HCR.VM Is Set

Xilinx Answer 65855

The Armv8 architecture requires that when all associated stages of translation are disabled for the current exception level, memory locations are only accessed due to instruction fetches within the same or next translation granule while an instruction that has been or will be fetched due to sequential execution.

This is a third-party errata (Arm, Inc. 843819); this issue will not be fixed.

Non-Allocating Reads Might Prevent A Store Exclusive From Passing

Xilinx Answer 65857

If an Arm Cortex-A53 processor is executing a load and store exclusive instruction in a loop, certain allowed conditions might cause the store exclusive instruction to repeatedly fail. This includes another processor repeatedly writing to the same cache line. In addition, a non-allocating load from another processor might also cause the store exclusive instruction to repeatedly fail.

This is a third-party errata (Arm, Inc. 836870); this issue will not be fixed.

Write Of JMCR In EL0 Does Not Generate An UNDEFINED Exception

Xilinx Answer 65858

When EL0 is using AArch32 register width state and a write is performed in EL0 to JMCR, the write is permitted but ignored. The intended behavior is that the instruction should be UNDEFINED.

This is a third-party errata (Arm, Inc. 836919); this issue will not be fixed.

Boot and Configuration

Boot From NAND Might Fail If There Is Data Corruption In The First Parameter Page

Xilinx Answer 68615

When NAND is used as the primary boot device and there is data or CRC corruption in the first parameter page, the CSU Boot ROM (CBR) might fail to boot from the NAND device.

This issue will not be fixed.

Controller for PCI Express

Sending Modified Compliance Pattern Requires Additional PCIe Register Programming

Xilinx Answer 68534

The controller for PCIe is capable of sending both a compliance pattern and a modified compliance pattern. Transmission of a modified compliance pattern requires programming of Device Control Register 2, Enter Modified Compliance bit set to 1.

This issue will not be fixed.

PCIe DMA Status Update Might Happen After Interrupt Is Generated

Xilinx Answer 68535

The PCIe DMA controller's data transfer completion status might get updated after a completion interrupt is generated when the destination for the interrupt is configured as PCIe.

This issue will not be fixed.

Under Heavy Read Traffic Conditions, The AXI-PCIe Bridge Arbitration Algorithm Might Incorrectly Select A Winning Requestor

Xilinx Answer 68536

Under heavy read traffic conditions, the AXI-PCIe bridge might incorrectly select a winning port requesting arbitration, resulting in additional delay for completion of read requests from specific sources.

This issue will not be fixed.

AXI-PCIe Bridge Does Not Drop MemWr TLP With ECRC Errors

Xilinx Answer 68537

The AXI-PCIe bridge does not drop MemWr TLPs with ECRC errors. The host software must check Advanced Error Reporting (AER) registers and determine if there are errors in the packet. An interrupt can be generated to indicate the condition in software.

This issue will not be fixed.

PCIe Generates Two Fatal Errors For Poisoned CfgWr TLPs

Xilinx Answer 68539

When configured as an Endpoint, the controller for PCIe transmits two fatal error message packets to the link partner for poisoned CfgWr requests, instead of one.

This issue will not be fixed.

PCIe Logs Incorrect Header In AER Register

Xilinx Answer 68540

When advanced error reporting (AER) is enabled and the controller for PCIe receives an unexpected completion packet, it logs the AER header register incorrectly with all 1s.

This issue will not be fixed.

Controller For PCI Express Might Not Exit From Loopback Mode

Xilinx Answer 68541

When loopback is enabled in PCIe Gen2 mode and a rate change is requested by the link partner followed by a loopback exit request, the controller might not exit loopback mode if Electrical Idle Ordered Sets (EIOSs) are dropped at the receiver.

This issue will not be fixed.

PCIe DMA Completion Error Status Bit From Aborted DMA Transfers Might Persist Through DMA Channel Reset

Xilinx Answer 68542

When a PCIe DMA transfer is aborted and the PCIe DMA channel is unable to finish the DMA transfer, the DMA completion register error status bit persists after a DMA reset is issued.

This issue will not be fixed.

DDR Memory Controller

DDR Memory Controller Minimum Data Rate Is 1,000Mb/s

Xilinx Answer 71707

The PS DDR memory controller minimum data rate is 1,000Mb/s for industrial (I) and military (M) temperature grade devices. Extended (E) temperature grade devices are not affected.

This issue will not be fixed.

LPDDR3/LPDDR4 Temperature Derating Does Not Work When Initial DRAM Temperature Is Greater Than 85°C

Xilinx Answer 70769

The PS DDR memory controller defaults to an initial nominal 1x refresh rate (1x tREFI), and only updates the refresh rate when the temperature update flag (TUF) from MR4[7] is 1.

If the LPDDR3/LPDDR4 memory starts above 85°C, the TUF will not be asserted. Thus, the controller will not adjust the DRAM refresh rate and the associated temperature derating AC timing parameters.

This issue will not be fixed.

DDR Memory Controller Does Not Meet tSTAB Requirement For DDR3/DDR4 RDIMMs

Xilinx Answer 68543

When the PS DDR3/DDR4 clock is enabled after exiting from a power-save mode, the stabilization time tSTAB for DDR3/DDR4 RDIMM is not guaranteed, which causes a violation of the registering clock driver specification.

This issue will not be fixed.

Accessing Unimplemented Registers In DDR Controller Causes Slave Error

Xilinx Answer 65865

When an unimplemented register in the PS DDR controller is accessed by a read or write operation, a slave error is incorrectly returned.

This issue will not be fixed.

Gigabit Ethernet Controller

Incorrect Transmission Of Pause Frames In Response To Reception Of Pause Frames With Unicast Or Known Multicast Address

Xilinx Answer 68546

When the Gigabit Ethernet controller receives pause frames with a destination address not set to a known multicast address or unicast address, the controller does not inhibit transmission and transmits pause frames incorrectly, leading to compliance failure.

This issue will not be fixed.

I2C

Dynamically Changing Controller Mode To Master From A Previous Slave Mode Might Cause Unnecessary Transfer On The I2C Bus

Xilinx Answer 65869

When the I2C controller's mode is dynamically changed from slave to master after a slave address is written, an unwanted start condition might be generated, causing unnecessary transfers on the bus.

This issue will not be fixed.

PS-GTR

Multi-lane Link Alignment Of PCIe Might Require Greater Than One SKP Ordered Set

Xilinx Answer 65875

The PS-GTR block might repeat or drop two bytes of data during multi-lane link alignment, causing data corruption in the controller for PCIe. The corruption continues until the next SKP ordered set (OS) is received. PCIe protocol is capable of handling such errors by re-transmitting the packets that have not been received by the connected device. No work-around is necessary. There is no impact on PCIe performance.

This issue will not be fixed.

PS-GTR Ignores PCIe SKP Ordered Set With Odd Boundary Alignment

Xilinx Answer 68547

The deskew block in the PS-GTR block ignores the PCIe SKP ordered set (OS) that is aligned to an odd word boundary. It performs lane-to-lane deskew based on an even word boundary.

This issue will not be fixed.

Real-Time Processing Unit (RPU)

Self-Modify Code In Non-Cacheable Memory Might Not Work With A Slow Memory System

Xilinx Answer 68548

The Cortex-R5F processor might execute an old instruction or a corrupted instruction when a program executing on the processor writes to a non-cacheable memory location that is subsequently used to execute an instruction.

This is a third-party errata (Arm, Inc. 853474). This issue will not be fixed.

Processor Might Deadlock Or Lose Data When Configured With Cache-ECC

Xilinx Answer 65878

In a very rare scenario, when the Cortex-R5F processor accesses the cache memory with ECC enabled, resulting in an L1 data cache miss, the store buffer present in the Cortex-R5F processor might enter into a state that prevents any write transactions to proceed to the L1 cache memory or L2 memory system, causing prevention of instruction execution or write data loss scenarios.

This is a third-party errata (Arm, Inc. 780125); this issue will not be fixed.

Watchpoint Access In A Store Multiple Is Not Masked

Xilinx Answer 65879

The Arm Cortex-R5F processor implements synchronous watchpoints. A synchronous watchpoint generated during a store multiple instruction must ensure that the watchpointed access does not perform writes on the bus to update memory. This requirement is not met, and the processor incorrectly updates memory for a watchpointed access.

This is a third-party errata (Arm, Inc. 756523); this issue will not be fixed.

SATA Controller

Switching From Slumber Or Partial Sleep To The Active State Does Not Always Work Properly

Xilinx Answer 68971

Wakeup occurs from slumber or partial sleep using the PxCMD [ICC] interface communication control bits, but the controller does not signal the PxIS [DHRS] interrupt response bit, causing the interrupt handler to hang. When using the DMA trigger wakeup bit in the PxCI register, the controller does not initiate an H2D FIS command to the device, causing software to time out and re-enumerate the device.

This issue will not be fixed.

Incorrect Indication Of Overflow As CRC Error

Xilinx Answer 65880

The SATA controller reports a CRC error instead of an overflow error in the PxSERR register when there is an overflow condition.

This issue will not be fixed.

Incorrect SRST Completion Indication To SATA Host Software

Xilinx Answer 65881

When the SATA host controller software sends SRST OFF FIS to the device, the controller does not set the BSY bit, which incorrectly communicates completion of the SRST FIS command to the host software.

This issue will not be fixed.

SATA Device Sleep State Is Not Supported In The Controller

Xilinx Answer 65882

The SATA controller does not support device sleep state.

This issue will not be fixed.

SD/SDIO/eMMC Controller

In An Asynchronous Multiprocessing Environment, The SD/SDIO Tap Delays Might Get Asynchronously Updated, Resulting In Incorrect Configuration Of Tap Delay Settings

Xilinx Answer 68549

The SD/SDIO controllers share a common register (with different bit fields) for configuring the tap delay values. In an asynchronous multiprocessing environment, when each processor updates the tap delay settings asynchronously, it is possible that the tap delay settings are not properly updated when the following conditions occur:

1. Processor 0 reads tap delay register for SD/SDIO controller instance 0
2. Processor 1 reads tap delay register for SD/SDIO controller instance 1 (which is the same as instance 0)
3. Processor 1 writes tap delay register for SD/SDIO controller instance 1 (which is the same as instance 0)
4. Processor 0 over-writes (based on step 1) tap delay register for SD/SDIO controller instance 1 (which is the same as instance 0)

Software needs to ensure that only one processor updates the tap delay configurations.

This issue will not be fixed.

Default Value Of SDIO Auto-Tuning Refresh Register Is Incorrect

Xilinx Answer 68550

The default value of the auto-tuning refresh register is incorrect and indicates auto-tuning needs to be triggered periodically by the SDIO software.

This issue will not be fixed.

SD Auto-Tuning Requires Received Data Buffer To Be Emptied By Software

Xilinx Answer 68551

During the auto-tuning process, the SD host controller fills the received buffer with training data, which needs to be emptied by host software after auto-tuning is completed.

This issue will not be fixed.

Switching From 64-Bit DMA Mode To 32-Bit DMA Mode Might Cause Incomplete Data Transfer

Xilinx Answer 65883

When the DMA transfer mode is dynamically changed from 64-bit mode to 32-bit mode in the SD/SDIO controller, the DMA fails to complete the data transfer and generates an error response.

This issue will not be fixed.

Security

PS DNA Is Not Write Protected And Is Different Than PL DNA

Xilinx Answer 71342

The PS DNA value, which is read via PS APB addresses `0xFFCC100C`, `0xFFCC1010`, and `0xFFCC1014`, or read via the SDK XilSKey_ZynqMp_EfusePs_ReadDna API, is not protected against change from intentional writes. Use the PL DNA for applications requiring an unchangeable, unique device identifier. The PS DNA value is different than the PL DNA value, which is used with 2D barcode device lookup.

This issue will not be fixed.

SPI Controller

SPI Controller Might Not Update RX_NEMPTY Flag, Showing Incorrect Status Of The Receive FIFO

Xilinx Answer 65885

The RX_NEMPTY flag in the SPI Controller is not updated for every change in the received FIFO's threshold value. The flag might show an incorrect value and might not reflect the RX FIFO non-empty status.

This issue will not be fixed.

System Test and Debug

PS DDR Inputs Do Not Switch To Boundary-Scan Compatible Mode

Xilinx Answer 69180

The PS DDR inputs do not switch to a boundary-scan compatible mode during the JTAG EXTEST, EXTEST_PULSE, or EXTEST_TRAIN operations and can fail to capture valid input High signal values.

This issue will not be fixed.

ETM Might Assert AFREADY Before All Data Has Been Output

Xilinx Answer 68879

The ready signal from the AMBA Trace Bus (ATB) might assert before the entire trace is output.

This is a third-party errata (Arm, Inc. 853172); this issue will not be fixed.

ETM Might Lose Counter Events While Entering wfx Mode

Xilinx Answer 68883

If the ETM resources become inactive because of low-power state, there is a one-cycle window during which the counters and the sequencer might ignore counter-at-zero resources.

This is a third-party errata (Arm, Inc. 851871); this issue will not be fixed.

ETM Might Trace An Incorrect Exception Address

Xilinx Answer 68884

Under certain conditions, the address in an exception packet might be incorrectly set to the target address of the exception. The trace stream is not corrupted.

This is a third-party errata (Arm, Inc. 851672); this issue will not be fixed.

APB Access To ETM Space While Core Is In Retention Will Never Complete

Xilinx Answer 68885

When a core is in retention mode, an APB request to the ETM causes the core to exit retention, but not drive PREADYDBG HIGH, and the APB transaction hangs.

This is a third-party errata (Arm, Inc. 853175); this issue will not be fixed.

ETM Does Not Report IDLE State When Disabled And Using OS Lock

Xilinx Answer 68886

When the OS Lock feature is used by software to disable the debug access, the ETM does not indicate when it is safe to power down.

This is a third-party errata (Arm, Inc. 855871); this issue will not be fixed.

ATB Asynchronous Bridge Breaks Discovery In Integration Mode

Xilinx Answer 65887

The ATB asynchronous bridge has no support for integration mode. A static 1 output at the source is transferred as a toggling signal to the sink instead of a static 1.

This issue will not be fixed.

TPIU Fails To Output Sync After The Pattern Generator Is Disabled In Normal Mode

Xilinx Answer 65889

When the TPIU is configured to operate in normal mode (FFCR.EnFCont==0), the synchronization sequence that is required between the test pattern and the trace data is not generated. Synchronization will be generated later as determined by the synchronization counter.

This is a third-party errata (Arm, Inc. 813569); this issue will not be fixed.

Reset State Of ATB Flush Acknowledge Is Incorrect

Xilinx Answer 65890

When any of the following components are held in reset, it will not respond to a flush request: ATB asynchronous bridge, ATB synchronous bridge, ATB funnel, ATB replicator, ATB upsizer, or ATB downsizer.

This is a third-party errata (Arm, Inc. 816720); this issue will not be fixed.

Timestamp Replicator Might Stall Synchronization

Xilinx Answer 65892

Under specific clock ratio conditions, the synchronization operation in the timestamp replicator unit might stall, preventing the timestamp consumers to synchronize with the timestamp replicator unit.

This is a third-party errata (Arm, Inc. 832019); this issue will not be fixed.

USB 2.0/3.0 Host and Device, and USB 2.0 OTG Controller

System Might Hang During Suspend/Resume Stages

Xilinx Answer 67667

When the USB controller is configured for USB 2.0 and suspend/resume power states are enabled, the controller sends the ULPI PHY a single command to select the termination and transceiver, causing the system to hang when the PHY requires that these be sent in two separate commands.

This issue will not be fixed.

The tPortConfiguration Timer Resets During Recovery, Violating USB 3.0 Specification

Xilinx Answer 68553

When the USB 3.0 link transitions through a recovery state before link management packets (LMPs) are exchanged, the tPortConfiguration timer in the controller resets, causing a violation of the USB 3.0 specification.

This issue will not be fixed.

USB 2.0 Host Controller Does Not Assert Port Reset In Resume State

Xilinx Answer 68554

When the USB 2.0 host controller is in resume state, it does not drive a port reset if register PORTSC.PR is set to 1.

This issue will not be fixed.

Incorrect Assertion Of Hot Reset Might Occur In USB 3.0 Host Mode

Xilinx Answer 68555

When the USB controller is configured in USB 3.0 host mode, the controller might incorrectly enter a recovery state instead of a U1/U2 state when the register PORTSC.PR is set to 1 within a certain timing window, causing a hot reset assertion.

This issue will not be fixed.

Request For U3 Transition Might Get Dropped When The USB 3.0 Host Controller Transitions From U1 To U2 State

Xilinx Answer 68556

In the USB 3.0 host mode, if a U3 transition is requested during a certain timing window of a U1 to U2 state transition, the U3 state transition request might be dropped by the controller.

This issue will not be fixed.

USB Full-Speed Device Does Not Enter Hibernation State During Disconnect

Xilinx Answer 68557

When the controller is configured as a full-speed device and a USB disconnect happens, the controller does not enter the hibernation state if there are pending IN tokens or acknowledgment packets from the host.

This issue will not be fixed.

Design Tool Requirements

Refer to DS926, *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* for the minimum Vivado® software releases required for production. Xilinx recommends using the latest supported release.

Traceability

The electronic IDCODE, unique electronic DNA serial number, and 2D barcode top mark provide traceability for the devices listed in Table 1. For more information about the 2D barcode, see https://www.xilinx.com/support/quality/support.html#2dBarcode.

Additional Questions or Clarification

For additional questions regarding these errata, contact your Xilinx Sales Representative: www.xilinx.com/company/contact/index.htm.

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at: www.xilinx.com/support.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/29/2021	1.5	Added XCZU43DR, XCZU46DR, XCZU47DR, XCZU48DR, XCZU49DR, XQZU48DR, and XQZU49DR devices. Updated Traceability.
02/14/2020	1.4	Replaced Watchpoint On A Load Or Store Multiple Might Be Missed with Watchpoint Access In A Store Multiple Is Not Masked.
07/15/2019	1.3	Added XCZU39DR to Table 1. Updated Figure 1.
12/07/2018	1.2	Added XQZU21DR, XQZU28DR, and XQZU29DR devices to Table 1. Added DDR Memory Controller Minimum Data Rate Is 1,000Mb/s.
08/20/2018	1.1	Added PS DNA Is Not Write Protected And Is Different Than PL DNA.
04/17/2018	1.0	Initial Xilinx release.

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