Introduction

The LogiCORE™ IP Aurora 8B/10B core supports the AMBA® protocol AXI4-Stream user interface. The core implements the Aurora 8B/10B protocol using the high-speed serial transceivers on the Virtex®-7 and Kintex™-7 families (including the -2L lower power devices); Virtex-6 LXT, SXT, CXT, HXT, and lower power families; and the Spartan®-6 LXT family.

The Aurora 8B/10B core is a scalable, lightweight, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented using Xilinx® FPGA technology. The protocol is typically used in applications requiring simple, low-cost, high-rate, data channels.

The CORE Generator™ software produces source code for Aurora 8B/10B cores with variable datapath width. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control.

Features

- General-purpose data channels with throughput range from 480 Mbps to 84.48 Gbps
- Supports up to any 16 of 56 Virtex-7/Kintex-7 FPGA GTX transceivers, 16 of 36 Virtex-6 FPGA GTX transceivers or 4 of 8 Spartan-6 FPGA GTP transceivers
- Aurora 8B/10B protocol specification v2.2 compliant
- Low resource cost (see Resource Utilization)
- Easy-to-use framing and flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation
- AXI4-Stream (framing) or streaming user interface

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[(1)]	Virtex-7, Kintex-7, Virtex-6, Spartan-6				
Supported User Interfaces	AXI4-Stream				
	Resources[(2)]				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.[(3)]**
Config1	2076	2307	0	0	330 MHz
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Test Bench	Verilog and VHDL				
Constraints File	User Constraints File (UCF)				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	CORE Generator tool				
Simulation[(4)]	ISim 13.3, Mentor Graphics ModelSim, and Cadence Incisive Enterprise Simulator (IES)				
Synthesis Tools[(4)]	XST 13.3, PlanAhead™ 13.3, and Synopsys Synplify Pro				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. For a complete listing of supported devices, see the release notes for this core.
2. For device performance numbers, see Table 2 through Table 13.
3. For more complete performance data, see Performance, page 13.
4. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Functional Overview

The Aurora 8B/10B core is a lightweight, serial communications protocol for multi-gigabit links. It is used to transfer data between devices using one or many GTP/GTX transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (Figure 1).

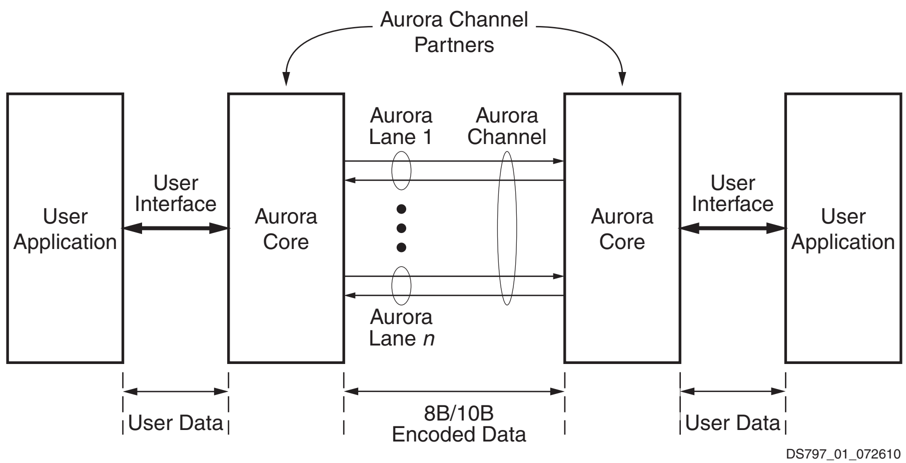

Figure 1: **Aurora 8B/10B Channel Overview**

Aurora 8B/10B cores automatically initialize a channel when they are connected to an Aurora channel partner. After initialization, applications can pass data freely across the channel as *frames* or *streams* of data. Aurora *frames* can be any size, and can be interrupted at any time. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora, and can be used to reduce the rate of incoming data, or to send brief, high-priority messages through the channel.

Streams are implemented in the Aurora 8B/10B core as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. The Aurora 8B/10B core detects single-bit and most multi-bit errors using 8B/10B coding rules. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to re-initialize a new channel.

Applications

Aurora 8B/10B cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora 8B/10B core applications include:

- **Chip-to-chip links**: Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The core provides the logic needed to use GTP/GTX transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links**: The Aurora 8B/10B core uses standard 8B/10B encoding, making it compatible with many existing hardware standards for cables and backplanes. Aurora 8B/10B cores can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **Simplex connections (unidirectional)**: In some applications, there is no need for a high-speed back channel. The Aurora protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTP/GTX transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.
- **ASIC applications**: The Aurora protocol is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora bus functional model (ABFM 8B/10B) with compliance testing make it easy to get an Aurora channel up and running.

  Note: Contact Xilinx Sales or Auroramkt@xilinx.com for information on licensing the Aurora 8B/10B core for ASIC applications.

Functional Blocks

Figure 2 shows a block diagram of the implementation of the Aurora 8B/10B core.

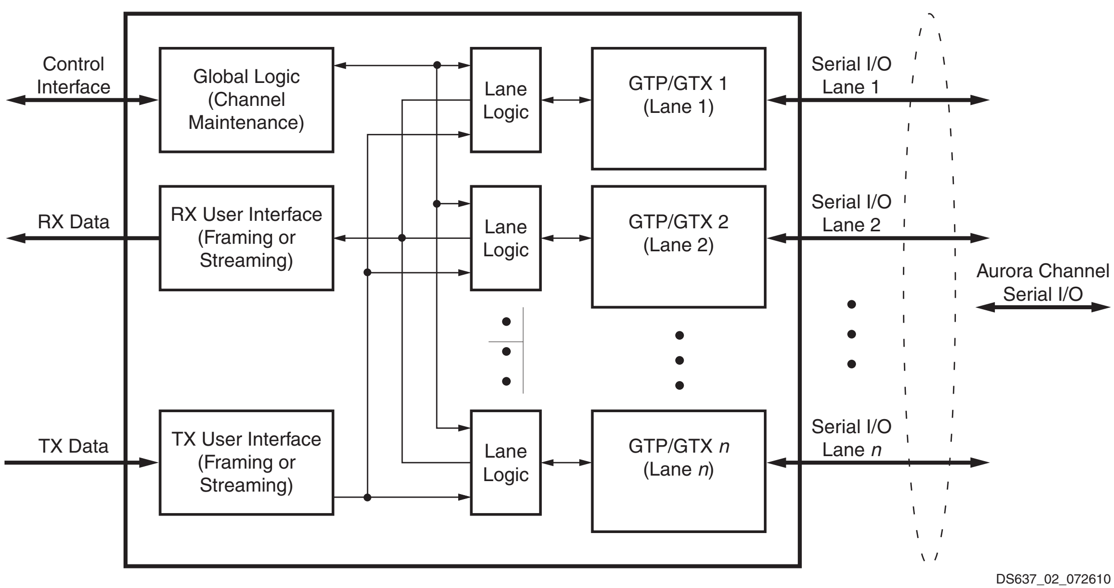

Figure 2: **Aurora 8B/10B Core Block Diagram**

The major functional modules of the Aurora 8B/10B core are:

- **Lane logic**: Each GTP/GTX transceiver is driven by an instance of the lane logic module, which initializes each individual GTP/GTX transceiver and handles the encoding and decoding of control characters and error detection.
- **Global logic**: The global logic module in each Aurora 8B/10B core performs the bonding and verification phases of channel initialization. While the channel is operating, the module generates the random idle characters required by the Aurora protocol and monitors all the lane logic modules for errors.
- **RX user interface**: The RX user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and a data valid signal. Frames are presented using a standard AXI4-Stream interface. This module also performs flow control functions.
- **TX user interface:** The TX user interface moves data from the application to the channel. A stream interface with a data valid and a ready signal is used for streaming data. A standard AXI4-Stream interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora 8B/10B cores). This interface is normally driven by a standard clock compensation manager module provided with the Aurora 8B/10B core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

The users can customize Aurora 8B/10B cores by setting the parameters for the core using the CORE Generator software. Table 1 describes the customizable parameters. For examples of the GUI, see the *LogiCORE IP Aurora 8B/10B v7.1 User Guide*.

Table 1: **Core Parameters**

Parameter	Description	Values Supported
Aurora Lanes	The number of GTP/GTX transceivers used in the channel.	• Virtex-7/Kintex-7 devices GTX transceivers: 1 to 16 • Virtex-6 devices GTX transceivers: 1 to 16 • Spartan-6 devices GTP transceivers: 1, 2, and 4
Lane Width	The Virtex-7/Kintex-7 FPGA GTX transceivers, Virtex-6 FPGA GTX transceivers and Spartan-6 FPGA GTP transceivers in the core are set to use 2-byte and 4-byte user data.	• Virtex-7/Kintex-7 devices GTX transceivers: 2 or 4 bytes • Virtex-6 devices GTX transceivers: 2 or 4 bytes • Spartan-6 devices GTP transceivers: 2 or 4 bytes
Dataflow Mode	The type of channel to be generated by the CORE Generator software. Can be full-duplex, simplex in the TX direction, or simplex in the RX direction.	Full-Duplex Simplex-TX Simplex-RX
Back Channel	There are two types of Simplex Aurora 8B/10B cores: • Sidebands: Simplex TX state transition is through Sideband signals from the Simplex partner • Timer: Simplex TX state transition during initialization is achieved through a built-in Timer instead of sidebands	Sidebands Timer

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported
Flow Control	Enables optional Aurora flow control. There are two types: • Native Flow Control (NFC): NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • User Flow Control (UFC): UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
Interface	The user can specify one of two types of interfaces: • Framing: The framing user interface is AXI4-Stream compliant. After initialization, it allows framed data to be sent across the Aurora channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • Streaming: The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface with a data valid signal.	Framing (AXI4-Stream) Streaming
Line Rate	The line rate dictates the speed at which the transceiver works. This parameter relates to performance of the Aurora 8B/10B core. Choose the higher line rate for better performance. See the *LogiCORE IP Aurora 8B/10B v7.1 User Guide* for detailed instructions.	• Virtex-7/Kintex-7 Lower Power devices GTX transceiver: 500 Mbps to 5.0 Gbps for 2-byte 500 Mbps to 6.6 Gbps for 4-byte • Virtex-7/Kintex-7 devices GTX transceiver: 500 Mbps to 6.6 Gbps • Virtex-6 LXT/SXT devices GTX transceiver: 600 Mbps to 6.6 Gbps • Virtex-6 CXT devices GTX transceiver: 675 Mbps to 3.75 Gbps • Lower-power Virtex-6 devices GTX transceiver: 600 Mbps to 5.0 Gbps • Spartan-6 devices GTP transceiver: 614 Mbps to 3.125 Gbps
GT REFCLK (MHz)	The CORE Generator software generates set of frequencies in MHz based on the given line rate to set the transceiver reference clock frequency for the selected Virtex-7, Kintex-7, Virtex-6, and Spartan-6 FPGA transceiver(s). See the *LogiCORE IP Aurora 8B/10B v7.1 User Guide* for detailed instructions.	A selection of reference clock frequency based on the selected line rate and available clock multipliers in the: • Virtex-7/Kintex-7 FPGA GTX transceivers • Virtex-6 FPGA GTX transceivers • Spartan-6 FPGA GTP transceivers

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported
GT REFCLK Source 1 and GT REFCLK Source 2	GTP/GTX transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *LogiCORE IP Aurora 8B/10B v7.1 User Guide* for instructions to select the best reference clock network for a given application.	• Virtex-7/Kintex-7 devices: GTXQ clocks • Virtex-6 devices: GTXQ clocks • Spartan-6 devices: GTPD clocks
Lane Assignment	The CORE Generator software provides a graphical interface that allows users to assign lanes to specific GTP/GTX transceivers. The *7 Series FPGAs GTX Transceivers User Guide*, *Virtex-6 FPGA GTX Transceivers User Guide*, and *Spartan-6 FPGA GTP Transceivers User Guide* include guidelines for placing GTP/GTX transceivers for best timing results.	Any combination of GTP/GTX transceivers can be selected. It is recommended to select the transceivers consecutively to meet timing closure. See the *LogiCORE IP Aurora 8B/10B v7.1 User Guide* for more information.

Core Interfaces

The parameters used to generate each Aurora 8B/10B core determine the interfaces available (Figure 3) for that specific core. The Aurora 8B/10B cores have four to six interfaces:

- User Interface, page 7
- User Flow Control Interface, page 7
- Native Flow Control Interface, page 8
- Transceiver Interface, page 8
- Clock Interface, page 8
- Clock Compensation Interface, page 8

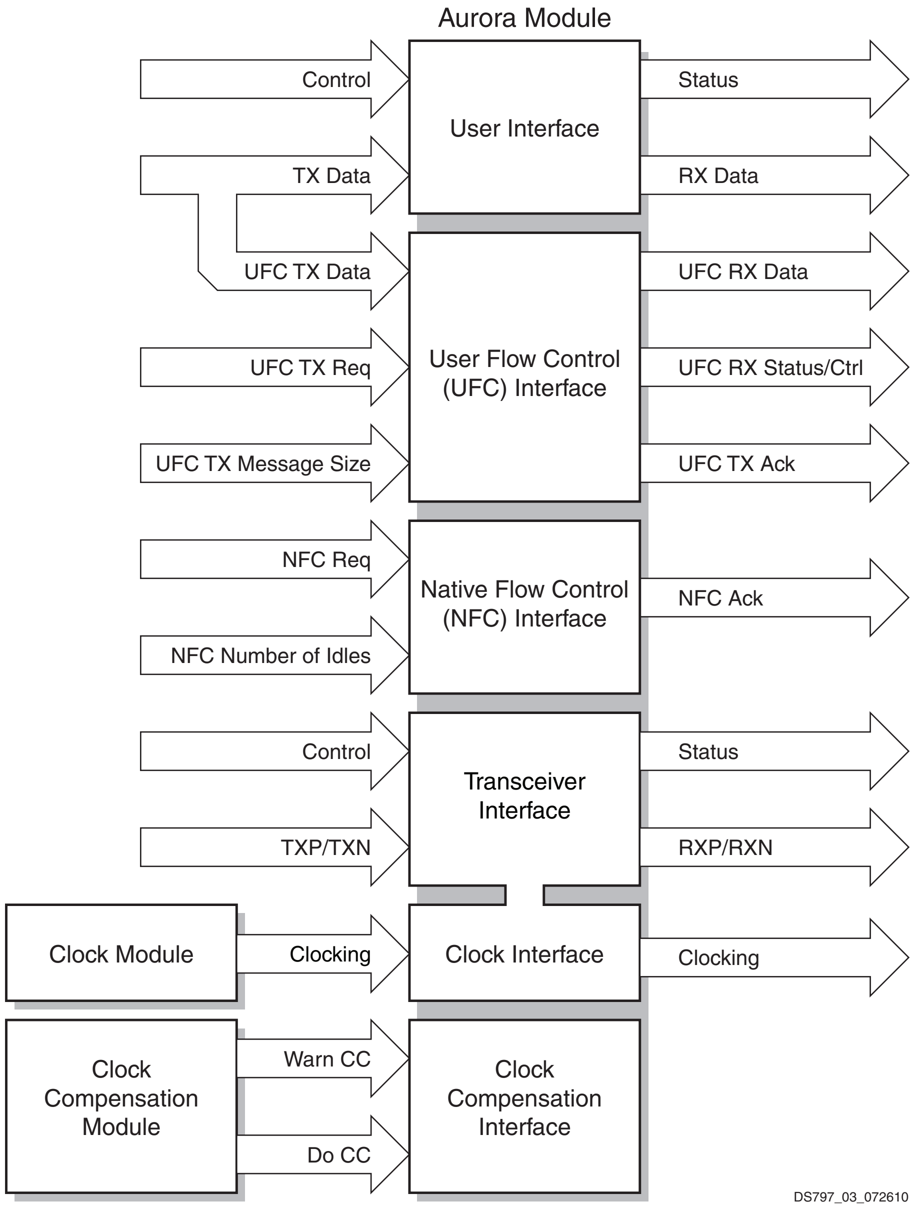

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora 8B/10B core. AXI4-Stream ports are used if the Aurora 8B/10B core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports and data valid ports. Full-duplex cores include ports for both transmit and receive; simplex cores use only the ports they require to send data in the direction they support. The width of the data ports in all interfaces depends on the number of GTP/GTX transceivers in the core, and on the width selected for these transceivers.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request and an acknowledge port that are used to start a UFC message, and a 3-bit port to specify the length of the message. The user supplies the message data to the data port of the user interface; immediately after a UFC request is acknowledged, the user interface indicates it is no longer ready for normal data, thereby allowing UFC data to be written to the data port.

The RX side of the UFC interface consists of a set of AXI4-Stream ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, and a 4-bit port to specify the number of idle cycles requested.

Transceiver Interface

This interface includes the serial I/O ports of the GTP/GTX transceivers, and the control and status ports of the Aurora 8B/10B core. This interface is the user's access to control functions such as reset, loopback, channel bonding, clock correction, and powerdown. Status information about the state of the channel, and error information is also available here.

Clock Interface

This interface is most critical for correct Aurora 8B/10B core operation. The clock interface has ports for the reference clocks that drive the GTP/GTX transceivers, and ports for the parallel clocks that the Aurora 8B/10B core shares with application logic.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. For modules with UFC and NFC, the WARN_CC port prevents UFC messages and CC sequences from colliding. Each Aurora 8B/10B core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance with the *Aurora 8B/10B Protocol Specification*. When the same physical clock is used on both sides of the channel, WARN_CC and DO_CC should be tied Low.

Resource Utilization

Table 2 through Table 13 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora modules. The Aurora 8B/10B core is also available in configurations not shown in the tables; the estimated resource usage for these other modules can be extrapolated from the tables. These tables do not include the additional resource usage for flow control. These tables do not include the additional resource usage for the example design modules such as FRAME_GEN and FRAME_CHECK.

Table 2: **Virtex-7 and Kintex-7 Family Resource Usage for Streaming with 2-Byte Lane Width**

Virtex-7/Virtex-7 Lower Power/ Kintex-7/Kintex-7 Lower Power Families			Streaming		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full Duplex	TX Only	RX Only
1	2	FFs	245	158	123
		LUTs	190	120	84
2	2	FFs	391	199	241
		LUTs	338	158	176
4	2	FFs	633	262	417
		LUTs	551	235	298
8	2	FFs	1119	386	769
		LUTs	1029	397	552
16	2	FFs	2086	642	1473
		LUTs	1922	670	1028

Table 3: **Virtex-7 and Kintex-7 Family Resource Usage for Framing with 2-Byte Lane Width**

Virtex-7/Virtex-7 Lower Power/ Kintex-7/Kintex-7 Lower Power Families			Framing		
Lanes	Lane Width	Resource Type	Duplex	Simplex	
			Full Duplex	TX Only	RX Only
1	2	FFs	266	168	136
		LUTs	208	137	94
2	2	FFs	439	204	283
		LUTs	352	164	195
4	2	FFs	711	267	489
		LUTs	587	223	335
8	2	FFs	1253	393	899
		LUTs	1052	373	622
16	2	FFs	2369	649	1752
		LUTs	2003	608	1191

Table 4: **Virtex-7 and Kintex-7 Family Resource Usage for Streaming with 4-Byte Lane Width**

Virtex-7/Virtex-7 Lower Power/ Kintex-7/Kintex-7 Lower Power Family			Streaming		
Lanes	Lane Width	Resource Type	Duplex	Simplex	
			Full-Duplex	TX Only	RX Only
1	4	FFs	308	158	180
		LUTs	270	126	119
2	4	FFs	543	211	365
		LUTs	492	191	272
4	4	FFs	940	294	665
		LUTs	880	307	493
8	4	FFs	1734	452	1265
		LUTs	1593	542	902
16	4	FFs	3325	780	2465
		LUTs	3144	979	1723

Table 5: **Virtex-7 and Kintex-7 Family Resource Usage for Framing with 4-Byte Lane Width**

Virtex-7/Virtex-7 Lower Power/ Kintex-7/Kintex-7 Lower Power Family			Framing		
Lanes	Lane Width	Resource Type	Duplex	Simplex	
			Full Duplex	TX Only	RX Only
1	4	FFs	361	166	223
		LUTs	279	137	148
2	4	FFs	620	215	439
		LUTs	497	175	315
4	4	FFs	1074	299	799
		LUTs	925	250	580
8	4	FFs	2013	453	1552
		LUTs	1714	499	1125
16	4	FFs	3863	773	3027
		LUTs	3334	822	2176

Table 6: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Streaming with 2-Byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Streaming		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	2	FFs	243	162	131
		LUTs	209	134	102
2	2	FFs	405	218	262
		LUTs	345	181	196

Table 6: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Streaming with 2-Byte Lane Width *(Cont'd)***

Virtex-6 LXT/SXT/CXT/HXT Family			Streaming		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
4	2	FFs	678	319	438
		LUTs	579	284	320
8	2	FFs	1219	516	789
		LUTs	1112	505	573
16	2	FFs	2307	916	1493
		LUTs	2070	820	1073

Table 7: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Framing with 2-Byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Framing		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	2	FFs	265	170	145
		LUTs	225	140	111
2	2	FFs	457	227	305
		LUTs	375	191	227
4	2	FFs	765	333	481
		LUTs	641	269	335
8	2	FFs	1373	538	890
		LUTs	1124	459	628
16	2	FFs	2627	954	1744
		LUTs	2200	750	1240

Table 8: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Streaming with 4-Byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Streaming		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	4	FFs	321	176	173
		LUTs	271	148	123
2	4	FFs	579	258	356
		LUTs	508	230	256
4	4	FFs	1034	407	656
		LUTs	927	376	469
8	4	FFs	1945	706	1255
		LUTs	1659	626	892
16	4	FFs	3768	1305	2455
		LUTs	3273	1153	1759

Table 9: **Virtex-6 LXT/SXT/CXT/HXT Family Resource Usage for Framing with 4-Byte Lane Width**

Virtex-6 LXT/SXT/CXT/HXT Family			Framing		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	4	FFs	366	181	217
		LUTs	303	146	155
2	4	FFs	663	269	431
		LUTs	549	209	314
4	4	FFs	1180	422	791
		LUTs	960	308	580
8	4	FFs	2249	729	1544
		LUTs	1778	531	1130
16	4	FFs	4338	1344	3001
		LUTs	3543	927	2233

Table 10: **Spartan-6 LXT Family Resource Usage for Streaming with 2-Byte Lane Width**

Spartan-6 LXT Family			Streaming		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	2	FFs	243	157	126
		LUTs	198	122	96
2	2	FFs	406	206	259
		LUTs	340	171	191
4	2	FFs	677	299	435
		LUTs	601	263	308

Table 11: **Spartan-6 LXT Family Resource Usage for Framing with 2-Byte Lane Width**

Spartan-6 LXT Family			Framing		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	2	FFs	264	166	142
		LUTs	217	133	105
2	2	FFs	454	217	302
		LUTs	362	181	220
4	2	FFs	762	313	508
		LUTs	648	266	363

Table 12: **Spartan-6 LXT Family Resource Usage for Streaming with 4-Byte Lane Width**

Spartan-6 LXT Family			Streaming		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	4	FFs	318	171	170
		LUTs	263	137	117
2	4	FFs	583	246	383
		LUTs	516	211	284
4	4	FFs	1035	393	683
		LUTs	947	374	493

Table 13: **Spartan-6 LXT Family Resource Usage for Framing with 4-Byte Lane Width**

Spartan-6 LXT Family			Framing		
			Duplex	Simplex	
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only
1	4	FFs	369	175	214
		LUTs	312	139	149
2	4	FFs	666	256	458
		LUTs	553	199	351
4	4	FFs	1183	401	818
		LUTs	1004	300	621

Performance

Config1 cited in the LogiCORE IP Facts table runs at 330 MHz in a Virtex-6 LX240T-FF1156 device with -2 speed grade. Config1 is a 16-lane Aurora 8B/10B core with Streaming interface, 2-byte lane width, Duplex dataflow, targeting a 6.6 Gbps line rate.

The Aurora 8B/10B cores listed in Table 2, page 9 through Table 13 run at 156.25 MHz in devices with speed grades ranging from -1 to -3. For more details about performance and core latency, see the *LogiCORE IP Aurora 8B/10B v7.1 User Guide*.

Verification

Aurora 8B/10B cores are verified for protocol compliance using an array of automated hardware and simulation tests. The core comes with an example design implemented using a linear feedback shift register (LFSR) for understanding/verification of the core features.

The Aurora 8B/10B core is verified using the Aurora 8B/10B BFM and proprietary custom test benches. The Aurora 8B/10B BFM verifies the protocol compliance along with interface level checks and error scenarios. An automated test system runs a series of simulation tests on the most widely used set of design configurations chosen at random. Aurora 8B/10B cores are also tested in hardware for functionality, performance, and reliability using Xilinx GTP/GTX transceiver demonstration boards. Aurora verification test suites for all possible modules are continuously being updated to increase test coverage across the range of possible parameters for each individual module.

The test boards used for verification are:

- ML623
- ML605
- SP605

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

This Xilinx LogiCORE IP module is included at no additional charge with the Xilinx ISE® Design Suite software and is provided under the terms of the Xilinx End User License Agreement. The core is generated using the Xilinx CORE Generator software, which is a standard component of the Xilinx ISE software.

For more information, visit the Aurora 8B/10B product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

References

The following documents provide additional information useful to this data sheet:

1. SP002, *Aurora 8B/10B Protocol Specification*
2. *AMBA AXI4-Stream Protocol Specification*
3. UG058, *Aurora 8B/10B Bus Functional Model User Guide* (Contact: auroramkt@xilinx.com)
4. UG766, *LogiCORE IP Aurora 8B/10B v7.1 User Guide*
5. DS180, *7 Series FPGAs Overview*
6. DS150, *Virtex-6 Family Overview*
7. DS160, *Spartan-6 Family Overview*
8. UG476, *7 Series FPGAs GTX Transceivers User Guide*
9. UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
10. UG386, *Spartan-6 FPGA GTP Transceivers User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/21/10	1.0	First release of the core with AXI interface support. The previous release of this document was DS637.
03/01/11	1.1	Updated document with v6.2 core changes for the ISE software 13.1 release. Removed Virtex-5 device references.
10/19/11	1.2	Updated document with v7.1 core changes for the ISE software 13.3 release. Added support for Virtex-7 and Kintex-7 devices. Removed RX/TX simplex mode support.

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