Virtex-5 FPGA Aurora v3.0

DS637 June 27, 2008 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-5 FPGA Aurora core implements the Aurora protocol using the high-speed serial RocketIO™ transceivers on Virtex-5 LXT, SXT, and FXT devices. The core can use up to 24 GTP/GTX transceivers running at any supported line rate to provide a low cost, general purpose, data channel with throughput range from 100 Mbps to 117 Gbps.

Aurora is a scalable, lightweight, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented by Aurora protocol licensees using any technology. The protocol is typically used in applications requiring simple, low-cost, high-rate, data channels.

The CORE Generator™ software produces source code for Aurora cores with variable datapath width. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control.

Aurora cores are verified for protocol compliance using the Aurora bus functional model (BFM) and an array of automated hardware and simulation tests. The core comes with an example design.

Features

- General purpose data channels with throughput range from 100 Mbps to 117 Gbps
- Supports up to 24 Virtex-5 FPGA RocketIO GTP or GTX transceivers
- Supports line rates GTP: 100 Mbps to 3.75 Gbps and GTX: 200 Mbps to 6.5 Gbps
- Aurora v2.0 compliant (8B/10B encoding)
- Low resource cost (see "Resource Utilization")
- Easy-to-use framing and flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation
- LocalLink (framing) or streaming user interface

LogiCORE IP Facts				
Core Specifics				
Supported Device Family	Virtex-5 LXT/SXT/FXT Platforms (1)			
Resources Used	I/O	LUTs	FFs	Block RAMs
	Varies with channel size See "Resource Utilization," page 8			0
Special Features	Open source; Core is free to use with Xilinx devices			
Provided with Core				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	Verilog and VHDL			
Constraints File	`.ucf` (user constraints file)			
Verification	Aurora Bus Functional Model			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 10.1 (2)			
Verification	Mentor Graphics® ModelSim® 6.3c			
Simulation	Mentor Graphics ModelSim 6.3c			
Synthesis	Synplicity® Synplify 8.9 XST 10.1			
Support				
Provided by Xilinx, Inc., www.xilinx.com/support				

1. For more information on the Virtex-5 FPGAs, see DS100, *Virtex-5 Family Overview*
2. ISE Service Packs can be downloaded at http://www.xilinx.com/support/download.htm

Functional Overview

Aurora is a lightweight, serial communications protocol for multi-gigabit links. It is used to transfer data between devices using one or many GTP/GTX transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (Figure 1).

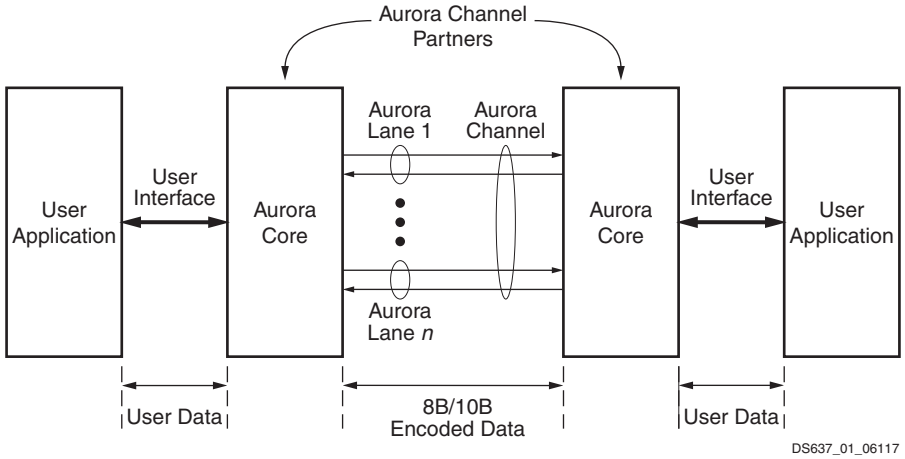

Figure 1: **Aurora Channel Overview**

Aurora cores automatically initialize a channel when they are connected to an Aurora channel partner. After initialization, applications can pass data freely across the channel as *frames* or *streams* of data. Aurora *frames* can be any size, and can be interrupted at any time. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora, and can be used to reduce the rate of incoming data, or to send brief, high-priority messages through the channel.

Streams are implemented in Aurora as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. The Aurora core detects single-bit, and most multi-bit errors using 8B/10B coding rules. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to initialize a new channel.

Applications

Aurora cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora core applications include:

- **Chip-to-chip links:** Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The core provides the logic needed to use GTP/GTX transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links:** Aurora uses standard 8B/10B encoding, making it compatible with many existing hardware standards for cables and backplanes. Aurora can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **One-way connections:** In some applications there is no need for a high-speed back channel. The Aurora simplex protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTP/GTX transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.

- **ASIC connections:** Aurora is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora bus functional model with automated compliance testing make it easy to get an Aurora connection up and running.

Functional Description

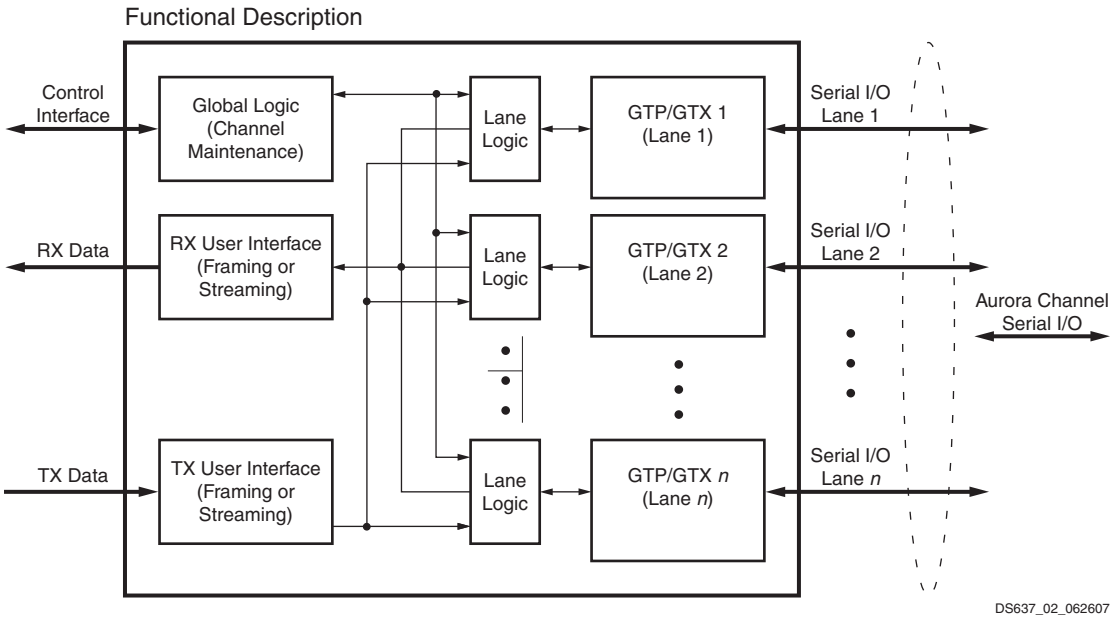

Figure 2: **Aurora Core Block Diagram**

Figure 2 shows a block diagram of the implementation of the Aurora core. The major functional modules of the Aurora core are:

- **Lane logic:** Each GTP/GTX tile is driven by an instance of the lane logic module, which initializes each individual GTP/GTX transceiver and handles the encoding and decoding of control characters and error detection.
- **Global logic:** The global logic module in each Aurora core performs the bonding and verification phases of channel initialization. While the channel is operating, the module generates the random idle characters required by the Aurora protocol and monitors all the lane logic modules for errors.
- **RX user interface:** The RX user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and a data valid signal. Frames are presented using a standard LocalLink interface. This module also performs flow control functions.
- **TX user interface:** The TX user interface moves data from the application to the channel. A stream interface with a data valid and a ready signal is used for streaming data. A standard LocalLink interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora cores). This interface is normally driven by a standard clock compensation manager module provided with the Aurora core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

CORE Generator software users can customize Aurora cores by setting the parameters for the core. Table 1 describes the customizable parameters. For examples of the GUI, see the *Virtex-5 FPGA Aurora v3.0 Getting Started Guide* and the *Virtex-5 FPGA Aurora v3.0 User Guide*.

Table 1: **Core Parameters**

Parameter	Description	Values Supported by the Virtex-5 FPGA Aurora Core
Lanes	The number of GTP/GTX transceivers used in the channel.	From 1 to 24 GTP/GTX transceivers on the chosen device
Lane Width	The GTP transceivers in the core are set to use 2-byte SERDES. For a given line rate, this 2-byte mode (vs. 1-byte mode) has the effect of reducing the required clock rate of application logic connected to the Aurora core. The GTX transceivers in the core are set to use 2-byte as well as 4-byte SERDES.	GTP: 2 bytes GTX: 2/4 bytes
Device	The type of FGPA used to implement the design.	Virtex-5 LXT/SXT/FXT FPGAs with GTP/GTX transceivers
HDL	The language in which the source code for the core will be generated.	Verilog or VHDL
Direction	The type of channel to be generated by the CORE Generator software. Can be full-duplex, simplex in the TX direction, simplex in the RX direction, or two separate simplex modules (one TX and one RX) sharing the same GTP/GTX transceivers.	Full-Duplex Simplex-TX Simplex-RX Simplex-Both
Flow Control	Enables optional Aurora flow control. There are two types: • **Native Flow Control (NFC):** NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • **User Flow Control (UFC):** UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
Interface	The user can specify one of two types of interfaces: • **Framing:** The framing user interface is LocalLink compliant. After initialization, it allows framed data to be sent across the Aurora channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • **Streaming**: The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface with a data valid signal.	Framing (LocalLink) Streaming
Line Rate	The line rate for Aurora cores that use GTP transceivers can be set from 100 Mbps to 3.75 Gbps and GTX transceivers can be set from 200 Mbps to 6.5 Gbps using the CORE Generator software. See the *Virtex-5 FPGA Aurora v3.0 User Guide* for detailed instructions.	GTP: 100 Mbps to 3.75 Gbps GTX: 200 Mbps to 6.5 Gbps
Reference Clock Frequency	The CORE Generator software accepts parameters to set the reference clock rate for Virtex-5 FPGAs. See the *Virtex-5 FPGA Aurora v3.0 User Guide* for detailed instructions.	A selection of legal rates based on the selected line rate and available clock multipliers in the Virtex-5 FPGA GTP/GTX transceivers

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported by the Virtex-5 FPGA Aurora Core
Reference Clock	GTP/GTX transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *Virtex-5 FPGA Aurora v3.0 User Guide* for instructions to select the best reference clock network for a given application.	GREFCLK and GTPD/GTXD
GTP/GTX Placement	The CORE Generator software provides a graphical interface that allows users to assign lanes to specific GTP/GTX transceivers. The *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* and the *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* includes guidelines for placing GTP/GTX transceivers for best timing results.	Any combination of GTP/GTX transceivers can be selected

Core Interfaces

The parameters used to generate each Aurora core determine the interfaces available (Figure 3) for that specific core. The Aurora cores have three to six interfaces:

- "User Interface," page 7
- "User Flow Control Interface," page 7
- "Native Flow Control Interface," page 7
- "GTP/GTX Interface," page 7
- "Clock Interface," page 7
- "Clock Compensation Interface," page 7

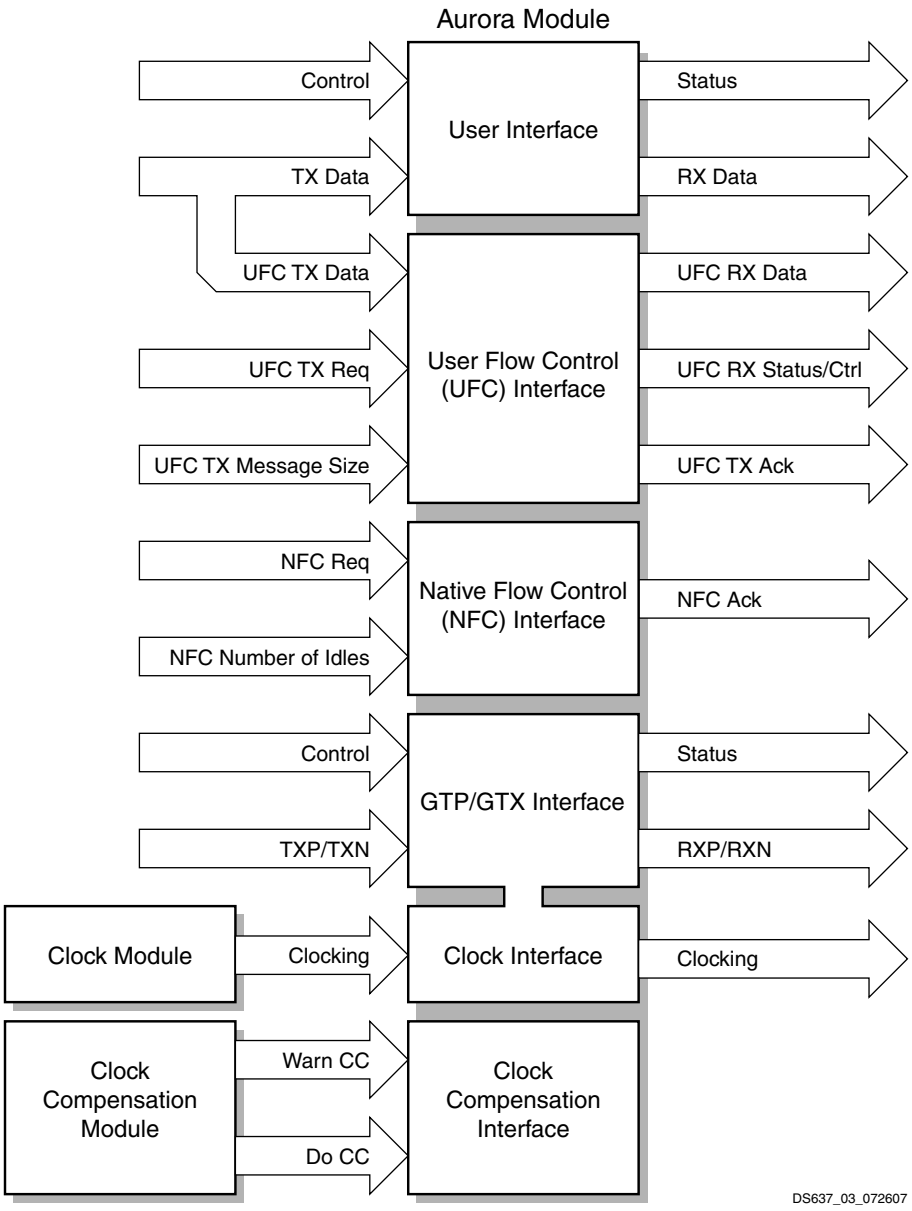

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora core. LocalLink ports are used if the Aurora core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports and data_valid ports. Full-duplex cores include ports for both transmit and receive; simplex cores use only the ports they require to send data in the direction they support. The width of the data ports in all interfaces depends on the number of GTP/GTX transceivers in the core, and on the width selected for these transceivers.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request and an acknowledge port that are used to start a UFC message, and a port to specify the length of the message. The user supplies the message data to the data port of the user interface; immediately after a UFC request is acknowledged, the user interface indicates it is no longer ready for normal data, thereby allowing UFC data to be written to the data port.

The RX side of the UFC interface consists of a set of LocalLink ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, and a 4-bit port to specify the number of idle cycles requested.

GTP/GTX Interface

This interface includes the serial I/O ports of the GTP/GTX transceivers, and the control and status ports of the Aurora core. This interface is the user's access to control functions such as reset, loopback, and powerdown. Status information about the state of the channel, and error information is also available here.

Clock Interface

This interface is most critical for correct Aurora core operation. The clock interface has ports for the reference clocks that drive the GTP/GTX transceivers, and ports for the parallel clocks that the Aurora core shares with application logic.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. For modules with UFC, the WARN_CC port prevents UFC messages and CC sequences from colliding. Each Aurora core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance with the *Aurora Protocol Specification*. When the same physical clock is used on both sides of the channel, DO_CC should be tied Low.

Resource Utilization

Table 2 through Table 9 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora modules. The Aurora core is also available in configurations not shown in the tables; the estimated resource usage for these other modules can be extrapolated from the tables. These tables do not include the additional resource usage for flow control. These tables include the additional resource usage for the example design.

Table 2: **Virtex-5 LXT Platform Resource Usage for Streaming**

Virtex-5 LXT Platform			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	242	96	140	236
		FFs	275	141	152	287
2	2	LUTs	440	143	277	417
		FFs	519	246	300	538
4	2	LUTs	788	230	508	733
		FFs	965	444	552	988
8	2	LUTs	1495	788	979	1378
		FFs	1865	965	1058	1890
16	2	LUTs	2898	758	1913	2653
		FFs	3657	1633	2062	3686

Table 3: **Virtex-5 LXT Platform Resource Usage for Framing**

Virtex-5 LXT Platform			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	344	201	157	328
		FFs	382	177	200	395
2	2	LUTs	666	243	398	639
		FFs	751	324	453	769
4	2	LUTs	1200	369	779	1147
		FFs	1449	636	845	1473
8	2	LUTs	2609	619	1874	2486
		FFs	2779	1169	1663	2826
16	2	LUTs	6607	1109	5258	6348
		FFs	6072	2233	3877	6101

Table 4: **Virtex-5 SXT Platform Resource Usage for Streaming**

Virtex-5 SXT Platform			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	241	94	142	233
		FFs	275	140	149	283
2	2	LUTs	441	142	280	419
		FFs	519	243	294	531
4	2	LUTs	795	230	514	736
		FFs	965	441	542	977
8	2	LUTs	1492	397	968	1357
		FFs	1865	837	1046	1877
16	2	LUTs	2888	756	1884	2598
		FFs	3657	1630	2046	3670

Table 5: **Virtex-5 SXT Platform Resource Usage for Framing**

Virtex-5 SXT Platform			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	344	200	156	329
		FFs	382	179	197	391
2	2	LUTs	657	243	396	630
		FFs	751	322	447	763
4	2	LUTs	1203	373	782	1140
		FFs	1442	627	833	1454
8	2	LUTs	2583	617	1862	2475
		FFs	2763	1159	1623	2776
16	2	LUTs	6541	1124	5189	6275
		FFs	6064	2224	3859	6076

Table 6: **Virtex-5 FXT Platform Resource Usage for Framing for 2-Lane Width**

Virtex-5 FXT Platform			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	267	127	130	257
		FFs	276	122	162	284
2	2	LUTs	641	238	390	624
		FFs	716	286	447	727
4	2	LUTs	1184	363	767	1130
		FFs	1370	555	833	1382
8	2	LUTs	2591	616	1854	2470
		FFs	2619	1015	1622	2631
16	2	LUTs	6393	1112	5052	6153
		FFs	5777	1937	3860	5789

Table 7: **Virtex-5 FXT Platform Resource Usage for Streaming for 2-Lane Width**

Virtex-5 FXT Platform			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	2	LUTs	241	92	139	227
		FFs	258	123	150	266
2	2	LUTs	432	136	274	410
		FFs	483	207	294	495
4	2	LUTs	784	221	503	721
		FFs	893	369	542	905
8	2	LUTs	1476	386	956	1340
		FFs	1721	693	1046	1733
16	2	LUTs	2814	717	1833	2545
		FFs	3370	1343	2047	3383

Table 8: **Virtex-5 FXT Platform Resource Usage for Framing for 4-Lane Width**

Virtex-5 FXT Platform			Framing			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	533	225	308	534
		FFs	633	260	393	645
2	4	LUTs	997	316	668	992
		FFs	1243	500	778	1272
4	4	LUTs	2246	521	1683	2198
		FFs	2340	907	1483	2385
8	4	LUTs	5866	928	4850	5768
		FFs	5228	1719	3587	5301
16	4	LUTs	17915	1745	15944	17672
		FFs	13450	3368	10219	13581

Table 9: **Virtex-5 FXT Platform Resource Usage for Streaming for 4-Lane Width**

Virtex-5 FXT Platform			Streaming			
			Duplex	Simplex		
Lanes	Lane Width	Resource Type	Full-Duplex	TX Only	RX Only	Both
1	4	LUTs	316	124	193	318
		FFs	403	183	238	413
2	4	LUTs	610	177	388	564
		FFs	782	318	468	778
4	4	LUTs	1164	308	758	1065
		FFs	1469	592	877	1463
8	4	LUTs	2242	565	1482	2052
		FFs	2869	1142	1725	2860
16	4	LUTs	4313	1104	2884	4016
		FFs	5665	2257	3429	5679

Performance

The Virtex-5 FPGA Aurora cores listed in Table 2, page 8 through Table 9 run at 156.25 MHz in devices with speed grades ranging from -1 to -3.

Verification

The Aurora core is verified using the Aurora BFM and proprietary custom testbenches. An automated test system runs a series of simulation tests on the most widely used set of cores, as well as cores chosen at random. Aurora cores are also tested in hardware for functionality, performance, and reliability using Xilinx® GTP/GTX demonstration boards. Aurora verification tests suites for all possible modules are continuously being modified to increase test coverage across the range of possible parameters for each individual module.

Table 10: **Boards Used for Verification**

Test Boards
ML523

References

1. Xilinx Aurora Web site, http://www.xilinx.com/aurora:
   - SP002, *Aurora Protocol Specification*
   - UG058, *Aurora Bus Functional Model User Guide*
   - UG352, *Virtex-5 FPGA Aurora v3.0 Getting Started Guide*
   - UG353, *Virtex-5 FPGA Aurora v3.0 User Guide*
2. UG196: *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*
3. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Aurora core is provided free of charge to licensed users. The licence for the Aurora core is also free and can be obtained by visiting www.xilinx.com/aurora.

There are three steps required to obtain the core:

1. Install Xilinx ISE 10.1. See the ISE product page for instructions if ISE software is not already installed.
2. Install Xilinx ISE 10.1 IP Update 2 to add version 3.0 of the Virtex-5 FPGA Aurora core to the list of cores available in the Core Selection window in the CORE Generator software. Instructions for this step are available in the *Virtex-5 FPGA Aurora v3.0 Getting Started Guide*.
3. Electronically sign the Aurora Core License Agreement to obtain a license file for the Aurora core. Instructions for this step and the link to the page with the license and the CORE Generator software license file are also at www.xilinx.com/aurora. You must be a registered user on www.xilinx.com to sign the license.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	2.9	Initial Xilinx release.
03/24/08	2.9.1	Post-release updates and corrections.
06/27/08	3.0	Virtex-5 FPGA Aurora 3.0 release.

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