LogiCORE IP AXI Performance Monitor v1.00.a

Product Guide

PG037 May 22, 2012

XILINX®

XILINX®

Table of Contents

LogiCORE IP AXI Performance Monitor v1.00.a

Introduction

The LogiCORE™ IP AXI Performance Monitor (axi_perf_mon) measures major performance metrics for the AMBA Advanced eXtensible Interface (AXI) system. The Performance Monitor measures bus latency of a specific master/slave (AXI4/AXI4-Lite/AXI4-Stream) in a system, the amount of memory traffic for specific durations and other performance metrics.

The Performance Monitor Unit (PMU) monitors and analyzes system behavior on an AXI bus of multi-core systems. The PMU provides monitoring hardware for counting events associated with AXI bus transactions. The included hardware counters can be set and read by software and used to analyze and enhance the performance of the entire system.

Features

- AXI protocol compliant and configurable as AXI4 or an AXI4-Lite slave interface
- Interface data widths:
  - AXI4: 32, 64, 128, or 256 bits
  - AXI4-Lite: 32 bits
- 32-bit address width
- Computes performance metrics for up to four AXI4/AXI4-Lite agents and two AXI4-Stream agents
- Includes a free-running global clock counter
- Samples metrics at pre-configured sample intervals or when an external capture event occurs
- Allows more software/application control for obtaining the metrics for the system
- Flexible support for agents (master/slave) with any data width, frequency and ID width

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq™-7000, Artix™-7, Kintex™-7, Virtex®-7,Virtex-6, Spartan®-6
Supported User Interfaces	AXI4-Stream, AXI4-Lite and AXI4
Resources	See Table 2-1, Table 2-2, and Table 2-3.
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	None
Supported S/W Driver[2]	Standalone
Tested Design Tools	
Design Entry Tools	ISE Design Suite v14.1
Simulation[3]	Mentor Graphics ModelSim
Synthesis Tools[3]	XST v14.1
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see IDS Embedded Edition Derivative Device Support.
2. Standalone driver details can be found in the EDK or SDK directory (<*install_directory*>/doc/usenglish/xilinx_drivers.htm). Linux OS and driver support information is available from //wiki.xilinx.com.
3. For the supported versions of the tools, see the ISE Design Suite 14: Release Notes Guide.

Overview

The top level block diagram of the AXI Performance Monitor is shown in Figure 1-1.

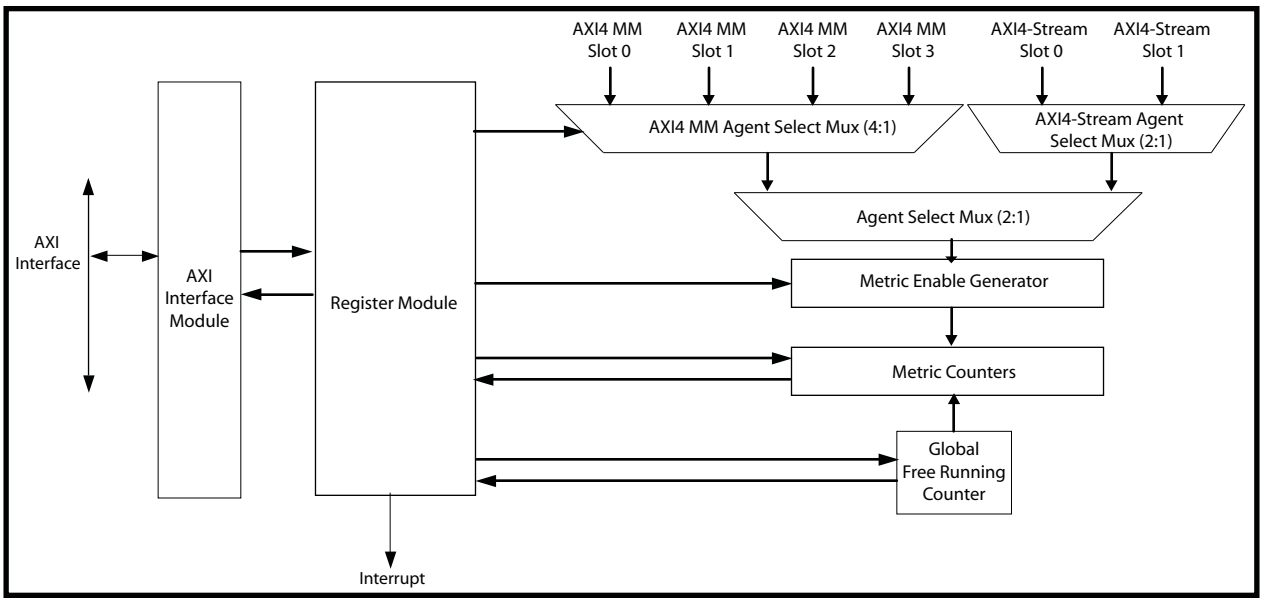

Figure 1-1: **Block Diagram of AXI Performance Monitor**

All the AXI signals of agents in an AXI system are connected to the monitor slots of the core. AXI4 and AXI4-Lite agents can be connected to AXI4 Memory Mapped (MM) slots, and AXI4-Stream agents can be connected to AXI4-Stream slots. This core assists in obtaining the performance metrics of any chosen agent. The available metrics are categorized into seven sets. For a single run of the application on the system, one set of metrics of the chosen agent can be obtained. So to get all the metrics of one agent, it is necessary to run the application multiple times. This approach reduces the footprint of the core in the FPGA and gives more control for the software/application.

There is a set of 10 counters in the core that counts the events based on the selected metric set. The events are generated based on the activities on the AXI interface of the selected agent.

The metric counters can be sampled into another similar register set upon getting a capture event from outside the core or an overflow of the sample interval counter.

The global clock counter runs for the total application duration and is used in calculating the read/write latencies of an agent. It also gives the application runtime and is considered

for calculating the throughput of the agent. An interrupt can be generated when the global clock counter overflows or the sample interval counter overflows.

Configuration registers can be configured through the AXI interface the core provides. At the end of the application, the metric counters and the global clock counter are read through the same AXI interface.

The performance metrics that can be computed, and the seven categories of metrics are described in Table 2-28, page 36 and Table 2-29, page 36.

AXI4-Lite Interface Support

For system where burst is not supported or not required by the AXI master, this core can be configured for an AXI4-Lite interface. This configuration reduces the FPGA resource utilization. The AXI Performance Monitor supports all requests from an AXI master as per the AXI4-Lite specification. The AXI4-Lite interface is selected by configuring the parameter C_S_AXI_PROTOCOL as "AXI4LITE".

Performance Metrics

Details about the metrics collected by the AXI Performance Monitor are as follows:

- Each agent connected on the monitor slots can independently have data widths of 32, 64, 128, or 256 bits.
- There are four AXI4 MM monitor slots and two AXI4-Stream monitor slots in the performance monitor.
- The metrics are obtained for the selected agent/slot. This selection is done through the configuration register.
- The configurable read latency ranges have eight intervals. Because the read/write latency has a wide distribution (from a couple of cycles to several hundreds of cycles), it is not effective to have dedicated counters for each latency cycle. So, an interval-based counting method is used for counting read/write latency.
- The configurable write latency ranges have four intervals.
- Metrics computed for an AXI4 MM agent:
    - Write Request Count: Total number of write requests by/to the agent.
    - Read Request Count: Total number of read requests given by/to the agent.
    - Read Latency Distribution: Number of read requests that fall in eight different latency intervals.
    - Write Latency Distribution: Number of write requests that fall in four different latency intervals.

- Write Byte Count: Total number of bytes written by/to the agent. This metric is helpful when calculating the throughput of the system.
- Read Byte Count: Total number of bytes read from/by the agent.
- Average Write Latency: Average write latency seen by the agent.
- Average Read Latency: Average read latency.
- Master Write Idle Cycle Count: Number of idle cycles caused by the masters during write transactions to the slave.
- Slave Write Idle Cycle Count: Number of idle cycles caused by this slave during write transactions to the slave.
- Master Read Idle Cycle Count: Number of idle cycles caused by the master during read transactions to the slave.
- Slave Read Idle Cycle Count: Number of idle cycles caused by this slave during read transactions to the slave.
- Global Clock Count: Number of cycles for which the application is run.

- Metrics computed for an AXI4-Stream agent:
  - Transfer Cycle Count: Total number of writes by/to the agent (cycles TVALID & TREADY are active High).
  - Data Byte Count: Total number of data bytes written by/to the agent. This metric helps in calculating the throughput of the system.
  - Position Byte Count: Total number of position bytes transferred.
  - Null Byte Count: Total number of null bytes transferred.
  - Packet Count: Total number of packets transferred (counts TLAST).

System-level metrics like write data throughput, read data throughput, interconnect read latency can be computed by obtaining all metrics for all the agents in the system.

Target Technology

This solution targets the Zynq-7000, Artix-7, Kintex-7, Virtex-7,Virtex-6, and Spartan-6 FPGA families.

Applications

The AXI Performance Monitor has the following applications:

- Computing the cache hits/misses (hit ratio) and determining the optimal cache size for an application.
- Studying the latencies involved for any AXI-based slave, like a memory controller, and tuning the core.
- Comparing different applications by facilitating benchmarking.
- Debugging a system, for example, counting the responses against requests.
- Getting charts like latency distribution, throughput, burst distribution and others for a slave and across the system.
- Getting the system-level metrics like write throughput, read throughput, average interconnect read latency and others.
- Getting the run time of an application and optimizing the software.
- Analyzing the latencies involved in transactions by identifying the agent causing more idle cycles in the transactions.
- Comparing two similar AXI agents.

Unsupported Features

The AXI Performance Monitor has the following known limitations:

- Bus contention metrics are not computed.
- Due to logic constraints, the core does not provide the metrics for all the agents in the system in a single run of the application.
- Only supports a reordering depth of 1. The read data reordering depth is the number of addresses pending in the slave that can be reordered.
- Does not support out-of-order transactions.
- The Monitor Slot's clock must be synchronous to the core clock of the monitor.

Licensing

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The core may be generated using ISE Embedded Edition software (EDK). For full access to all core functionality in simulation and in hardware, you must purchase a license for the core. Please contact your local Xilinx sales representative for information on pricing and availability of Xilinx LogiCORE IP.

For more information, please visit the AXI Performance Monitor product page.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Product Specification

This chapter contains resource usage data, signal descriptions and details about the registers.

Resource Utilization

Because the AXI Performance Monitor is a module that will be used with other design pieces in the FPGA, the resource utilization and timing numbers reported in this section are estimates only. When the AXI Performance Monitor is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the design will vary from the results reported here.

The AXI Performance Monitor resource utilization benchmarks for a variety of parameter combinations measured with Kintex™-7 FPGA as the target device are shown in Table 2-1. Resource usage for Zynq™-7000, Artix™-7, and Virtex®-7 devices can also be estimated based on Table 2-1.

Table 2-1: **Resource Usage for Kintex-7 (XC7K325T-2-FFG900)**

C_NUM_MONITOR_SLOTS	C_NUM_AXIS_MONITOR_SLOTS	C_REG_ALL_MONITOR_SLOTS	C_MON_SLOTS_AXI_ID_MAX_WIDTH	C_MON_SLOTS_AXI_ADDR_MAX_WIDTH	C_MON_SLOTS_AXI_DATA_MAX_WIDTH	C_MAX_OUTSTAND_DEPTH	Slices	Slice Reg	LUTs
1	0	1	1	32	32	4	1444	1669	1424
1	0	1	1	32	32	1	1441	1685	1411
3	0	0	1	32	32	1	1445	1672	1432

Table 2-1: **Resource Usage for Kintex-7 (XC7K325T-2-FFG900) *(Cont'd)***

C_NUM_MONITOR_SLOTS	C_NUM_AXIS_MONITOR_SLOTS	C_REG_ALL_MONITOR_SLOTS	C_MON_SLOTS_AXI_ID_MAX_WIDTH	C_MON_SLOTS_AXI_ADDR_MAX_WIDTH	C_MON_SLOTS_AXI_DATA_MAX_WIDTH	C_MAX_OUTSTAND_DEPTH	Slices	Slice Reg	LUTs
1	1	1	1	32	32	4	1448	1695	1456
3	0	1	1	32	32	1	1004	1719	1495
1	1	0	1	32	32	1	1444	1681	1446

The AXI Performance Monitor resource utilization benchmarks for a variety of parameter combinations measured with Virtex-6 FPGA as the target device are shown in Table 2-2.

Table 2-2: **Resource Usage for Virtex-6 (XC6VLX240T-1-FF1156)**

C_NUM_MONITOR_SLOTS	C_NUM_AXIS_MONITOR_SLOTS	C_REG_ALL_MONITOR_SLOTS	C_MON_SLOTS_AXI_ID_MAX_WIDTH	C_MON_SLOTS_AXI_ADDR_MAX_WIDTH	C_MON_SLOTS_AXI_DATA_MAX_WIDTH	C_MAX_OUTSTAND_DEPTH	Slices	Slice Reg	LUTs
1	0	1	1	32	32	4	920	1673	1506
1	0	1	1	32	32	1	919	1689	1483
3	0	0	1	32	32	1	920	1673	1506
1	1	1	1	32	32	4	921	1698	1539
3	0	1	1	32	32	1	856	1719	1574
1	1	0	1	32	32	1	918	1681	1537

The AXI Performance Monitor resource utilization benchmarks for a variety of parameter combinations measured with Spartan-6 FPGA as the target device are shown in Table 2-3.

Table 2-3: **Resource Usage for Spartan-6 (XC6SLX45T-3-FGG484)**

C_NUM_MONITOR_SLOTS	C_NUM_AXIS_MONITOR_SLOTS	C_REG_ALL_MONITOR_SLOTS	C_MON_SLOTS_AXI_ID_MAX_WIDTH	C_MON_SLOTS_AXI_ADDR_MAX_WIDTH	C_MON_SLOTS_AXI_DATA_MAX_WIDTH	C_MAX_OUTSTAND_DEPTH	Slices	Slice Reg	LUTs
1	0	1	1	32	32	4	901	1683	1531
1	0	1	1	32	32	1	897	1699	1507
3	0	0	1	32	32	1	914	1729	1518
1	1	1	1	32	32	4	916	1750	1541
3	0	1	1	32	32	1	851	1772	1579
1	1	0	1	32	32	1	894	1690	1557

Signal Descriptions

This section describes the AXI Performance Monitor signals. The I/O signals include AXI interface signals through which the IP is configured and registers are read, and Monitor slot I/O signals to which the agents (masters/slaves) that need to be monitored are connected. Table 2-4 through Table 2-8 detail the pins.

AXI4 / AXI4-Lite I/O signals

Table 2-4: **AXI4 / AXI4-Lite I/O Signal Description**

Port	Name	Interface	I/O	Initial State	Description
AXI Interface System Signals					
P1	S_AXI_ACLK	System	I	-	AXI clock.
P2	S_AXI_ARESETN	System	I	-	AXI reset. Active Low.

Table 2-4: **AXI4 / AXI4-Lite I/O Signal Description *(Cont'd)***

Port	Name	Interface	I/O	Initial State	Description
AXI Write Address Channel Signals					
P3	S_AXI_AWADDR[C_S_AXI_ ADDR_WIDTH-1:0]	AXI4	I	-	AXI Write address. The write address bus gives the address of the first transfer in a write burst transaction
P4	S_AXI_AWPROT[2:0]	AXI4	I	-	Protection type. This signal indicates the normal, privileged, or secure protection level of the write transaction and whether the transaction is a data access or an instruction access. The default value is normal non secure data access
P5	S_AXI_AWVALID	AXI4	I	-	Write address valid. This signal indicates that valid write address and control information are available
P6	S_AXI_AWREADY	AXI4	O	0	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals
AXI Write Data Channel Signals					
P7	S_AXI_WDATA[C_S_AXI_ DATA_WIDTH-1:0]	AXI4	I	-	Write data bus.
P8	S_AXI_WSTB[C_S_AXI_ DATA_WIDTH/8-1:0]	AXI4	I	-	Write strobes. This signal indicates which byte lanes to update in memory
P10	S_AXI_WVALID	AXI4	I	-	Write valid. This signal indicates that valid write data and strobes are available
P11	S_AXI_WREADY	AXI4	O	0	Write ready. This signal indicates that the slave can accept the write data
AXI Write Response Channel Signals					
P12	S_AXI_BRESP[1:0]	AXI4	O	0	Write response. This signal indicates the status of the write transaction
P13	S_AXI_BVALID	AXI4	O	0	Write response valid. This signal indicates that a valid write response is available
P14	S_AXI_BREADY	AXI4	I	-	Response ready. This signal indicates that the master can accept the response information
AXI Read Address Channel Signals					
P15	S_AXI_ARADDR[C_S_AXI_ ADDR_WIDTH -1:0]	AXI4	I	-	Read address. The read address bus gives the initial address of a read burst transaction
P16	S_AXI_ARPROT[2:0]	AXI4	I	-	Protection type. This signal provides protection unit information for the read transaction. The default value is normal non secure data access

Table 2-4: **AXI4 / AXI4-Lite I/O Signal Description *(Cont'd)***

Port	Name	Interface	I/O	Initial State	Description
P17	S_AXI_ARVALID	AXI4	I	-	Read address valid. This signal indicates, when HIGH, that the read address and control information is valid and will remain stable until the address acknowledgement signal, S_AXI_ARREDY, is high.
P18	S_AXI_ARREADY	AXI4	O	0	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AXI Read Data Channel Signals					
P19	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	AXI4	O	0	Read data bus.
P20	S_AXI_RRESP[1:0]	AXI4	O	0	Read response. This signal indicates the status of the read transfer.
P21	S_AXI_RVALID	AXI4	O	0	Read valid. This signal indicates that the required read data is available and the read transfer can complete
P22	S_AXI_RREADY	AXI4	I	-	Read ready. This signal indicates that the master can accept the read data and response information
P23	IP2INTC_Irpt		O	0	Active-High Level triggered interrupt.

AXI4 MM Monitor Slot 0 I/O Signals

Table 2-5 describes the AXI4 Memory Mapped (MM) Monitor Slot 0 Interface signals.

Table 2-5: **AXI4 MM Monitor Slot 0 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_0_AXI_ACLK	Input	1	AXI Clock
SLOT_0_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_0_AXI_AWID	Input	C_SLOT_0_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_0_AXI_AWADDR	Input	C_SLOT_0_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_0_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)
SLOT_0_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_0_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2)
SLOT_0_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)

Table 2-5: **AXI4 MM Monitor Slot 0 I/O Signals *(Cont'd)***

Signal Name	Direction	Width	Description (Range)
SLOT_0_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_0_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_0_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_0_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_0_AXI_WDATA	Input	C_SLOT_0_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_0_AXI_WSTRB	Input	C_SLOT_0_AXI_DATA_WIDTH/ 8	Write Data Channel Byte Strobes
SLOT_0_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_0_AXI_WVALID	Input	1	Write Data Channel Valid
SLOT_0_AXI_WREADY	Input	1	Write Data Channel Ready
SLOT_0_AXI_BID	Input	C_SLOT_0_AXI_ID_WIDTH	Write Response Channel Transaction ID
SLOT_0_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3)
SLOT_0_AXI_BVALID	Input	1	Write Response Channel Valid
SLOT_0_AXI_BREADY	Input	1	Write Response Channel Ready
SLOT_0_AXI_ARID	Input	C_SLOT_0_AXI_ID_WIDTH	Read Address Channel Transaction ID
SLOT_0_AXI_ARADDR	Input	C_SLOT_0_AXI_ADDR_WIDTH	Read Address Channel Address
SLOT_0_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255)
SLOT_0_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7)
SLOT_0_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2)
SLOT_0_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1)
SLOT_0_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics
SLOT_0_AXI_ARPROT	Input	3	Read Address Channel Protection Bits
SLOT_0_AXI_ARVALID	Input	1	Read Address Channel Valid
SLOT_0_AXI_ARREADY	Input	1	Read Address Channel Ready
SLOT_0_AXI_RID	Input	C_SLOT_0_AXI_ID_WIDTH	Read Data Channel Transaction ID
SLOT_0_AXI_RDATA	Input	C_SLOT_0_AXI_DATA_WIDTH	Read Data Channel Data
SLOT_0_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3)

Table 2-5: **AXI4 MM Monitor Slot 0 I/O Signals *(Cont'd)***

Signal Name	Direction	Width	Description (Range)
SLOT_0_AXI_RLAST	Input	1	Read Data Channel Last Data Beat
SLOT_0_AXI_RVALID	Input	1	Read Data Channel Valid
SLOT_0_AXI_RREADY	Input	1	Read Data Channel Ready

AXI4 MM Monitor Slot 1 I/O Signals

Table 2-6 lists the AXI4 Memory Mapped (MM) Monitor Slot 1 Interface signals.

Table 2-6: **AXI4 MM Monitor Slot 1 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_1_AXI_ACLK	Input	1	AXI Clock
SLOT_1_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_1_AXI_AWID	Input	C_SLOT_1_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_1_AXI_AWADDR	Input	C_SLOT_1_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_1_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)
SLOT_1_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_1_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2)
SLOT_1_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_1_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_1_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_1_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_1_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_1_AXI_WDATA	Input	C_SLOT_1_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_1_AXI_WSTRB	Input	C_SLOT_1_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_1_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_1_AXI_WVALID	Input	1	Write Data Channel Valid
SLOT_1_AXI_WREADY	Input	1	Write Data Channel Ready
SLOT_1_AXI_BID	Input	C_SLOT_1_AXI_ID_WIDTH	Write Response Channel Transaction ID
SLOT_1_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3)
SLOT_1_AXI_BVALID	Input	1	Write Response Channel Valid

Table 2-6: **AXI4 MM Monitor Slot 1 I/O Signals *(Cont'd)***

Signal Name	Direction	Width	Description (Range)
SLOT_1_AXI_BREADY	Input	1	Write Response Channel Ready
SLOT_1_AXI_ARID	Input	C_SLOT_1_AXI_ID_WIDTH	Read Address Channel Transaction ID
SLOT_1_AXI_ARADDR	Input	C_SLOT_1_AXI_ADDR_WIDTH	Read Address Channel Address
SLOT_1_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255)
SLOT_1_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7)
SLOT_1_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2)
SLOT_1_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1)
SLOT_1_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics
SLOT_1_AXI_ARPROT	Input	3	Read Address Channel Protection Bits
SLOT_1_AXI_ARVALID	Input	1	Read Address Channel Valid
SLOT_1_AXI_ARREADY	Input	1	Read Address Channel Ready
SLOT_1_AXI_RID	Input	C_SLOT_1_AXI_ID_WIDTH	Read Data Channel Transaction ID
SLOT_1_AXI_RDATA	Input	C_SLOT_1_AXI_DATA_WIDTH	Read Data Channel Data
SLOT_1_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3)
SLOT_1_AXI_RLAST	Input	1	Read Data Channel Last Data Beat
SLOT_1_AXI_RVALID	Input	1	Read Data Channel Valid
SLOT_1_AXI_RREADY	Input	1	Read Data Channel Ready

AXI4 MM Monitor Slot 2 I/O Signals

Table 2-7 lists the AXI4 Memory Mapped (MM) Monitor Slot 2 Interface signals.

Table 2-7: **AXI4 MM Monitor Slot 2 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_2_AXI_ACLK	Input	1	AXI Clock
SLOT_2_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_2_AXI_AWID	Input	C_SLOT_2_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_2_AXI_AWADDR	Input	C_SLOT_2_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_2_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)

Table 2-7: **AXI4 MM Monitor Slot 2 I/O Signals *(Cont'd)***

Signal Name	Direction	Width	Description (Range)
SLOT_2_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_2_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2)
SLOT_2_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_2_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_2_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_2_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_2_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_2_AXI_WDATA	Input	C_SLOT_2_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_2_AXI_WSTRB	Input	C_SLOT_2_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_2_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_2_AXI_WVALID	Input	1	Write Data Channel Valid
SLOT_2_AXI_WREADY	Input	1	Write Data Channel Ready
SLOT_2_AXI_BID	Input	C_SLOT_2_AXI_ID_WIDTH	Write Response Channel Transaction ID
SLOT_2_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3)
SLOT_2_AXI_BVALID	Input	1	Write Response Channel Valid
SLOT_2_AXI_BREADY	Input	1	Write Response Channel Ready
SLOT_2_AXI_ARID	Input	C_SLOT_2_AXI_ID_WIDTH	Read Address Channel Transaction ID
SLOT_2_AXI_ARADDR	Input	C_SLOT_2_AXI_ADDR_WIDTH	Read Address Channel Address
SLOT_2_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255)
SLOT_2_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7)
SLOT_2_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2)
SLOT_2_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1)
SLOT_2_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics
SLOT_2_AXI_ARPROT	Input	3	Read Address Channel Protection Bits
SLOT_2_AXI_ARVALID	Input	1	Read Address Channel Valid

Table 2-7: **AXI4 MM Monitor Slot 2 I/O Signals *(Cont'd)***

Signal Name	Direction	Width	Description (Range)
SLOT_2_AXI_ARREADY	Input	1	Read Address Channel Ready
SLOT_2_AXI_RID	Input	C_SLOT_2_AXI_ID_WIDTH	Read Data Channel Transaction ID
SLOT_2_AXI_RDATA	Input	C_SLOT_2_AXI_DATA_WIDTH	Read Data Channel Data
SLOT_2_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3)
SLOT_2_AXI_RLAST	Input	1	Read Data Channel Last Data Beat
SLOT_2_AXI_RVALID	Input	1	Read Data Channel Valid
SLOT_2_AXI_RREADY	Input	1	Read Data Channel Ready

AXI4 MM Monitor Slot 3 I/O Signals

Table 2-8 lists the AXI4 Memory Mapped (MM) Monitor Slot 3 I/O signals.

Table 2-8: **AXI4 MM Monitor Slot 3 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_3_AXI_ACLK	Input	1	AXI Clock
SLOT_3_AXI_ARESETN	Input	1	AXI Active Low Reset
SLOT_3_AXI_AWID	Input	C_SLOT_3_AXI_ID_WIDTH	Write Address Channel Transaction ID
SLOT_3_AXI_AWADDR	Input	C_SLOT_3_AXI_ADDR_WIDTH	Write Address Channel Address
SLOT_3_AXI_AWLEN	Input	8	Write Address Channel Burst Length (0-255)
SLOT_3_AXI_AWSIZE	Input	3	Write Address Channel Transfer Size code (0-7)
SLOT_3_AXI_AWBURST	Input	2	Write Address Channel Burst Type code (0-2)
SLOT_3_AXI_AWLOCK	Input	2	Write Address Channel Atomic Access Type (0, 1)
SLOT_3_AXI_AWCACHE	Input	4	Write Address Channel Cache Characteristics
SLOT_3_AXI_AWPROT	Input	3	Write Address Channel Protection Bits
SLOT_3_AXI_AWVALID	Input	1	Write Address Channel Valid
SLOT_3_AXI_AWREADY	Input	1	Write Address Channel Ready
SLOT_3_AXI_WDATA	Input	C_SLOT_3_AXI_DATA_WIDTH	Write Data Channel Data
SLOT_3_AXI_WSTRB	Input	C_SLOT_3_AXI_DATA_WIDTH/8	Write Data Channel Byte Strobes
SLOT_3_AXI_WLAST	Input	1	Write Data Channel Last Data Beat
SLOT_3_AXI_WVALID	Input	1	Write Data Channel Valid.

Table 2-8: **AXI4 MM Monitor Slot 3 I/O Signals *(Cont'd)***

Signal Name	Direction	Width	Description (Range)
SLOT_3_AXI_WREADY	Input	1	Write Data Channel Ready.
SLOT_3_AXI_BID	Input	C_SLOT_3_AXI_ID_WIDTH	Write Response Channel Transaction ID
SLOT_3_AXI_BRESP	Input	2	Write Response Channel Response Code (0-3)
SLOT_3_AXI_BVALID	Input	1	Write Response Channel Valid
SLOT_3_AXI_BREADY	Input	1	Write Response Channel Ready
SLOT_3_AXI_ARID	Input	C_SLOT_3_AXI_ID_WIDTH	Read Address Channel Transaction ID
SLOT_3_AXI_ARADDR	Input	C_SLOT_3_AXI_ADDR_WIDTH	Read Address Channel Address
SLOT_3_AXI_ARLEN	Input	8	Read Address Channel Burst Length code(0-255)
SLOT_3_AXI_ARSIZE	Input	3	Read Address Channel Transfer Size code (0-7)
SLOT_3_AXI_ARBURST	Input	2	Read Address Channel Burst Type (0-2)
SLOT_3_AXI_ARLOCK	Input	2	Read Address Channel Atomic Access Type (0, 1)
SLOT_3_AXI_ARCACHE	Input	4	Read Address Channel Cache Characteristics
SLOT_3_AXI_ARPROT	Input	3	Read Address Channel Protection Bits
SLOT_3_AXI_ARVALID	Input	1	Read Address Channel Valid
SLOT_3_AXI_ARREADY	Input	1	Read Address Channel Ready
SLOT_3_AXI_RID	Input	C_SLOT_3_AXI_ID_WIDTH	Read Data Channel Transaction ID
SLOT_3_AXI_RDATA	Input	C_SLOT_3_AXI_DATA_WIDTH	Read Data Channel Data
SLOT_3_AXI_RRESP	Input	2	Read Data Channel Response Code (0-3)
SLOT_3_AXI_RLAST	Input	1	Read Data Channel Last Data Beat
SLOT_3_AXI_RVALID	Input	1	Read Data Channel Valid
SLOT_3_AXI_RREADY	Input	1	Read Data Channel Ready

AXI4-Stream Monitor Slot 0I/O Signals

Table 2-9 lists the AXI4-Stream Monitor Slot 0 I/O signals.

Table 2-9: **Monitor Slot 0 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_0_AXIS_ACLK	Input	1	AXI Clock
SLOT_0_AXIS_ARESETN	Input	1	AXI Active Low Reset
SLOT_0_AXIS_TVALID	Input	1	Indicates that the master is driving valid transfer
SLOT_0_AXIS_TREADY	Input	1	Indicates that the slave can accept a transfer in the current cycle
SLOT_0_AXIS_TDATA	Input	C_SLOT_0_AXIS_DATA_WIDTH	Primary payload
SLOT_0_AXIS_TSTRB	Input	C_SLOT_0_AXI_DATA_WIDTH/8	Byte qualifier (data byte or a position byte)
SLOT_0_AXIS_TKEEP	Input	C_SLOT_0_AXI_DATA_WIDTH/8	Byte qualifier (data byte or a null byte)
SLOT_0_AXIS_TLAST	Input	1	Indicates the boundary of a packet
SLOT_0_AXIS_TID	Input	C_SLOT_0_AXIS_ID_WIDTH	Data stream identifier
SLOT_0_AXIS_TDEST	Input	C_SLOT_0_AXIS_DEST_WIDTH	Provides routing information for the data stream
SLOT_0_AXIS_TUSER	Input	C_SLOT_0_AXIS_USER_WIDTH	User defined sideband information

AXI4-Stream Monitor Slot 1 I/O Signals

Table 2-10 lists the AXI4-Stream Monitor Slot 1 I/O signals.

Table 2-10: **Monitor Slot 1 I/O Signals**

Signal Name	Direction	Width	Description (Range)
SLOT_1_AXIS_ACLK	Input	1	AXI Clock
SLOT_1_AXIS_ARESETN	Input	1	AXI Active Low Reset
SLOT_1_AXIS_TVALID	Input	1	Indicates that the master is driving valid transfer
SLOT_1_AXIS_TREADY	Input	1	Indicates that the slave can accept a transfer in the current cycle
SLOT_1_AXIS_TDATA	Input	C_SLOT_1_AXIS_DATA_WIDTH	Primary payload
SLOT_1_AXIS_TSTRB	Input	C_SLOT_1_AXI_DATA_WIDTH/8	Byte qualifier (data byte or a position byte)
SLOT_1_AXIS_TKEEP	Input	C_SLOT_1_AXI_DATA_WIDTH/8	Byte qualifier (data byte or a null byte)
SLOT_1_AXIS_TLAST	Input	1	Indicates the boundary of a packet
SLOT_1_AXIS_TID	Input	C_SLOT_1_AXIS_ID_WIDTH	Data stream identifier
SLOT_1_AXIS_TDEST	Input	C_SLOT_1_AXIS_DEST_WIDTH	Provides routing information for the data stream
SLOT_1_AXIS_TUSER	Input	C_SLOT_1_AXIS_USER_WIDTH	User defined sideband information

Core Signals

Table 2-11 lists the core signals.

Table 2-11: **Core I/O Signals**

Signal Name	Direction	Width	Description (Range)
CORE_ACLK	Input	1	Core Clock. Highest frequency clock in the system (Interconnect clock)
CORE_ARESETN	Input	1	Active-Low Reset. Reset of the slowest clock domain in the system
CAPTURE_EVENT	Input	1	Active-High Capture Event. Metric counters are sampled into Sampled Metric Counter registers. Synchronous to CORE_ACLK.
RESET_EVENT	Input	1	Active-High Reset Event. Metric counters are reset. Synchronous to CORE_ACLK.

Design Parameters

Table 2-12 describes the core design parameters.

Table 2-12: **AXI Performance Monitor Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters					
G1	Target FPGA family	C_FAMILY	virtex6, spartan6	virtex6	string
G2	AXI Base Address	C_BASEADDR	Valid Address (1)	0xFFFFFFFF (3)	std_logic_vector
G3	AXI High Address	C_HIGHADDR	Valid Address (2)	0x00000000 (3)	std_logic_vector
AXI Interface Parameters					
G4	AXI Identification tag width	C_S_AXI_ID_WIDTH	1-16	4	integer
G5	AXI most significant address bus width	C_S_AXI_ADDR_WIDTH	32	32	integer
G6	AXI data bus width	C_S_AXI_DATA_WIDTH	32, 64	32	integer
G7	AXI protocol	C_S_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
AXI4-MM SLOT 0 Monitor Interface Parameters					
G8	SLOT 0 AXI Identification tag width	C_SLOT_0_AXI_ID_WIDTH	1-16	4	integer

Table 2-12: **AXI Performance Monitor Design Parameters *(Cont'd)***

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G9	SLOT 0 AXI address bus width	C_SLOT_0_AXI_ADDR_WIDTH	32	32	integer
G10	SLOT 0 AXI data bus width	C_SLOT_0_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer
G11	SLOT 0 AXI protocol	C_SLOT_0_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G12	SLOT 0 AXI clock div value	C_SLOT_0_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
AXI4-MM SLOT 1 Monitor Interface Parameters					
G13	SLOT 1 AXI Identification tag width	C_SLOT_1_AXI_ID_WIDTH	1-16	4	integer
G14	SLOT 1 AXI address bus width	C_SLOT_1_AXI_ADDR_WIDTH	32	32	integer
G15	SLOT 1 AXI data bus width	C_SLOT_1_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer
G16	SLOT 1 AXI protocol	C_SLOT_1_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G17	SLOT 1 AXI clock div value	C_SLOT_1_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
AXI4-MM SLOT 2 Monitor Interface Parameters					
G18	SLOT 2 AXI Identification tag width	C_SLOT_2_AXI_ID_WIDTH	1-16	4	integer
G19	SLOT 2 AXI address bus width	C_SLOT_2_AXI_ADDR_WIDTH	32	32	integer
G20	SLOT 2 AXI data bus width	C_SLOT_2_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer
G21	SLOT 2 AXI protocol	C_SLOT_2_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G22	SLOT 2 AXI clock div value	C_SLOT_2_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
AXI4-MM SLOT 3 Monitor Interface Parameters					
G23	SLOT 3 AXI Identification tag width	C_SLOT_3_AXI_ID_WIDTH	1-16	4	integer
G24	SLOT 3 AXI address bus width	C_SLOT_3_AXI_ADDR_WIDTH	32	32	integer
G25	SLOT 3 AXI data bus width	C_SLOT_3_AXI_DATA_WIDTH	32, 64, 128, 256	32	integer

Table 2-12: **AXI Performance Monitor Design Parameters *(Cont'd)***

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G26	SLOT 3 AXI protocol	C_SLOT_3_AXI_PROTOCOL	AXI4, AXI4LITE	AXI4	string
G27	SLOT 3 AXI clock div value	C_SLOT_3_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
AXI4-S SLOT 0 Monitor Interface Parameters					
G28	SLOT 0 AXIS data bus width	C_SLOT_0_AXIS_DATA_WIDTH	32, 64, 128, 256	32	integer
G29	SLOT 0 AXIS Identification tag width	C_SLOT_0_AXIS_ID_WIDTH	1-8	1	integer
G30	SLOT 0 AXIS Destination tag width	C_SLOT_0_AXIS_DEST_WIDTH	1-4	1	integer
G31	SLOT 0 AXIS Destination tag width	C_SLOT_0_AXIS_USER_WIDTH	1-128	1	integer
G32	SLOT 0 AXIS clock div value	C_SLOT_0_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
AXI4-S SLOT 1 Monitor Interface Parameters					
G33	SLOT 1 AXIS data bus width	C_SLOT_1_AXIS_DATA_WIDTH	32, 64, 128, 256	32	integer
G34	SLOT 1 AXIS Identification tag width	C_SLOT_1_AXIS_ID_WIDTH	1-8	1	integer
G35	SLOT 1 AXIS Destination tag width	C_SLOT_1_AXIS_DEST_WIDTH	1-4	1	integer
G36	SLOT 1 AXIS Destination tag width	C_SLOT_1_AXIS_USER_WIDTH	1-128	1	integer
G37	SLOT 1 AXIS clock div value	C_SLOT_1_AXI_CLK_DIV_VAL	1-16	X"1"	std_logic_vector
Monitor Slots Maximum Widths					
G38	Maximum width of AXI Identification tag	C_MON_SLOTS_AXI_ID_MAX_WIDTH	1-16	4	integer
G39	Maximum AXI address bus width	C_MON_SLOTS_AXI_ADDR_MAX_WIDTH	32	32	integer
G40	Maximum AXI data bus width	C_MON_SLOTS_AXI_DATA_MAX_WIDTH	32, 64, 128, 256	32	integer

Table 2-12: **AXI Performance Monitor Design Parameters *(Cont'd)***

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Counter Width and max outstanding Parameters					
G41	Width of all the counters inside the monitors	C_METRIC_COUNT_WIDTH	32, 64	32	integer
G42	Width of the Global Free running counter	C_GLOBAL_COUNT_WIDTH	32, 64, 128	32	integer
G43	Maximum Number of outstanding requests given/ taken by any agent in the system	C_MAX_OUTSTAND_DEPTH	1-16	1	integer

Notes:

1. The user must set values.
2. The range specified by C_HIGHADDR - C_BASEADDR must be a power of 2 and greater than equal to C_BASEADDR + 0x1FFF.
3. An invalid default value will be specified to insure that the actual value is set, i.e., if the value is not set, a compiler error will be generated.

Register Space

This section details the registers and reset values of the AXI Performance Monitor core. Table 2-13 shows all the AXI Performance Monitor registers and addresses.

Table 2-13: **Registers**

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x0000	Control Register	Write/Read	0x0	Control Register
C_BASEADDR + 0x0004	Read Latency Range A Register	Write/Read	0x0	Read Latency Range A Register
C_BASEADDR + 0x0008	Read Latency Range B Register	Write/Read	0x0	Read Latency Range B Register
C_BASEADDR + 0x000C	Read Latency Range C Register	Write/Read	0x0	Read Latency Range C Register
C_BASEADDR + 0x0010	Read Latency Range D Register	Write/Read	0x0	Read Latency Range D Register

Table 2-13: **Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x0014	Write Latency Range A Register	Write/Read	0x0	Write Latency Range A Register
C_BASEADDR + 0x0018	Write Latency Range B Register	Write/Read	0x0	Write Latency Range B Register
C_BASEADDR + 0x0024	Metric Selector Register	Write/Read	0x0	Metric Selector register
C_BASEADDR + 0x0028	Sample Interval MSB(1)	Write/Read	0x0	Higher 32-bit data of Sample Interval Register
C_BASEADDR + 0x002C	Sample Interval LSB	Write/Read	0x0	Lower 32-bit data of Sample Interval Register
C_BASEADDR + 0x0030	Sample Interval Control Register	Write/Read	0x0	Sample Interval Control Register
C_BASEADDR + 0x0040	Global Interrupt Enable Register	Write/Read	0x0	Global Interrupt Enable Register
C_BASEADDR + 0x0044	Interrupt Enable Register	Write/Read	0x0	Interrupt Enable Register
C_BASEADDR + 0x0048	Interrupt Status Register	Read	0x0	Interrupt Status Register
C_BASEADDR + 0x1000	Metric Counter 0(2)	Read	0x0	Higher 32-bit data of the Metric Counter 0 Register
C_BASEADDR + 0x1004	Metric Counter 0	Read	0x0	Lower 32-bit data of the Metric Counter 0 Register
C_BASEADDR + 0x1008	Metric Counter 1(2)	Read	0x0	Higher 32-bit data of the Metric Counter 1 Register
C_BASEADDR + 0x100C	Metric Counter 1	Read	0x0	Lower 32-bit data of the Metric Counter 1 Register
C_BASEADDR + 0x1010	Metric Counter 2(2)	Read	0x0	Higher 32-bit data of the Metric Counter 2 Register
C_BASEADDR + 0x1014	Metric Counter 2	Read	0x0	Lower 32-bit data of the Metric Counter 2 Register
C_BASEADDR + 0x1018	Metric Counter 3(2)	Read	0x0	Higher 32-bit data of the Metric Counter 3 Register

Table 2-13: **Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x101C	Metric Counter 3	Read	0x0	Lower 32-bit data of the Metric Counter 3 Register
C_BASEADDR + 0x1020	Metric Counter 4(2)	Read	0x0	Higher 32-bit data of the Metric Counter 4 Register
C_BASEADDR + 0x1024	Metric Counter 4	Read	0x0	Lower 32-bit data of the Metric Counter 4 Register
C_BASEADDR + 0x1028	Metric Counter 5(2)	Read	0x0	Higher 32-bit data of the Metric Counter 5 Register
C_BASEADDR + 0x102C	Metric Counter 5	Read	0x0	Lower 32-bit data of the Metric Counter 5 Register
C_BASEADDR + 0x1030	Metric Counter 6(2)	Read	0x0	Higher 32-bit data of the Metric Counter 6 Register
C_BASEADDR + 0x1034	Metric Counter 6	Read	0x0	Lower 32-bit data of the Metric Counter 6 Register
C_BASEADDR + 0x1038	Metric Counter 7(2)	Read	0x0	Higher 32-bit data of the Metric Counter 7 Register
C_BASEADDR + 0x103C	Metric Counter 7	Read	0x0	Lower 32-bit data of the Metric Counter 7 Register
C_BASEADDR + 0x1040	Metric Counter 8(2)	Read	0x0	Higher 32-bit data of the Metric Counter 8 Register
C_BASEADDR + 0x1044	Metric Counter 8	Read	0x0	Lower 32-bit data of the Metric Counter 8 Register
C_BASEADDR + 0x1048	Metric Counter 9(2)	Read	0x0	Higher 32-bit data of the Metric Counter 9 Register
C_BASEADDR + 0x104C	Metric Counter 9	Read	0x0	Lower 32-bit data of the Metric Counter 9 Register
C_BASEADDR + 0x0800	Global Clock Counter(2)	Read	0x0	(127 downto 96) data of the Global Clock Counter Register
C_BASEADDR + 0x0804	Global Clock Counter(3)	Read	0x0	(95 downto 64) data of the Global Clock Counter Register
C_BASEADDR + 0x0808	Global Clock Counter(4)	Read	0x0	(63 downto 32) data of the Global Clock Counter Register
C_BASEADDR + 0x080C	Global Clock Counter	Read	0x0	Lower 32-bit data of the Global Clock Counter Register
C_BASEADDR + 0x2000	Sampled Metric Counter 0(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 0 Register
C_BASEADDR + 0x2004	Sampled Metric Counter 0	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 0 Register

Table 2-13: **Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x2008	Sampled Metric Counter 1(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 1 Register
C_BASEADDR + 0x200C	Sampled Metric Counter 1	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 1 Register
C_BASEADDR + 0x2010	Sampled Metric Counter 2(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 2 Register
C_BASEADDR + 0x2014	Sampled Metric Counter 2	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 2 Register
C_BASEADDR + 0x2018	Sampled Metric Counter 3(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 3 Register
C_BASEADDR + 0x201C	Sampled Metric Counter 3	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 3 Register
C_BASEADDR + 0x2020	Sampled Metric Counter 4(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 4 Register
C_BASEADDR + 0x2024	Sampled Metric Counter 4	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 4 Register
C_BASEADDR + 0x2028	Sampled Metric Counter 5(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 5 Register
C_BASEADDR + 0x202C	Sampled Metric Counter 5	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 5 Register
C_BASEADDR + 0x2030	Sampled Metric Counter 6(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 6 Register
C_BASEADDR + 0x2034	Sampled Metric Counter 6	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 6 Register
C_BASEADDR + 0x2038	Sampled Metric Counter 7(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 7 Register
C_BASEADDR + 0x203C	Sampled Metric Counter 7	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 7 Register

Table 2-13: **Registers *(Cont'd)***

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x2040	Sampled Metric Counter 8(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 8 Register
C_BASEADDR + 0x2044	Sampled Metric Counter 8	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 8 Register
C_BASEADDR + 0x2048	Sampled Metric Counter 9(2)	Read	0x0	Higher 32-bit data of the Sampled Metric Counter 9 Register
C_BASEADDR + 0x204C	Sampled Metric Counter 9	Read	0x0	Lower 32-bit data of the Sampled Metric Counter 9 Register

1. These registers are valid only if C_METRICS_SAMPLE_COUNT_WIDTH is > 32.
2. These registers are valid only if C_METRIC_COUNT_WIDTH is 64.
3. These registers are valid only if C_GLOBAL_COUNT_WIDTH is 128.
4. These registers are valid only if C_GLOBAL_COUNT_WIDTH is 64 or 128.

Control Register

The Control Register is a 32-bit register as shown in Figure 2-1. This register is used to enable the global free-running counter and metrics counters inside the core. The bit definition and accessibility of this register are shown in Table 2-14.

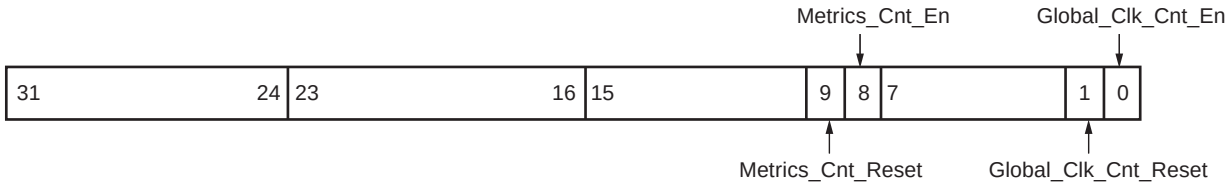

Figure 2-1: **Control Register**

Table 2-14: **Control Register Bit Definitions (C_BASEADDR + 0x0000)**

Bit	Name	Access	Reset Value	Description
31-10	Reserved	N/A	N/A	Reserved
9	Metrics_Cnt_Reset	Read/Write	0	1: Resets all the metrics counters in the monitor.
8	Metrics_Cnt_En	Read/Write	0	1: Enables all the metrics counters in the monitor.
7-2	Reserved	N/A	N/A	Reserved

Table 2-14: **Control Register Bit Definitions (C_BASEADDR + 0x0000) *(Cont'd)***

Bit	Name	Access	Reset Value	Description
1	Global_Clk_Cnt_Reset	Read/Write	0	1: Resets the free-running Global Clock Counter
0	Global_Clk_Cnt_En	Read/Write	0	1: Enables the free-running Global Clock Counter

Read Latency Range A Register

The Read Latency Range A Register is a 32-bit register as shown in Figure 2-2. This register is used to store two read latency ranges. The bit definition and accessibility of this register are shown in Table 2-15.

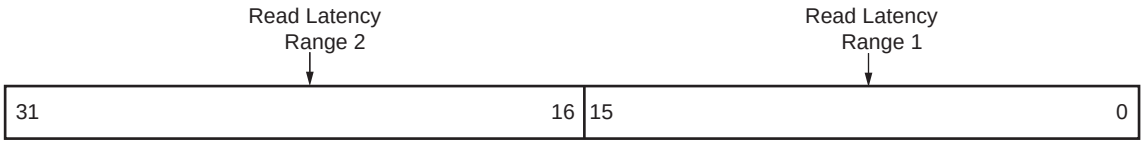

Figure 2-2: **Read Latency Range A Register**

Table 2-15: **Read Latency Range A Register Bit Definitions (C_BASEADDR + 0x0004)**

Bit	Name	Access	Reset Value	Description
31-16	Read Latency Range 2	Write	0x00	Read Latency Range 2. Read transactions with a latency between Read Latency Range 1 and this value have a Range 2 Latency.
15-0	Read Latency Range 1	Write	0x00	Read Latency Range 1. Read transactions with a latency between 0 and this value have a Range 1 Latency.

Read Latency Range B Register

The Read Latency Range B Register is a 32-bit register, as shown in Figure 2-3. This register is used to store two read latency ranges. The bit definition and accessibility of this register are shown in Table 2-16.

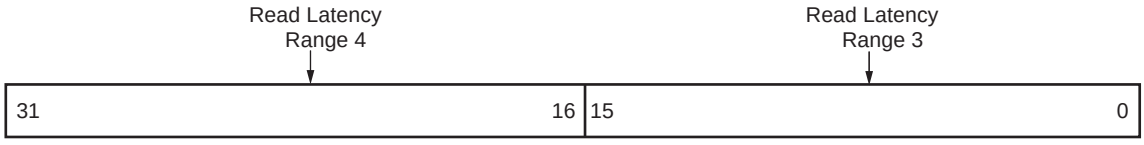

Figure 2-3: **Read Latency Range B Register**

Table 2-16: **Read Latency Range B Register Bit Definitions (C_BASEADDR + 0x0008)**

Bit	Name	Access	Reset Value	Description
31-16	Read Latency Range 4	Read/Write	0x50	Read Latency Range 4. Read transactions with a latency between Read Latency Range 3 and this value have a Range 4 Latency.
15-0	Read Latency Range 3	Read/Write	0x40	Read Latency Range 3. Read transactions with a latency between Read Latency Range 2 and this value have a Range 3 Latency.

Read Latency Range C Register

The Read Latency Range C Register is a 32-bit register as shown in Figure 2-4. This register is used to store two read latency ranges. The bit definition and accessibility of this register are shown in Table 2-17.

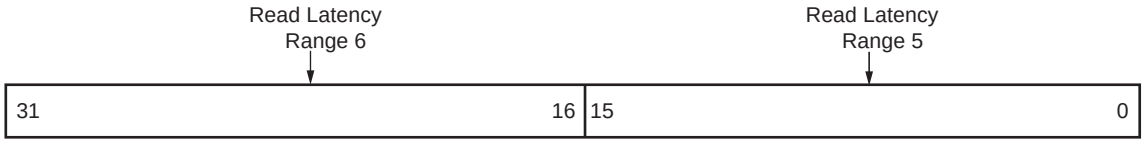

Figure 2-4: **Read Latency Range C Register**

Table 2-17: **Read Latency Range C Register Bit Definitions (C_BASEADDR + 0x000C)**

Bit	Name	Access	Reset Value	Description
31-16	Read Latency Range 6	Read/Write	0x00	Read Latency Range 6. Read transactions with a latency between Read Latency Range 5 and this value have a Range 6 Latency.
15-0	Read Latency Range 5	Read/Write	0x00	Read Latency Range 5. Read transactions with a latency between Read Latency Range 4 and this value have a Range 5 Latency.

Read Latency Range D Register

The Read Latency Range D Register is a 32-bit register as shown in Figure 2-5. This register is used to store two read latency ranges. The bit definition and accessibility of this register are shown in Table 2-18.

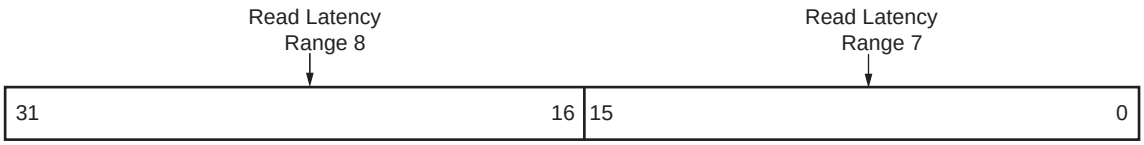

Figure 2-5: **Read Latency Range D Register**

Table 2-18: **Read Latency Range D Register Bit Definitions (C_BASEADDR + 0x0010)**

Bit	Name	Access	Reset Value	Description
31-16	Read Latency Range 8	Read/Write	0x00	Read Latency Range 8. Read transactions with a latency between Read Latency Range 7 and this value have a Range 8 Latency.
15-0	Read Latency Range 7	Read/Write	0x00	Read Latency Range 7. Read transactions with a latency between Read Latency Range 6 and this value have a Range 7 Latency.

Write Latency Range A Register

The Write Latency Range A Register is a 32-bit register as shown in Figure 2-6. This register is used to store two Write latency ranges. The bit definition and accessibility of this register are shown in Table 2-19.

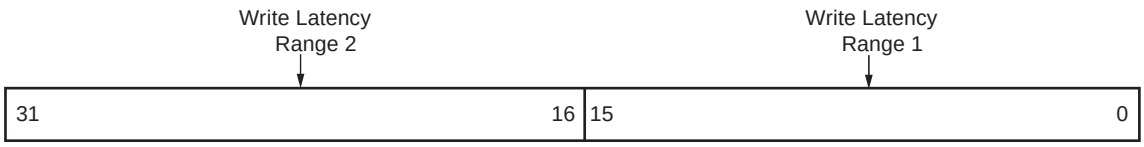

Figure 2-6: **Write Latency Range A Register**

Table 2-19: **Write Latency Range A Register Bit Definitions (C_BASEADDR + 0x0014)**

Bit	Name	Access	Reset Value	Description
31-16	Write Latency Range 2	Read/Write	0x00	Write Latency Range 2. WRite transactions with a latency between Write Latency Range 1 and this value have a Range 2 Latency.
15-0	Write Latency Range 1	Read/Write	0x00	Write Latency Range 1. Write transactions with a latency between 0 and this value have a Range 1 Latency.

Write Latency Range B Register

The Write Latency Range B Register is a 32-bit register as shown in Figure 2-7. This register is used to store two Write latency ranges. The bit definition and accessibility of this register is shown in Table 2-20.

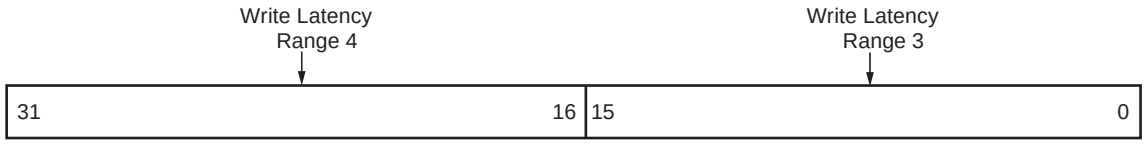

Figure 2-7: **Write Latency Range B Register**

Table 2-20: **Write Latency Range A Register Bit Definitions (C_BASEADDR + 0x0018)**

Bit	Name	Access	Reset Value	Description
31-16	Write Latency Range 4	Read/Write	0x00	Write Latency Range 4. Write transactions with a latency between Write Latency Range 3 and this value have a Range 4 Latency.
15-0	Write Latency Range 3	Read/Write	0x00	Write Latency Range 3. Write transactions with a latency between Write Latency Range 2 and this value have a Range 3 Latency.

Metric Selector Register

The Metric Selector Register is a 32-bit register, as shown in Figure 2-8. This register is used to select the metric set and the agent for which the metrics need to be computed. The bit definition and accessibility of this register are shown in Table 2-21.

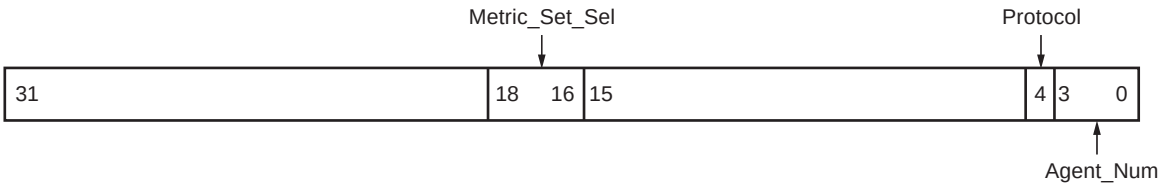

Figure 2-8: **Metric Selector Register**

Table 2-21: **Metric Selector Register Bit Definitions (C_BASEADDR + 0x0024)**

Bit	Name	Access	Reset Value	Description
31-19	Reserved	N/A	N/A	Reserved
18-16	Metric_Set_Sel	Write	x0	• b000: Set 0 of metrics • b001: Set 1 of metrics • b010: Set 2 of metrics • b011: Set 3 of metrics • b100: Set 4 of metrics • b101: Set 5 of metrics • b110: Set 6 of metrics • b111: Set 7 of metrics
15-5	Reserved	N/A	N/A	Reserved
4	Protocol	Write	0	Protocol is the type of monitor slot that will be selected. • 0: AXI4 MM monitor slots • 1: AXI4-Stream monitor slots
3-0	Agent_Num	Write	x00	Agent Number is the slot number for which the metrics would be computed. Agent Number should be less than the number of monitor slots.

Sample Interval Register

The Sample Interval is a 32/64-bit read/write register as shown in Figure 2-9. This register holds the load value for the sample interval down counter used in generating a capture event for capturing the metric counters into Sampled Metric Counter registers. The bit definition and accessibility of this register is shown in Table 2-12.

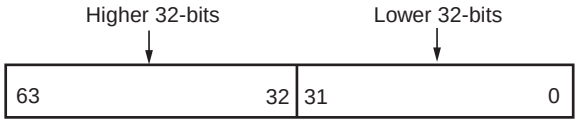

Figure 2-9: **Sample Interval Register**

Table 2-22: **Sample Interval Register Bit Definitions (C_BASEADDR + 0x0028)**

Bit	Name	Access	Reset Value	Description
63-32	Sample Interval	Read/Write	0x00	[63:32] bits of Sample Interval Register
31-0	Sample Interval	Read/Write	0x00	Lower 32-bits of Sample Interval Register

Notes:

1. If parameter C_S_AXI_DATA_WIDTH is 32, then the register can be read by doing a read transaction to 2 locations, i.e. to (C_BASEADDR + 0x0028) and (C_BASEADDR + 0x002C) locations
2. If C_METRICS_SAMPLE_COUNT_WIDTH<=32, then only lower 32-bits of the register are valid
3. If C_METRICS_SAMPLE_COUNT_WIDTH>64, then higher 64-bits of the register are also valid

Sample Interval Control Register

The Sample Interval Control Register is a 32-bit register as shown in Figure 2-10. This register is used to control the sample interval down counter inside the monitor. The bit definition and accessibility of this register is shown in Table 2-23.

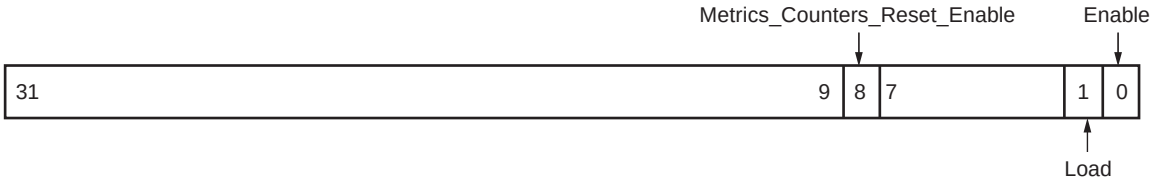

Figure 2-10: **Sample Interval Control Register**

Table 2-23: **Sample Interval Control Register Bit Definitions (C_BASEADDR + 0x0030)**

Bit	Name	Access	Reset Value	Description
31-9	Reserved	N/A	N/A	Reserved
8	Metric_Counters_ Reset_Enable	Read/Write	'0'	1: Metric Counters are reset when sample interval counter overflows.
7-2	Reserved	N/A	N/A	Reserved

Table 2-23: **Sample Interval Control Register Bit Definitions (C_BASEADDR + 0x0030) *(Cont'd)***

Bit	Name	Access	Reset Value	Description
1	Load	Read/Write	'0'	1: Loads the Sample Interval register value into the Sample Interval Counter.
0	Enable	Read/Write	'0'	1: Enable the down counter. Before enabling, the counter should be loaded with the sample Interval Register value.

Global Interrupt Enable Register

The Global Interrupt Enable Register provides the master enable/disable for the interrupt output to the processor. This is a single read/write register as shown in Figure 2-11.

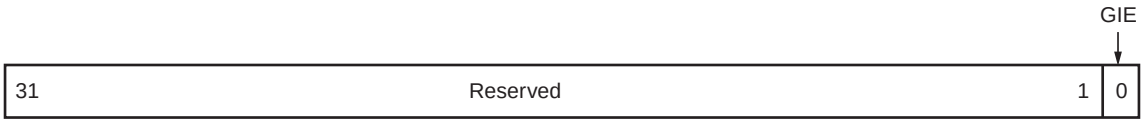

Figure 2-11: **Global Interrupt Enable Register**

Table 2-24: **Global Interrupt Enable Register Bit Definitions (C_BASEADDR + 0x0040)**

Bit	Name	Access	Reset Value	Description
31-1	Reserved	N/A	0	Reserved. Set to zeros on a read.
0	GIE	Read/Write	'0'	Master enable for the device interrupt output to the system interrupt controller: • 1: Enabled • 0: Disabled

Interrupt Enable Register

This is a read/write register. Writing a '1' to a bit in this register enables the corresponding ISR bit to cause assertion of the Interrupt. An IER bit set to '0' does not inhibit an interrupt condition for being captured, just reported. Writing a '0' to a bit disables, or masks, will disable the generation of interrupt output for corresponding interrupt signal.

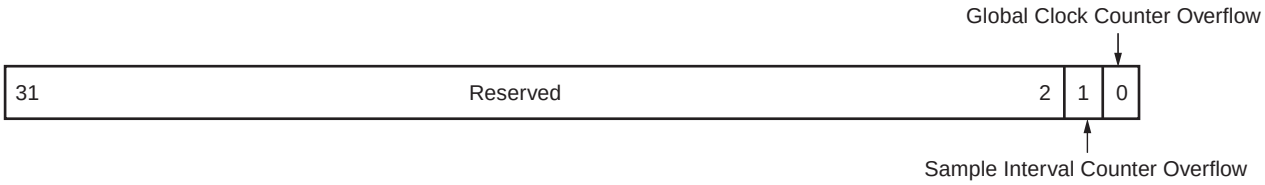

Figure 2-12: **Interrupt Enable Register**

Table 2-25: **Interrupt Enable Register Bit Definitions (C_BASEADDR + 0x0044)**

Bit	Name	Access	Reset Value	Description
31-2	Reserved	N/A	0	Reserved. Set to zeros on a read.
1	Sample Interval Counter Overflow Interrupt Enable	Read/Write	'0'	Sample Interval Counter Overflow Interrupt • 1: Enabled • 0: Disabled
0	Global Clock Counter Overflow Interrupt Enable	Read/Write	'0'	Enable Global Clock Counter Overflow Interrupt • 1: Enabled • 0: Disabled

Interrupt Status Register

When read, the contents of this register indicate the presence or absence of an active interrupt signal. Each bit in this register that is set to a '1' indicates an active interrupt signal. Bits that are '0' are not active. The bits in the ISR are independent of the interrupt enable bits in the IER. The interrupt can be cleared by writing '1' to the corresponding bit in the Interrupt Status registers.

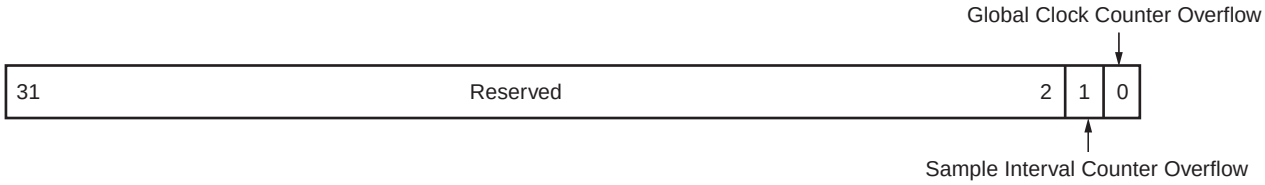

Figure 2-13: **Interrupt Status Register**

Table 2-26: **Interrupt Status Register Bit Definitions (C_BASEADDR + 0x0048)**

Bit	Name	Access	Reset Value	Description
31-2	Reserved	N/A	0	Reserved. Set to zeros on a read.
1	Sample Interval Counter Overflow Interrupt	Read/Write	0	Sample Interval Counter Overflow Interrupt • 1: Active • 0: Not Active
0	Global Clock Counter Overflow Interrupt	Read/Write	0	Global Clock Counter Overflow Interrupt • 1: Active • 0: Not Active

Global Clock Count Register

The Global Clock Count is a 32/64/128-bit read register, as shown in Figure 2-14. This register holds the total number of simulation cycles. This register should only be read after making Global Clock Count Enable Low. The bit definition and accessibility of this register are shown in Table 2-27.

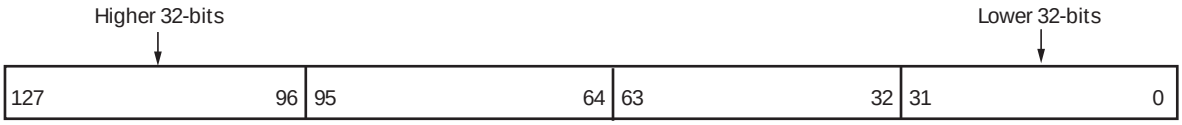

Figure 2-14: **Global Clock Count Register**

Table 2-27: **Global Clock Count Register Bit Definitions (C_BASEADDR + 0x0800)**

Bit	Name	Access	Reset Value	Description
127-96	Global Clock Count	Read	0x00	Higher 32 bits of Global Clock Count Register
95-64	Global Clock Count	Read	0x00	[95:64] bits of Global Clock Count Register
63-32	Global Clock Count	Read	0x00	[63:32] bits of Global Clock Count Register
31-0	Global Clock Count	Read	0x00	Lower 32 bits of Global Clock Count Register

Notes:

1. If parameter C_S_AXI_DATA_WIDTH is 32, the register can be read by a read transaction to four locations: (C_BASEADDR + 0x800), (C_BASEADDR + 0x804), (C_BASEADDR + 0x808) and (C_BASEADDR + 0x80C).
2. If C_GLOBAL_COUNT_WIDTH=32, only the lower 32 bits of the register are valid.
3. If C_GLOBAL_COUNT_WIDTH=64, only the lower 64 bits of the register are valid.

Metric Counter Registers

Table 2-28 through Table 2-30 show sets 0 through 7 of the Metric Counter registers. These registers should be only be read after making Metric Count Enable Low.

Table 2-28: **Metric Counter Registers: Sets 0 through 2**

Metric Counter	Address	Set 0 (Metric_Set_Sel =b000)	Set 1 (Metric_Set_Sel = b001)	Set 2 (Metric_Set_Sel = b010)
0	0x1000 - 0x1004	Read Latency Range 1	Write Latency Range 1	Write Transaction Count
1	0x1008 - 0x100C	Read Latency Range 2	Write Latency Range 2	Read Transaction Count
2	0x1010 - 0x1014	Read Latency Range 3	Write Latency Range 3	Slv_Wr_Idle_Cnt
3	0x1018 - 0x101C	Read Latency Range 4	Write Latency Range 4	Mst_Rd_Idle_Cnt
4	0x1020 - 0x1024	Read Latency Range 5	Write Latency Range 5	Num_BValids
5	0x1028 - 0x102C	Read Latency Range 6	Write Transaction Count	Num_WLasts
6	0x1030 - 0x1034	Read Latency Range 7	Read Transaction Count	Num_RLasts
7	0x1038 - 0x103C	Read Latency Range 8	Write Byte Count	Num_Wr_Bursts_Len0
8	0x1040 - 0x1044	Read Latency Range 9	Read Byte Count	Num_Rd_Bursts_Len0
9	0x1048 - 0x104C	Total Read Latency	Total Write Latency	Total Write Latency

Table 2-29 shows sets 3 through 5 of the Metric Counter registers.

Table 2-29: **Metric Counter Registers: Sets 3 through 5**

Metric Counter	Address	Set 3 (Metric_Set_Sel =b011)	Set 4 (Metric_Set_Sel = b100)	Set 5 (Metric_Set_Sel = b101)
0	0x1000 - 0x1004	Read Latency Range 1	Write Latency Range 1	Write Transaction Count
1	0x1008 - 0x100C	Read Latency Range 2	Write Latency Range 2	Read Transaction Count
2	0x1010 - 0x1014	Read Latency Range 3	Write Latency Range 3	Slv_Wr_Idle_Cnt
3	0x1018 - 0x101C	Read Latency Range 4	Write Latency Range 4	Mst_Rd_Idle_Cnt
4	0x1020 - 0x1024	Read Latency Range 5	Write Latency Range 5	Num_BValids
5	0x1028 - 0x102C	Read Transaction Count	Write Transaction Count	Num_WLasts
6	0x1030 - 0x1034	Num_RLasts	Num_WLasts	Num_RLasts
7	0x1038 - 0x103C	Num_Rd_Bursts_Len0	Num_BValids	Num_BValids
8	0x1040 - 0x1044	Read Byte Count	Write Byte Count	Num_Rd_Bursts_Len0
9	0x1048 - 0x104C	Total Read Latency	Total Write Latency	Total Write Latency

1. . If parameter C_S_AXI_DATA_WIDTH is 32, the register can be read by a read transaction to two locations: (C_BASEADDR + 0x1000) and (C_BASEADDR + 0x1004).
2. If C_METRIC_COUNT_WIDTH=32, only the lower 32 bits of the register are valid.

Table 2-30: **Metric Counter Registers: Sets 6 and 7**

Metric Counter	Address	Set 6 (for AXI4-Stream) (Metric_Set_Sel =b110)	Set 7 (for AXI4-Stream) (Metric_Set_Sel = b111)
0	0x1000 - 0x1004	Transfer Cycle Count	Transfer Cycle Count
1	0x1008 - 0x100C	Packet Count	Packet Count
2	0x1010 - 0x1014	Transfer Cycle Count	Transfer Cycle Count
3	0x1018 - 0x101C	Mst_Idle_Cnt	Mst_Idle_Cnt
4	0x1020 - 0x1024	Slv_Idle_Cnt	Slv_Idle_Cnt
5	0x1028 - 0x102C	Packet Count	Packet Count
6	0x1030 - 0x1034	Transfer Cycle Count	Transfer Cycle Count
7	0x1038 - 0x103C	Data Byte Count	Data Byte Count
8	0x1040 - 0x1044	Position Byte Count	Position Byte Count
9	0x1048 - 0x104C	Null Byte Count	Null Byte Count

The metric counters give metrics based on the metric set chosen in the Metric Selector register. The metrics are further detailed in the following sections.

Table 2-31 lists the metrics computed for the AXI4 MM agent.

Table 2-31: **Metrics Computed for AXI4-MM Agent**

Metric	Description
Read Latency Range 1	Number of read transactions by/to a particular master/slave that falls in the read latency range 1.
Read Latency Range 2	Number of read transactions by/to a particular master/slave that falls in the read latency range 2.
Read Latency Range 3	Number of read transactions by/to a particular master/slave that falls in the read latency range 3.
Read Latency Range 4	Number of read transactions by/to a particular master/slave that falls in the read latency range 4.
Read Latency Range 5	Number of read transactions by/to a particular master/slave that falls in the read latency range 5.
Read Latency Range 6	Number of read transactions by/to a particular master/slave that falls in the read latency range 6.
Read Latency Range 7	Number of read transactions by/to a particular master/slave that falls in the read latency range 7.
Read Latency Range 8	Number of read transactions by/to a particular master/slave that falls in the read latency range 8.
Read Latency Range 9	Number of read transactions by/to a particular master/slave that falls in the read latency range 9.
Write Latency Range 1	Number of write transactions by/to a particular master/slave that falls in the write latency range 1.

Table 2-31: **Metrics Computed for AXI4-MM Agent *(Cont'd)***

Metric	Description
Write Latency Range 2	Number of write transactions by/to a particular master/slave that falls in the write latency range 2.
Write Latency Range 3	Number of write transactions by/to a particular master/slave that falls in the write latency range 3.
Write Latency Range 4	Number of write transactions by/to a particular master/slave that falls in the write latency range 4.
Write Latency Range 5	Number of write transactions by/to a particular master/slave that falls in the write latency range 5.
Write Transaction Count	Number of write transactions by/to a particular master/slave.
Read Transaction Count	Number of read transactions by/to a particular master/slave.
Write Byte Count	Number of bytes written by/to a particular master/slave.
Read Byte Count	Number of bytes read from/by a particular slave/master.
Total Read Latency	Used with Num_Rd_Reqs (Read Transaction Count) to compute the Average Read Latency.
Total Write Latency	Used with Num_Wr_Reqs (Write Transaction Count) to determine the Average Write Latency.
Slv_Wr_Idle_Cnt	Number of idle cycles caused by the slave during a Write transaction.
Mst_Rd_Idle_Cnt	Number of idle cycles caused by the master during a read transaction.
Num_BValids	Number of BValids given by a slave to the master. This count helps in checking the responses against the number of requests given.
Num_WLasts	Number of WLasts given by the master. This count should exactly match the number of requests given by the master. This helps in debugging of the system.
Num_RLasts	Number of RLasts given by the slave to the master. This count helps in checking the responses against requests. This count should exactly match the number of requests given by the master.
Num_Wr_Bursts_Len0	Number of write requests given with a burst length of 1.
Num_Rd_Bursts_Len0	Number of read requests given with a burst length of 1.

Table 2-32 lists the metrics computed for the AXI4-Stream agent.

Table 2-32: **Metrics Computed for the AXI4-Stream Agent**

Metric	Description
Transfer Cycle Count	Gives the total number of cycles the data is transferred.
Packet Count	Gives the total number of packets transferred.
Data Byte Count	Gives the total number of data bytes transferred.
Position Byte Count	Gives the total number of position bytes transferred.
Null Byte Count	Gives the total number of null bytes transferred.

Table 2-32: **Metrics Computed for the AXI4-Stream Agent *(Cont'd)***

Metric	Description
Slv_Idle_Cnt	Gives the number of idle cycles caused by the slave.
Mst_Idle_Cnt	Gives the number of idle cycles caused by the master.

Sampled Metric Counter Registers

The Metric Counters are captured into the Metric Counter registers when there is a capture event. The capture event can be an external event passed to the core or an overflow event of the sample interval counter. These registers are in AXI clock domain.

Designing with the Core

This chapter includes guidelines and additional information to make designing with the core easier. summary

General Design Guidelines

The following steps are recommended for all designs:

1. Instantiate the Performance Monitor core in the EDK system. See Figure 3-1.
2. Configure the core based on the agents connected to the monitor slots and their operating frequencies.
3. Verify `CORE_ACLK` is the fastest clock in the design (or of the interconnect).
4. Program the configuration registers.
5. Write to `Metric_Selector_Registers` with the metric type and targeted agent.
6. Enable the metrics and global counter (Control register).
7. Give control to the application.
8. Read Sampled Metric registers based on the requirement.
9. Once the application is complete, disable the metrics and global counters by writing '0' to the Control registers.
10. Read the Metrics registers and Global Clock Counter register.

The core can be instantiated in an EDK system as shown in Figure 3-1 and Figure 3-2.

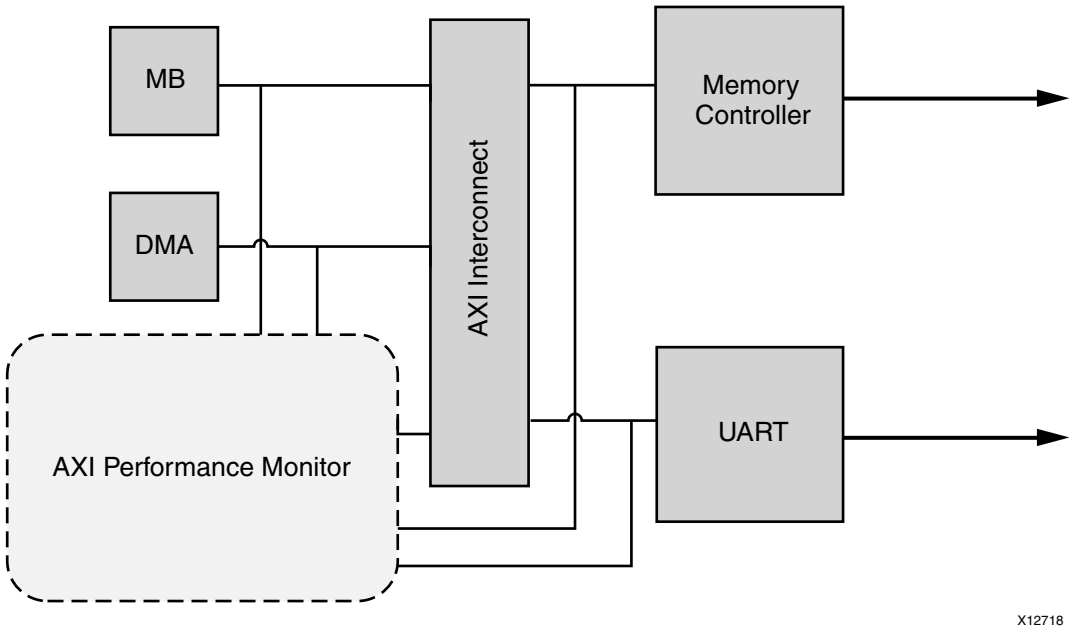

Figure 3-1: **AXI Performance Monitor in EDK System**

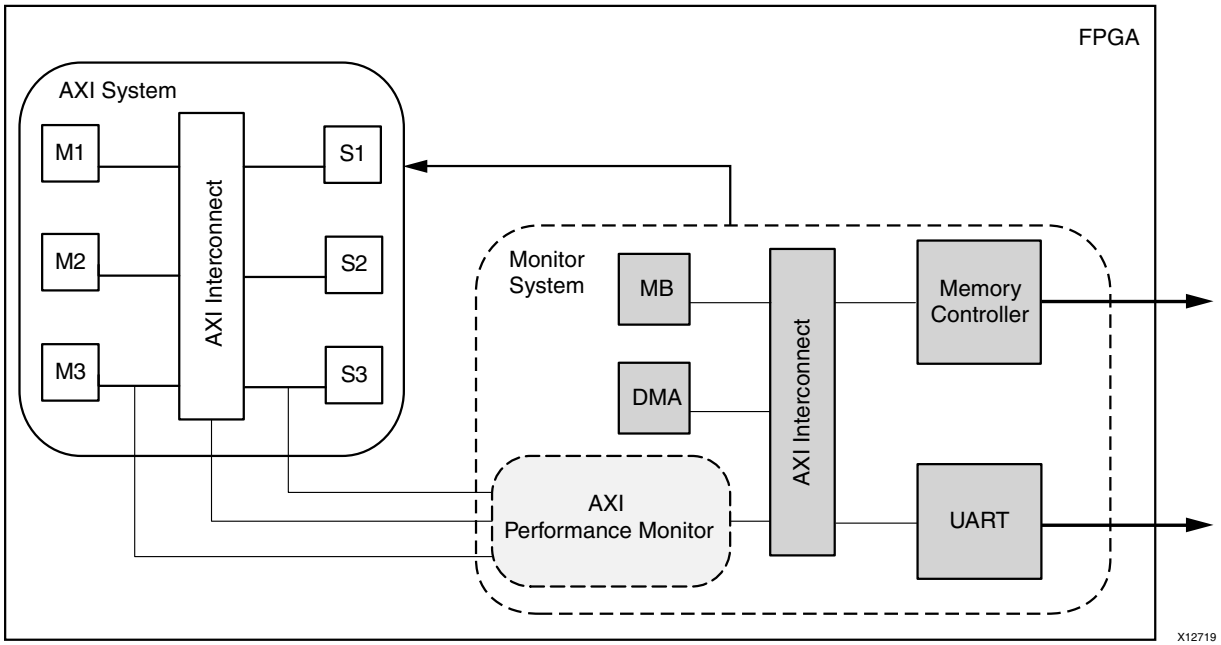

Figure 3-2: **AXI Performance Monitor in Separate System**

Clocking

All the monitor slots' clocks are synchronous to the CORE_ACLK and the time periods are integer multiples of CORE_ACLK time period. CORE_ACLK should be the fastest clock in the design.

Resets

All resets are Active Low.

Appendix 4

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

References

These documents provide supplemental material useful with this user guide:

- *AXI4 AMBA AXI Protocol Version: 2.0 Specification*

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/24/12	1.0	Initial Xilinx release.
05/22/12	1.1	Added Zynq-7000 support.

Notice of Disclaimer